TPS65218x Power Management for ARM® Cortex™-A8/A9 SOCs and FPGA

1 Features

- Two Low-Quiescent Current, High Efficiency Step-Down Converters for Battery Backup Domain
  - DCDC5: 1.0 V Output
  - DCDC6: 1.8 V Output
  - VIN Range from 2.2 to 5.5 V
  - Supplied from System Power or Coin-Cell Backup Battery
- Three Adjustable Step-Down Converters With Integrated Switching FETs:
  - DCDC1: 1.1 V Default up to 1.8 A
  - DCDC2: 1.1 V Default up to 1.8 A
  - DCDC3: 1.2 V Default up to 1.8 A
  - VIN Range from 2.7 to 5.5 V
  - Adjustable Output Voltage Range 0.85 to 3.5 V
  - Power Save Mode at Light Load Current
  - 100% Duty Cycle for Lowest Dropout
  - Active Output-Discharge When Disabled
- One Adjustable Buck-Boost Converter With Integrated Switching FETs:
  - DCDC4: 3.3 V Default up to 1.0 A
  - VIN Range from 2.7 to 5.5 V
  - Adjustable Output Voltage Range 0.85 to 3.4 V
  - Active Output-Discharge When Disabled
- Adjustable General-Purpose LDO (LDO1)
  - LDO1: 1.8 V Default up to 400 mA
  - VIN Range from 1.8 to 5.5 V
  - Adjustable Output Voltage Range from 0.9 to 3.4 V
  - Active Output-Discharge When Disabled
- 5-V Load Switch With 100-mA/ 500-mA Selectable Current Limit
  - VIN Range From 3.0 to 5.5 V
  - 500 mΩ (Max) Switch Impedance at 5 V
- Low Voltage Load Switch With 350-mA Current Limit
  - VIN Range From 1.2 to 3.6 V
  - 110 mΩ (Max) Switch Impedance at 1.35 V
- High Voltage Load Switch (LS3) With 100-mA/ 500-mA Selectable Current Limit
  - VIN Range from 1.8 to 10.0 V
  - 500 mΩ (Max) Switch Impedance
- Supervisor With Built-in Supervisor Function Monitors
- Protection, Diagnostics, and Control:
  - Undervoltage Lockout (UVLO)
  - Always-on Push-Button Monitor
  - Overtemperature Warning and Shutdown
  - Separate Power-Good Output for Backup and Main Supplies
  - I^2C Interface (Address 0x24h)

2 Applications

- Industrial Automation
- Point of Sale
- Test and Measurement
- Personal Navigation

3 Description

The TPS65218x is a single chip power management IC, specifically designed to support both portable (Li-Ion battery) and non-portable (5-V adapter) applications. The device is characterized across a –40°C to 105°C temperature range, making it suitable for a wide range of industrial applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65218	VQFN (48)	6.00 mm × 6.00 mm × 0.40 mm
	HTQFP (48)	7.00 mm × 7.00 mm × 0.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

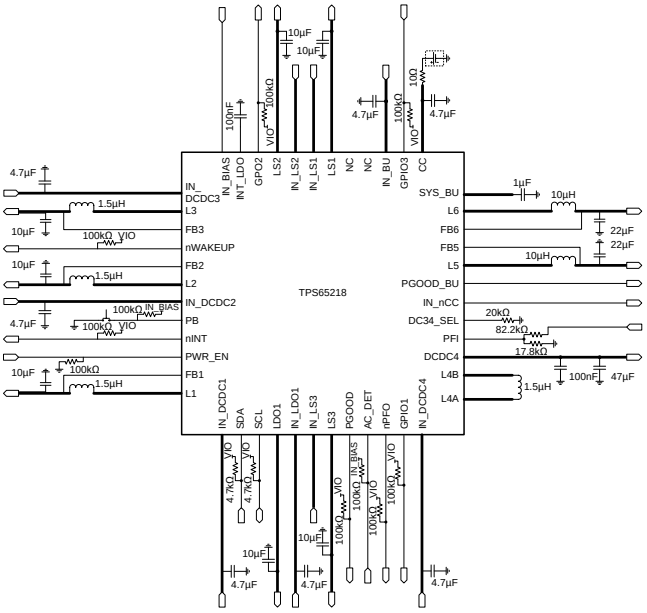


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2015) to Revision B **Page**

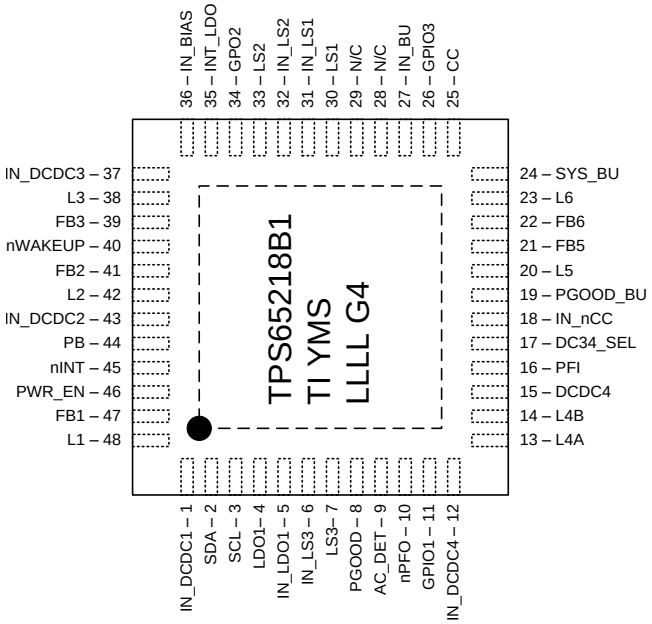
- Updated description for PGOOD to clarify that the output can be configured as open drain ... 3
- Added V_{IN_LS3} conditions to I_{LIMIT} for Load Switch 3 and updated the values ... 13

Changes from Original (November 2014) to Revision A **Page**

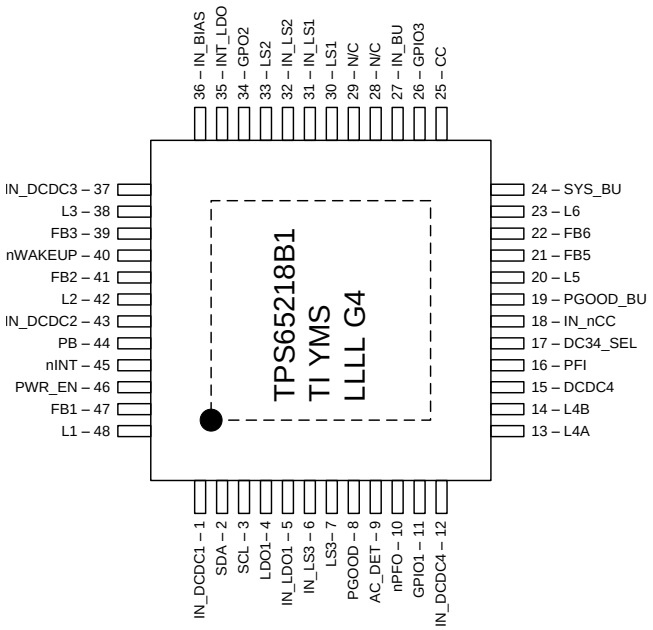
- Added part number TPS65218B101 ... 1
- Increased VIN range for low voltage load switch with 350-mA current limit ... 1
- Moved T_{stg} to the *Absolute Maximum Ratings* table and updated *Handling Ratings* table to an *ESD Ratings* table ... 5
- Added device part number to *Thermal Information* table ... 6
- Added test conditions and values for V_{UVLO} hysteresis ... 7
- Changed test conditions for input voltage ranges from "V_{IN_BIAS} > 2.7 V" to "V_{IN_BIAS} > V_{UVLO}" ... 7
- Updated values for DCDC1-4 V_{OUT} falling and rising ... 8
- Added more test conditions and values for V_{IN_DCDC4} ... 9
- Updated V_{DCDC4} test conditions and values and added output voltage ripple specification for PFM mode ... 9
- Updated test conditions and added new values for V_{DCDC5}, V_{DCDC6} DC accuracy ... 10
- Updated V_{IN_LS1} max value and added additional test condition for $R_{DS(ON)}$ ... 12
- Added note for t_{HIGH} ... 15
- Updated *I²C Bus Operation* and added a note ... 39
- Added note to *Application and Implementation* ... 72
- Added *Community Resources* ... 77

5 Pin Configuration and Functions

RSL Package
48-Pin VQFN
Top View



PHP Package
48-Pin HTQFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN_DCDC1	1	Power	Input supply pin for DCDC1
SDA	2	I/O	Data line for the I^2C interface. Connect to pullup resistor.
SCL	3	I	Clock input for the I^2C interface. Connect to pullup resistor.
LDO1	4	O	Output voltage pin for LDO1. Connect to capacitor.
IN_LDO1	5	Power	Input supply pin for LDO1
IN_LS3	6	Power	Input supply pin for load switch 3
LS3	7	O	Output voltage pin for load switch 3. Connect to capacitor
PGOOD	8	O	Power-good output (configured as open drain). Pulled low when either DCDC1-4 or LDO1 are out of regulation. Load switches and DCDC5-6 do not affect PGOOD pin.
AC_DET	9	I	Power enable input for DCDC1-4, LDOs and load switches. See state diagram for details. Tie pin to IN_BIAS if not used. Switch pin for DCDC3. Connect to inductor.
nPFO	10	O	Power-fail comparator output, deglitched (open drain). Pin is pulled low when PFI input is below power-fail threshold.
GPIO1	11	I/O	Pin configured as DDR reset-input (driving GPO2) or as general-purpose, open-drain output.
IN_DCDC4	12	Power	Input supply pin for DCDC4
L4A	13	Power	Switch pin for DCDC4. Connect to inductor.
L4B	14	Power	Switch pin for DCDC4. Connect to inductor.
DCDC4	15	Power	Output voltage pin for DCDC4. Connect to capacitor.
PFI	16	I	Power-Fail comparator input. Connect to resistor divider.
DC34_SEL	17	I	Power-up default selection pin for DCDC3 or DCDC4. Power-up default is programmed by a resistor connected to ground.
IN_nCC	18	O	Output pin indicates if DCDC5 and DCDC6 are powered from main supply (IN_BU) or coin-cell battery (CC).
PGOOD_BU	19	O	Power-good output (push or pull) for battery backup supplies. Pulled low when either DCDC5 or DCDC6 is out of regulation. Pulled high (to DCDC6 output voltage) when both rails are in regulation.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
L5	20	Power	Switch pin for DCDC5. Connect to inductor.
FB5	21	I	Feedback voltage pin for DCDC5. Connect to output capacitor.
FB6	22	I	Feedback voltage pin for DCDC6. Connect to output capacitor.
L6	23	Power	Switch pin for DCDC6. Connect to inductor.
SYS_BU	24	Power	System voltage pin for battery-backup supply power path. Connect to capacitor. Connecting any external load to this pin is not recommended.
CC	25	Power	Coin Cell battery input. Serves as the supply to DCDC5 and DCDC6 if no voltage is applied to IN_BU. Tie this pin to ground if it is not in use.
GPIO3	26	I/O	Pin configured as PMIC reset or general-purpose, open-drain output.
IN_BU	27	Power	Default input supply pin for battery backup supplies (DCDC5 and DCDC6).
N/C	28	N/A	No connect. Leave pin floating.
N/C	29	N/A	No connect. Leave pin floating.
LS1	30	O	Output voltage pin for load switch 1. Connect to capacitor.
IN_LS1	31	Power	Input supply pin for load switch 1
IN_LS2	32	I	Input supply pin for load switch 2
LS2	33	O	Output voltage pin for load switch 2. Connect to capacitor.
GPO2	34	O	Pin configured as DDR reset signal (controlled by GPIO1) or as general-purpose output. Buffer can be configured as push-pull or open-drain.
INT_LDO	35	Power	Internal bias voltage. Connecting any external load to this pin is not recommended.
IN_BIAS	36	Power	Input supply pin for reference system
IN_DCDC3	37	Power	Input supply pin for DCDC3
L3	38	Power	Switch pin for DCDC3. Connect to inductor.
FB3	39	I	Feedback voltage pin for DCDC3. Connect to feedback resistor divider.
nWAKEUP	40	O	Signal to SOC to indicate a power on event (active low, open-drain output)
FB2	41	I	Feedback voltage pin for DCDC2. Connect to output capacitor.
L2	42	Power	Switch pin for DCDC2. Connect to inductor.
IN_DCDC2	43	Power	Input supply pin for DCDC2
PB	44	I	Push-button monitor input. Typically connected to a momentary switch to ground (active low). See state diagram for details.
nINT	45	O	Interrupt output (active low, open drain). Pin is pulled low if an interrupt bit is set. The returns to HiZ state after the bit causing the interrupt has been read. Interrupts can be masked.
PWR_EN	46	I	Power enable input for DCDC1-4, LDOs and load switches. See state diagram for details.
FB1	47	I	Feedback voltage pin for DCDC1. Connect to output capacitor.
L1	48	Power	Switch pin for DCDC1. Connect to inductor.
PowerPAD™	—	Power	Power ground and thermal relief. Connect to ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

Operating under free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Supply voltage	IN_BIAS, IN_LDO1, IN_LS, IN_DCDC1, IN_DCDC2, IN_DCDC3, IN_DCDC4	–0.3	7	V
		IN_LS1, CC	–0.3	3.6	
		IN_LS3	–0.3	11.2	
		IN_BU	–0.3	5.8	
	Input voltage	DC34_SEL	–0.3	3.6	V
		All pins unless specified separately	–0.3	7	
	Output voltage	DC34_SEL	–0.3	3.6	V
		All pins unless specified separately	–0.3	7	
	Source or sink current	GPO2		6	mA
		PGOOD_BU, IN_nCC		1	
	Sink current	PGOOD, nWAKEUP, nINT, nPFO, SDA, GPIO1, GPIO3		6	mA
T_A	Operating ambient temperature		–40	105	°C
T_J	Junction temperature		–40	125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, IN_BIAS	2.7		5.5	V
Input voltage range for DCDC1, DCDC2, DCDC3, DCDC4	2.7		5.5	V
Supply voltage, IN_BU	2.2		5.5	V
Supply voltage, CC	2.2		3.3	V
Input voltage range for LDO1	1.8		5.5	V
Input voltage range for LS1	1.2		3.3	V
Input voltage range for LS2	3.0		5.5	V
Input voltage range for LS3	1.8		9.9	V
Output voltage range for DCDC1, DCDC2, DCDC3, DCDC4	0.85		3.5	V
Output voltage range for DCDC5	1.0		1.1	V
Output voltage range for DCDC6	1.8		1.8	V
Output voltage range for LDO1	0.9		3.4	V
Output current DCDC1, DCDC2, DCDC3	0		1.8	A
Output current DCDC4	0		1.0	A
Output current DCDC5, DCDC6	0		10	mA
Output current LDO1	0		400	mA
Output current LS1	0		300	mA
Output current LS2	0		1000	mA
Output current LS3	0		1000	mA

6.4 Thermal Information

THERMAL METRIC[1]		TPS65218x		UNIT
		RSL (VQFN)	PHP (HTQFP)	
		16 PINS	16 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top)	17.2	13.3	°C/W
$R_{\theta JB}$	Junction-to-board	5.8	7.9	°C/W
$R_{\theta JA}$	Thermal resistance, junction to ambient. JEDEC 4layer high-K board	30.6	26.7	°C/W
Ψ_{JT}	Junction-to-package top	0.2	0.3	°C/W
Ψ_{JB}	Junction-to-board	5.6	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom)	1.5	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENTS							
V_{IN_BIAS}	Input supply voltage range	Normal operation		2.7		5.5	V
		EEPROM programming		4.5		5.5	
V_{UVLO}	Undervoltage lockout	Measured in respect to V_{IN_BIAS}; supply falling;	UVLO[1:0] = 00	2.7	2.75	2.8	V
			UVLO[1:0] = 01	2.85	2.95	3.05	
			UVLO[1:0] = 10	3.15	3.25	3.35	
			UVLO[1:0] = 11	3.25	3.35	3.45	
	Hysteresis	Supply rising; V_{IN_BIAS} slew rate < 30 V/s	UVLOHYS = 0 (1)		200		mV
			UVLOHYS = 1		400		
		Supply rising; V_{IN_BIAS} slew rate > 30 V/s	UVLOHYS = 0 (1)		0		
			UVLOHYS = 1		0		
	Deglitch time				5		ms
I_{OFF}	OFF state current, Total current into IN_BIAS, IN_DCDCx, IN_LDO1, IN_LSx, IN_BU	V_{IN} = 3.6 V; All rails disabled. T_J = 0 to 85°C.			5		µA
$I_{SUSPEND}$	SUSPEND Current Total current into IN_BIAS, IN_DCDCx, IN_LDO1, IN_LSx, IN_BU	V_{IN} = 3.6 V; DCDC3 enabled, low-power mode, no load. All other rails disabled. T_J = 0 to 105°C			220		µA
INT_LDO							
V_{OUT}	Output voltage				2.5		V
	DC accuracy	I_{OUT} < 10 mA		–2%		2%	
I_{OUT}	Output current range	Maximum allowable external load		0		10	mA
I_{LIMIT}	Short circuit current limit	Output shorted to GND			23		mA
t_{HOLD}	Hold-up time	Measured from V_{IN_BIAS} = 2.7 V to V_{OUT} = 2.25 V. All rails enabled. V_{IN_BIAS} = 2.8 V to 0 in <1 µs No external load on INT_LDO C_{OUT}= 22 µF		150			ms
C_{OUT}	Nominal output capacitor value	Ceramic, X5R or X7R		0.1		22	µF
	Tolerance			–20%		20%	
DCDC1, DCDC2 (1.1-V BUCK)							
$V_{IN\_DCDC1,2}$	Input voltage range	V_{IN_BIAS} > V_{UVLO}		2.7		5.5	V
$V_{DCDC1,2}$	Output voltage range	Adjustable through I^2C		0.85		1.65	V
	DC accuracy	2.7 V ≤ V_{IN} ≤ 5.5 V; 0 A ≤ I_{OUT} ≤ 1.8 A		–2%		2%	
I_{OUT}	Continuous output current	$V_{IN\_DCDC1,2}$ > 2.8 V				1.8	A
I_Q	Quiescent current	Total current from $I_{N\_DCDC1,2}$ pin; device not switching, no load			25	50	µA
$R_{DS(ON)}$	High-side FET ON-resistance	$V_{IN\_DCDC1,2}$ = 3.6 V			230	355	mΩ
	Low-side FET ON-resistance	$V_{IN\_DCDC1,2}$ = 3.6 V			90	145	
I_{LIMIT}	High-side current limit	$V_{IN\_DCDC1,2}$ = 3.6 V			2.8		A
	Low-side current limit	$V_{IN\_DCDC1,2}$ = 3.6 V			3.1		

(1) 200-mV hysteresis option is available for TPS65218B101

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{PG}	Power-good threshold	V_{OUT} falling	STRICT = 0	88.5%	90%	91.5%	
			STRICT = 1	96%	96.5%	97%	
	Hysteresis	V_{OUT} rising	STRICT = 0	3.8%	4.1%	4.4%	
			STRICT = 1		0.25%		
	Deglitch	V_{OUT} falling	STRICT = 0		1		ms
			STRICT = 1		50		µs
		V_{OUT} rising	STRICT = 0		10		
			STRICT = 1		10		
	Time-out				5		ms
V_{OV}	Overvoltage detection threshold (2)	V_{OUT} rising		103%	103.5%	104%	
	Hysteresis	V_{OUT} falling			0.25%		
	Deglitch	V_{OUT} rising			50		µs
I_{INRUSH}	Inrush current	$V_{IN\_DCDC1,2}$ = 3.6 V; C_{OUT} = 10 to 100 µF				500	mA
R_{DIS}	Discharge resistor			150	250	350	Ω
L	Nominal inductor value			1.0	1.5	2.2	µH
	Tolerance			–30%		30%	
C_{OUT}	Nominal output capacitor value	Ceramic, X5R or X7R				500	µF
	Tolerance			–20%		20%	
DCDC3 (1.2-V BUCK)							
V_{IN_DCDC3}	Input voltage range	V_{IN_BIAS} > V_{UVLO}		2.7		5.5	V
V_{DCDC3}	Output voltage range	Adjustable through I^2C		0.9		3.4	V
	DC Accuracy	2.7 V ≤ V_{IN} ≤ 5.5 V; 0 A ≤ I_{OUT} ≤ 1.8 A		–2%		2%	
I_{OUT}	Continuous output current	V_{IN_DCDC3} > 2.8 V				1.8	A
I_Q	Quiescent current	Total current from IN_DCDC3 pin; Device not switching, no load			25	50	µA
$R_{DS(ON)}$	High-side FET ON-resistance	V_{IN_DCDC3} = 3.6 V			230	345	mΩ
	Low-side FET ON-resistance	V_{IN_DCDC3} = 3.6 V			100	150	
I_{LIMIT}	High-side current limit	V_{IN_DCDC3} = 3.6 V			2.8		A
	Low-side current limit	V_{IN_DCDC3} = 3.6 V			3		
V_{PG}	Power-good threshold	V_{OUT} falling	STRICT = 0	88.5%	90%	91.5%	
			STRICT = 1	95%	95.5%	96%	
	Hysteresis	V_{OUT} rising	STRICT = 0	3.8%	4.1%	4.4%	
			STRICT = 1		0.25%		
	Deglitch	V_{OUT} falling	STRICT = 0		1		ms
			STRICT = 1		50		µs
		V_{OUT} rising	STRICT = 0		10		
			STRICT = 1		10		
	Time-out				5		ms
V_{OV}	Overvoltage detection threshold (2)	V_{OUT} rising		104%	104.5%	105%	
	Hysteresis	V_{OUT} falling			0.25%		
	Deglitch	V_{OUT} rising			50		µs
I_{INRUSH}	Inrush current	V_{IN_DCDC3} = 3.6 V; C_{OUT} = 10 to 100 µF				500	mA
R_{DIS}	Discharge resistor			150	250	350	Ω

(2) Over-voltage is monitored only if STRICT = 1.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
L	Nominal inductor value			1.0	1.5	2.2	µH
	Tolerance			–30%		30%	
C_{OUT}	Nominal output capacitor value	Ceramic, X5R or X7R		10		100	µF
	Tolerance			–20%		20%	
DCDC4 (3.3-V BUCK-BOOST) / ANALOG AND I/O							
V_{IN_DCDC4}	Input voltage soft-start range	$V_{IN\_BIAS} > V_{UVLO}$, –40°C to 55°C		3.4			V
		$V_{IN\_BIAS} > V_{UVLO}$, 56°C to 105°C		3.8			
	Input voltage operating range	$V_{IN\_BIAS} > V_{UVLO}$, –40°C to 105°C		2.7		5.5	V
V_{DCDC4}	Output voltage range	Adjustable through I^2C		1.175		3.4	V
	DC accuracy	2.7 V ≤ V_{IN} ≤ 5.5 V; 0 A ≤ I_{OUT} ≤ 1 A		–2%		2%	
	Output voltage ripple	PFM mode enabled; 4.2 V ≤ V_{IN} ≤ 5.5 V; 0 A ≤ I_{OUT} ≤ 1 A; C_{OUT} = 80 µF				200	mV_{pp}
	Minimum duty cycle in step-down mode					18%	
I_{OUT}	Continuous output current	V_{IN_DCDC4} = 2.8 V, V_{OUT} = 3.3 V				1.0	A
		V_{IN_DCDC4} = 3.6 V, V_{OUT} = 3.3 V				1.3	
		V_{IN_DCDC4} = 5.0 V, V_{OUT} = 3.3 V				1.6	
I_Q	Quiescent current	Total current from IN_DCDC4 pin; Device not switching, no load			25	50	µA
f_{SW}	Switching frequency				2400		kHz
$R_{DS(ON)}$	High-side FET ON-resistance	V_{IN_DCDC3} = 3.6 V	IN_DCDC4 to L4A		166		mΩ
			L4B to DCDC4		149		
	Low-side FET ON-resistance	V_{IN_DCDC3} = 3.6 V	L4A to GND		142	190	
			L4B to GND		144	190	
I_{LIMIT}	Average switch current limit	V_{IN_DCDC4} = 3.6 V			3000		mA
V_{PG}	Power-good threshold	V_{OUT} falling	STRICT = 0	88.5%	90%	91.5%	
			STRICT = 1	95%	95.5%	96%	
	Hysteresis	V_{OUT} rising	STRICT = 0	3.8%	4.1%	4.4%	
			STRICT = 1		0.25%		
	Deglitch	V_{OUT} falling	STRICT = 0		1		ms
			STRICT = 1		50		µs
		V_{OUT} rising	STRICT = 0		10		
			STRICT = 1		10		
	Time-out				5		ms
V_{OV}	Overvoltage detection threshold[2]	V_{OUT} rising		104%	104.5%	105%	
	Hysteresis	V_{OUT} falling			0.25%		
	Deglitch	V_{OUT} rising			50		µs
I_{INRUSH}	Inrush current	V_{IN_DCDC4} = 3.6 V; C_{OUT} = 10 to 100 µF				500	mA
R_{DIS}	Discharge resistor			150	250	350	Ω
L	Nominal inductor value			1.2	1.5	2.2	µH
	Tolerance			–30%		30%	
C_{OUT}	Nominal output capacitor value	Ceramic, X5R or X7R		40		100	µF
	Tolerance			–20%		20%	

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DCDC5,6 POWER PATH						
V_{CC}	DCDC5, 6 input voltage range	V_{IN_BU} = 0	2.2		3.3	V
V_{IN_BU}	DCDC5, 6 input voltage range(3)	0 < V_{CC} < 5.5 V	2.2		5.5	V
t_{RISE}	V_{CC}, V_{IN_BU} rise time	Voltage rising from 0 to 5.5 V	30			µs
$R_{DS(ON)}$	Power path switch impedance	CC to SYS_BU V_{CC} = 2.4 V, V_{IN_BU} = 0 V		14.5		Ω
	Power path switch impedance	IN_BU to SYS_BU V_{IN_BU} = 3.6 V		10.5		
I_{LEAK}	Forward leakage current	Into CC pin; V_{CC} = 3.3 V, V_{IN_BU} = 0; OFF state; FSEAL = 0; over full temperature range		50	300	nA
	Reverse leakage current	Out of CC pin; V_{CC} = 1.5 V; V_{IN_BU} = 5.5 V; over full temperature range			500	
R_{CC}	Acceptable CC source impedance	$I_{OUT,\ DCDC5}$ < 10 µA; $I_{OUT,\ DCDC6}$ < 10 µA			1000	Ω
I_Q	Quiescent current	Average current into CC pin; RECOVERY or POWER_OFF state; V_{IN_BU} = 0; V_{CC} = 2.4 V DCDC5 and DCDC6 enabled, no load T_J = 25ºC		350		nA
DCDC5 (1.0-V BATTERY BACKUP SUPPLY)						
V_{DCDC5}	Output voltage			1		V
	DC accuracy	2.7 V ≤ V_{IN_BU} ≤ 5.5 V; 1 µA ≤ I_{OUT} ≤ 25 mA	–1.5%		1.5%	
		2.2 V ≤ V_{CC} ≤ 3.3 V; 1 µA ≤ I_{OUT} ≤ 100 µA V_{IN_BIAS} decay rate during CC transition > 150 V/s	–1.5%		1.5%	
		2.2 V ≤ V_{CC} ≤ 3.3 V; 1 µA ≤ I_{OUT} ≤ 100 µA V_{IN_BIAS} decay rate during CC transition < 150 V/s	–10%		5%	
	Output voltage ripple	L = 10 µH; C_{OUT} = 22 µF; 100-µA load			32	mV_{pp}
I_{OUT}	Continuous output current	2.2 V < V_{CC} < 3.3 V V_{IN_BU} = 0		10	100	µA
		2.7 V < V_{IN_BU} < 5.5 V			25	mA
$R_{DS(ON)}$	High-side FET ON-resistance	V_{IN_BU} = 2.8 V		2.5	3.5	Ω
	Low-side FET ON-resistance	V_{IN_BU} = 2.8 V		2	3	
I_{LIMIT}	High-side current limit	V_{IN_BU} = 2.8 V		50		mA
V_{PG}	Power-good threshold	V_{OUT} falling	79%	85%	91%	
	Hysteresis	V_{OUT} rising		6%		
I_{INRUSH}	Inrush current	V_{CC} = 3.0 V; V_{IN_BU} = 0; C_{OUT} = 10 to 47 µF			500	µA
L	Nominal inductor value	Chip inductor	4.7	10	22	µH
	Tolerance		–30%		30%	
C_{OUT}	Nominal output capacitor value	Ceramic, X5R or X7R	20		47	µF
	Tolerance		–20%		20%	

(3) IN_BU has priority over CC input.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DCDC6 (1.8-V BATTERY BACKUP SUPPLY)							
V_{DCDC6}	Output voltage				1.8		V
	DC accuracy	2.7 V ≤ V_{IN_BU} ≤ 5.5 V; 1 µA ≤ I_{OUT} ≤ 25 mA		–1.5%		1.5%	
		2.2 V ≤ V_{CC} ≤ 3.3 V; 1 µA ≤ I_{OUT} ≤ 100 µA; V_{IN_BIAS} decay rate during CC transition > 150 V/s		–1.5%		1.5%	
		2.2 V ≤ V_{CC} ≤ 3.3 V; 1 µA ≤ I_{OUT} ≤ 100 µA; V_{IN_BIAS} decay rate during CC transition < 150 V/s		–10%		5%	
	Output voltage ripple	L = 10 µH; C_{OUT} = 22 µF; 100-µA load				30	mV_{pp}
I_{OUT}	Continuous output current	2.2 V < V_{CC} < 3.3 V; V_{IN_BU} = 0			10	100	µA
$R_{DS(ON)}$	High-side FET ON-resistance	V_{IN_BU} = 3.0 V			2.5	3.5	Ω
	Low-side FET ON-resistance	V_{IN_BU} = 3.0 V			2	3	
I_{LIMIT}	High-side current limit	V_{IN_BU} = 3.0 V			50		mA
V_{PG}	Power-good threshold	V_{OUT} falling		87%	91%	95%	
	Hysteresis	V_{OUT} rising			3%		
I_{INRUSH}	Inrush current	V_{CC} = 3.0 V; V_{IN_BU} = 0; C_{OUT} = 10 to 47 µF				500	µA
L	Nominal inductor value	Chip inductor		4.7	10	22	µH
	Tolerance			–30%		30%	
C_{OUT}	Nominal output capacitor value	Ceramic, X5R or X7R		20		47	µF
	Tolerance			–20%		20%	
LDO1 (1.8-V LDO)							
V_{IN_LDO1}	Input voltage range	V_{IN_BIAS} > V_{UVLO}		1.8		5.5	V
I_Q	Quiescent current	No load			35		µA
V_{OUT}	Output voltage range	Adjustable through I^2C		0.9		3.4	V
	DC Accuracy	V_{OUT}+0.2 V ≤ V_{IN} ≤ 5.5 V; 0 A ≤ I_{OUT} ≤ 200 mA		–2%		2%	
I_{OUT}	Output current range			0		200	mA
		V_{IN_LDO1} > 2.7 V, V_{OUT} = 1.8 V		0		400	
I_{LIMIT}	Short circuit current limit	Output shorted to GND		490	550		mA
V_{DO}	Dropout voltage	I_{OUT} = 100 mA, V_{IN} = 3.6 V				200	mV
V_{PG}	Power-good threshold	V_{OUT} falling	STRICT = 0	86%	90%	94%	
			STRICT = 1	95%	95.5%	96%	
		Hysteresis, V_{OUT} rising	STRICT = 0	3%	4%	5%	
			STRICT = 1		0.25%		
	Deglitch	V_{OUT} falling	STRICT = 0		1		ms
			STRICT = 1		50		µs
		V_{OUT} rising	STRICT = 0		10		
			STRICT = 1		10		
	Time-out				5		ms
V_{OV}	Over-voltage detection threshold(2)	V_{OUT} rising		104%	104.5%	105%	
	Hysteresis	V_{OUT} falling			0.25%		
	Deglitch	V_{OUT} rising			50		µs
		V_{OUT} falling			1		ms
R_{DIS}	Discharge resistor			150	250	350	Ω

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{OUT}	Nominal output capacitor value	Ceramic, X5R or X7R		10		100	µF
	Tolerance			–20%		20%	
LOAD SWITCH 1 (LS1)							
V_{IN_LS1}	Input voltage range	$V_{IN\_BIAS} > V_{UVLO}$		1.2		3.6	V
$R_{DS(ON)}$	Static on-resistance	V_{IN_LS1} = 3.3 V, I_{OUT} = 300 mA, over full temperature range				110	mΩ
		V_{IN_LS1} = 1.8 V, I_{OUT} = 300 mA, DDR2 / LPDDR / MDDR at 266 MHz over full temperature range				110	
		V_{IN_LS1} = 1.5 V, I_{OUT} = 300 mA, DDR3 at 333 MHz over full temperature range				110	
		V_{IN_LS1} = 1.35 V, I_{OUT} = 300 mA, DDR3L at 333 MHz over full temperature range				110	
		V_{IN_LS1} = 1.2 V, I_{OUT} = 200 mA, LPDDR2 at 333 MHz over full temperature range				150	
I_{LIMIT}	Short circuit current limit	Output shorted to GND		350			mA
t_{BLANK}	Interrupt blanking time	Output shorted to GND until interrupt is triggered			15		ms
R_{DIS}	Internal discharge resistor at output (4)			150	250	350	Ω
T_{OTS}	Overtemperature shutdown(5)			125	132	139	°C
	Hysteresis				10		
C_{OUT}	Nominal output capacitor value	Ceramic, X5R or X7R		10		100	µF
	Tolerance			–20%		20%	
LOAD SWITCH 2 (LS2)							
V_{IN_LS2}	Input voltage range	$V_{IN\_BIAS} > V_{UVLO}$		4.0		5.5	V
V_{UVLO}	Undervoltage lockout	Measured at IN_LS2. Supply falling (6)		2.48	2.60	2.70	V
	Hysteresis	Input voltage rising			170		mV
$R_{DS(ON)}$	Static on-resistance	V_{IN_LS2} = 5.0 V, I_{OUT} = 500 mA, over full temperature range				500	mΩ
I_{LIMIT}	Short circuit current limit	Output shorted to GND; $V_{IN\_LS2} > 4.0$ V	LS2ILIM[1:0] = 00	100		126	mA
			LS2ILIM[1:0] = 10	200		251	
			LS2ILIM[1:0] = 01	500		631	
			LS2ILIM[1:0] = 11	1000		1290	
I_{LEAK}	Reverse leakage current	$V_{LS2} > V_{IN\_LS2}$ + 1 V			12	30	µA
t_{BLANK}	Interrupt blanking time	Output shorted to GND until interrupt is triggered			15		ms
R_{DIS}	Internal discharge resistor at output(4)			150	250	380	Ω
T_{OTS}	Overtemperature shutdown (6)			125	132	139	°C
	Hysteresis				10		
C_{OUT}	Nominal output capacitor value	Ceramic, X5R or X7R		1		100	µF
	Tolerance			–20%		20%	

(4) Discharge function disabled by default.
(5) Switch is temporarily turned OFF if temperature exceeds OTS threshold.
(6) Switch is temporarily turned OFF if input voltage drops below UVLO threshold.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LOAD SWITCH 3 (LS3)							
V_{IN_LS3}	Input voltage range	$V_{IN\_BIAS} > V_{UVLO}$		1.8		10.0	V
$R_{DS(ON)}$	Static on-resistance	V_{IN_LS3} = 9.0 V, I_{OUT}= 500 mA, over full temperature range				440	mΩ
		V_{IN_LS3} = 5.0 V, I_{OUT}= 500 mA, over full temperature range				526	
		V_{IN_LS3} = 2.8 V, I_{OUT}= 200 mA, over full temperature range				656	
		V_{IN_LS3} = 1.8 V, I_{OUT}= 200 mA, over full temperature range				910	
I_{LIMIT}	Short circuit current limit	V_{IN_LS3} > 2.3 V, Output shorted to GND	LS3ILIM[1:0] = 00	100		126	mA
			LS3ILIM[1:0] = 10	200		253	
			LS3ILIM[1:0] = 01	500		738	
			LS3ILIM[1:0] = 11	950		1234	
		V_{IN_LS3} ≤ 2.3 V, Output shorted to GND	LS3ILIM[1:0] = 00	100		126	mA
			LS3ILIM[1:0] = 10	200		253	
			LS3ILIM[1:0] = 01	500		738	
t_{BLANK}	Interrupt blanking time	Output shorted to GND until interrupt is triggered			15		ms
R_{DIS}	Internal discharge resistor at output(4)			650	1000	1500	Ω
T_{OTS}	Overtemperature shutdown(6)			125	132	139	°C
	Hysteresis				10		
C_{OUT}	Nominal output capacitor value	Ceramic, X5R or X7R		1	100	220	µF
	Tolerance			–20%		20%	
BACKUP BATTERY MONITOR							
V_{TH}	Comparator threshold	Ideal level			3.00		V
		Good level			2.60		
		Low level			2.30		
	Accuracy			–3%		3%	
R_{LOAD}	Load impedance	Applied from CC to GND during comparison		70	100	130	kΩ
t_{DLY}	Measurement delay	R_{LOAD} is connected during delay time. Measurement is taken at the end of delay.			600		ms
I/O LEVELS AND TIMING CHARACTERISTICS							
PG_{DLY}	PGOOD delay time	PGDLY[1:0] = 00			10		ms
		PGDLY[1:0] = 01			20		
		PGDLY[1:0] = 10			50		
		PGDLY[1:0] = 11			150		
t_{DG}	Deglitch time	PB input	Rising edge		100		ms
			Falling edge		50		
		AC_DET input	Rising edge		100		µs
			Falling edge		10		ms
		PWR_EN input	Rising edge		10		ms
			Falling edge		100		µs
		GPIO1	Rising edge		1		ms
			Falling edge		1		
		GPIO3	Rising edge		5		µs
			Falling edge		5		

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{RESET}	Reset time	PB input held low	TRST = 0		8		s
			TRST = 1		15		
V_{IH}	High level input voltage	SCL, SDA, GPIO1, GPIO3		1.3			V
		AC_DET, PB		0.66 × IN_BIAS			
		PWR_EN		1.3			
V_{IL}	Low level input voltage	SCL, SDA, PWR_EN, AC_DET, PB, GPIO1, GPIO3		0		0.4	V
V_{OH}	High level output voltage	GPO2; I_{SOURCE} = 5 mA; GPO2_CNF = 1		V_{IN_LS1} – 0.3		V_{IN_LS1}	V
		PGOOD_BU; I_{SOURCE} = 100 µA		(VDD_18 – 10 mV)			
V_{OL}	Low level output voltage	nPFO, nWAKEUP, nINT, SDA, PGOOD, GPIO1, GPO2, GPIO3; I_{SINK} = 2 mA		0		0.3	V
		PGOOD_BU; I_{SINK} = 100 µA		0		0.3	
V_{PFI}	Power-fail comparator threshold	Input falling			800		mV
	Hysteresis	Input rising			40		
	Accuracy			–4%		4%	
	Deglitch	Input falling			25		µs
		Input rising			10		ms
I_{DC34_SEL}	DC34_SEL bias current	Enabled only at power-up			10		µA
V_{DC34_SEL}	DCDC3 / DCDC4 power-up default selection thresholds	Threshold 1			100		mV
		Threshold 2			163		
		Threshold 3			275		
		Threshold 4			400		
		Threshold 5			575		
		Threshold 6			825		
		Threshold 7			1200		
R_{DC34_SEL}	DCDC3 / DCDC4 power-up default selection resistor values	Setting 0		0	0	7.7	kΩ
		Setting 1		11.3	12.1	13.0	
		Setting 2		18.1	20.0	22.0	
		Setting 3		30.9	31.6	32.3	
		Setting 4		44.8	45.3	46.4	
		Setting 5		64.2	64.9	66.3	
		Setting 6		92.9	95.3	96.9	
		Setting 7		135.3	150		
I_{BIAS}	Input bias current	SCL, SDA, GPIO1(7), GPIO3(7); V_{IN} = 3.3 V			0.01	1.0	µA
		PB, AC_DET, PFI; V_{IN} = 3.3 V				500	nA
I_{LEAK}	Pin leakage current	nINT, nWAKEUP, nPFO, PGOOD, PWR_EN, GPIO1(8), GPO2(9), GPIO3(8) V_{OUT} = 3.3 V				500	nA
OSCILLATOR							
f_{OSC}	Oscillator frequency				2400		kHz
	Frequency accuracy	T_J = –40°C to 105°C		–12%		12%	

(7) Configured as input.
(8) Configured as output.
(9) Configured as open-drain output.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERTEMPERATURE SHUTDOWN						
T_{OTS}	Overtemperature shutdown	Increasing junction temperature	135	145	155	°C
	Hysteresis	Decreasing junction temperature		20		
T_{WARN}	High-temperature warning	Increasing junction temperature	90	100	110	°C
	Hysteresis	Decreasing junction temperature		15		

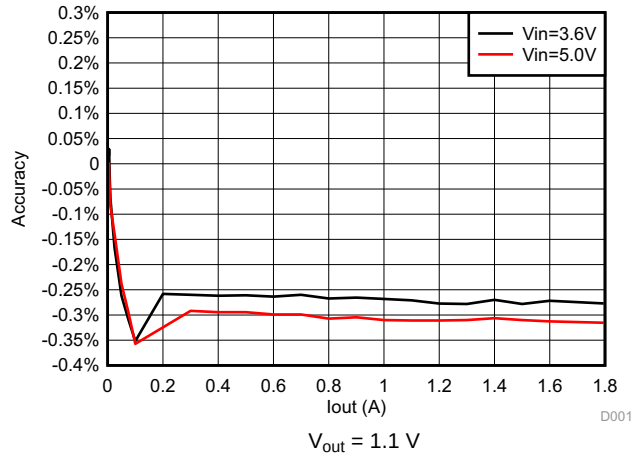
6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
f_{SCL}	Serial clock frequency				100	kHz
					400	
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	SCL = 100 kHz	4.0			µs
		SCL = 400 kHz	600			ns
t_{LOW}	LOW period of the SCL clock	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	1.3			
t_{HIGH}	HIGH period of the SCL clock	SCL = 100 kHz	4.0			µs
		SCL = 400 kHz (1)	1.0			
$t_{SU;STA}$	Set-up time for a repeated START condition	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	600			ns
$t_{HD;DAT}$	Data hold time	SCL = 100 kHz	0		3.45	µs
		SCL = 400 kHz	0		900	ns
$t_{SU;DAT}$	Data set-up time	SCL = 100 kHz	250			ns
		SCL = 400 kHz	100			
t_r	Rise time of both SDA and SCL signals	SCL = 100 kHz			1000	ns
		SCL = 400 kHz			300	
t_f	Fall time of both SDA and SCL signals	SCL = 100 kHz			300	ns
		SCL = 400 kHz			300	
$t_{SU;STO}$	Set-up time for STOP condition	SCL = 100 kHz	4.0			µs
		SCL = 400 kHz	600			ns
t_{BUF}	Bus free time between Stop and Start condition	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	1.3			
t_{SP}	Pulse width of spikes which mst be suppressed by the input filter	SCL = 100 kHz	—		—	ns
		SCL = 400 kHz	0		50	
C_b	Capacitive load for each bus line	SCL = 100 kHz			400	pF
		SCL = 400 kHz			400	

(1) The SCL duty cycle at 400 kHz must be >40%.

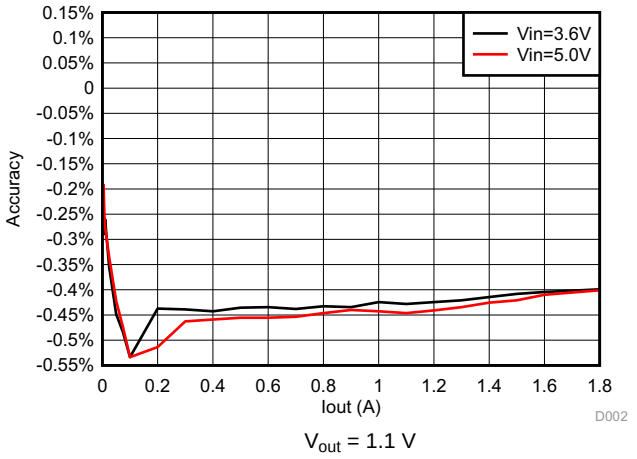
6.7 Typical Characteristics

at T_J = 25°C unless otherwise noted



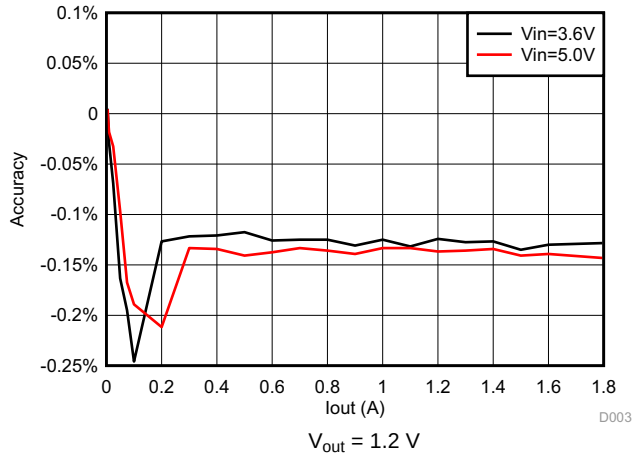
V_{out} = 1.1 V

Figure 1. DCDC1 Accuracy



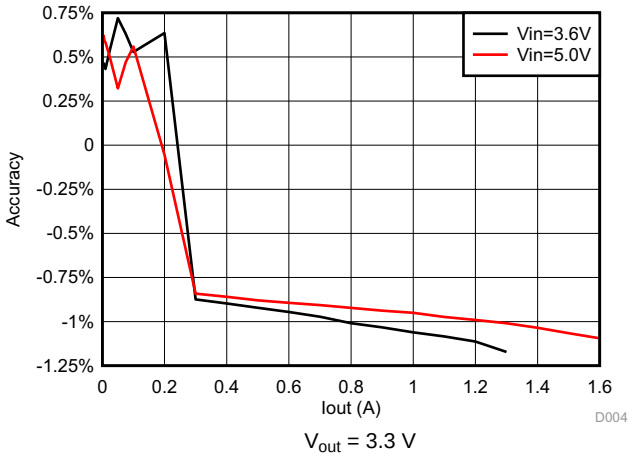
V_{out} = 1.1 V

Figure 2. DCDC2 Accuracy



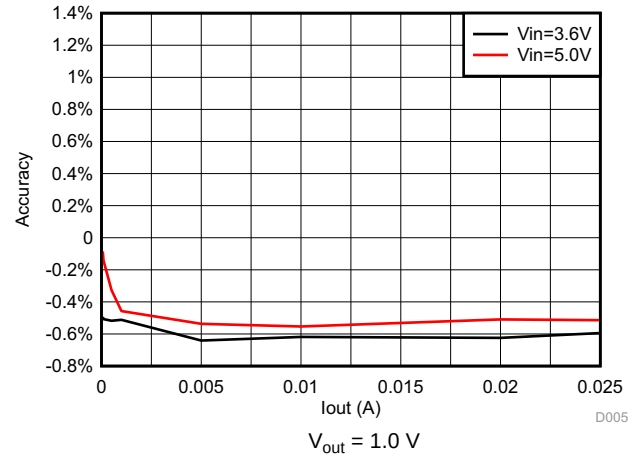
V_{out} = 1.2 V

Figure 3. DCDC3 Accuracy



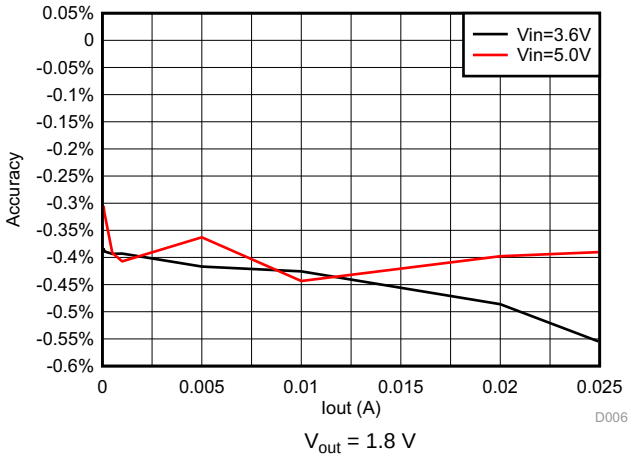
V_{out} = 3.3 V

Figure 4. DCDC4 Accuracy



V_{out} = 1.0 V

Figure 5. DCDC5 Accuracy



V_{out} = 1.8 V

Figure 6. DCDC6 Accuracy

7 Detailed Description

7.1 Overview

The TPS65218x provides three step-down converters, three load switches, three general-purpose I/Os, two battery backup supplies, one buck-boost converter and one LDO. The system can be supplied by a single cell Li-Ion battery or regulated 5-V supply. A coin-cell battery can be added to supply the two always-on backup supplies. The device is characterized across a –40°C to 105°C temperature range, which makes it suitable for various industrial applications.

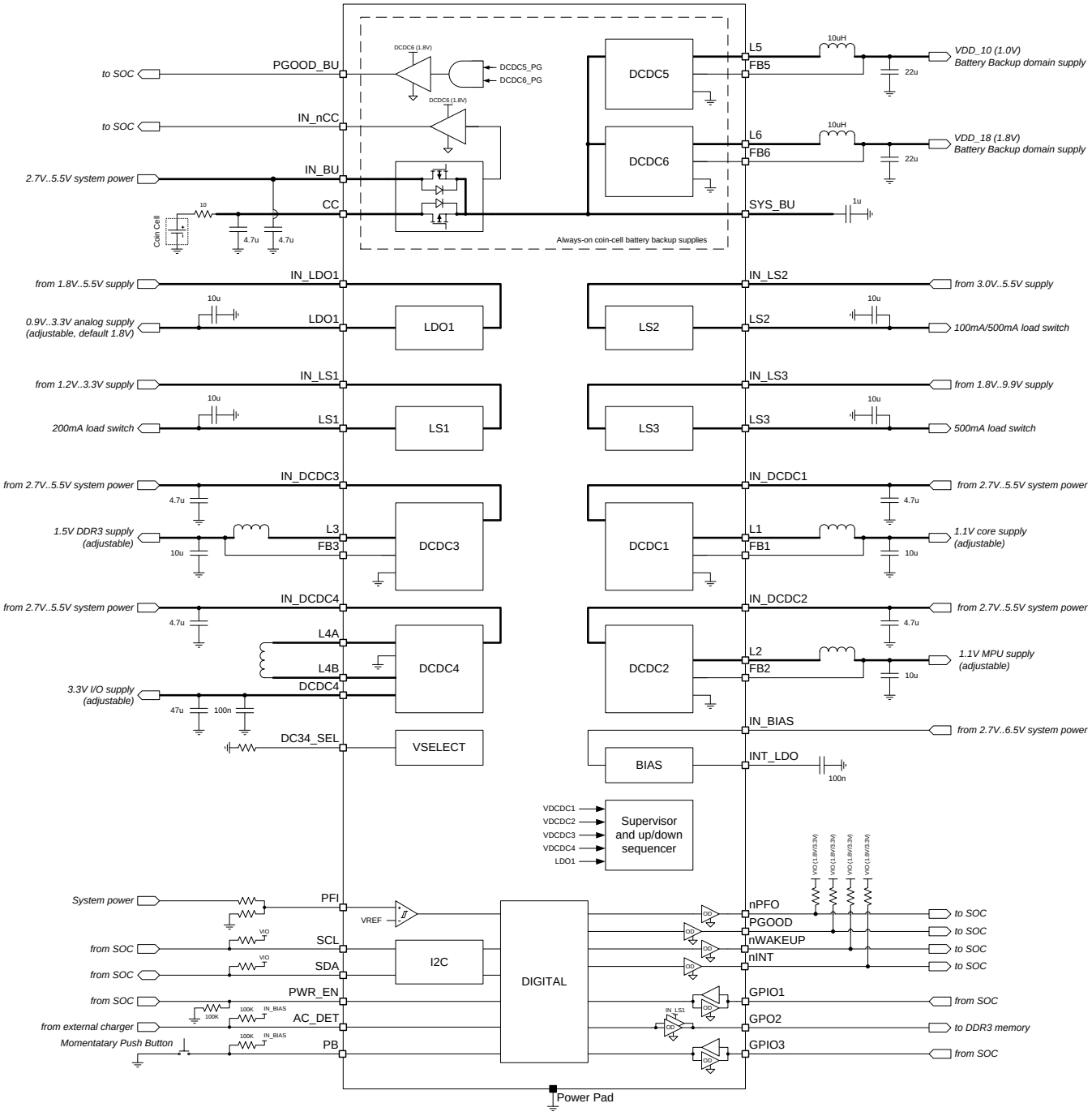
The I^2C interface provides comprehensive features for using TPS65218x. All rails, load-switches, and GPIOs can be enabled / disabled. Voltage thresholds for the UVLO and supervisor can be customized. Power-up and power-down sequences can also be programmed through I^2C. Interrupts for over-temperature, over-current, and under-voltage can be monitored as well.

The integrated voltage supervisor monitors DCDC 1-4 and LDO1. It has two settings; the standard settings only monitors for under-voltage, while the strict settings implements tight tolerances on both under-voltage and over-voltage. A power good signal is provided to report the regulation state of the five rails.

The three hysteretic step-down converters can each supply up to 1.8 A of current. The default output voltages for each converter can be adjusted through the I^2C interface. DCDC 1 and 2 feature dynamic voltage scaling with adjustable slew rate. The step-down converters operate in a low power mode at light load, and can be forced into PWM operation for noise sensitive applications.

The battery backup supplies consist of two low power step-down converters optimized for very light loads and are monitored with a separate power good signal. The converters can be configured to operate as always-on supplies with the addition of a coin cell battery. The state of the battery can be monitored over I^2C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Wake-Up and Power-Up and Power-Down Sequencing

The TPS65218x has a pre-defined power-up and power-down sequence, which in a typical application does not need to be changed. The user defines custom sequences under I^2C control. The power-up sequence is defined by a series of ten strobes and nine delay times. Each output rail is assigned to a strobe to determine the order of enabling rails. A single rail is assigned to only one strobe, but multiple rails can be assigned to the same strobe. The delay times between strobes are between 2 and 5 ms.

7.3.1.1 Power-Up Sequencing

When the power-up sequence initiates, STROBE1 occurs, and any rail assigned to this strobe is enabled. After a delay time of DLY1, STROBE2 occurs and the rail assigned to this strobe is powered up. The sequence continues until all strobes occur and all DLYx times execute. Strobe assignments and delay times are defined in the SEQx registers, and are changed under I^2C control. The power-up sequence executes if one of the following events occurs:

- From the OFF state:
  - The push-button is pressed (falling edge on PB) OR
  - The AC_DET pin is pulled low OR
  - The PWR_EN is asserted (driven to high-level) OR
  - The main power is connected (IN_BIAS) and AC_DET is grounded AND
  - The device is not in undervoltage lockout (UVLO) or overtemperature shutdown (OTS).
- From the SUSPEND state:
  - The push-button is pressed (falling edge on PB_IN) OR
  - The AC_DET pin is pulled low (falling edge) OR
  - The PWR_EN pin is pulled high (level sensitive) AND
  - The device is not in UVLO or OTS.

When a power-up event is detected, the device enters a WAIT_PWR_EN state and triggers the power-up sequence. The device remains in WAIT_PWR_EN as long as the PWR_EN and either the PB or AC_DET pin are held low. If both, the PB and AC_DET return to logic-high state and the PWR_EN pin has not been asserted within 20 s of entering WAIT_PWR_EN state, the power-down sequence is triggered and the device returns to OFF state. Once PWR_EN is asserted, the device advances to ACTIVE state, which is functionally equivalent to WAIT_PWR_EN. However, the AC_DET pin is ignored and power-down is controlled by the PWR_EN pin only.

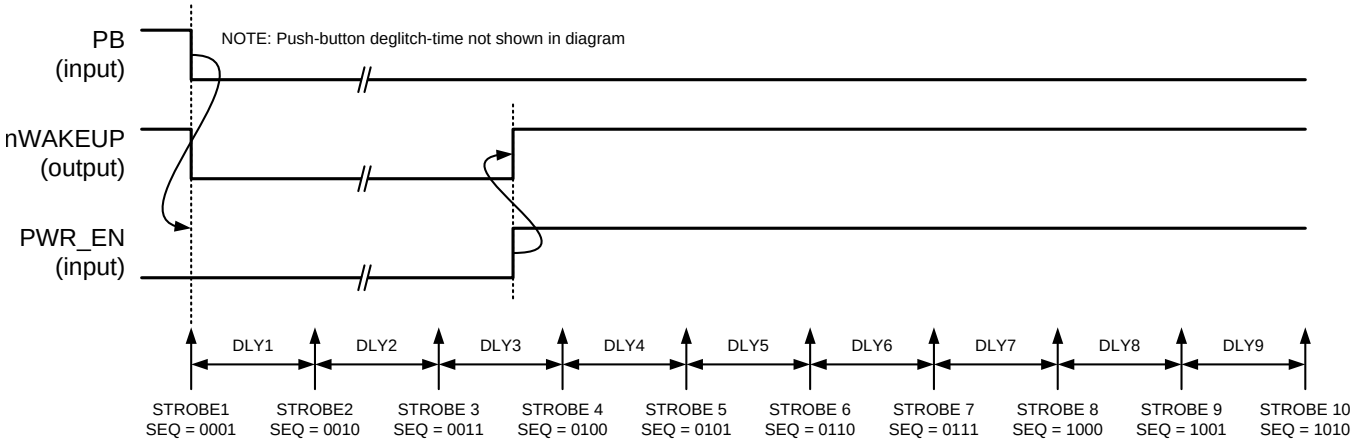
Rails not assigned to a strobe (SEQ = 0000b) are not affected by power-up and power-down sequencing and remain in their current ON/OFF state regardless of the sequencer. A rail can be enabled/disabled at any time by setting the corresponding enable bit in the ENABLE register, with the exception that the ENABLE register cannot be accessed while the sequencer is active. Enable bits always reflect the current enable state of the rail, for example the sequencer sets and resets the enable bits for the rails under its control.

NOTE

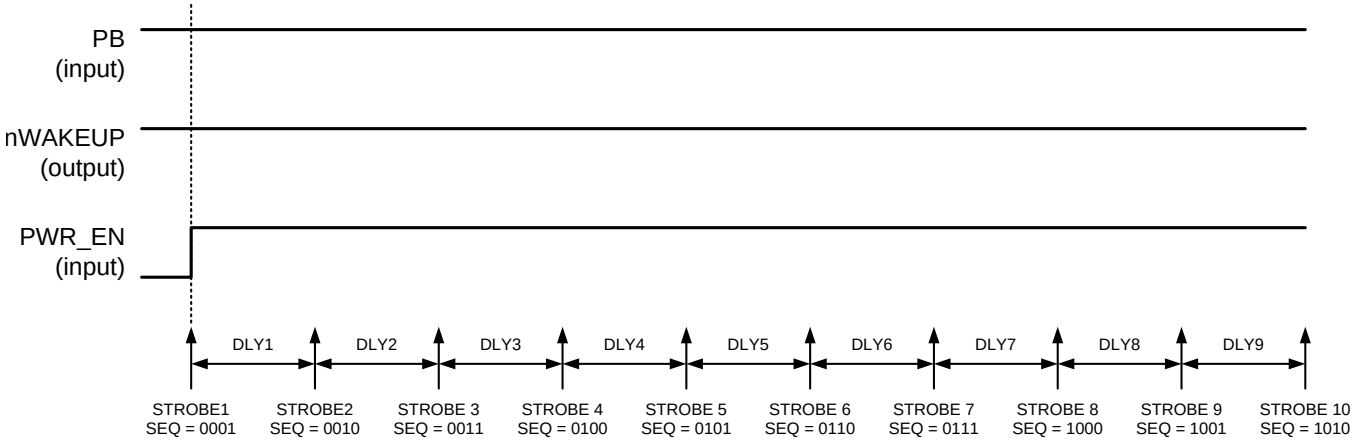
The power-up sequence is defined by strobes and delay times, and can be triggered by the PB, AC_DET (not shown, same as PB), or PWR_EN pin.

Feature Description (continued)

Power-up from OFF or SUSPEND state; PB is power-up event.



Power-up from SUSPEND state; PWR_EN is power-up event.



Power-up from RECOVERY state

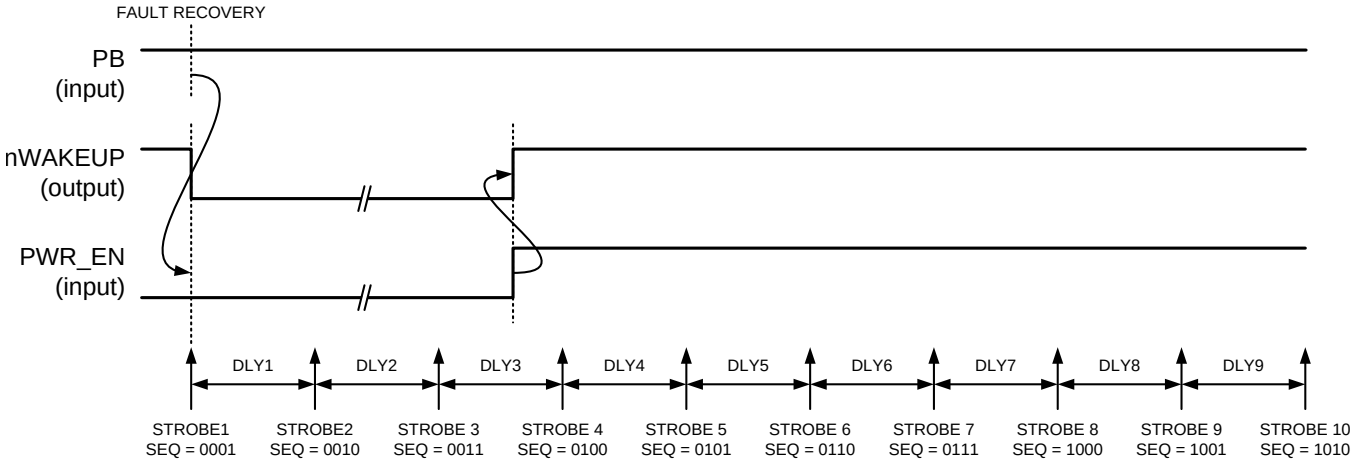


Figure 7. Power-Up Sequences from Different States

Feature Description (continued)

7.3.1.2 Power-Down Sequencing

By default, the power-down sequence follows the reverse of the power-up sequence. When the power-down sequence is triggered, STROBE10 occurs and any rail assigned to STROBE10 is shut down and its discharge circuit is enabled. After a delay time of DLY9, STROBE9 occurs and any rail assigned to it is shut down and its discharge circuit enabled. The sequence continues until all strobes occur and all DLYx times execute. The DLYx times are extended by a factor of 10x to provide ample time for discharge, and preventing output voltages from crossing during shut-down. The DLFCTR bit is applied globally to all power-down delay times. Regardless of the DLYx and DLFCTR settings, the PMIC enters OFF, SUSPEND, or RECOVERY state 500 ms after the power-down sequence initiates, to ensure that the discharge circuits remain enabled for a minimum of 50 ms before the next power-up sequence starts.

A power-down sequence executes if one of the following events occurs:

- The device is in the WAIT_PWR_EN state, the PB and AC_DET pins are high, PWR_EN is low, and the 5s timer has expired.
- The device is in the ACTIVE state and the PWR_EN pin is pulled low.
- The device is in the WAIT_PWR_EN, ACTIVE, or SUSPEND state and the push-button is pressed for >8s (15s if TRST = 1)
- A fault occurs in the IC (OTS, UVLO, PGOOD failure).

When transitioning from ACTIVE to SUSPEND state, rails not controlled by the power-down sequencer maintains the same ON/OFF state in SUSPEND state that it had in ACTIVE state. This allows keeping selected power rails up in SUSPEND.

When transitioning to the OFF or RECOVERY state, rails not under sequencer control are shut-down as follows:

- DCDC1, 2, 3, 4, LDO1, and LS1 shut down at the beginning of the power-down sequence, if not under sequencer control (SEQ = 0).
- LS2 and LS3 shut down as the state machine enters an OFF or RECOVERY state; 500 ms after the power-down sequence is triggered.

7.3.1.3 Strobes 1 and 2

STROBE1 and STROBE2 are dedicated to DCDC5 and DCDC6 which are ‘always-on’; powered up as soon as the device exits the OFF state, and ON in any other state. STROBE 1 and 2 options are available only for DCDC5 and DCDC6, not for any other rails.

STROBE 1 and STROBE 2 occur in every power-up sequence, regardless if the rail is already powered up. If the rail is not to be powered up, its respective strobe setting must be set to 0x00.

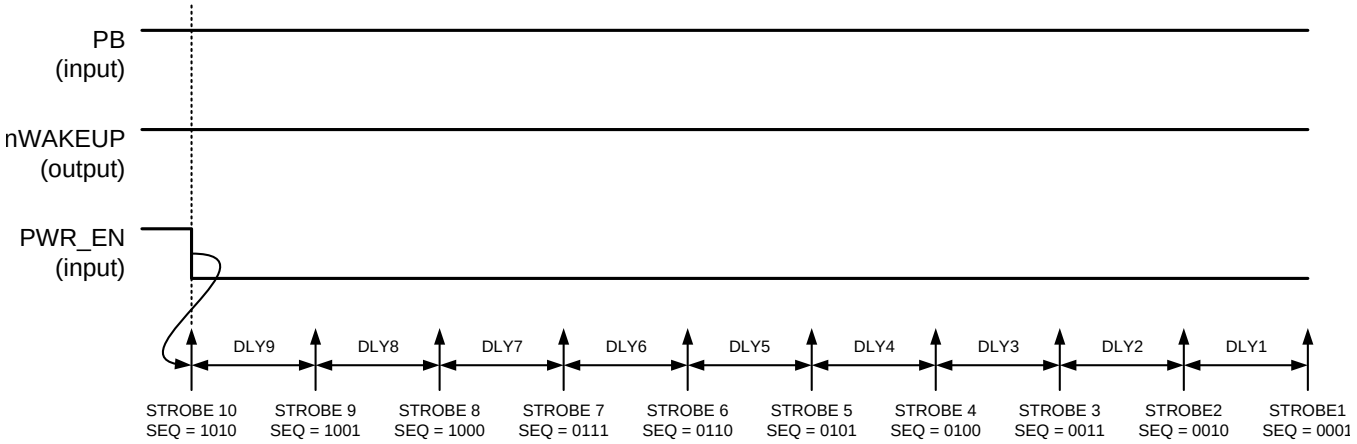
When a power-down sequence initiates, STROBE1 and STROBE2 occur only if the FSEAL bit is 0. Otherwise, both strobes are omitted and DCDC5 and DCDC6 maintain state.

NOTE

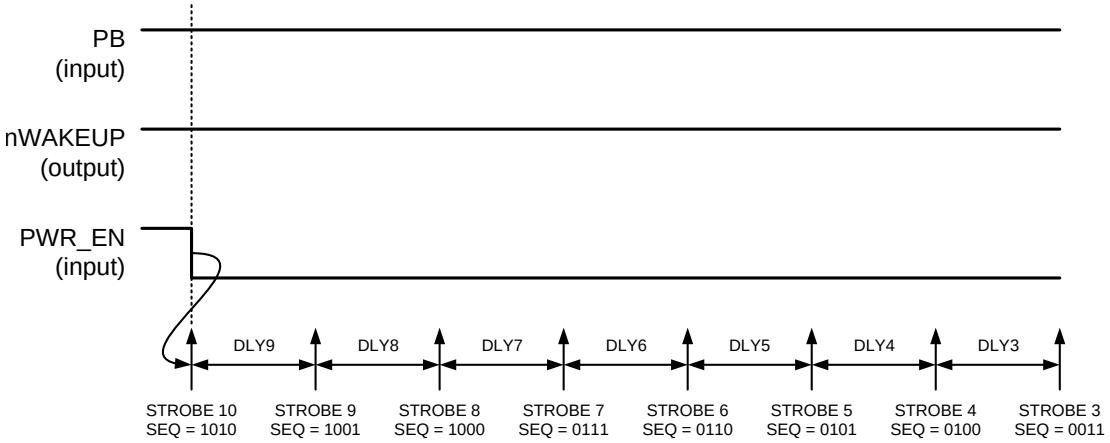
The power-down sequence follows the reverse of the power-up sequence. STROBE2 and STROBE1 are executed only if FSEAL bit is 0.

Feature Description (continued)

Power-down to OFF state. PWR_EN is power-down event. FSEAL = 0.



Power-down to SUSPEND state. PWR_EN is power-down event. FSEAL = 1.
Note that STROBE2 and STROBE1 are omitted.



Power-down to RECOVERY state. TSD or UV is power-down event. FSEAL = 1.
Note that STROBE2 and STROBE1 are omitted.

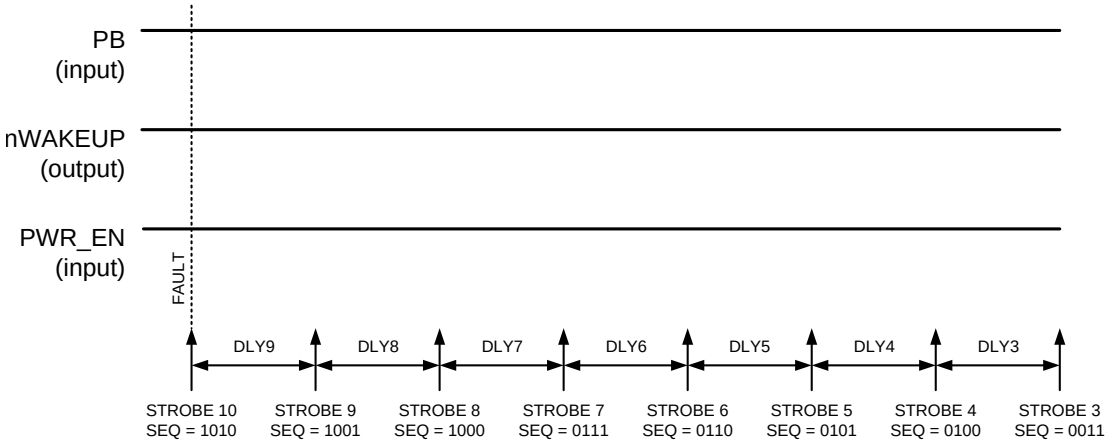


Figure 8. Power-Down Sequences to Different States

Feature Description (continued)

7.3.1.4 Supply Voltage Supervisor and Power Good (PGOOD)

Power-good (PGOOD) is an open-drain output of the built-in voltage supervisor that monitors DCDC1, DCDC2, DCDC3, DCDC4, and LDO1. The output is HiZ when all enabled rails are in regulation and driven low when one or more rails encounter a fault which brings the output voltage outside the specified tolerance range. In a typical application PGOOD drives the reset signal of the SOC.

The supervisor has two modes of operation, controlled by the STRICT bit. With the STRICT bit set to 0, all five rails are monitored for under-voltage only with relaxed thresholds and deglitch times. With the STRCT bit set to 1, all five rails are monitored for under-voltage and over-voltage with tight limits and short deglitch times. Table 1 summarizes these details.

Table 1. Supervisor Characteristics Controlled by the STRICT Bit

PARAMETER		STRICT = 0	STRICT = 1
Undervoltage monitoring	Threshold (output falling)	90%	96.5% (DCDC1, DCDC2) 95.5% (DCDC3, DCDC4)
	Deglitch (output falling)	1 ms	50 µs
	Deglitch (output rising)	10 µs	10 µs
Overvoltage monitoring	Threshold (output falling)	N/A	103.5% (DCDC1, DCDC2) 104.5% (DCDC3, DCDC4)
	Deglitch (output falling)	N/A	1 ms
	Deglitch (output rising)	N/A	50 µs

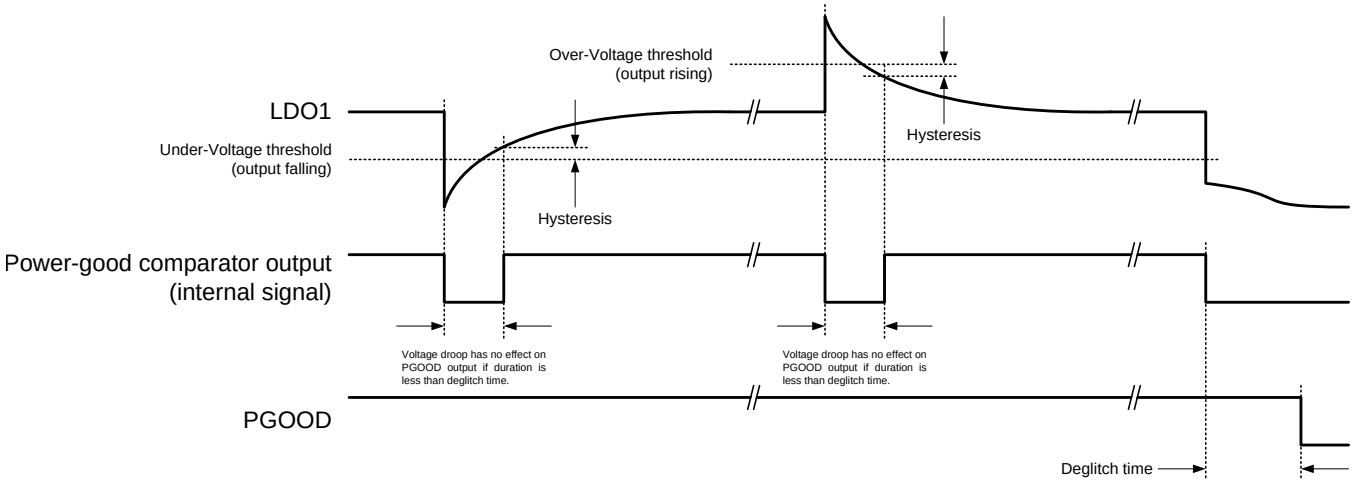


Figure 9. Definition of Undervoltage, Overvoltage Thresholds, Hysteresis, and Deglitch Times

The following rules apply to the PGOOD output:

- The power-up default state for PGOOD is low. When all rails are disabled, PGOOD output is driven low.
- Only enabled rails are monitored. Disabled rails are ignored.
- Power-good monitoring of a particular rail starts 5 ms after the rail is enabled and is continuously monitored thereafter. This allows the rail to power-up.
- PGOOD is delayed by PGDLY time after the sequencer is finished and the last rail is enabled.
- If an enabled rail is continuously outside the monitoring threshold for longer than the deglitch time, PGOOD is pulled low, and all rails are shut-down following the power-down sequence. PGDLY does not apply.
- Disabling a rail manually by resetting the DCx_EN or LDO1_EN bit has no effect on the PGOOD pin. If all rails are disabled, PGOOD is driven low as the last rail is disabled.
- If the power-down sequencer is triggered, PGOOD is driven low together with the disabling of the first power rail.
- PGOOD is driven low in SUSPEND state, regardless of the number of rails that are enabled.

Figure 10 shows a typical power-up sequence and PGOOD timing.

7.3.1.5 Backup Supply Power-Good (PGOOD_BU)

PGOOD_BU is a push-pull output indicating if DCDC5 and DCDC6 are in regulation. The output is driven to high when both rails are in regulation, and driven low if at least one of the rails is below the power-good threshold. The output-high level is equal to the output voltage of DCDC6.

PGOOD_BU is the logical AND between PGOOD(DCDC5) and PGOOD(DCDC6), and has no delay time built-in. Unlike main power-good, a fault on DCDC5 or DCDC6 does not trigger the power-down sequencer, does not disable any of the rails in the system, and has no effect on the PGOOD pin. DCDC5 and DCDC6 recover automatically once the fault is removed.

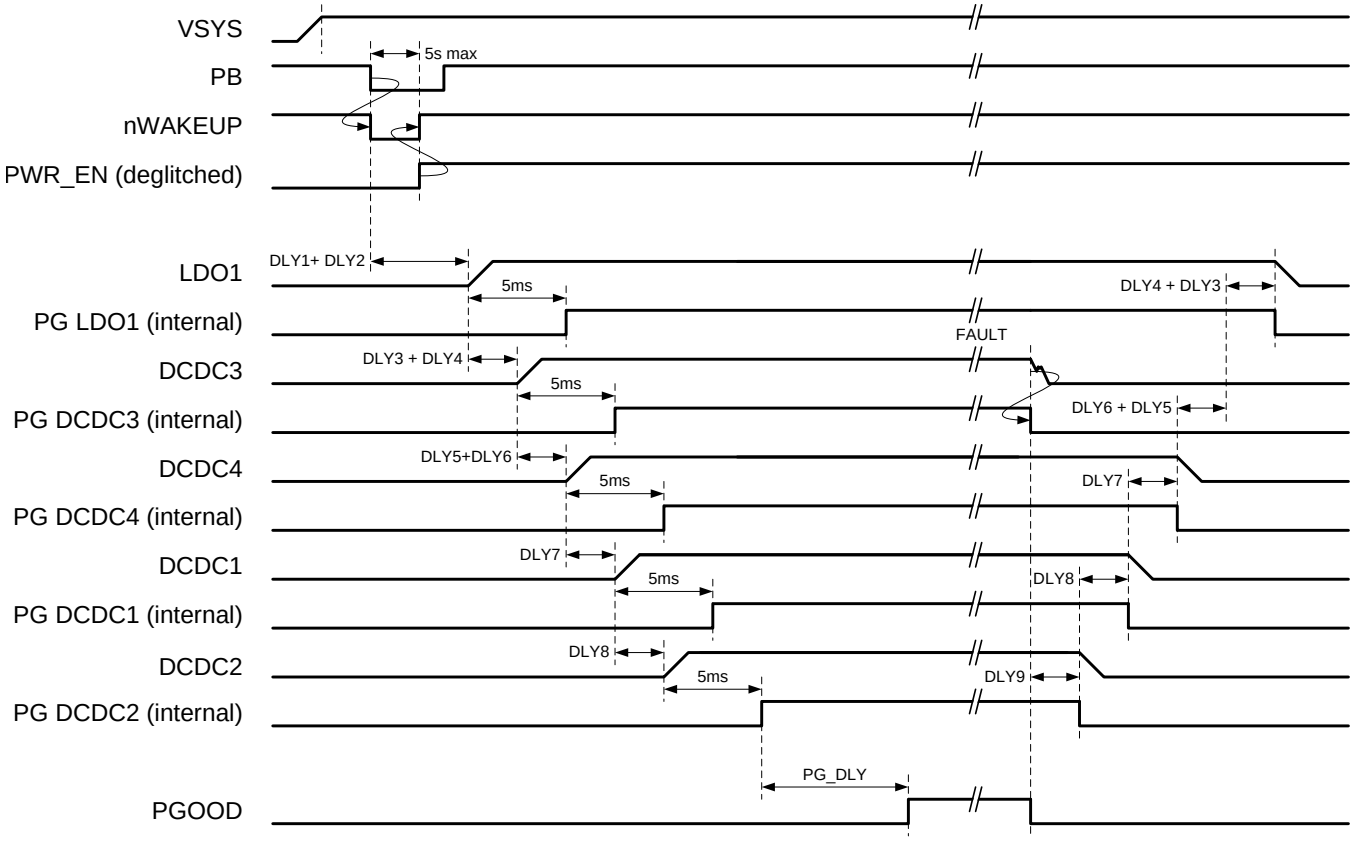


Figure 10. Typical Power-Up Sequence of the Main Output Rails

NOTE

In this example, the power-down is triggered by a fault on DCDC3.

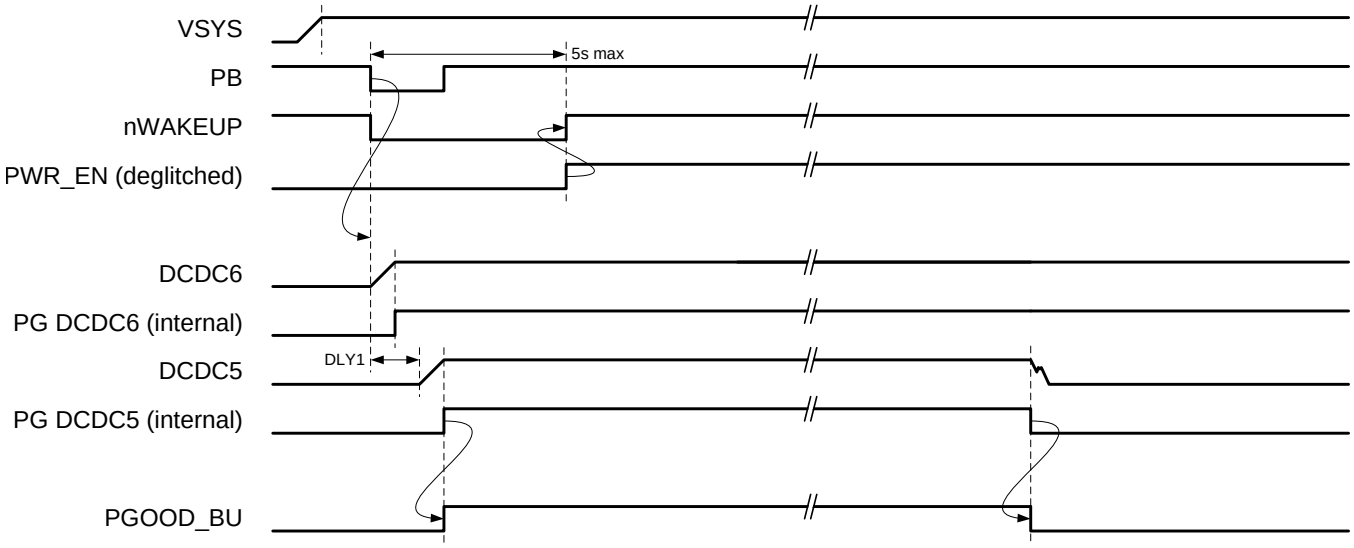


Figure 11. Typical Power-Up Sequence of DCDC5 and DCDC6

7.3.1.6 Internal LDO (INT_LDO)

Internal LDO provides a regulated voltage to the internal digital core and analog circuitry. Internal LDO has a nominal output voltage of 2.5 V and can support up to 10 mA of external load.

When system power fails, the UVLO comparator triggers the power-down sequence. If system power drops below 2.5 V, the digital core is reset and all remaining power rails are shut down instantaneously.

The internal LDO reverse-blocks to prevent the discharge of the output capacitor, and the remaining charge on the INT_LDO output capacitor provides a supply for the power-rail discharge circuitry to ensure the outputs are discharged to ground even if the system supply has failed. The amount of hold-up time is a function of the output capacitor value, which should not exceed 22 µF and the amount of external load, if any.

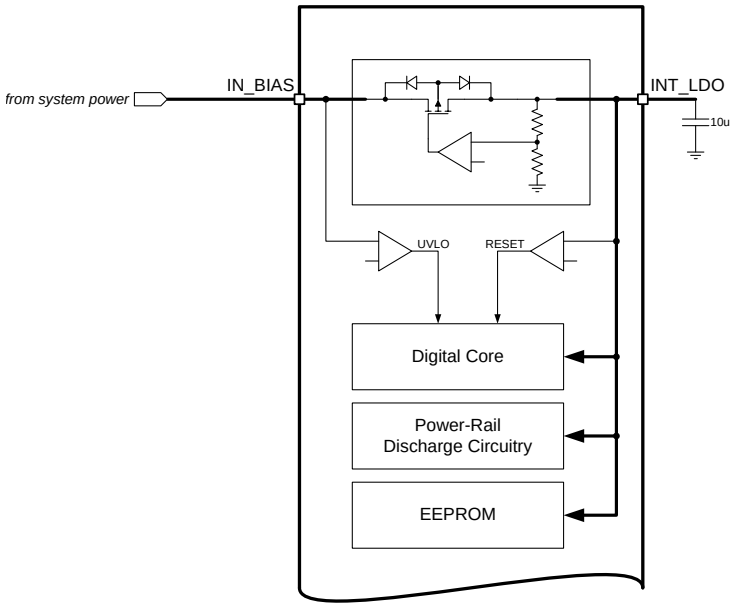


Figure 12. Internal LDO and UVLO Sensing

7.3.1.7 Current Limited Load Switches

The TPS65218x provides three current limited load switches with individual inputs, outputs, and enable control. Each switch provides the following control and diagnostic features:

- The ON/OFF state of the switch is controlled by the corresponding LSx_EN bit in the ENABLE register.
- Each switch has an active discharge function, disabled by default, and enabled through the LSxDCHRG bit. When enabled, the switch output is discharged to ground whenever the switch is disabled.
- When the PFI input drops below the power-fail threshold (the power-fail comparator trips), the load switches are automatically disabled to shed system load. This function must be individually enabled for each switch through the corresponding LSxnPFO bit. The switches do not turn back on automatically as the system voltage recovers, and must be manually re-enabled.
- An interrupt (LSx_I) issues whenever a load switch actively limits the output current, such as when the output load exceeds the current limit value. The switch remains ON and provides current to the load according the current-limit setting.
- All three load switches have local over-temperature sensors which disable the corresponding switch if the power dissipation and junction temperature exceeds safe operating value. The switch automatically recovers once the temperature drops below the OTS threshold value. The LSx_F (fault) interrupt bit is set while the switch is held OFF by the OTS function.

7.3.1.7.1 Load Switch 1 (LS1)

LS1 is a non-reverse blocking, low-voltage (<3.3 V), low-impedance switch intended to support DDR3 self-refresh mode by cutting off the DDR3 supply to the SOC DDR3 interface during SUSPEND mode. In a typical application, the input of LS1 is tied to the output of DCDC3 and the output connected to the memory-interface supply pin of the SOC. LS1 can be controlled by the internal sequencer, just as any power rail.

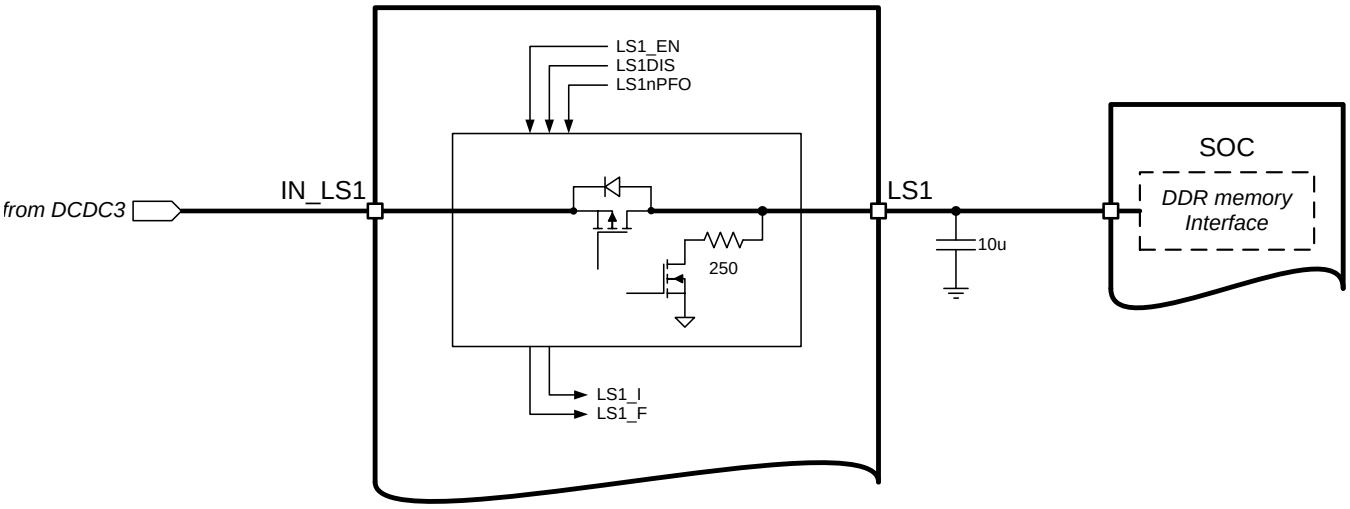


Figure 13. Typical Application of Load Switch 1

7.3.1.7.2 Load Switch 2 (LS2)

LS2 is a reverse-blocking, 5 V, low-impedance switch. Load switch 2 provides four different current limit values (100/200/500/1000 mA) that are selectable through LS2ILIM[1:0] bits. Over-current is reported through the LS2_I interrupt.

LS2 has its own input-under-voltage protection which forces the switch OFF if the switch input voltage (V_{IN_LS2}) is <2.7 V. Similar to OTS, the LS2_F interrupt is set when the switch is held OFF by the local UVLO function, and the switch recovers automatically when the input voltage rises above the UVLO threshold.

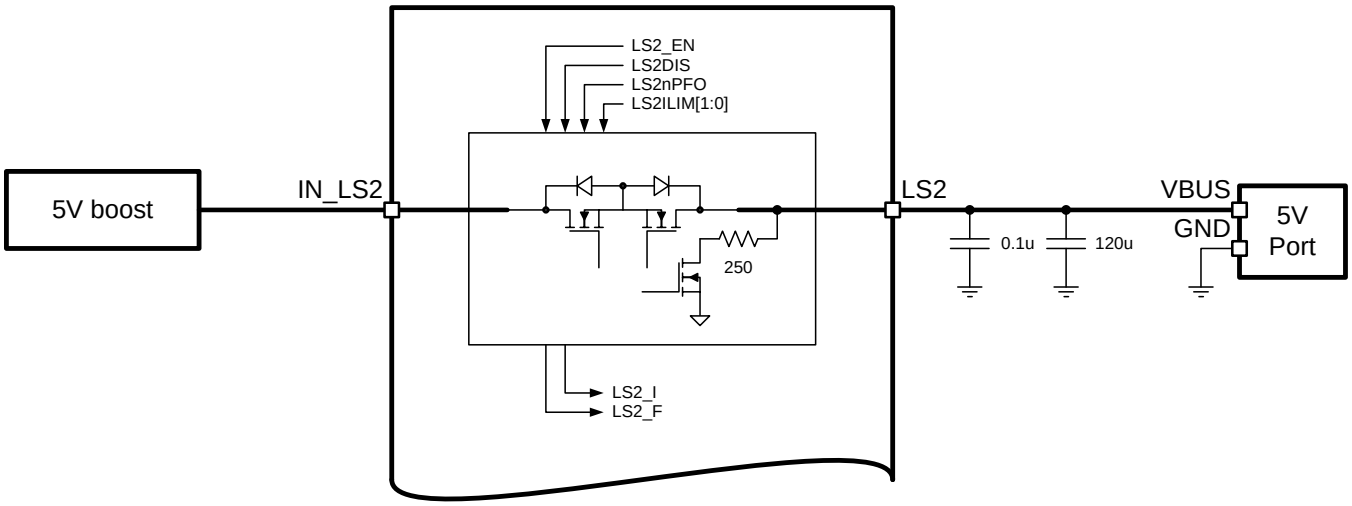


Figure 14. Typical Application of Load Switch 2

7.3.1.7.3 Load Switch 3 (LS3)

LS3 is a non-reverse blocking, medium-voltage (<10 V), low-impedance switch that can be used to provide 1.8 to 9 V power to an auxiliary port. LS3 has four selectable current limit values in the range of 100 mA to 1 A.

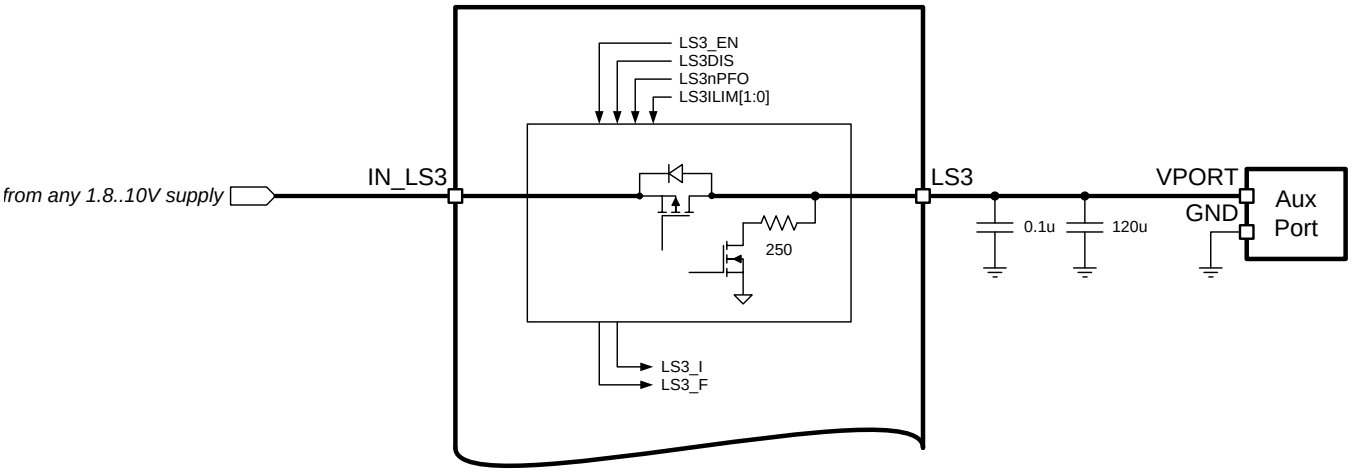


Figure 15. Typical Application of Load Switch 3

7.3.1.8 LDO1

LDO1 is a general-purpose LDO intended to provide power to analog circuitry on the SOC. LDO1 has an input voltage range from 1.8 to 5.5 V, and can be connected either directly to the system power or the output of a DCDC converter. The output voltage is programmable in the range of 0.9 to 3.4 V with a default of 1.8 V. LDO1 supports up to 200 mA at the minimum specified headroom voltage, and up to 400 mA at the typical operating condition of V_{OUT} = 1.8 V, V_{IN_LDO1} > 2.7 V.

7.3.1.9 Coin Cell Battery Voltage Acquisition

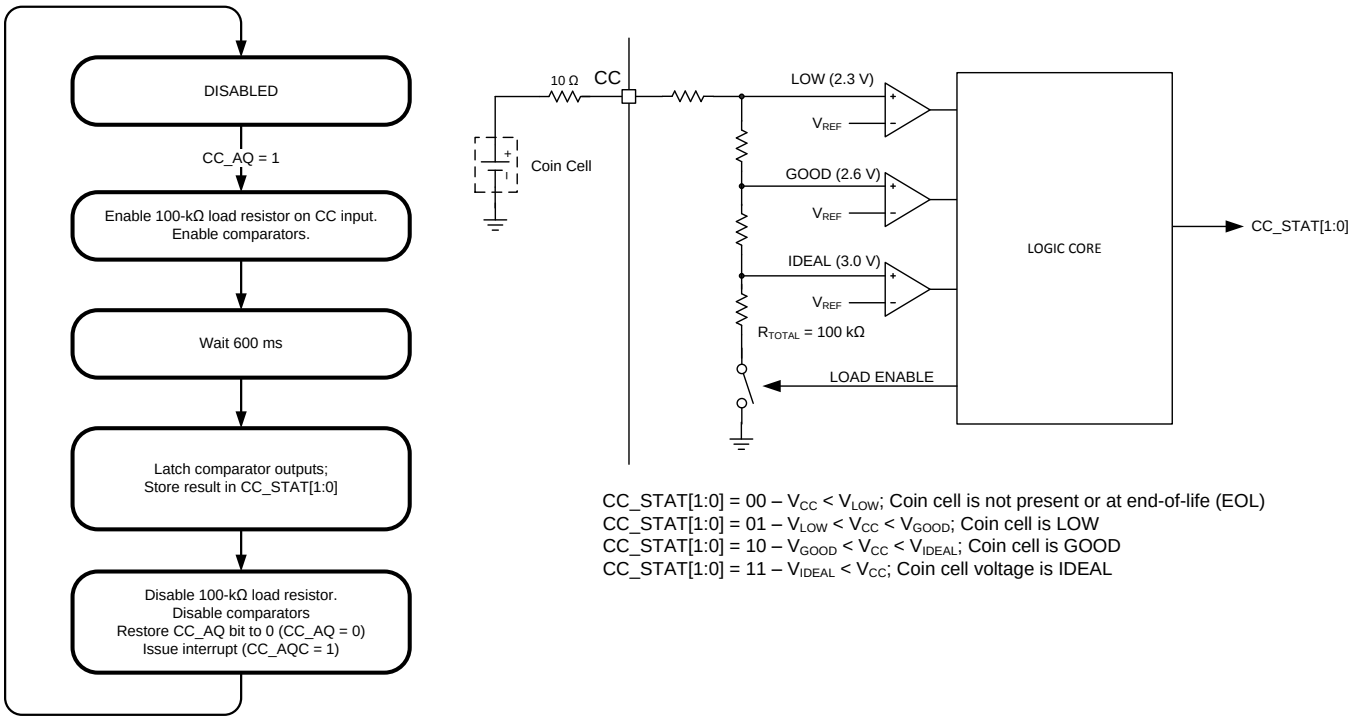


Figure 16. Left: Flow Chart for Acquiring Coin Cell Battery Voltage
Right: Comparator Circuit

7.3.1.10 UVLO

Power rails are only enabled if the input voltage measured at the IN_BIAS pin is greater than the under-voltage lockout threshold plus hysteresis (V_{UVLO} + V_{HYS}). Once the input voltage rises above this level, the input voltage may drop to the UVLO level before the PMIC shuts down. UVLO is deglitched by 5 ms on rising and falling edge.

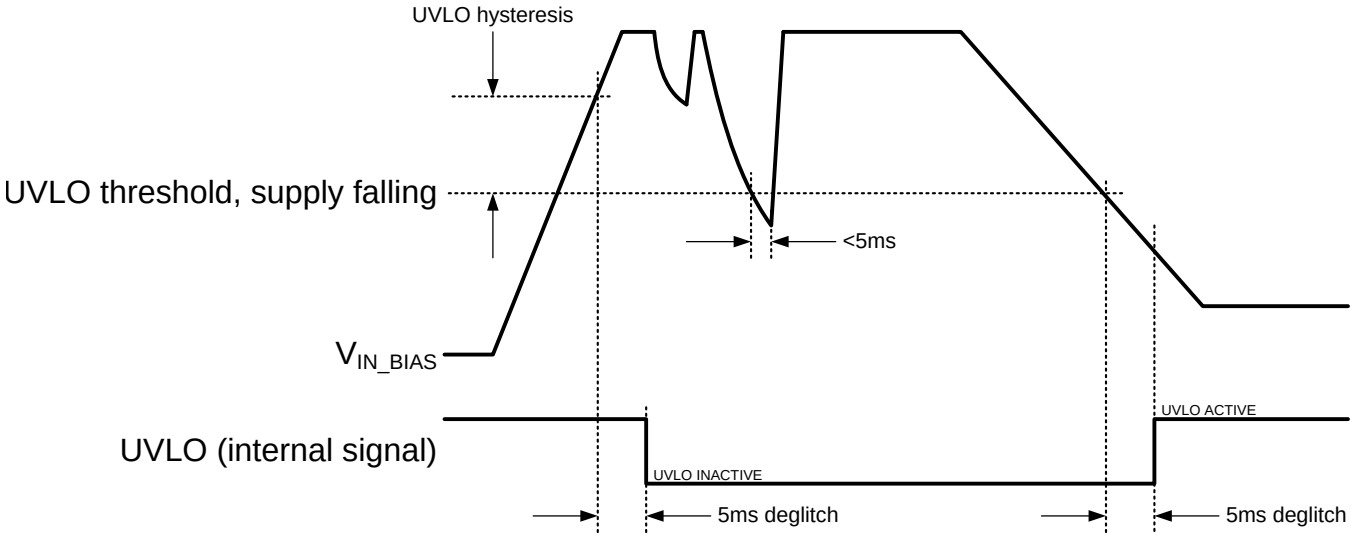


Figure 17. Definition of UVLO and Hysteresis

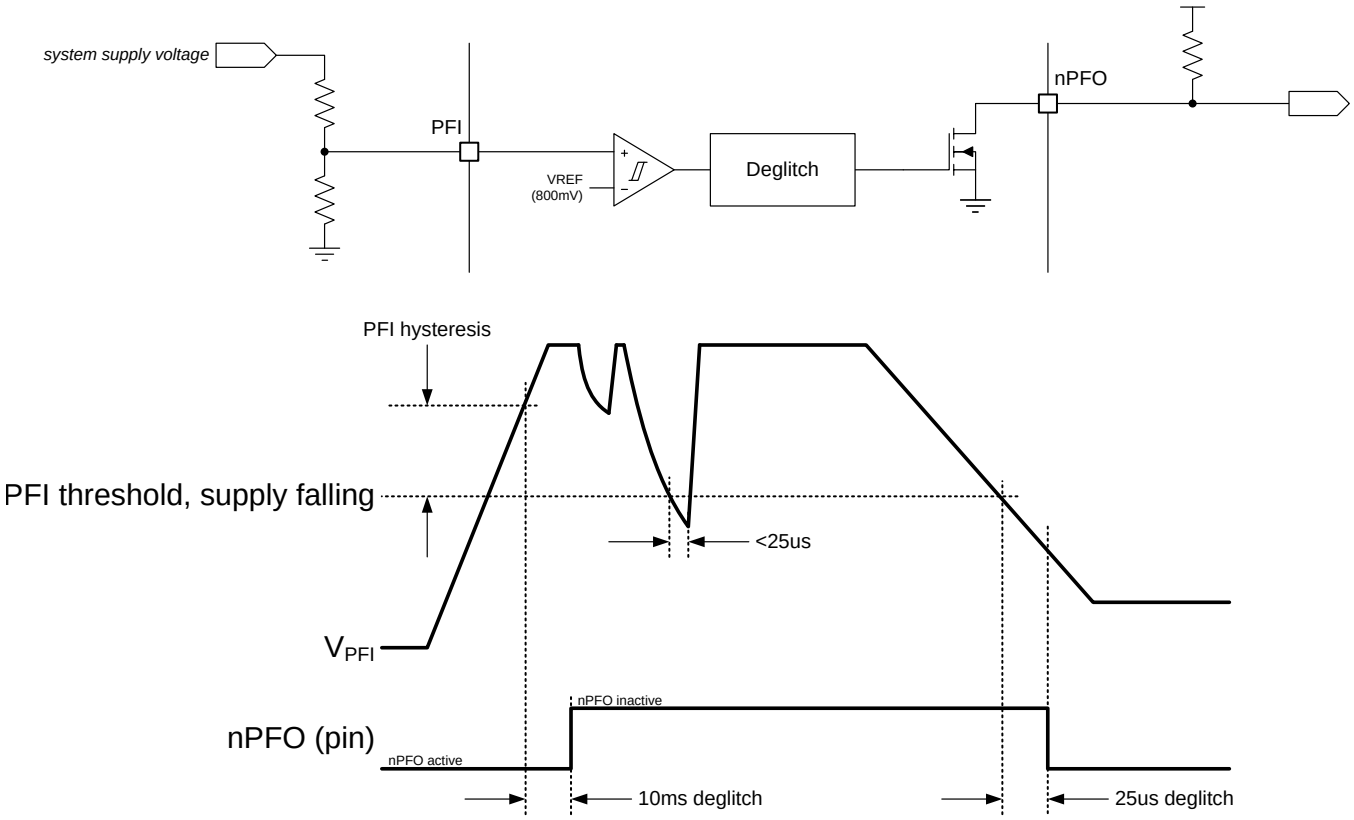
After the UVLO triggers, the internal LDO blocks current flow from its output capacitor back to the IN_BIAS pin, allowing the digital core and the discharge circuits to remain powered for a limited amount of time to properly shut-down and discharge the output rails. The hold-up time is determined by the size of the capacitor connected to INT_LDO. See *Internal LDO (INT_LDO)* for more details.

7.3.1.11 Power-Fail Comparator

The power-fail comparator notifies the system host if the system supply voltage drops and the system is at risk of shutting down. The comparator has an internal 800-mV threshold and the trip-point is adjusted by an external resistor divider.

By default, the power-fail comparator has no impact on any of the power rails or load switches. Load switches are configured individually, to be disabled when the PFI comparator trips to shed system load and extend hold-up time as described under *Current Limited Load Switches*. The power-fail comparator also triggers the power-down sequencer, such that all or selective rails power down when the system voltage fails. To tie the power-fail comparator into the power-down sequence, the OFFnPFO bit in the CONTROL register must be set to 1.

The power-fail comparator cannot be monitored by software, such that no interrupt or status bit is associated to this function.



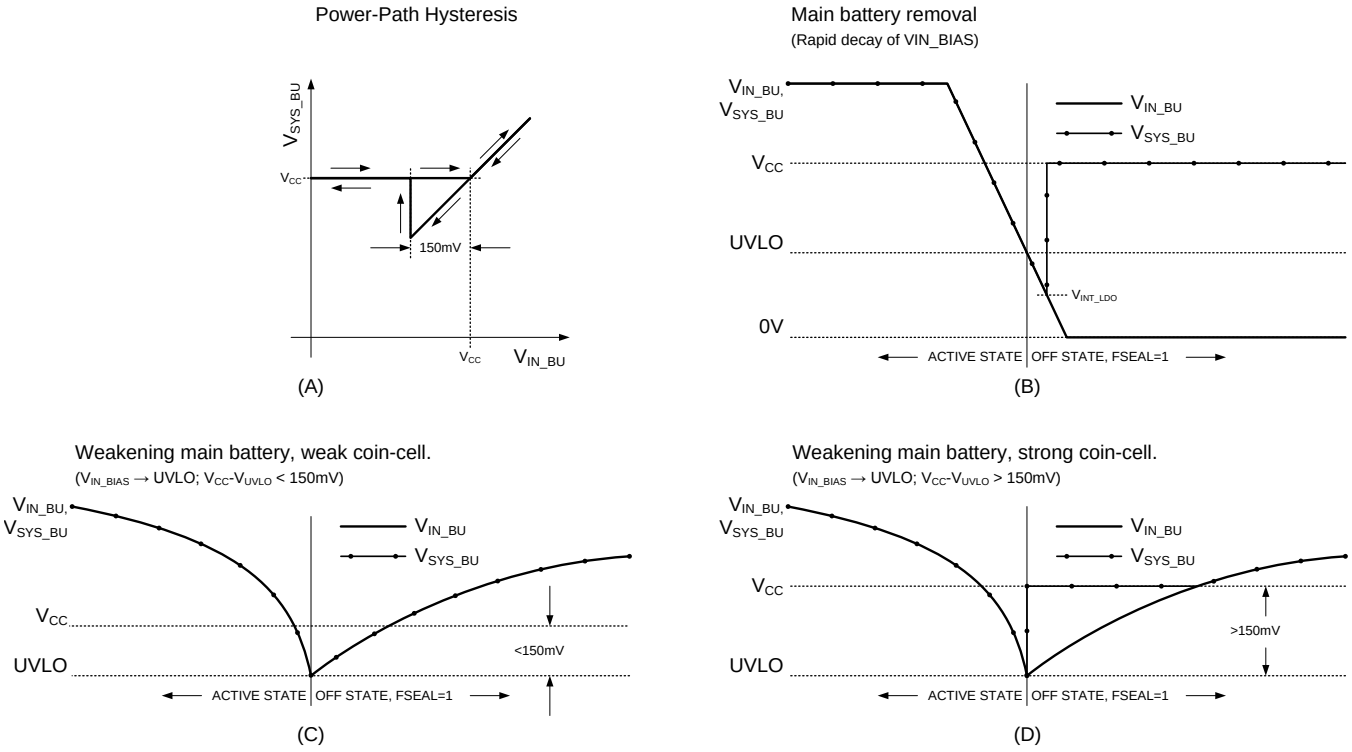
Top: Simplified circuit

Bottom: Timing diagram

Figure 18. Power-Fail Comparator

7.3.1.12 Battery-Backup Supply Power-Path

DCDC5 and DCDC6 are supplied from either the CC (coin-cell battery) input or IN_BU (main system supply). The power-path is designed to prioritize IN_BU to maximize coin-cell battery life. Whenever the PMIC is powered-up (WAIT_PWR_EN, ACTIVE, SUSPEND, RECOVERY state), the power-path is forced to select the IN_BU input. In OFF mode the power-path selects the higher of the two inputs with a built-in hysteresis of 150 mV as shown in Figure 19(A).



A. Power-path Hysteresis.
B. Main Supply is disconnected or decays rapidly.
C. System is supplied by Li-Ion battery with a weak coin-cell backup battery.
D. System is supplied by Li-Ion battery with a fresh coin-cell backup battery.

Figure 19. Switching Behavior of the Battery-Backup-Supply Power-Path

When V_{IN_BIAS} drops below the UVLO threshold, the PMIC shuts down all rails and enters OFF mode. At this point the power-path selects the higher of the two input supplies. If the coin-cell battery is less than 150 mV above the UVLO threshold, SYS_BU remains connected to IN_BU (see Figure 19(C)). If the coin-cell is >150 mV above the UVLO threshold, the power-path switches to the CC input as shown in Figure 19(D). With no load on the main supply, the input voltage may recover over time to a value greater than the coin-cell voltage and the power-path switches back to IN_BU. This is a typical behavior in a Li-Ion battery powered system.

Depending on the system load, V_{IN_BIAS} may drop below VI_{NT_LDO} before the power-down sequence is completed. In that case, INT_LDO is turned OFF and the digital core is reset forcing the unit into OFF mode and the power-path switches to IN_BU as shown in Figure 19(B).

7.3.1.12.1 Applications Without Backup Battery

In applications that require always-on supplies but no battery backup, the CC input to the power path must be connected to ground.

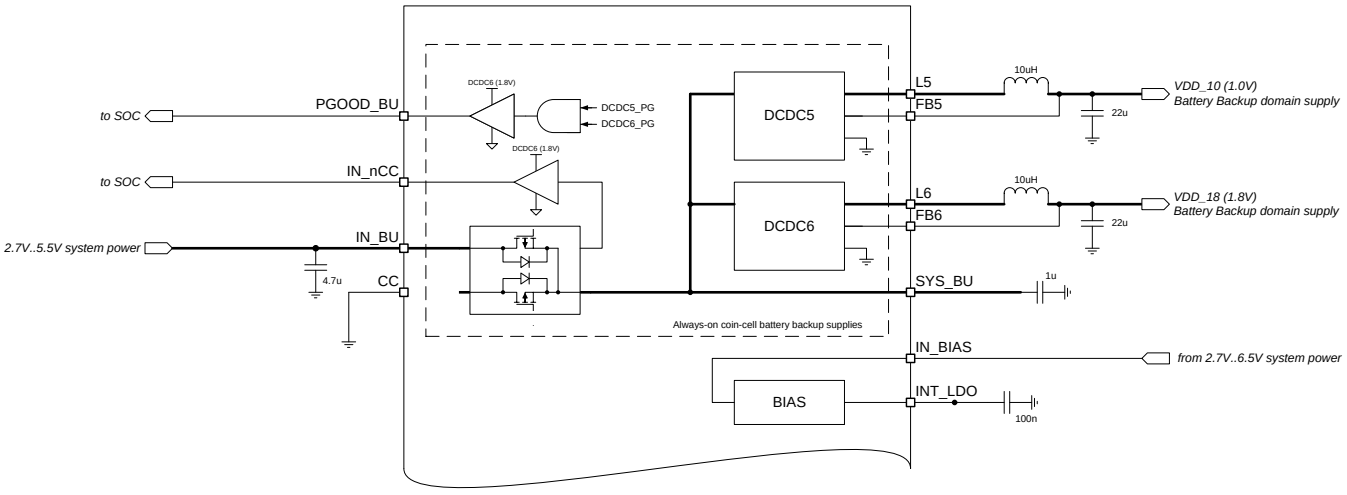


Figure 20. CC Input to Power Path

NOTE

In applications without backup battery, CC input must be tied to ground.

7.3.1.12.2 Applications Without Battery Backup Supplies

In applications that do not require always-on supplies, both inputs and the output of the power-path can simply be grounded. All pins related to DCDC5 and DCDC6 are also tied to ground, and PGOOD_BU and IN_nCC are kept floating. With the backup supplies completely disabled, the FSEAL bit in the STATUS register is undefined and should be ignored.

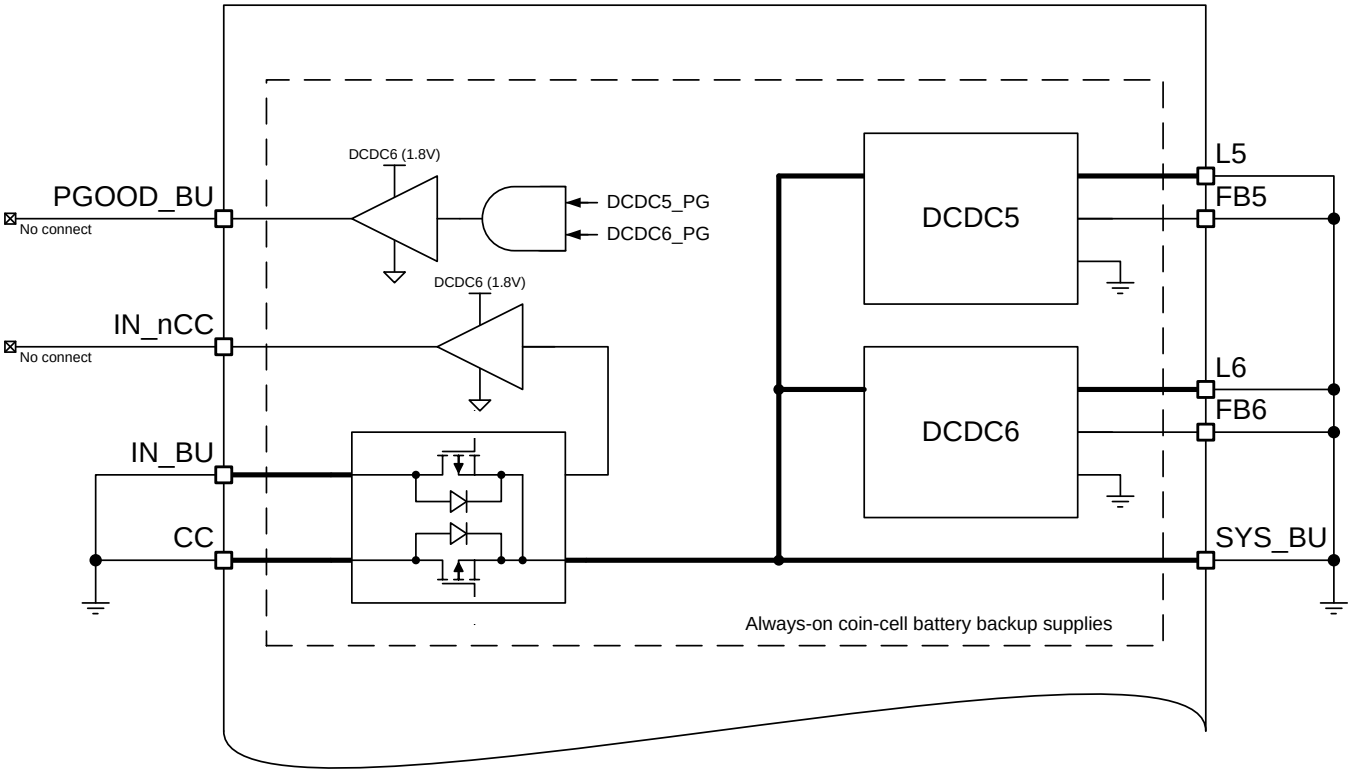


Figure 21. DCDC5 and DCDC6 Pins

NOTE

In applications that do not require always-on supplies, PGOOD_BU and IN_nCC can be kept floating. All other pins are tied to ground.

7.3.1.13 DCDC3 / DCDC4 Power-Up Default Selection

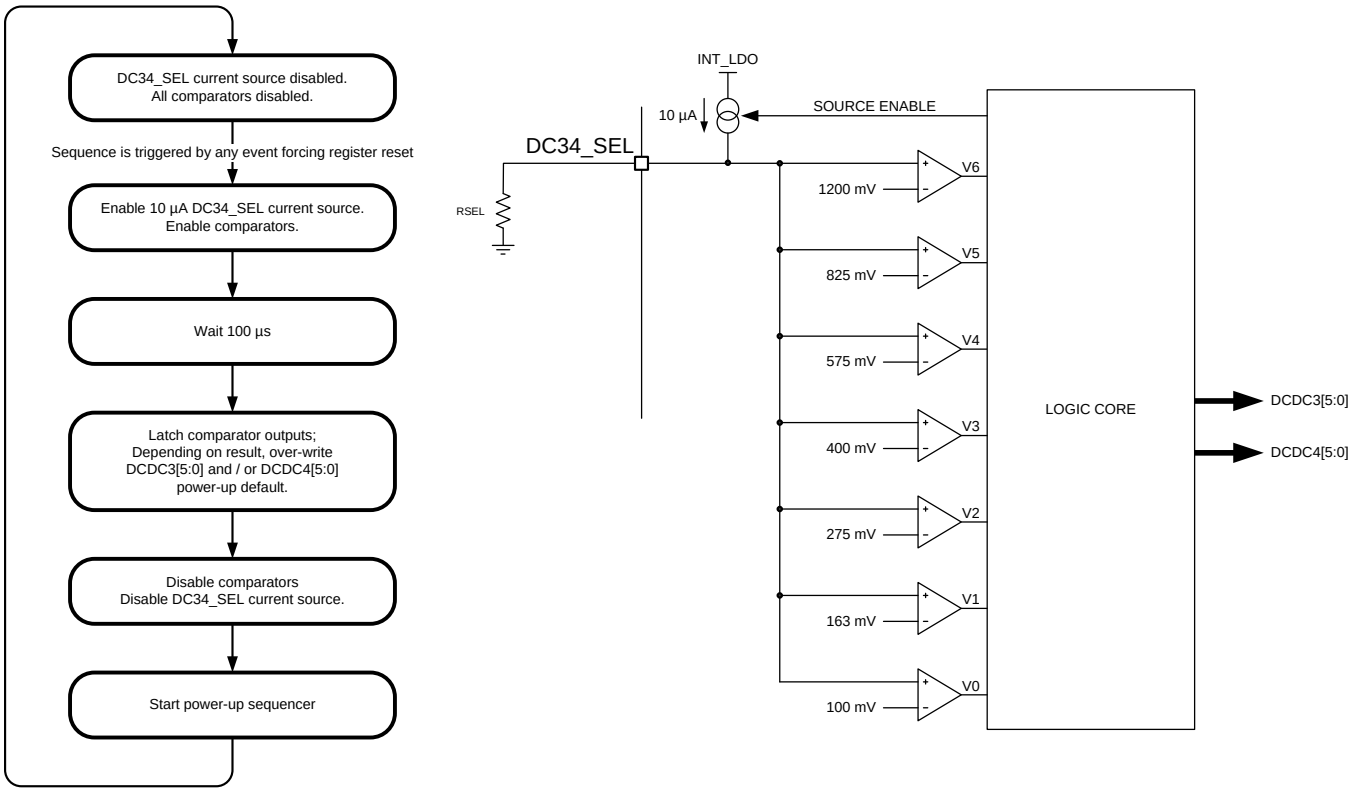


Figure 22. Left: Flow Chart for Selecting DCDC Power-Up Default Voltage Right: Comparator Circuit

Table 2. Power-Up Default Values of DCDC3 and DCDC4

RSEL [KΩ]			POWER-UP DEFAULT	
MIN	TYP	MAX	DCDC3[5:0]	DCDC4[5:0]
0	0	7.7	Programmed default (1.2 V)	Programmed default (3.3 V)
11.3	12.1	13.0	0x12 (1.35 V)	Programmed default (3.3 V)
18.1	20.0	22.0	0x18 (1.50 V)	Programmed default (3.3 V)
30.9	31.6	32.3	0x1F (1.80 V)	Programmed default (3.3 V)
44.8	45.3	46.4	0x3D (3.30 V)	0x01 (1.20 V)
64.2	64.9	66.3	Programmed default (1.2 V)	0x07 (1.35 V)
92.9	95.3	96.9	Programmed default (1.2 V)	0x0D (1.50 V)
135.3	150	Tied to INT_LDO	Programmed default (1.2 V)	0x14 (1.80 V)

7.3.1.14 I/O Configuration

The device has two GPIOs and one GPO pin which are configured as follows:

- GPIO1:
  - General-purpose, open-drain output controlled by GPO1 user bit or sequencer
  - DDR3 reset input signal from SOC. Signal is either latched or passed-trough to GPO2 pin. See Table 3 for details.
- GPO2:
  - General-purpose output controlled by GPO2 user bit
  - DDR3 reset output signal. Signal is controlled by GPIO1 and PGOOD. See Table 4 for details.
  - Output buffer is configured as open-drain or push-pull.
- GPIO3:
  - General-purpose, open-drain output controlled by GPO3 user bit or sequencer
  - Reset input-signal for DCDC1 and DCDC2

Table 3. GPIO1 Configuration

IO1_SEL (EEPROM)	GPO1 (USER BIT)	PGOOD (PMIC SIGNAL)	GPIO1 (I/O PIN)	COMMENTS
0	0	X	0	Open-drain output, driving low
0	1	X	HiZ	Open-drain output, HiZ
1	X	0	X	Pin is configured as input and intended as DDR RESET signal. Coming out of POR, GPO2 is driven low. Otherwise, GPO2 status is latched at falling edge of PGOOD. See Figure 25.
1	X	1	0	Pin is configured as input and intended as DDR RESET signal. GPO2 is driven low.
1	X	1	1	Pin is configured as input and intended as DDR RESET signal. GPO2 is driven high.

Table 4. GPO2 Configuration

IO1_SEL (EEPROM)	GPO2_BUF (EEPROM)	GPO2 (USER BIT)	COMMENTS
0	0	0	GPO2 is open drain output controlled by GPO2 user bit (driving low).
0	0	1	GPO2 is open drain output controlled by GPO2 user bit (HiZ).
0	1	0	GPO2 is push-pull output controlled by GPO2 user bit (driving low).
0	1	1	GPO2 is push-pull output controlled by GPO2 user bit (driving high).
1	0	X	GPO2 is open drain output controlled by GPIO1/PGOOD.
1	1	X	GPO2 is push-pull output controlled by GPIO1/PGOOD.

Table 5. GPO3 Configuration

DC12_RST (EEPROM)	GPO3 (USER BIT)	GPIO3 (I/O PIN)	COMMENTS
0	0	0	Open-drain output, driving low
0	1	HiZ	Open-drain output, HiZ
1	X	Active low	GPIO3 is DCDC1 and DCDC2 reset input signal to PMIC (active low). See *Using GPIO3 as Reset Signal to DCDC1 and DCDC2* for details.

7.3.1.14.1 Configuring GPO2 as Open-Drain Output

GPO2 may be configured as open-drain or push-pull output. The supply for the push-pull driver is internally connected to the IN_LS1 input pin, whereas an external pullup resistor and supply are required in the open-drain configuration. Because of the internal connection to IN_LS1, the external pullup supply must not exceed the voltage on the IN_LS1 pin, otherwise leakage current may be observed from GPO2 to IN_LS1 as shown in Figure 23.

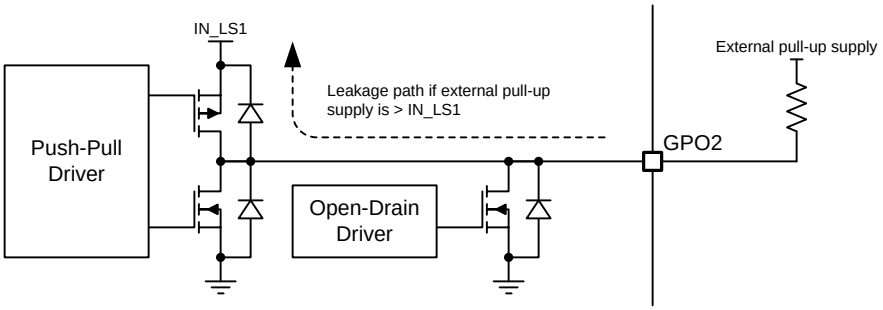


Figure 23. GPO2 as Open-Drain Output

NOTE

When configured as open-drain output, the external pullup supply must not exceed the voltage level on IN_LS1 pin.

7.3.1.14.2 Using GPIO3 as Reset Signal to DCDC1 and DCDC2

With the DC12_RST bit set to 1, GPIO3 is an edge-sensitive reset input to the PMIC. The reset signal affects DCDC1 and DCDC2 only, so that only those two registers are reset to the power-up default whenever GPIO3 input transitions from high to low, while all other registers maintain their current values. DCDC1 and DCDC2 transition back to the default value following the SLEW settings, and are not power cycled. This function recovers the processor from reset events while in low-power mode.

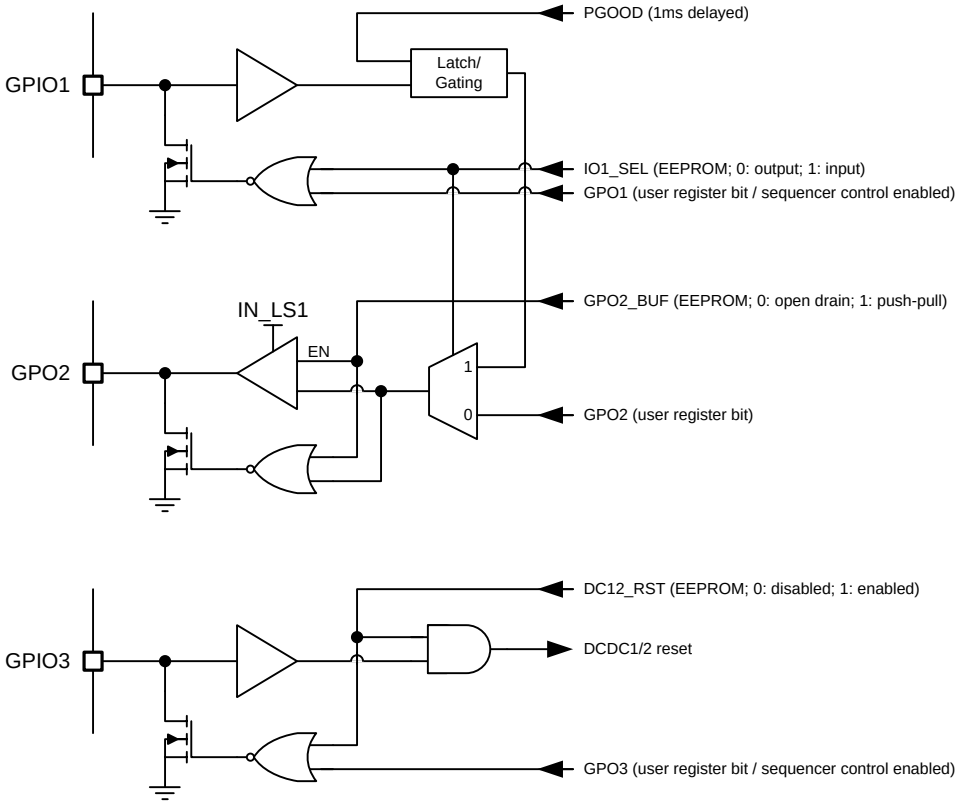


Figure 24. I/O Pin Logic

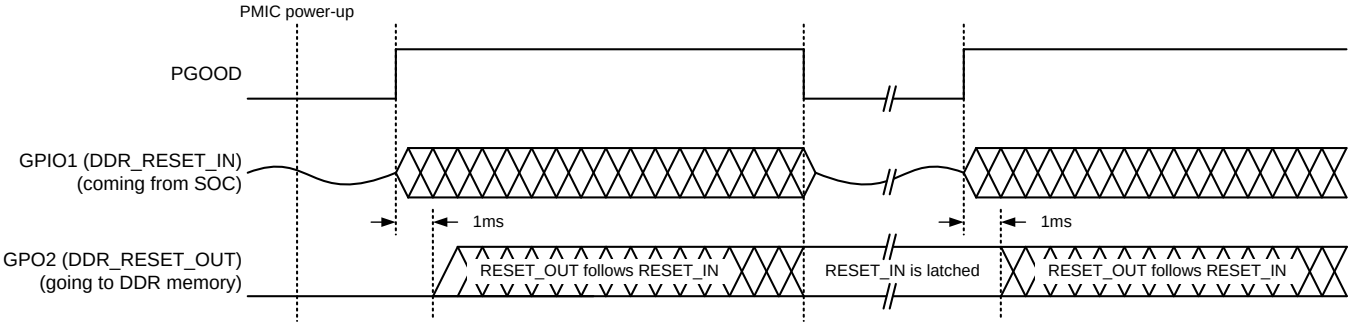


Figure 25. DDR3 Reset Timing Diagram

NOTE

GPIO must be configured as input (IO1_SEL = 1). GPO2 is automatically configured as output.

7.3.1.15 Push Button Input (PB)

The PB pin is a CMOS-type input used to power-up the PMIC. Typically, the PB pin is connected to a momentary switch to ground and an external pullup resistor. The power-up sequence is triggered if the PB input is held low for 600 ms.

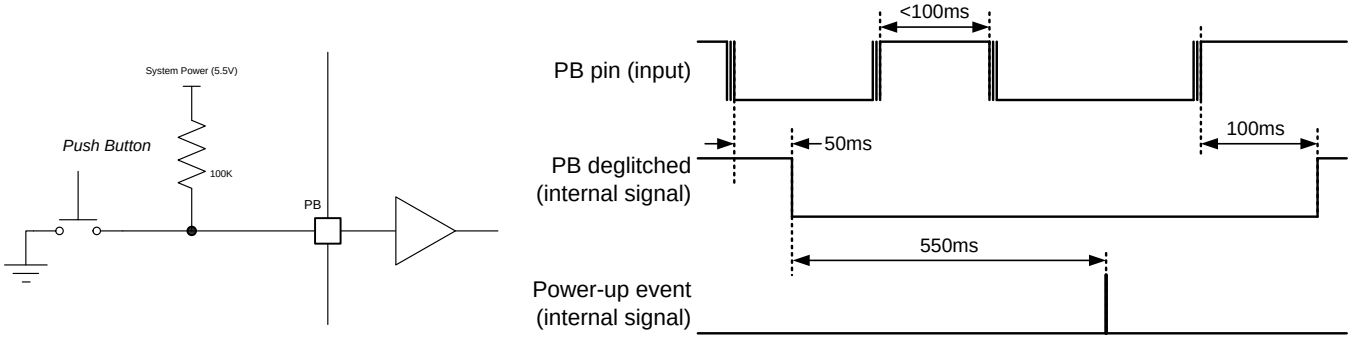


Figure 26. Left: Typical PB Input Circuit
Right: Push-Button Input (PB) Deglitch and Power-Up Timing

In ACTIVE mode, the TPS65218x monitors the PB input and issues an interrupt when the pin status changes, such as when it drops below or rises above the PB input-low or input-high thresholds. The interrupt is masked by the PBM bit in the INT_MASK1 register.

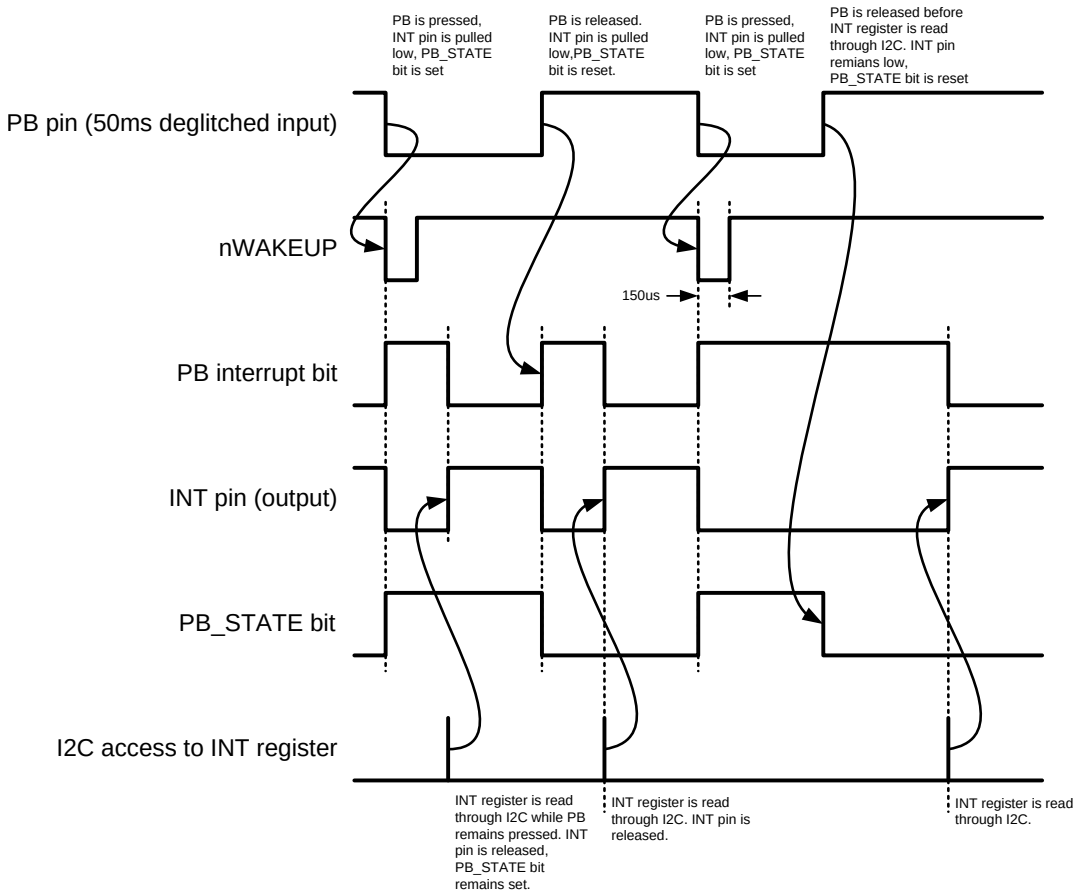


Figure 27. PB Input-Low or Input-High Thresholds

NOTE

Interrupts are issued whenever the PB pin status changes. The PB_STATE bit reflects the current status of the PB input. nWAKEUP is pulled low for 150 µs on every falling edge of PB.

7.3.1.15.1 Signaling PB-Low Event on the nWAKEUP Pin

In ACTIVE state, the nWAKEUP pin is pulled low for five 32-kHz clock cycles (approximately 150 µs) whenever a falling edge on the PB input is detected. This allows the host processor to wakeup from DEEP SLEEP mode of operation.

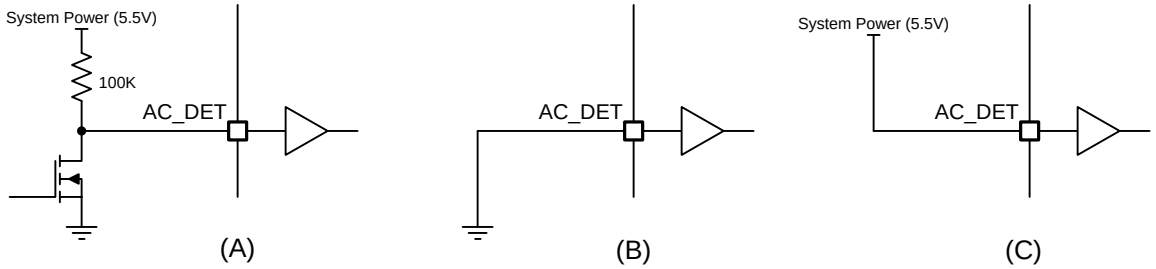
7.3.1.15.2 Push Button Reset

If the PB input is pulled low for 8 s (15 s if TRST = 1) or longer, all rails except for DCDC5 and DCDC6 are disabled, and the device enters the RECOVERY state. The device powers up automatically after the 500 ms power-down sequence is complete, regardless of the state of the PB input. Holding the PB pin low for 8 s (15 s if TRST = 1), only turns off the device temporarily and forces a system restart, and is not a power-down function. If the PB is held low continuously, the device power-cycles in 8-s and 15-s intervals.

7.3.1.16 AC_DET Input (AC_DET)

The AC_DET pin is a CMOS-type input used in three different ways to control the power-up of the PMIC:

- In a battery operated system, AC_DET is typically connected to an external battery charger with an open-drain power-good output pulled low when a valid charger supply is connected to the system. A falling edge on the AC_DET pin causes the PMIC to power up.
- In a non-portable system, the AC_DET pin may be shorted to ground and the IC powers up whenever system power is applied to the chip.
- If none of the above behaviors are desired, AC_DET may be tied to system power (IN_BIAS). Power-up is then controlled through the push-button input only.



A. Portable Systems
B. Non-portable Systems
C. Disabled

Figure 28. AC_DET Pin Configurations

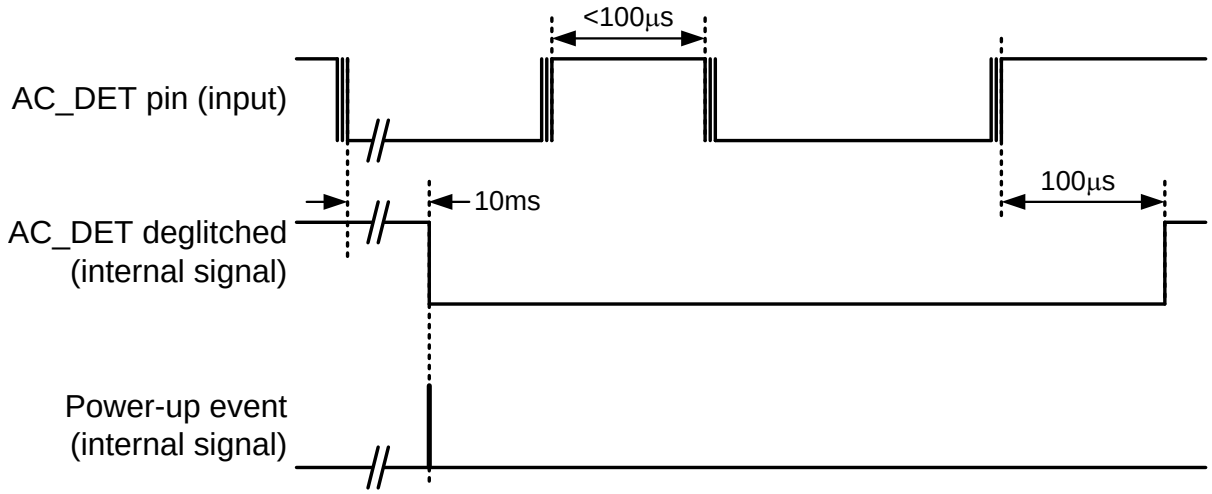


Figure 29. AC_DET Input Deglitch and Power-Up Timing (Portable Systems)

In ACTIVE state, the TPS65218x monitors the AC_DET input and issues an interrupt when the pin status changes, such as when it drops below or rises above the AC_DET input-low or input-high thresholds. The interrupt is masked by the ACM bit in the INT_MASK1 register.

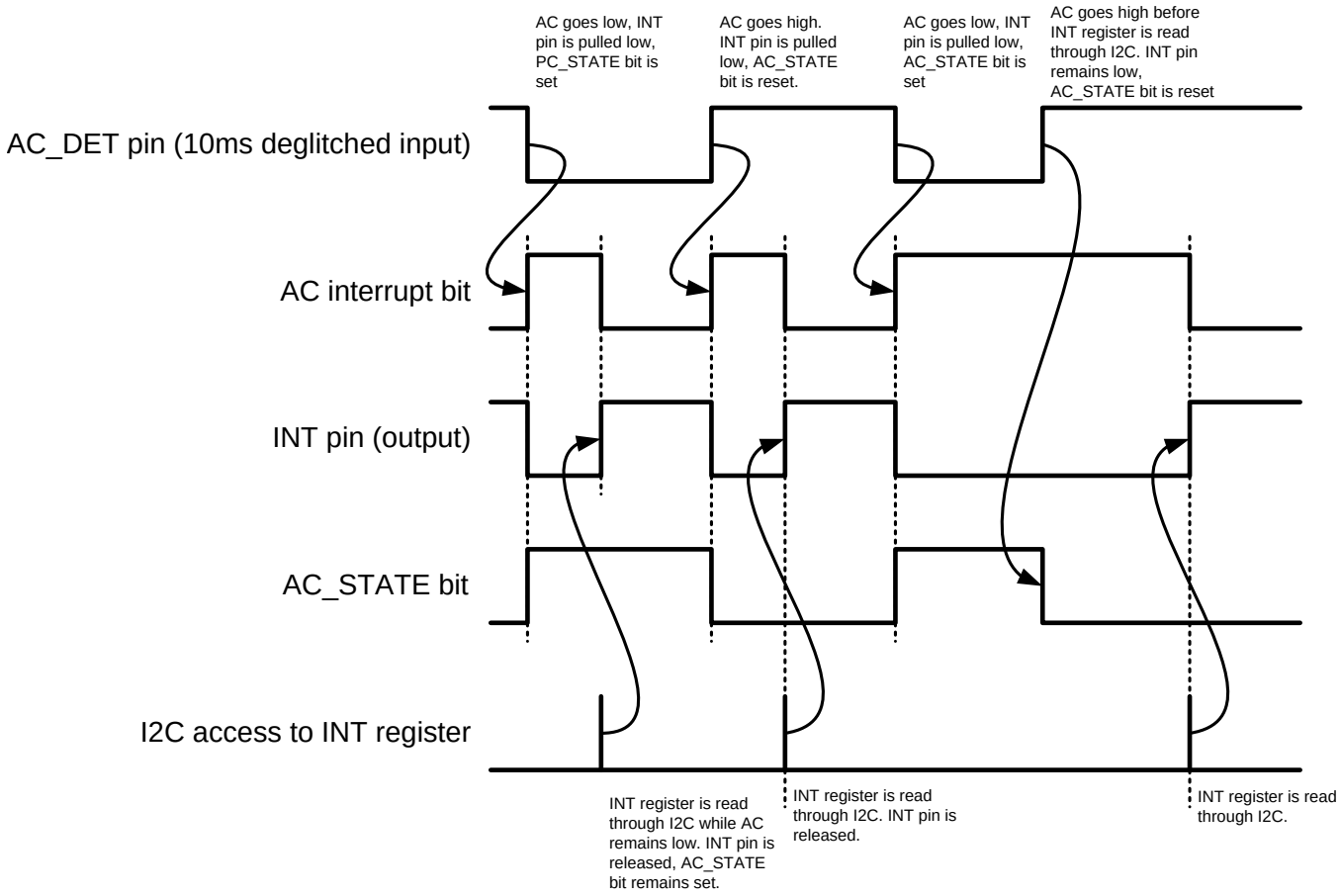


Figure 30. AC_STATE Pin

NOTE

Interrupts are issued whenever the AC_DET pin status changes. The AC_STATE bit reflects the current status of the AC_DET input.

7.3.1.17 Interrupt Pin (INT)

The interrupt pin signals any event or fault condition to the host processor. Whenever a fault or event occurs in the IC, the corresponding interrupt bit is set in the INT register, and the open-drain output is pulled low. The INT pin is released (returns to Hi-Z state) and fault bits are cleared when the host reads the INT register. If a failure persists, the corresponding INT bit remains set and the INT pin is pulled low again after a maximum of 32 µs.

The MASK register masks events from generating interrupts. The MASK settings affect the INT pin only, and have no impact on the protection and monitor circuits.

7.3.1.18 I²C Bus Operation

The TPS65218x hosts a slave I²C interface (address 0x24) that supports data rates up to 400kbps, auto-increment addressing. (1)

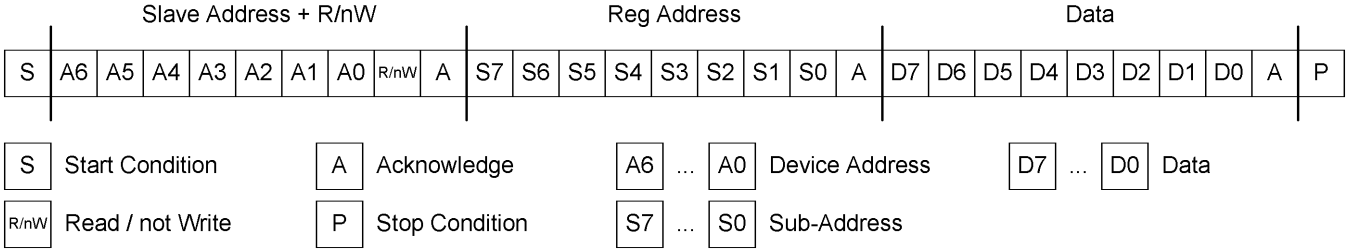
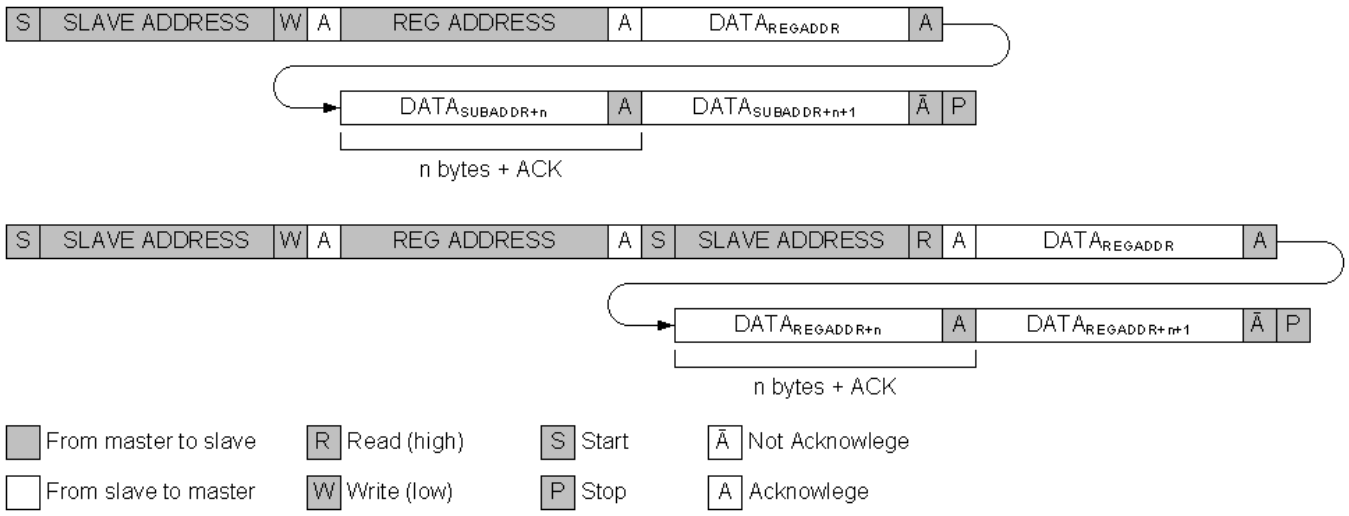


Figure 31. Subaddress in I²C Transmission

The I²C bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the slave terminals. Each device has an open drain output to transmit data on the serial data line. An external pullup resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission initiates with a start bit from the controller as shown in Figure 33. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device receives serial data on the SDA input and checks for valid address and control information. If the appropriate slave address is set for the device, the device issues an acknowledge pulse and prepares to receive register address and data. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge issues after the reception of valid slave address, register-address, and data words. The I²C interfaces auto-sequence through register addresses, so that multiple data words can be sent for a given I²C transmission. Reference Figure 32 and Figure 33 for details.

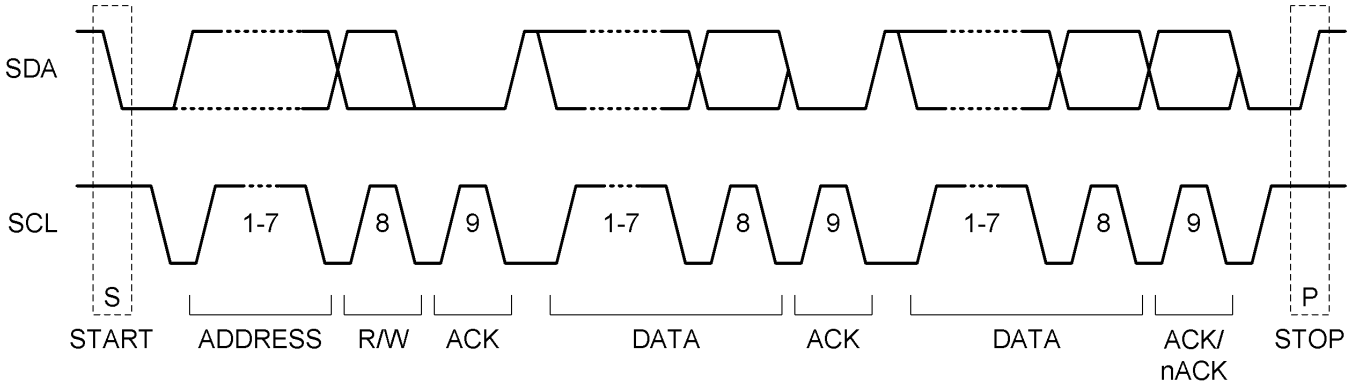


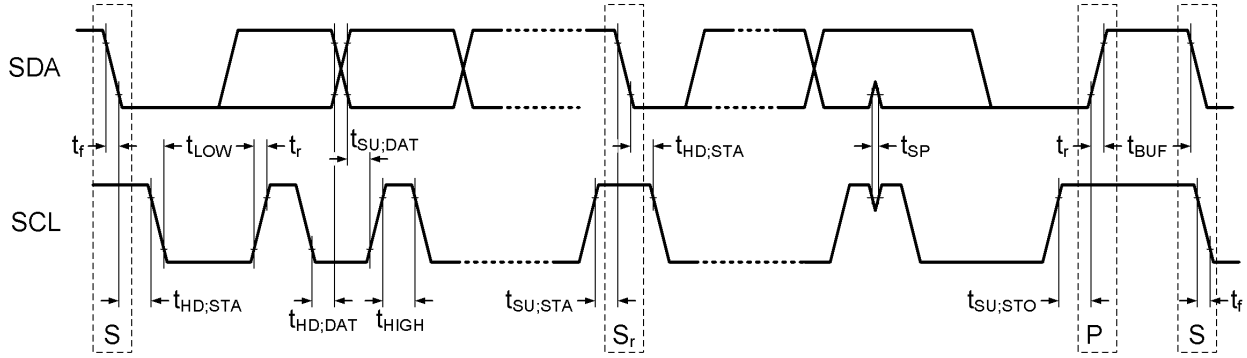
Top: Master Writes Data to Slave

Bottom: Master Reads Data from Slave

Figure 32. I²C Data Protocol

(1) Note: The SCL duty cycle at 400 kHz must be >40%.





Top: I²C Start/Stop/Acknowledge Protocol

Bottom: I²C Data Transmission Timing

Figure 33. I²C Protocol and Transmission Timing

7.4 Device Functional Modes

7.4.1 Modes of Operation

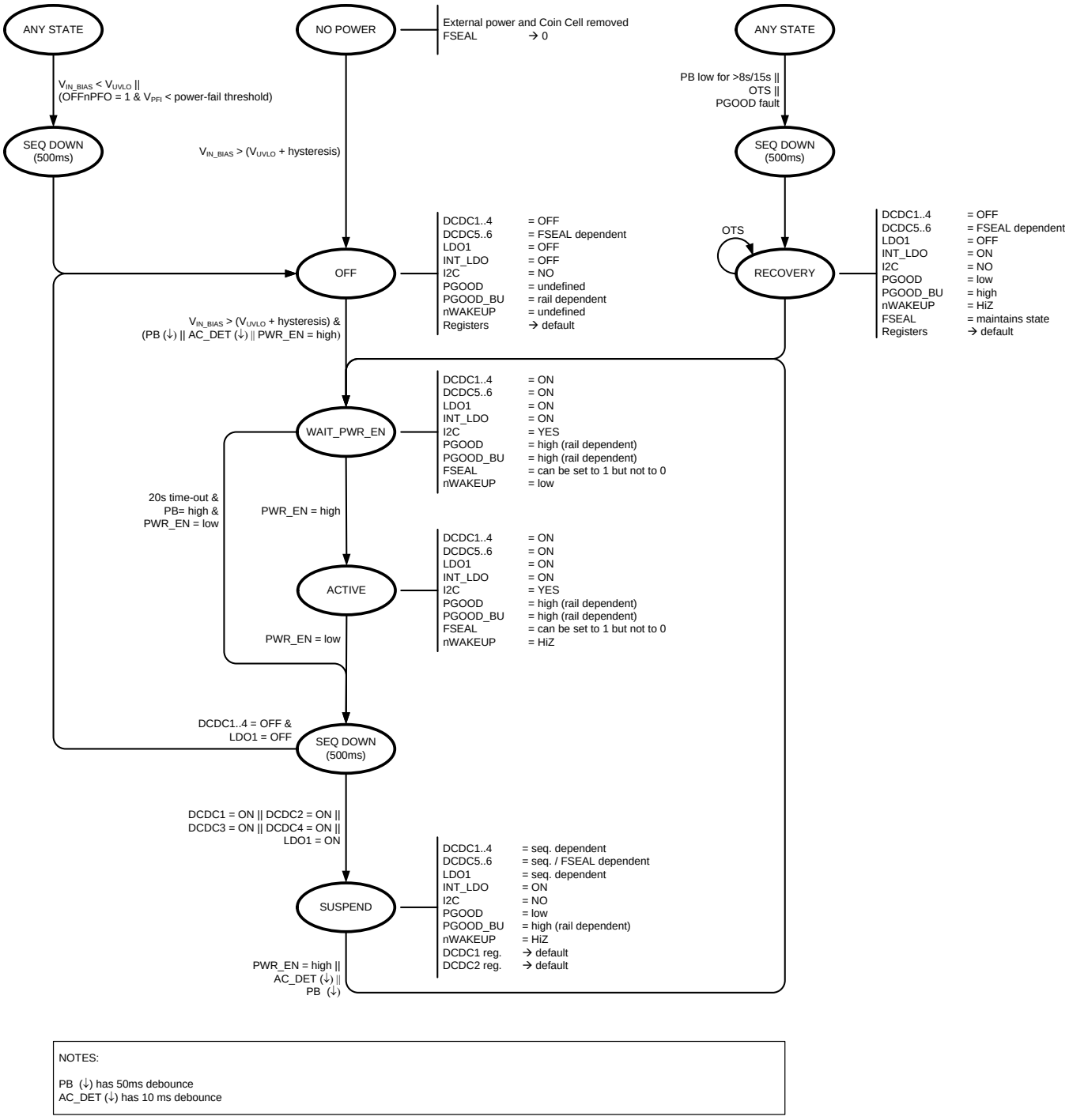


Figure 34. Modes of Operation Diagram

Device Functional Modes (continued)

7.4.2 OFF

In OFF mode, the PMIC is completely shut down with the exception of a few circuits to monitor the AC_DET, PWR_EN and PB input. All power rails are turned off and the registers are reset to their default values. The I^2C communication interface is turned off. This is the lowest-power mode of operation. To exit OFF mode V_{IN_BIAS} must exceed the UVLO threshold and one of the following wake-up events must occur:

- The PB input is pulled low.
- THE AC_DET input is pulled low.
- The PWR_EN input is pulled high.

To enter OFF state, ensure all power rails are assigned to e sequencer, then pull the PWR_EN pin low. Additionally, if the OFFnPFO bit is set to 1 and the PFI input falls below the power fail threshold the device transitions to the OFF state. If the freshness seal is broken, DCDC5 and DCDC6 remains on in the OFF state.

If a PGOOD or OTS fault occurs while in the ACTIVE state, TPS65218x will transition to the RESET state.

7.4.3 ACTIVE

This is the typical mode of operation when the system is up and running. All DCDC converters, LDOs, and load switches are operational and can be controlled through the I^2C interface. After a wake-up event, the PMIC enables all rails controlled by the sequencer and pulls the nWAKEUP pin low to signal the event to the host processor. The device only enters ACTIVE state if the host asserts the PWR_EN pin within 20 s after the wake-up event. Otherwise it will enter OFF state. The nWAKEUP pin returns to HiZ mode after the PWR_EN pin is asserted. ACTIVE state can also be directly entered from SUSPEND state by pulling the PWR_EN pin high. See SUSPEND state description for details. To exit ACTIVE mode, the PWR_EN pin must be pulled low.

7.4.4 SUSPEND

SUSPEND state is a low-power mode of operation intended to support system standby. Typically all power rails are turned off with the exception of any rail with an SEQ register set to 0h. DCDC5 and DCDC6 also remain enabled if the freshness seal is broken. To enter SUSPEND state, pull the PWR_EN pin low. All power rails controlled by the power-down sequencer are shut down, and after 500 ms the device enters SUSPEND state. All rails not controlled by the power-down sequencer will maintain state. Note that all register values are reset as the device enters the SUSPEND state. The device enters ACTIVE state after it detects a wake-up event as described in the sections above.

7.4.5 RESET

The TPS65218x can be reset by holding the PB pin low for more than 8 or 15 s, depending on the value of the TRST bit. All rails are shut down by the sequencer and all register values reset to their default values. Rails not controlled by the sequencer are shut down additionally. Note that the RESET function power-cycles the device and only temporarily shuts down the output rails. Resetting the device does not lead to OFF state. If the PB_IN pin is kept low for an extended amount of time, the device continues to cycle between ACTIVE and RESET state, entering RESET every 8 or 15 s.

The device is also reset if a PGOOD or OTS fault occurs. The TPS65218x remains in the recovery state until the fault is removed, at which time it transitions back to the ACTIVE state.

7.5 Register Maps

7.5.1 Password Protection

Registers 0x11h through 0x26h are protected against accidental write by a 8-bit password. The password must be written prior to writing to a protected register and automatically resets to 0x00h after the next I2C transaction, regardless of the register accessed or transaction type (read or write). The password is required for write access only and is not required for read access.

To write to a protected register:

1. Write the address of the destination register, XORed with the protection password (0x7Dh), to the PASSWORD register (0x10h).
2. Write the data to the password protected register.
3. If the content of the PASSWORD register XORed with the address send matches 0x7Dh, the data transfers to the protected register. Otherwise, the transaction is ignored. In either case the PASSWORD register resets to 0x00 after the transaction.

The cycle must be repeated for any other register that is Level1 write protected.

7.5.2 Freshness Seal (FSEAL) Bit

The FSEAL (freshness seal) bit prevents accidental shut-down of the always-on supplies, DCDC5 and DCDC6. The FSEAL bit exists in a default state of 0, and can be set to 1 and reset to 0 once for factory testing. The second time the bit is set to 1, it remains 1 and cannot reset again under software control. Coin-cell battery and main supply must be disconnected from the IC to reset the FSEAL bit again. With the FSEAL bit set to 1, DCDC5 and DCDC6 are forced ON regardless of the state of the DC5_EN and DC6_EN bit, and the rails do not turn off when the IC enters OFF mode.

A consecutive write of [0xB1, 0xFE, 0xA3] to the password register sets the FSEAL bit to 1. The three bytes must be written consecutively for the sequence to be valid. No other read or write transactions are allowed between the three bytes, or the sequence is invalid. After a valid sequence, the FSEAL bit in the STATUS register reflects the new setting.

After setting the FSEAL bit, the IC can enter OFF or any other mode of operation without affecting the state of the FSEAL bit, provided the coin-cell supply remains connected to the chip.

A second write of [0xB1, 0xFE, 0xA3] to the password register resets the FSEAL bit to 0. The three bytes must be written consecutively for the sequence to be valid.

A third write of [0xB1, 0xFE, 0xA3] to the password register sets the FSEAL bit to 1 and locks it into this state for as long as the coin-cell supply (CC) remains connected to the chip.

7.5.3 FLAG Register

The FLAG register contains a bit for each power rail and GPO to keep track of the enable state of the rails while the system is suspended. The following rules apply to the FLAG register:

- The power-up default value for any flag bit is 0.
- Flag bits are read-only and cannot be written to.
- Upon entering a SUSPEND state, the flag bits are set to same value as their corresponding ENABLE bits. Rails and GPOs enabled in a SUSPEND state have flag bits set to 1, while all other flag bits are set to 0. Flag bits are not updated while in the SUSPEND state or when exiting the SUSPEND state.
- The FLAG register is static in WAIT_PWR_EN and ACTIVE state. The FLAG register reflects the enable state of DCDC1, 2, 3, 4, LDO1, and GPO1, 2, 3 during the last SUSPEND state.

The host processor reads the FLAG register to determine if the system powered up from the OFF or SUSPEND state. In the SUSPEND state, typically the DDR memory is kept in self refresh mode and therefore the DC3_FLG or DC4_FLG bits are set.

Register Maps (continued)

7.5.4 TPS65218x Registers

Table 6 lists the memory-mapped registers for the TPS65218x. All register offset addresses not listed in Table 6 should be considered as reserved locations and the register contents should not be modified.

Table 6. TPS65218x Registers

SUBADDRESS	ACRONYM	REGISTER NAME	R/W	PASSWORD PROTECTED	SECTION
0x0h	CHIPID	CHIP ID	R	No	*CHIPID Register (subaddress = 0x0h) [reset = 0x1h]*
0x1h	INT1	INTERRUPT 1	R	No	*INT1 Register (sub-address= 0x1h) [reset = 0x0h]*
0x2h	INT2	INTERRUPT 2	R	No	*INT2 Register (subaddress = 0x2h) [reset = 0x0h]*
0x3h	INT_MASK1	INTERRUPT MASK 1	R/W	No	*INT_MASK1 Register (subaddress = 0x3h) [reset = 0x0h]*
0x4h	INT_MASK2	INTERRUPT MASK 2	R/W	No	*INT_MASK2 Register (subaddress = 0x4h) [reset = 0x0h]*
0x5h	STATUS	STATUS	R	No	*STATUS Register (subaddress = 0x5h) [reset = 0x0h]*
0x6h	CONTROL	CONTROL	R/W	No	*CONTROL Register (subaddress = 0x6h) [reset = 0x0h]*
0x7h	FLAG	FLAG	R	No	*FLAG Register (subaddress = 0x7h) [reset = 0x0h]*
0x10h	PASSWORD	PASSWORD	R/W	No	*PASSWORD Register (subaddress = 0x10h) [reset = 0x0h]*
0x11h	ENABLE1	ENABLE 1	R/W	Yes	*ENABLE1 Register (subaddress = 0x11h) [reset = 0x0h]*
0x12h	ENABLE2	ENABLE 2	R/W	Yes	*ENABLE2 Register (subaddress = 0x12h) [reset = 0x0h]*
0x13h	CONFIG1	CONFIGURATION 1	R/W	Yes	*CONFIG1 Register (subaddress = 0x13h) [reset = 0x48h]*
0x14h	CONFIG2	CONFIGURATION 2	R/W	Yes	*CONFIG2 Register (subaddress = 0x14h) [TPS65218 reset = 0xC0h; TPS65218B101 reset = 0x80h]*
0x15h	CONFIG3	CONFIGURATION 3	R/W	Yes	*CONFIG3 Register (subaddress = 0x15h) [reset = 0x0h]*
0x16h	DCDC1	DCDC1 CONTROL	R/W	Yes	*DCDC1 Register (offset = 0x16h) [reset = 0x99h]*
0x17h	DCDC2	DCDC2 CONTROL	R/W	Yes	*DCDC2 Register (subaddress = 0x17h) [reset = 0x99h]*
0x18h	DCDC3	DCDC3 CONTROL	R/W	Yes	*DCDC3 Register (subaddress = 0x18h) [reset = 0x8Ch]*
0x19h	DCDC4	DCDC4 CONTROL	R/W	Yes	*DCDC4 Register (subaddress = 0x19h) [reset = 0xB2h]*
0x1Ah	SLEW	SLEW RATE CONTROL	R/W	Yes	*SLEW Register (subaddress = 0x1Ah) [reset = 0x6h]*
0x1Bh	LDO1	LDO1 CONTROL	R/W	Yes	*LDO1 Register (subaddress = 0x1Bh) [reset = 0x1Fh]*
0x20h	SEQ1	SEQUENCER 1	R/W	Yes	*SEQ1 Register (subaddress = 0x20h) [reset = 0x0h]*
0x21h	SEQ2	SEQUENCER 2	R/W	Yes	*SEQ2 Register (subaddress = 0x21h) [reset = 0x0h]*
0x22h	SEQ3	SEQUENCER 3	R/W	Yes	*SEQ3 Register (subaddress = 0x22h) [reset = 0x98h]*
0x23h	SEQ4	SEQUENCER 4	R/W	Yes	*SEQ4 Register (subaddress = 0x23h) [reset = 0x75h]*

Register Maps (continued)

Table 6. TPS65218x Registers (continued)

SUBADDRESS	ACRONYM	REGISTER NAME	R/W	PASSWORD PROTECTED	SECTION
0x24h	SEQ5	SEQUENCER 5	R/W	Yes	*SEQ5 Register (subaddress = 0x24h) [reset = 0x12h]*
0x25h	SEQ6	SEQUENCER 6	R/W	Yes	*SEQ6 Register (subaddress = 0x25h) [reset = 0x63h]*
0x26h	SEQ7	SEQUENCER 7	R/W	Yes	*SEQ7 Register (subaddress = 0x26h) [reset = 0x3h]*

7.5.4.1 CHIPID Register (subaddress = 0x0h) [reset = 0x1h]

CHIPID is shown in Figure 35 and described in Table 7.

Figure 35. CHIPID Register

7	6	5	4	3	2	1	0
CHIP						REV	
R-0h						R-1h	

Table 7. CHIPID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	CHIP	R	0h	Chip ID 00000b = TPS65218x 00001b = Future use ... 11111b = Future use
2-0	REV	R	3h	Revision code 000b = Revision 1.0 001b = Revision 1.1 010b = Revision 2.0 011b = Revision 2.1 ... 111b = Future use

7.5.4.2 INT1 Register (sub-address= 0x1h) [reset = 0x0h]

INT1 is shown in Figure 36 and described in Table 8.

Figure 36. INT1 Register

7	6	5	4	3	2	1	0
RESERVED		VPRG	AC	PB	HOT	CC_AQC	PRGC
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8. INT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	VPRG	R	0h	Programming voltage interrupt 0b = No significance 1b = Input voltage is too low for programming power-up default values.
4	AC	R	0h	AC_DET pin status change interrupt. Note: Status information is available in STATUS register 0b = No change in status 1b = AC_DET status change (AC_DET pin changed high to low or low to high)
3	PB	R	0h	Push-button status change interrupt. Note: Status information is available in STATUS register 0b = No change in status 1b = Push-button status change (PB changed high to low or low to high)
2	HOT	R	0h	Thermal shutdown early warning 0b = Chip temperature is below HOT threshold 1b = Chip temperature exceeds HOT threshold
1	CC_AQC	R	0h	Coin cell battery voltage acquisition complete interrupt 0b = No significance 1b = Backup battery status comparators have settled and results are available in STATUS register
0	PRGC	R	0h	EEPROM programming complete interrupt 0b = No significance 1b = Programming of power-up default settings has completed successfully

7.5.4.3 INT2 Register (subaddress = 0x2h) [reset = 0x0h]

INT2 is shown in Figure 37 and described in Table 9.

Figure 37. INT2 Register

7	6	5	4	3	2	1	0
RESERVED		LS3_F	LS2_F	LS1_F	LS3_I	LS2_I	LS1_I
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 9. INT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	LS3_F	R	0h	Load switch3 fault interrupt 0b = No fault. Switch is working normally. 1b = Load switch exceeded operating temperature limit and is temporarily disabled.
4	LS2_F	R	0h	Load switch2 fault interrupt 0b = No fault. Switch is working normally. 1b = Load switch exceeded operating temperature limit or input voltage dropped below minimum value. Switch is temporarily disabled.
3	LS1_F	R	0h	Load switch1 fault interrupt 0b = No fault. Switch is working normally. 1b = Load switch exceeded operating temperature limit and is temporarily disabled.
2	LS3_I	R	0h	Load switch3 current-limit interrupt 0b = Load switch is disabled or not in current limit 1b = Load switch is actively limiting the output current (output load is exceeding current limit value)
1	LS2_I	R	0h	Load switch2 current-limit interrupt 0b = Load switch is disabled or not in current limit 1b = Load switch is actively limiting the output current (output load is exceeding current limit value)
0	LS1_I	R	0h	Load switch1 current-limit interrupt 0b = Load switch is disabled or not in current limit 1b = Load switch is actively limiting the output current (output load is exceeding current limit value)

7.5.4.4 INT_MASK1 Register (subaddress = 0x3h) [reset = 0x0h]

INT_MASK1 is shown in Figure 38 and described in Table 10.

Figure 38. INT_MASK1 Register

7	6	5	4	3	2	1	0
RESERVED		VPRGM	ACM	PBM	HOTM	CC_AQCM	PRGCM
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 10. INT_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	VPRGM	R/W	0h	Programming voltage interrupt mask bit. Note: mask bit has no effect on monitoring function 0b = Interrupt is unmasked (interrupt event pulls nINT pin low) 1b = Interrupt is masked (interrupt has no effect on nINT pin)
4	ACM	R/W	0h	AC_DET interrupt masking bit. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low) 1b = Interrupt is masked (interrupt has no effect on nINT pin) Note: mask bit has no effect on monitoring function
3	PBM	R/W	0h	PB interrupt masking bit. Note: mask bit has no effect on monitoring function 0b = Interrupt is unmasked (interrupt event pulls nINT pin low) 1b = Interrupt is masked (interrupt has no effect on nINT pin)
2	HOTM	R/W	0h	HOT interrupt masking bit. Note: mask bit has no effect on monitoring function 0b = Interrupt is unmasked (interrupt event pulls nINT pin low) 1b = Interrupt is masked (interrupt has no effect on nINT pin)
1	CC_AQCM	R/W	0h	C_AQC interrupt masking bit. Note: mask bit has no effect on monitoring function 0b = Interrupt is unmasked (interrupt event pulls nINT pin low) 1b = Interrupt is masked (interrupt has no effect on nINT pin)
0	PRGCM	R/W	0h	PRGC interrupt masking bit. Note: mask bit has no effect on monitoring function 0b = Interrupt is unmasked (interrupt event pulls nINT pin low) 1b = Interrupt is masked (interrupt has no effect on nINT pin)

7.5.4.5 INT_MASK2 Register (subaddress = 0x4h) [reset = 0x0h]

INT_MASK2 is shown in Figure 39 and described in Table 11.

Figure 39. INT_MASK2 Register

7	6	5	4	3	2	1	0
RESERVED		LS3_FM	LS2_FM	LS1_FM	LS3_IM	LS2_IM	LS1_IM
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 11. INT_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	LS3_FM	R/W	0h	LS3 fault interrupt mask bit. Note: mask bit has no effect on monitoring function 0b = Interrupt is unmasked (interrupt event pulls nINT pin low) 1b = Interrupt is masked (interrupt has no effect on nINT pin)
4	LS2_FM	R/W	0h	LS2 fault interrupt mask bit. Note: mask bit has no effect on monitoring function 0b = Interrupt is unmasked (interrupt event pulls nINT pin low) 1b = Interrupt is masked (interrupt has no effect on nINT pin)
3	LS1_FM	R/W	0h	LS1 fault interrupt mask bit. Note: mask bit has no effect on monitoring function 0b = Interrupt is unmasked (interrupt event pulls nINT pin low) 1b = Interrupt is masked (interrupt has no effect on nINT pin)
2	LS3_IM	R/W	0h	LS3 current-limit interrupt mask bit. Note: mask bit has no effect on monitoring function 0b = Interrupt is unmasked (interrupt event pulls nINT pin low) 1b = Interrupt is masked (interrupt has no effect on nINT pin)
1	LS2_IM	R/W	0h	LS2 current-limit interrupt mask bit. Note: mask bit has no effect on monitoring function 0b = Interrupt is unmasked (interrupt event pulls nINT pin low) 1b = Interrupt is masked (interrupt has no effect on nINT pin)
0	LS1_IM	R/W	0h	LS1 current-limit interrupt mask bit. Note: mask bit has no effect on monitoring function 0b = Interrupt is unmasked (interrupt event pulls nINT pin low) 1b = Interrupt is masked (interrupt has no effect on nINT pin)

7.5.4.6 STATUS Register (subaddress = 0x5h) [reset = 0x0h]

Register mask: C0h

STATUS is shown in Figure 40 and described in Table 12.

Figure 40. STATUS Register

7	6	5	4	3	2	1	0
FSEAL	EE	AC_STATE	PB_STATE	STATE		CC_STAT	
R-0h	R-0h	R-X	R-X	R-X		R-X	

Table 12. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FSEAL	R	0h	Freshness seal (FSEAL) status. Note: See for details. 0b = FSEAL is in native state (fresh) 1b = FSEAL is broken
6	EE	R	0h	EEPROM status 0b = EEPROM values have not been changed from factory default setting 1b = EEPROM values have been changed from factory default settings
5	AC_STATE	R	X	AC_DET input status bit 0b = AC_DET input is inactive (AC_DET input pin is low) 1b = AC_DET input is active (AC_DET input is high)
4	PB_STATE	R	X	PB input status bit 0b = Push Button input is inactive (PB input pin is high) 1b = Push Button input is active (PB input pin is low)
3-2	STATE	R	X	State machine STATE indication 00b = PMIC is in transitional state 01b = PMIC is in WAIT_PWR_EN state 10b = PMIC is in ACTIVE state 11b = PMIC is in SUSPEND state
1-0	CC_STAT	R	X	Coin cell state of charge. Note: Coin-cell voltage acquisition must be triggered first before status bits are valid. See CC_AQ bit in *CONTROL Register (subaddress = 0x6h) [reset = 0x0h]*. 00b = V_{CC} < V_{LOW_LEVEL}; Coin cell is not present or approaching end-of-life (EOL) 01b = V_{LOW_LEVEL} < V_{CC} < V_{GOOD_LEVEL}; Coin cell voltage is LOW. 10b = V_{GOOD_LEVEL} < V_{CC} <V_{IDEAL_LEVEL}; Coin cell voltage is GOOD. 11b = V_{IDEAL} < V_{CC}; Coin cell voltage is IDEAL.

7.5.4.7 CONTROL Register (subaddress = 0x6h) [reset = 0x0h]

CONTROL is shown in Figure 41 and described in Table 13.

Figure 41. CONTROL Register

7	6	5	4	3	2	1	0
RESERVED						OFFnPFO	CC_AQ
R-0h						R/W-0h	R/W-0h

Table 13. CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	OFFnPFO	R/W	0h	Power-fail shutdown bit 0b = nPFO has no effect on PMIC state 1b = All rails are shut down and PMIC enters OFF state when PFI comparator trips (nPFO is low)
0	CC_AQ	R/W	0h	Coin Cell battery voltage acquisition start bit 0b = No significance 1b = Triggers voltage acquisition. Bit is automatically reset to 0.

7.5.4.8 FLAG Register (subaddress = 0x7h) [reset = 0x0h]

FLAG is shown in Figure 42 and described in Table 14.

Figure 42. FLAG Register

7	6	5	4	3	2	1	0
GPO3_FLG	GPO2_FLG	GPO1_FLG	LDO1_FLG	DC4_FLG	DC3_FLG	DC2_FLG	DC1_FLG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 14. FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPO3_FLG	R	0h	GPO3 Flag bit 0b = Device powered up from OFF or SUSPEND state and GPO3 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and GPO3 was enabled while in SUSPEND.
6	GPO2_FLG	R	0h	GPO2 Flag bit 0b = Device powered up from OFF or SUSPEND state and GPO2 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and GPO2 was enabled while in SUSPEND.
5	GPO1_FLG	R	0h	GPO1 Flag bit 0b = Device powered up from OFF or SUSPEND state and GPO1 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and GPO1 was enabled while in SUSPEND.
4	LDO1_FLG	R	0h	LDO1 Flag bit 0b = Device powered up from OFF or SUSPEND state and LDO1 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and LDO1 was enabled while in SUSPEND.
3	DC4_FLG	R	0h	DCDC4 Flag bit 0b = Device powered up from OFF or SUSPEND state and DCDC4 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and DCDC4 was enabled while in SUSPEND.
2	DC3_FLG	R	0h	DCDC3 Flag bit 0b = Device powered up from OFF or SUSPEND state and DCDC3 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and DCDC3 was enabled while in SUSPEND.
1	DC2_FLG	R	0h	DCDC2 Flag bit 0b = Device powered up from OFF or SUSPEND state and DCDC2 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and DCDC2 was enabled while in SUSPEND.
0	DC1_FLG	R	0h	DCDC1 Flag bit 0b = Device powered up from OFF or SUSPEND state and DCDC1 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and GDCDC1PO3 was enabled while in SUSPEND.

7.5.4.9 PASSWORD Register (subaddress = 0x10h) [reset = 0x0h]

PASSWORD is shown in Figure 43 and described in Table 15.

Figure 43. PASSWORD Register

7	6	5	4	3	2	1	0
PWRD							
R/W-0h							

Table 15. PASSWORD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWRD	R/W	0h	Register is used for: Accessing password protected registers (see *Password Protection* for details). Breaking the freshness seal (see *Freshness Seal (FSEAL) Bit* for details).Programming power-up default values (see Programming power-up default values for details). Read-back always yields 0x00.

7.5.4.10 ENABLE1 Register (subaddress = 0x11h) [reset = 0x0h]

ENABLE1 is shown in Figure 44 and described in Table 16.

Password protected.

Figure 44. ENABLE1 Register

7	6	5	4	3	2	1	0
RESERVED		DC6_EN	DC5_EN	DC4_EN	DC3_EN	DC2_EN	DC1_EN
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 16. ENABLE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	DC6_EN	R/W	0h	DCDC6 enable bit. DCDC6 can only be disabled if FSEAL = 0. See *Freshness Seal (FSEAL) Bit* for details. 0b = Disabled 1b = Enabled
4	DC5_EN	R/W	0h	DCDC5 enable bit. Note: At power-up/down this bit is automatically updated by the internal power sequencer. DCDC5 can only be disabled if FSEAL = 0. See *Freshness Seal (FSEAL) Bit* for details. 0b = Disabled 1b = Enabled
3	DC4_EN	R/W	0h	DCDC4 enable bit. Note: At power-up/down this bit is automatically updated by the internal power sequencer. 0b = Disabled 1b = Enabled
2	DC3_EN	R/W	0h	DCDC3 enable bit. Note: At power-up/down this bit is automatically updated by the internal power sequencer. 0b = Disabled 1b = Enabled
1	DC2_EN	R/W	0h	DCDC2 enable bit. Note: At power-up/down this bit is automatically updated by the internal power sequencer. 0b = Disabled 1b = Enabled
0	DC1_EN	R/W	0h	DCDC1 enable bit. Note: At power-up/down this bit is automatically updated by the internal power sequencer. 0b = Disabled 1b = Enabled

7.5.4.11 ENABLE2 Register (subaddress = 0x12h) [reset = 0x0h]

ENABLE2 is shown in Figure 45 and described in Table 17.

Password protected.

Figure 45. ENABLE2 Register

7	6	5	4	3	2	1	0
RESERVED	GPIO3	GPIO2	GPIO1	LS3_EN	LS2_EN	LS1_EN	LDO1_EN
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 17. ENABLE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	GPIO3	R/W	0h	General purpose output 3 / reset polarity. Note: If DC12_RST bit (register 0x14) is set to 1 this bit has no function. 0b = GPIO3 output is driven low 1b = GPIO3 output is HiZ
5	GPIO2	R/W	0h	General purpose output 2. Note: If IO_SEL bit (register 0x13) is set to 1 this bit has no function. 0b = GPO2 output is driven low 1b = GPO2 output is HiZ
4	GPIO1	R/W	0h	General purpose output 1. Note: If IO_SEL bit (register 0x13) is set to 1 this bit has no function. 0b = GPO1 output is driven low 1b = GPO1 output is HiZ
3	LS3_EN	R/W	0h	Load switch 3 (LS3) enable bit 0b = Disabled 1b = Enabled
2	LS2_EN	R/W	0h	Load switch 2 (LS2) enable bit 0b = Disabled 1b = Enabled
1	LS1_EN	R/W	0h	Load switch 1 (LS1) enable bit. 0b = Disabled 1b = Enabled Note: At power-up/down this bit is automatically updated by the internal power sequencer.
0	LDO1_EN	R/W	0h	LDO1 enable bit. 0b = Disabled 1b = Enabled Note: At power-up/down this bit is automatically updated by the internal power sequencer.

7.5.4.12 CONFIG1 Register (subaddress = 0x13h) [reset = 0x48h]

CONFIG1 is shown in Figure 46 and described in Table 18.

Password protected.

Figure 46. CONFIG1 Register

7	6	5	4	3	2	1	0
TRST	GPO2_BUF	IO1_SEL	PGDLY		STRICT	UVLO	
R/W-0h	R/W-1h	R/W-0h	R/W-1h		R/W-0h	R/W-0h	

Table 18. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TRST	R/W	0h	Push-button reset time constant 0b = 8s 1b = 15s
6	GPO2_BUF	R/W	1h	GPO2 output buffer configuration 0b = GPO2 buffer is configured as open-drain 1b = GPO2 buffer is configured as push-pull (high-level is driven to IN_LS1)
5	IO1_SEL	R/W	0h	GPIO1 / GPO2 configuration bit. See *I/O Configuration* for details. 0b = GPIO1 is configured as general-purpose, open-drain output. GPO2 is independent output 1b = GPIO1 is configured as input, controlling GPO2. Intended for DDR3 reset signal control.
4-3	PGDLY	R/W	1h	Power-Good delay. Note: Power-good delay applies to rising-edge only (power-up), not falling edge (power-down or fault) 00b = 10 ms 01b = 20 ms 10b = 50 ms 11b = 150 ms
2	STRICT	R/W	0h	Supply Voltage Supervisor Sensitivity selection. See *Electrical Characteristics* for details. 0b = Power-good threshold (VOUT falling) has wider limits. Over-voltage is not monitored 1b = Power-good threshold (VOUT falling) has tight limits. Over-voltage is monitored.
1-0	UVLO	R/W	0h	UVLO setting 00b = 2.75 V 01b = 2.95 V 10b = 3.25 V 11b = 3.35 V

7.5.4.13 CONFIG2 Register (subaddress = 0x14h) [TPS65218 reset = 0xC0h; TPS65218B101 reset = 0x80h]

CONFIG2 is shown in Figure 47 and described in Table 19.

Password protected.

Figure 47. CONFIG2 Register

7	6	5	4	3	2	1	0
DC12_RST	UVLOHYS	RESERVED		LS3ILIM		LS2ILIM	
R/W-1h	R/W-1h	R-0h		R/W-0h		R/W-0h	

Table 19. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DC12_RST	R/W	1h	DCDC1 and DCDC2 reset-pin enable 0b = GPIO3 is configured as general-purpose output 1b = GPIO3 is configured as warm-reset input to DCDC1 and DCDC2
6	UVLOHYS	R/W	TPS65218: 1h TPS65218B101: 0h	UVLO hysteresis 0b = 200 mV(1) 1b = 400 mV
5-4	RESERVED	R	0h	
3-2	LS3ILIM	R/W	0h	Load switch 3 (LS3) current limit selection 00b = 100 mA 01b = 200 mA 10b = 500 mA 11b = 1000 mA
1-0	LS2ILIM	R/W	0h	Load switch 2 (LS2) current limit selection 00b = 100 mA 01b = 200 mA 10b = 500 mA 11b = 1000 mA

(1) 200-mV hysteresis option is available for TPS65218B101

7.5.4.14 CONFIG3 Register (subaddress = 0x15h) [reset = 0x0h]

CONFIG3 is shown in Figure 48 and described in Table 20.

Password protected.

Figure 48. CONFIG3 Register

7	6	5	4	3	2	1	0
RESERVED		LS3nPFO	LS2nPFO	LS1nPFO	LS3DCHRG	LS2DCHRG	LS1DCHRG
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 20. CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	LS3nPFO	R/W	0h	Load switch 3 power-fail disable bit 0b = Load switch status is not affected by power-fail comparator 1b = Load switch is disabled if power-fail comparator trips (nPFO is low)
4	LS2nPFO	R/W	0h	Load switch 2 power-fail disable bit 0b = Load switch status is not affected by power-fail comparator 1b = Load switch is disabled if power-fail comparator trips (nPFO is low)
3	LS1nPFO	R/W	0h	Load switch 1 power-fail disable bit 0b = Load switch status is not affected by power-fail comparator 1b = Load switch is disabled if power-fail comparator trips (nPFO is low)
2	LS3DCHRG	R/W	0h	Load switch 3 discharge enable bit 0b = Active discharge is disabled 1b = Active discharge is enabled (load switch output is actively discharged when switch is OFF)
1	LS2DCHRG	R/W	0h	Load switch 2 discharge enable bit 0b = Active discharge is disabled 1b = Active discharge is enabled (load switch output is actively discharged when switch is OFF)
0	LS1DCHRG	R/W	0h	Load switch 1 discharge enable bit 0b = Active discharge is disabled 1b = Active discharge is enabled (load switch output is actively discharged when switch is OFF)

7.5.4.15 DCDC1 Register (offset = 0x16h) [reset = 0x99h]

DCDC1 is shown in Figure 49 and described in Table 21.

Password protected.

Figure 49. DCDC1 Register

7	6	5	4	3	2	1	0
PFM	RESERVED	DCDC1					
R/W-1h	R-0h	R/W-19h					

Table 21. DCDC1 Register Field Descriptions

Bit	Field	Type	Reset	Description			
7	PFM	R/W	1h	Pulse Frequency Modulation (PFM, also known as pulse-skip-mode) enable. PFM mode improves light-load efficiency. Actual PFM mode operation depends on load condition. 0b = Disabled (forced PWM) 1b = Enabled			
6	RESERVED	R	0h				
5-0	DCDC1	R/W	19h	DCDC1 output voltage setting			
				000000b = 0.850	010000b = 1.010	100000b = 1.170	110000b = 1.330
				000001b = 0.860	010001b = 1.020	100001b = 1.180	110001b = 1.340
				000010b = 0.870	010010b = 1.030	100010b = 1.190	110010b = 1.350
				000011b = 0.880	010011b = 1.040	100011b = 1.200	110011b = 1.375
				000100b = 0.890	010100b = 1.050	100100b = 1.210	110100b = 1.400
				000101b = 0.900	010101b = 1.060	100101b = 1.220	110101b = 1.425
				000110b = 0.910	010110b = 1.070	100110b = 1.230	110110b = 1.450
				000111b = 0.920	010111b = 1.080	100111b = 1.240	110111b = 1.475
				001000b = 0.930	011000b = 1.090	101000b = 1.250	111000b = 1.500
				001001b = 0.940	011001b = 1.100	101001b = 1.260	111001b = 1.525
				001010b = 0.950	011010b = 1.110	101010b = 1.270	111010b = 1.550
				001011b = 0.960	011011b = 1.120	101011b = 1.280	111011b = 1.575
				001100b = 0.970	011100b = 1.130	101100b = 1.290	111100b = 1.600
				001101b = 0.980	011101b = 1.140	101101b = 1.300	111101b = 1.625
				001110b = 0.990	011110b = 1.150	101110b = 1.310	111110b = 1.650
				001111b = 1.000	011111b = 1.160	101111b = 1.320	111111b = 1.675

7.5.4.16 DCDC2 Register (subaddress = 0x17h) [reset = 0x99h]

DCDC2 is shown in Figure 50 and described in Table 22.

Password protected.

Figure 50. DCDC2 Register

7	6	5	4	3	2	1	0
PFM	RESERVED	DCDC2					
R/W-1h	R-0h	R/W-19h					

Table 22. DCDC2 Register Field Descriptions

Bit	Field	Type	Reset	Description			
7	PFM	R/W	1h	Pulse frequency modulation (PFM, also known as pulse-skip-mode) enable. PFM mode improves light-load efficiency. Actual PFM mode operation depends on load condition. 0b = Disabled (forced PWM) 1b = Enabled			
6	RESERVED	R	0h				
5-0	DCDC2	R/W	19h	DCDC2 output voltage setting			
				000000b = 0.850	010000b = 1.010	100000b = 1.170	110000b = 1.330
				000001b = 0.860	010001b = 1.020	100001b = 1.180	110001b = 1.340
				000010b = 0.870	010010b = 1.030	100010b = 1.190	110010b = 1.350
				000011b = 0.880	010011b = 1.040	100011b = 1.200	110011b = 1.375
				000100b = 0.890	010100b = 1.050	100100b = 1.210	110100b = 1.400
				000101b = 0.900	010101b = 1.060	100101b = 1.220	110101b = 1.425
				000110b = 0.910	010110b = 1.070	100110b = 1.230	110110b = 1.450
				000111b = 0.920	010111b = 1.080	100111b = 1.240	110111b = 1.475
				001000b = 0.930	011000b = 1.090	101000b = 1.250	111000b = 1.500
				001001b = 0.940	011001b = 1.100	101001b = 1.260	111001b = 1.525
				001010b = 0.950	011010b = 1.110	101010b = 1.270	111010b = 1.550
				001011b = 0.960	011011b = 1.120	101011b = 1.280	111011b = 1.575
				001100b = 0.970	011100b = 1.130	101100b = 1.290	111100b = 1.600
				001101b = 0.980	011101b = 1.140	101101b = 1.300	111101b = 1.625
				001110b = 0.990	011110b = 1.150	101110b = 1.310	111110b = 1.650
				001111b = 1.000	011111b = 1.160	101111b = 1.320	111111b = 1.675

7.5.4.17 DCDC3 Register (subaddress = 0x18h) [reset = 0x8Ch]

DCDC3 is shown in Figure 51 and described in Table 23.

NOTE

Power-up default may differ depending on RSEL value. See *DCDC3 / DCDC4 Power-Up Default Selection* for details.

Figure 51. DCDC3 Register

7	6	5	4	3	2	1	0
PFM	RESERVED	DCDC3					
R/W-1h	R-0h	R/W-Ch					

Table 23. DCDC3 Register Field Descriptions

Bit	Field	Type	Reset	Description			
7	PFM	R/W	1h	Pulse Frequency Modulation (PFM, also known as pulse-skip-mode) enable. PFM mode improves light-load efficiency. Actual PFM mode operation depends on load condition. 0h = Disabled (forced PWM) 1h = Enabled			
6	RESERVED	R	0h				
5-0	DCDC3	R/W	Ch	DCDC3 output voltage setting			
				000000b = 0.900	010000b = 1.300	100000b = 1.850	110000b = 2.650
				000001b = 0.925	010001b = 1.325	100001b = 1.900	110001b = 2.700
				000010b = 0.950	010010b = 1.350	100010b = 1.950	110010b = 2.750
				000011b = 0.975	010011b = 1.375	100011b = 2.000	110011b = 2.800
				000100b = 1.000	010100b = 1.400	100100b = 2.050	110100b = 2.850
				000101b = 1.025	010101b = 1.425	100101b = 2.100	110101b = 2.900
				000110b = 1.050	010110b = 1.450	100110b = 2.150	110110b = 2.950
				000111b = 1.075	010111b = 1.475	100111b = 2.200	110111b = 3.000
				001000b = 1.100	011000b = 1.500	101000b = 2.250	111000b = 3.050
				001001b = 1.125	011001b = 1.525	101001b = 2.300	111001b = 3.100
				001010b = 1.150	011010b = 1.550	101010b = 2.350	111010b = 3.150
				001011b = 1.175	011011b = 1.600	101011b = 2.400	111011b = 3.200
				001100b = 1.200	011100b = 1.650	101100b = 2.450	111100b = 3.250
				001101b = 1.225	011101b = 1.700	101101b = 2.500	111101b = 3.300
				001110b = 1.250	011110b = 1.750	101110b = 2.550	111110b = 3.350
				001111b = 1.275	011111b = 1.800	101111b = 2.600	111111b = 3.400

7.5.4.18 DCDC4 Register (subaddress = 0x19h) [reset = 0xB2h]

DCDC4 is shown in Figure 52 and described in Table 24.

NOTE

Power-up default may differ depending on RSEL value. See *DCDC3 / DCDC4 Power-Up Default Selection* for details. The Reserved setting should not be selected and the output voltage settings should not be modified while the converter is operating.

Figure 52. DCDC4 Register

7	6	5	4	3	2	1	0
PFM	RESERVED	DCDC4					
R/W-1h	R-0h	R/W-32h					

Table 24. DCDC4 Register Field Descriptions

Bit	Field	Type	Reset	Description			
7	PFM	R/W	1h	Pulse Frequency Modulation (PFM, also known as pulse-skip-mode) enable. PFM mode improves light-load efficiency. Actual PFM mode operation depends on load condition. 0b = Disabled (forced PWM) 1b = Enabled			
6	RESERVED	R	0h				
5-0	DCDC4	R/W	32h	DCDC4 output voltage setting			
				000000b = 1.175	010000b = 1.600	100000b = 2.400	110000b = 3.200
				000001b = 1.200	010001b = 1.650	100001b = 2.450	110001b = 3.250
				000010b = 1.225	010010b = 1.700	100010b = 2.500	110010b = 3.300
				000011b = 1.250	010011b = 1.750	100011b = 2.550	110011b = 3.350
				000100b = 1.275	010100b = 1.800	100100b = 2.600	110100b = 3.400
				000101b = 1.300	010101b = 1.850	100101b = 2.650	110101b = reserved
				000110b = 1.325	010110b = 1.900	100110b = 2.700	110110b = reserved
				000111b = 1.350	010111b = 1.950	100111b = 2.750	110111b = reserved
				001000b = 1.375	011000b = 2.000	101000b = 2.800	111000b = reserved
				001001b = 1.400	011001b = 2.050	101001b = 2.850	111001b = reserved
				001010b = 1.425	011010b = 2.100	101010b = 2.900	111010b = reserved
				001011b = 1.450	011011b = 2.150	101011b = 2.950	111011b = reserved
				001100b = 1.475	011100b = 2.200	101100b = 3.000	111100b = reserved
				001101b = 1.500	011101b = 2.250	101101b = 3.050	111101b = reserved
				001110b = 1.525	011110b = 2.300	101110b = 3.100	111110b = reserved
				001111b = 1.550	011111b = 2.3500	101111b = 3.150	111111b = reserved

7.5.4.19 SLEW Register (subaddress = 0x1Ah) [reset = 0x6h]

SLEW is shown in Figure 53 and described in Table 25.

NOTE

Slew-rate control applies to DCDC1 and DCDC2 only. If changing from a higher voltage to lower voltage while STRICT = 1 and converters are in a no load state, PFM bit for DCDC1 and DCDC2 must be set to 0.

Figure 53. SLEW Register

7	6	5	4	3	2	1	0
GO	GODSBL	RESERVED			SLEW		
R/W-0h	R/W-0h	R-0h			R/W-6h		

Table 25. SLEW Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GO	R/W	0h	Go bit. Note: Bit is automatically reset at the end of the voltage transition 0b = No change 1b = Initiates the transition from present state to the output voltage setting currently stored in DCDC1 / DCDC2 register. SLEW setting does apply.
6	GODSBL	R/W	0h	Go disable bit 0b = Enabled 1b = Disabled; DCDC1 and DCDC2 output voltage changes whenever set-point is updated in DCDC1 / DCDC2 register without having to write to the GO bit. SLEW setting does apply.
5-3	RESERVED	R	0h	
2-0	SLEW	R/W	6h	Output slew rate setting 000b = 160 µs/step (0.0625 mV/s at 10 mV per step) 001b = 80 µs/step (0.125 mV/s at 10 mV per step) 010b = 40 µs/step (0.250 mV/s at 10 mV per step) 011b = 20 µs/step (0.500 mV/s at 10 mV per step) 100b = 10 µs/step (1.0 mV/s at 10 mV per step) 101b = 5 µs/step (2.0 mV/s at 10 mV per step) 110b = 2.5 µs/step (4.0 mV/s at 10 mV per step) 111b = Immediate; Slew rate is only limited by control loop response time. Note: The actual slew rate depends on the voltage step per code. Refer to DCDCx registers for details.

7.5.4.20 LDO1 Register (subaddress = 0x1Bh) [reset = 0x1Fh]

LDO1 is shown in Figure 54 and described in Table 26.

Password protected.

Figure 54. LDO1 Register

7	6	5	4	3	2	1	0
RESERVED		LDO1					
R-0h		R/W-1Fh					

Table 26. LDO1 Register Field Descriptions

Bit	Field	Type	Reset	Description			
7-6	RESERVED	R	0h				
5-0	LDO1	R/W	1Fh	LDO1 output voltage setting			
				000000b = 0.900	010000b = 1.300	100000b = 1.850	110000b = 2.650
				000001b = 0.925	010001b = 1.325	100001b = 1.900	110001b = 2.700
				000010b = 0.950	010010b = 1.350	100010b = 1.950	110010b = 2.750
				000011b = 0.975	010011b = 1.375	100011b = 2.000	110011b = 2.800
				000100b = 1.000	010100b = 1.400	100100b = 2.050	110100b = 2.850
				000101b = 1.025	010101b = 1.425	100101b = 2.100	110101b = 2.900
				000110b = 1.050	010110b = 1.450	100110b = 2.150	110110b = 2.950
				000111b = 1.075	010111b = 1.475	100111b = 2.200	110111b = 3.000
				001000b = 1.100	011000b = 1.500	101000b = 2.250	111000b = 3.050
				001001b = 1.125	011001b = 1.525	101001b = 2.300	111001b = 3.100
				001010b = 1.150	011010b = 1.550	101010b = 2.350	111010b = 3.150
				001011b = 1.175	011011b = 1.600	101011b = 2.400	111011b = 3.200
				001100b = 1.200	011100b = 1.650	101100b = 2.450	111100b = 3.250
				001101b = 1.225	011101b = 1.700	101101b = 2.500	111101b = 3.300
				001110b = 1.250	011110b = 1.750	101110b = 2.550	111110b = 3.350
				001111b = 1.275	011111b = 1.800	101111b = 2.600	111111b = 3.400

7.5.4.21 SEQ1 Register (subaddress = 0x20h) [reset = 0x0h]

SEQ1 is shown in Figure 55 and described in Table 27.

Password protected.

Figure 55. SEQ1 Register

7	6	5	4	3	2	1	0
DLY8	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 27. SEQ1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DLY8	R/W	0h	Delay8 (occurs after Stobe8 and before Strobe9) 0b = 2 ms 1b = 5 ms
6	DLY7	R/W	0h	Delay7 (occurs after Stobe7 and before Strobe8) 0b = 2 ms 1b = 5 ms
5	DLY6	R/W	0h	Delay6 (occurs after Stobe6 and before Strobe7) 0b = 2 ms 1b = 5 ms
4	DLY5	R/W	0h	Delay5 (occurs after Stobe5 and before Strobe6) 0b = 2 ms 1b = 5 ms
3	DLY4	R/W	0h	Delay4 (occurs after Stobe4 and before Strobe5) 0b = 2 ms 1b = 5 ms
2	DLY3	R/W	0h	Delay3 (occurs after Stobe3 and before Strobe4) 0b = 2 ms 1b = 5 ms
1	DLY2	R/W	0h	Delay2 (occurs after Stobe2 and before Strobe3) 0b = 2 ms 1b = 5 ms
0	DLY1	R/W	0h	Delay1 (occurs after Stobe1 and before Strobe2) 0b = 2 ms 1b = 5 ms

7.5.4.22 SEQ2 Register (subaddress = 0x21h) [reset = 0x0h]

SEQ2 is shown in Figure 56 and described in Table 28.

Password protected.

Figure 56. SEQ2 Register

7	6	5	4	3	2	1	0
DLYFCTR	RESERVED						DLY9
R/W -0h	R-0h						R/W -0h

Table 28. SEQ2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DLYFCTR	R/W	0h	Power-down delay factor 0b = 1x 1b = 10x (delay times are multiplied by 10x during power-down) Note: DLYFCTR has no effect on power-up timing.
6-1	RESERVED	R	0h	
0	DLY9	R/W	0h	Delay9 (occurs after Stobe9 and before Strobe10) 0b = 2 ms 1b = 5 ms

7.5.4.23 SEQ3 Register (subaddress = 0x22h) [reset = 0x98h]

SEQ3 is shown in Figure 57 and described in Table 29.

Password protected.

Figure 57. SEQ3 Register

7	6	5	4	3	2	1	0
DC2_SEQ				DC1_SEQ			
R/W-9h				R/W-8h			

Table 29. SEQ3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DC2_SEQ	R/W	9h	DCDC2 enable STROBE 0000b = Rail is not controlled by sequencer 0001b = Rail is not controlled by sequencer 0010b = Rail is not controlled by sequencer 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7 1000b = Enable at STROBE8 1001b = Enable at STROBE9 1010b = Enable at STROBE10 1011b = Rail is not controlled by sequencer 1100b = Rail is not controlled by sequencer 1101b = Rail is not controlled by sequencer 1110b = Rail is not controlled by sequencer 1111b = Rail is not controlled by sequencer
3-0	DC1_SEQ	R/W	8h	DCDC1 enable STROBE 0000b = Rail is not controlled by sequencer 0001b = Rail is not controlled by sequencer 0010b = Rail is not controlled by sequencer 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7 1000b = Enable at STROBE8 1001b = Enable at STROBE9 1010b = Enable at STROBE10 1011b = Rail is not controlled by sequencer 1100b = Rail is not controlled by sequencer 1101b = Rail is not controlled by sequencer 1110b = Rail is not controlled by sequencer 1111b = Rail is not controlled by sequencer

7.5.4.24 SEQ4 Register (subaddress = 0x23h) [reset = 0x75h]

SEQ4 is shown in Figure 58 and described in Table 30.

Password protected.

Figure 58. SEQ4 Register

7	6	5	4	3	2	1	0
DC4_SEQ				DC3_SEQ			
R/W-7h				R/W-5h			

Table 30. SEQ4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DC4_SEQ	R/W	7h	DCDC4 enable STROBE 0000b = Rail is not controlled by sequencer 0001b = Rail is not controlled by sequencer 0010b = Rail is not controlled by sequencer 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7 1000b = Enable at STROBE8 1001b = Enable at STROBE9 1010b = Enable at STROBE10 1011b = Rail is not controlled by sequencer 1100b = Rail is not controlled by sequencer 1101b = Rail is not controlled by sequencer 1110b = Rail is not controlled by sequencer 1111b = Rail is not controlled by sequencer
3-0	DC3_SEQ	R/W	5h	DCDC3 enable STROBE 0000b = Rail is not controlled by sequencer 0001b = Rail is not controlled by sequencer 0010b = Rail is not controlled by sequencer 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7 1000b = Enable at STROBE8 1001b = Enable at STROBE9 1010b = Enable at STROBE10 1011b = Rail is not controlled by sequencer 1100b = Rail is not controlled by sequencer 1101b = Rail is not controlled by sequencer 1110b = Rail is not controlled by sequencer 1111b = Rail is not controlled by sequencer

7.5.4.25 SEQ5 Register (subaddress = 0x24h) [reset = 0x12h]

SEQ5 is shown in Figure 59 and described in Table 31.

Password protected.

Figure 59. SEQ5 Register

7	6	5	4	3	2	1	0
DC6_SEQ				DC5_SEQ			
R/W-1h				R/W-2h			

Table 31. SEQ5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DC6_SEQ	R/W	1h	DCDC6 enable STROBE. Note: Strobe 1 and 2 are executed only if FSEAL = 0. DCDC5 and 6 cannot be disabled by sequencer once freshness seal is broken. 00b = Rail is not controlled by sequencer 01b = Enable at STROBE1 10b = Enable at STROBE2 11b = Rail is not controlled by sequencer
3-0	DC5_SEQ	R/W	2h	DCDC5 enable STROBE. Note: Strobe 1 and 2 are executed only if FSEAL = 0. DCDC5 and 6 cannot be disabled by sequencer once freshness seal is broken. 00b = Rail is not controlled by sequencer 01b = Enable at STROBE1 10b = Enable at STROBE2 11b = Rail is not controlled by sequencer

7.5.4.26 SEQ6 Register (subaddress = 0x25h) [reset = 0x63h]

SEQ6 is shown in Figure 60 and described in Table 32.

Password protected.

Figure 60. SEQ6 Register

7	6	5	4	3	2	1	0
LS1_SEQ				LDO1_SEQ			
R/W-6h				R/W-3h			

Table 32. SEQ6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LS1_SEQ	R/W	6h	LS1 enable STROBE 0000b = Rail is not controlled by sequencer 0001b = Rail is not controlled by sequencer 0010b = Rail is not controlled by sequencer 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7 1000b = Enable at STROBE8 1001b = Enable at STROBE9 1010b = Enable at STROBE10 1011b = Rail is not controlled by sequencer 1100b = Rail is not controlled by sequencer 1101b = Rail is not controlled by sequencer 1110b = Rail is not controlled by sequencer 1111b = Rail is not controlled by sequencer
3-0	LDO1_SEQ	R/W	3h	LDO1 enable STROBE 0000b = Rail is not controlled by sequencer 0001b = Rail is not controlled by sequencer 0010b = Rail is not controlled by sequencer 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7 1000b = Enable at STROBE8 1001b = Enable at STROBE9 1010b = Enable at STROBE10 1011b = Rail is not controlled by sequencer 1100b = Rail is not controlled by sequencer 1101b = Rail is not controlled by sequencer 1110b = Rail is not controlled by sequencer 1111b = Rail is not controlled by sequencer

7.5.4.27 SEQ7 Register (subaddress = 0x26h) [reset = 0x3h]

SEQ7 is shown in Figure 61 and described in Table 33.

Password protected.

Figure 61. SEQ7 Register

7	6	5	4	3	2	1	0
GPO3_SEQ				GPO1_SEQ			
R/W-0h				R/W-3h			

Table 33. SEQ7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO3_SEQ	R/W	0h	GPO3 enable STROBE 0000b = Rail is not controlled by sequencer 0001b = Rail is not controlled by sequencer 0010b = Rail is not controlled by sequencer 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7 1000b = Enable at STROBE8 1001b = Enable at STROBE9 1010b = Enable at STROBE10 1011b = Rail is not controlled by sequencer 1100b = Rail is not controlled by sequencer 1101b = Rail is not controlled by sequencer 1110b = Rail is not controlled by sequencer 1111b = Rail is not controlled by sequencer
3-0	GPO1_SEQ	R/W	3h	GPO1 enable STROBE 0000b = Rail is not controlled by sequencer 0001b = Rail is not controlled by sequencer 0010b = Rail is not controlled by sequencer 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7 1000b = Enable at STROBE8 1001b = Enable at STROBE9 1010b = Enable at STROBE10 1011b = Rail is not controlled by sequencer 1100b = Rail is not controlled by sequencer 1101b = Rail is not controlled by sequencer 1110b = Rail is not controlled by sequencer 1111b = Rail is not controlled by sequencer

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65218x is designed to pair with various application processors. For detailed information on using TPS65218x with Sitara AM335x or Sitara AM437x processors, see *Powering the AM335x/AM437x with TPS65218x* (SLVUAA9).

8.2 Typical Application

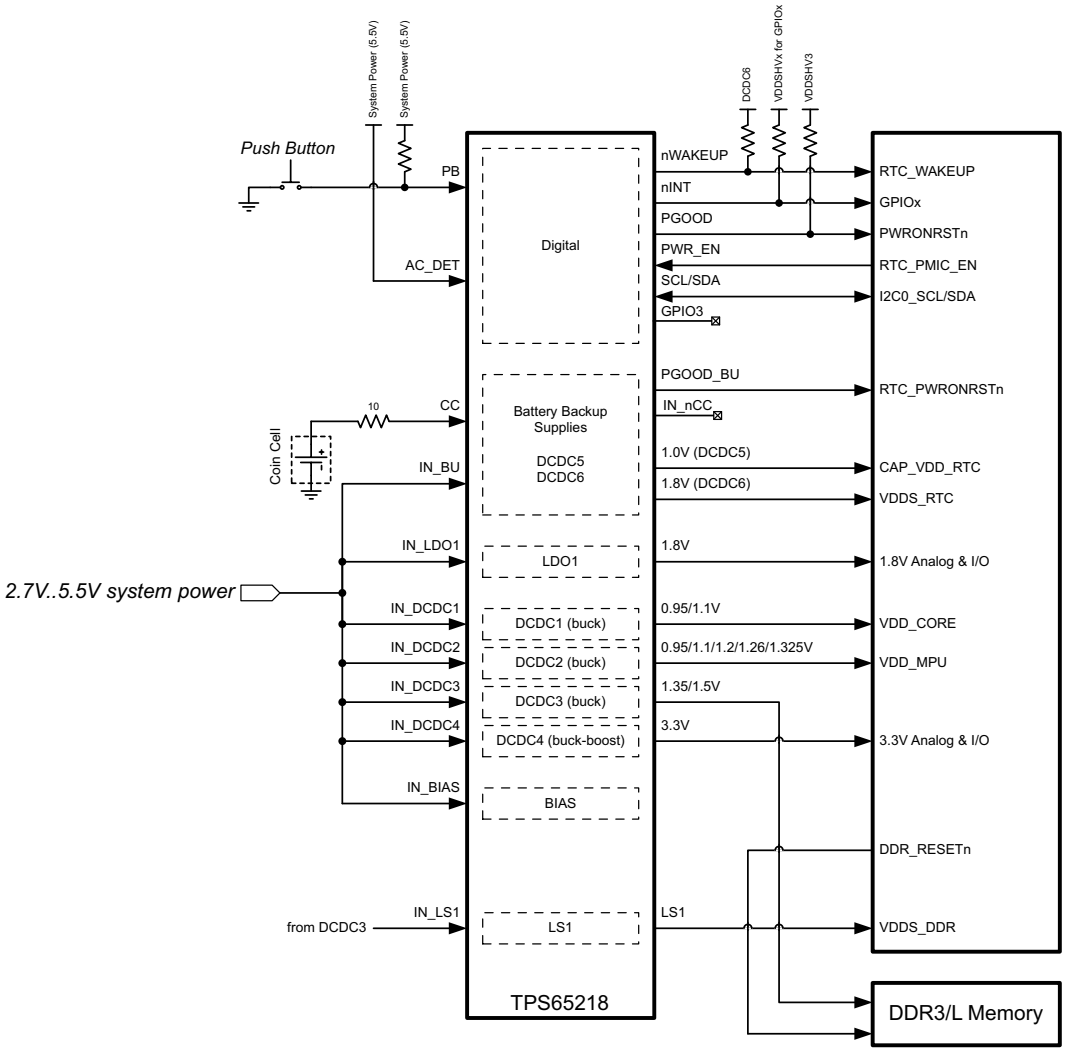


Figure 62. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 34 shows the design requirements.

Table 34. Design Parameters

	VOLTAGE	SEQUENCE
DCDC1	1.1 V	8
DCDC2	1.1 V	9
DCDC3	1.2 V	5
DCDC4	3.3 V	7
DCDC5	1.0 V	2
DCDC6	1.8 V	1
LDO1	1.8 V	3

8.2.2 Detailed Design Procedure

8.2.2.1 Output Filter Design

The step down converters (DCDC1, DCDC2, and DCDC3) on TPS65218x are designed to operate with effective inductance values in the range of 1 to 2.2 µH and with effective output capacitance in the range of 10 to 100 µF. The internal compensation is optimized to operate with an output filter of L = 1.5 µH and Cout = 10 µF.

The buck boost converter (DCDC4) on TPS65218x is designed to operate with effective inductance values in the range of 1.2 to 2.2 µH. The internal compensation is optimized to operate with an output filter of L = 1.5 µH and Cout = 47 µF.

The two battery backup converters (DCDC5 and DCDC6) are designed to operate with effective inductance values in the range of 4.7 to 22 µH. The internal compensation is optimized with an output filter of L = 10 µH and Cout = 20 µF.

Larger or smaller inductor/capacitance values can be used to optimize performance of the device for specific operation conditions.

8.2.2.2 Inductor Selection for Buck Converters

The inductor value affects its peak to peak ripple current, the PWM to PFM transition point, the output voltage ripple, and the efficiency. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current (ΔL) decreases with higher inductance and increases with higher Vin or Vout. Equation 1 calculates the maximum inductor current ripple under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. This is recommended as during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2} \quad (2)$$

where

- F = Switching frequency
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current

The following inductors have been used with the TPS65218x (see Table 35).

Table 35. List of Components: Inductors

PART NUMBER	VALUE	SIZE (mm)	MANUFACTURER
INDUCTORS FOR DCDC1, DCDC2, DCDC3, DCDC4			
SPM3012T-1R5M	1.5 µH, 2.8 A, 77 mΩ	3.2 × 3.0 × 1.2 (LxWxH)	TDK
IHLP1212BZER1R5M11	1.5 µH, 4.0 A, 28.5 mΩ	3.6 × 3.0 × 2.0 (LxWxH)	Vishay
INDUCTORS FOR DCDC5, DCDC6			
MLZ2012N100L	10 µH, 110 mA, 300 mΩ	2012 / 0805 (2.00 × 1.25 × 1.25 LxWxH)	TDK
LQM21FN100M80	10 µH, 100 mA, 300 mΩ	2012 / 0805 (2.00 × 1.25 × 1.25 LxWxH)	Murata

8.2.2.3 Output Capacitor Selection

The hysteretic PWM control scheme of the TPS65218x switching converters allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric.

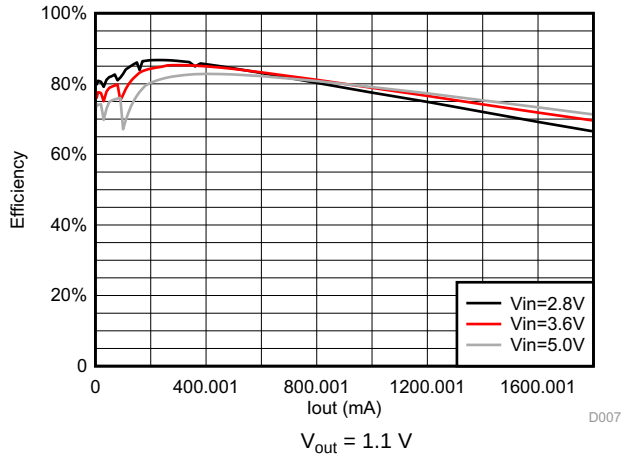
At light load currents the converter operates in power save mode, and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode and tighten DC output accuracy in PFM mode.

The two battery backup converters (DCDC5 and DCDC6) always operate in PFM mode. For these converters at least 20 µF is recommended on the output to help minimize voltage ripple.

The buck-boost converter requires additional output capacitance to help maintain converter stability during high load conditions. At least 40 µF of output capacitance is recommended and an additional 100-nF capacitor can be added to further filter output ripple.

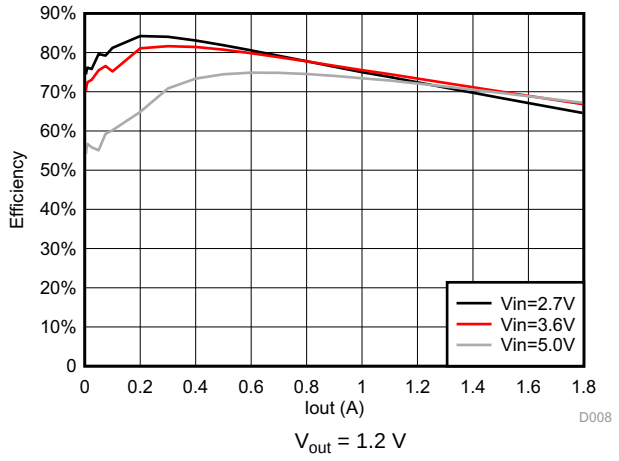
8.2.3 Application Curves

at T_J = 25°C unless otherwise noted



V_{out} = 1.1 V

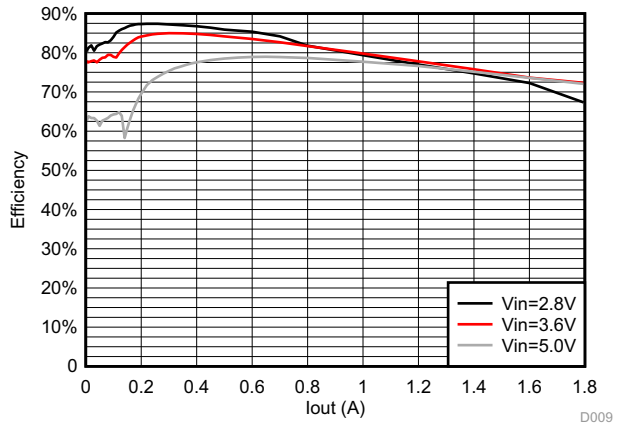
Figure 63. DCDC1/DCDC2 Efficiency



V_{out} = 1.2 V

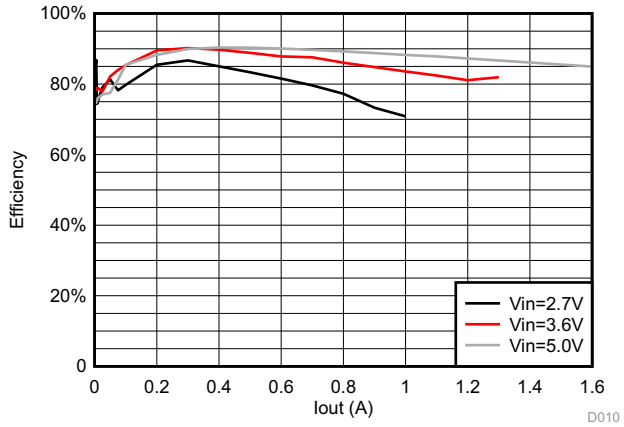
Figure 64. DCDC3 Efficiency

at T_J = 25°C unless otherwise noted



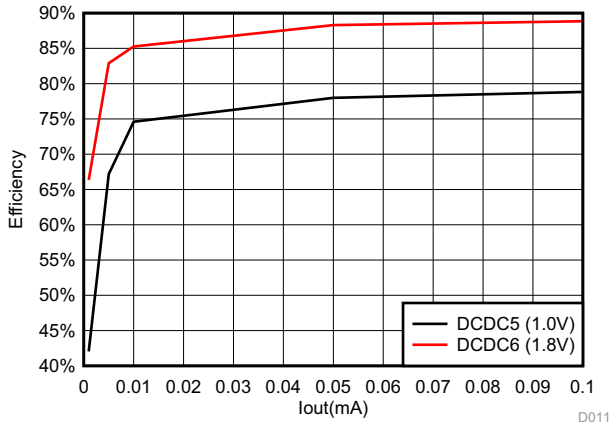
V_{out} = 1.5 V

Figure 65. DCDC3 Efficiency



V_{out} = 3.3 V

Figure 66. DCDC4 Efficiency



IN_BU = 0 V

CC = 3 V

Figure 67. DCDC5/DCDC6 Efficiency

9 Power Supply Recommendations

The device is designed to operate with an input voltage supply range between 2.7 and 5.5 V. This input supply can be from a single cell Li-Ion battery or other externally regulated supply. If the input supply is located more than a few inches from the TPS65218x additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

The coin cell back up input is designed to operate with a input voltage supply between 2.2 and 3.3 V This input should be supplied by a coin cell battery with 3-V nominal voltage.

10 Layout

10.1 Layout Guidelines

- The IN_X pins should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 4.7-µF with a X5R or X7R dielectric.
- The optimum placement is closest to the IN_X pins of the device. Take care to minimize the loop area formed by the bypass capacitor connection, the IN_X pin, and the PowerPAD of the device.
- The PowerPAD should be tied to the PCB ground plane with multiple vias.
- The LX trace should be kept on the PCB top layer and free of any vias.
- The FBX traces should be routed away from any potential noise source to avoid coupling.
- DCDC4 Output capacitance should be placed immediately at the DCDC4 pin. Excessive distance between the capacitance and DCDC4 pin may cause poor converter performance.

10.2 Layout Example

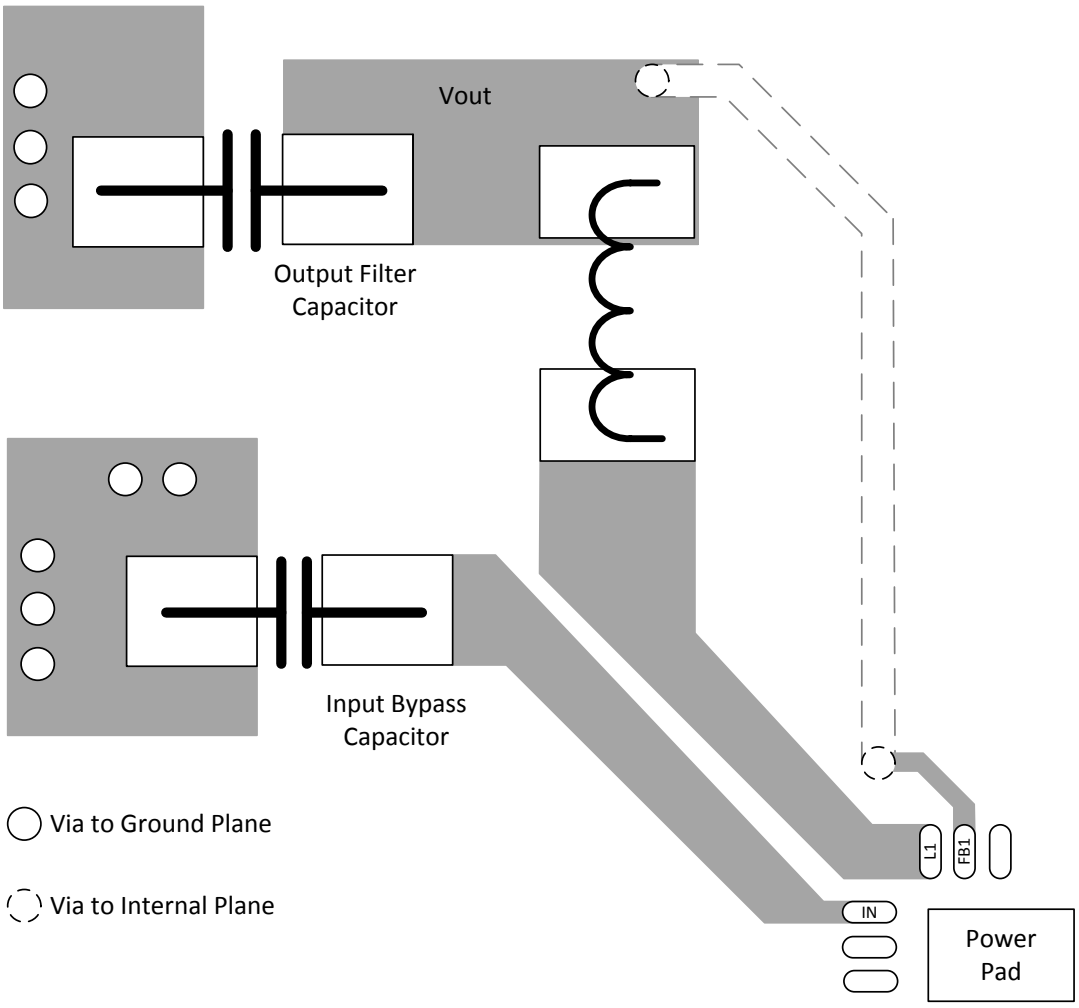


Figure 68. Layout Recommendation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65218B101PHPR	ACTIVE	HTQFP	PHP	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	65218B101	Samples
TPS65218B101PHPT	ACTIVE	HTQFP	PHP	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	65218B101	Samples
TPS65218B1PHPR	ACTIVE	HTQFP	PHP	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	T65218B1	Samples
TPS65218B1PHPT	ACTIVE	HTQFP	PHP	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	T65218B1	Samples
TPS65218B1RSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65218B1	Samples
TPS65218B1RSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65218B1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

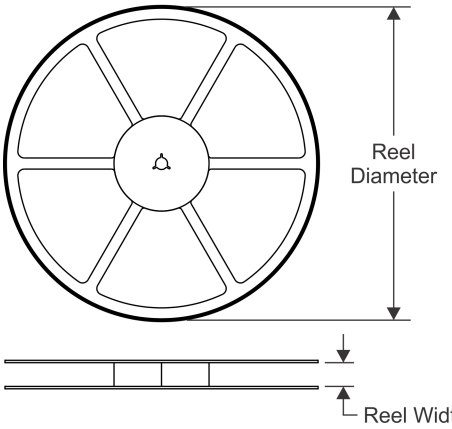
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

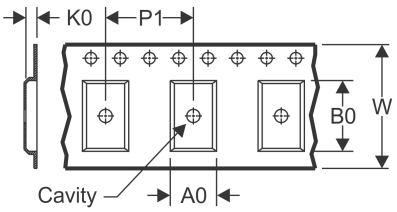
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

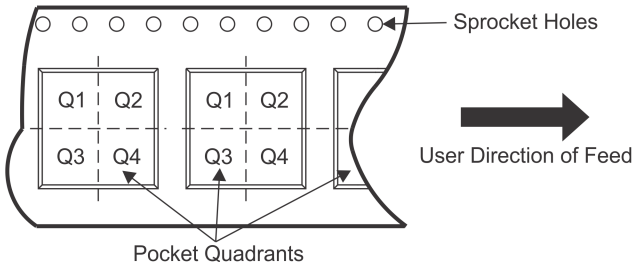


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

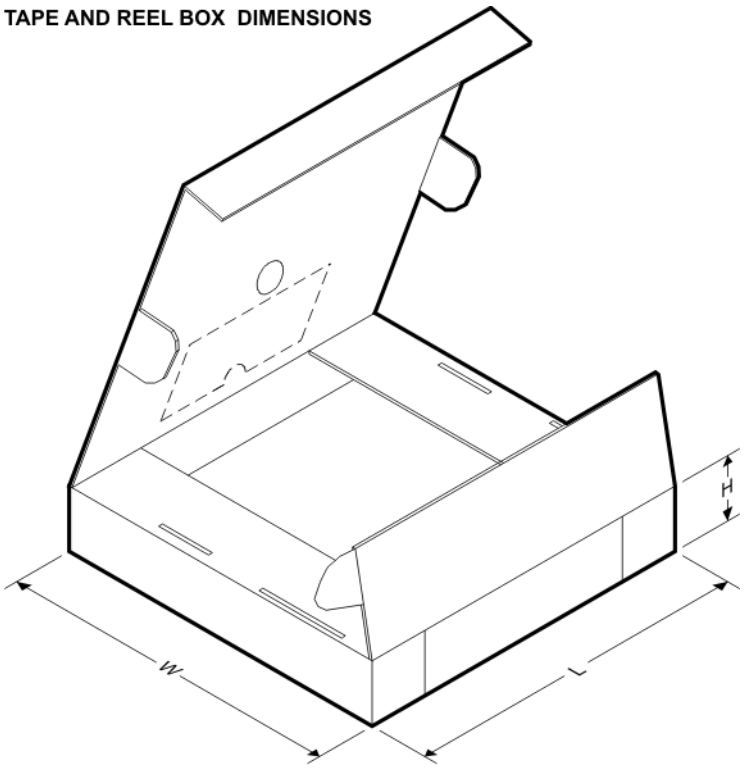
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65218B101PHPR	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TPS65218B101PHPT	HTQFP	PHP	48	250	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TPS65218B1PHPR	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TPS65218B1PHPT	HTQFP	PHP	48	250	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TPS65218B1RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65218B1RSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

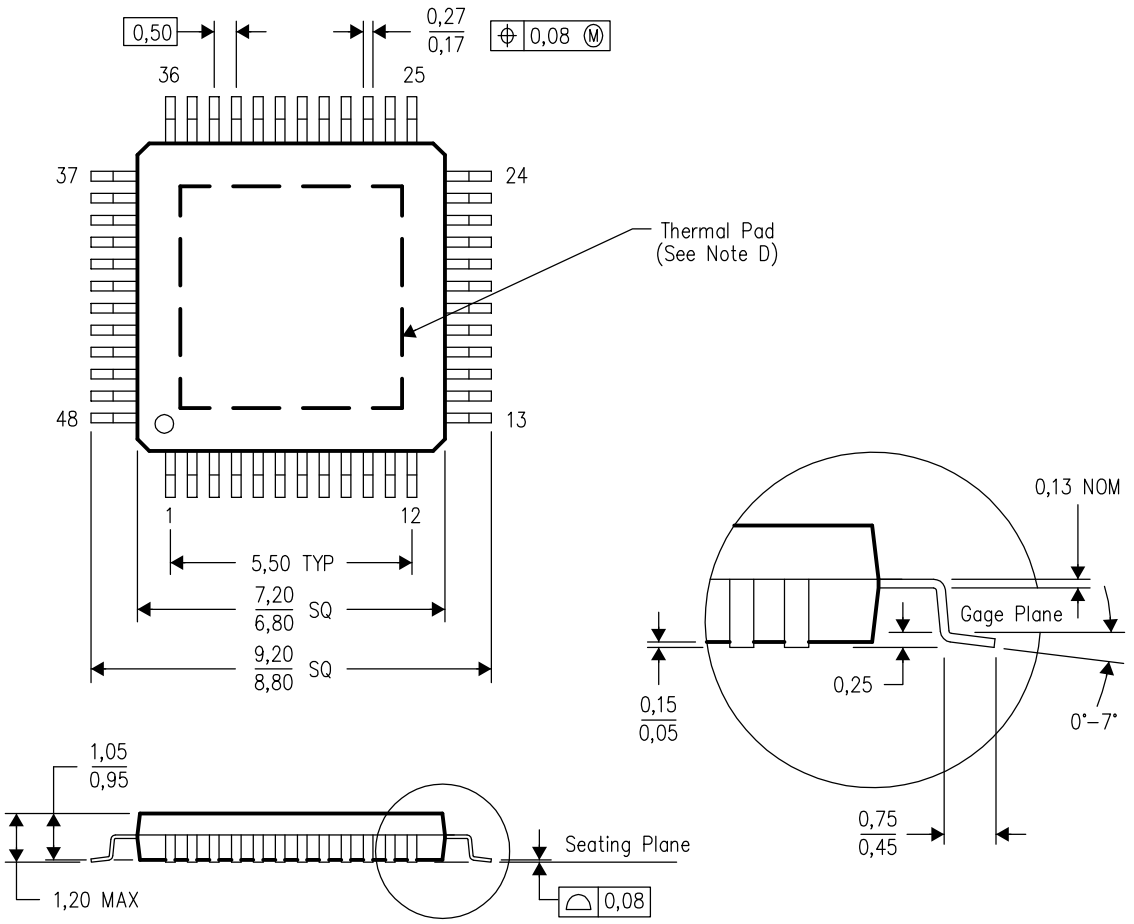
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65218B101PHPR	HTQFP	PHP	48	1000	336.6	336.6	31.8
TPS65218B101PHPT	HTQFP	PHP	48	250	336.6	336.6	31.8
TPS65218B1PHPR	HTQFP	PHP	48	1000	336.6	336.6	31.8
TPS65218B1PHPT	HTQFP	PHP	48	250	336.6	336.6	31.8
TPS65218B1RSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65218B1RSLT	VQFN	RSL	48	250	210.0	185.0	35.0

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

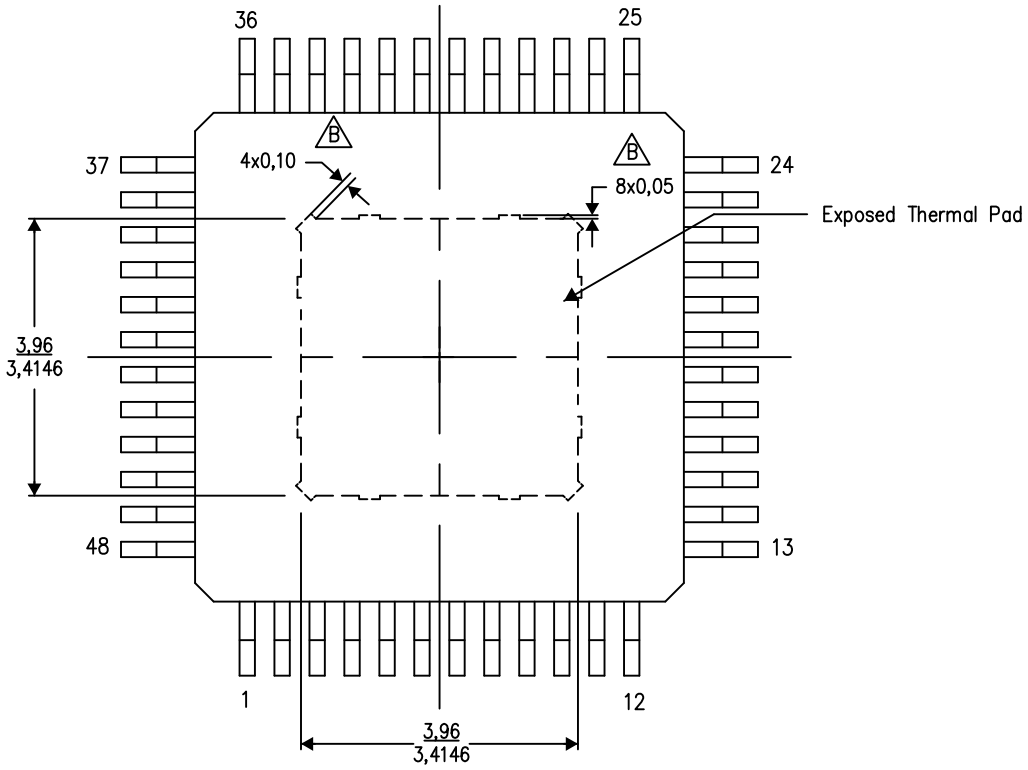
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

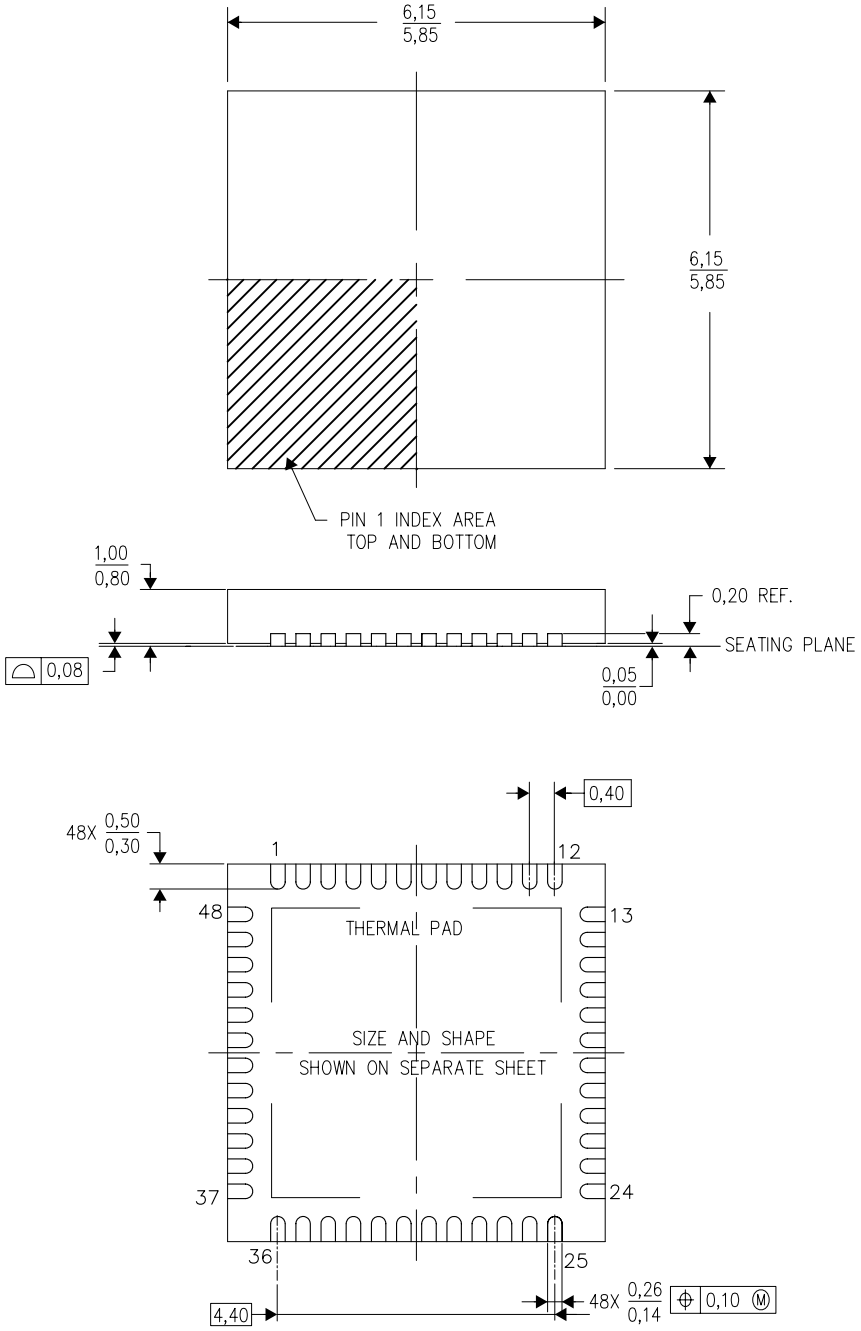
4206329–14/P 03/15

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

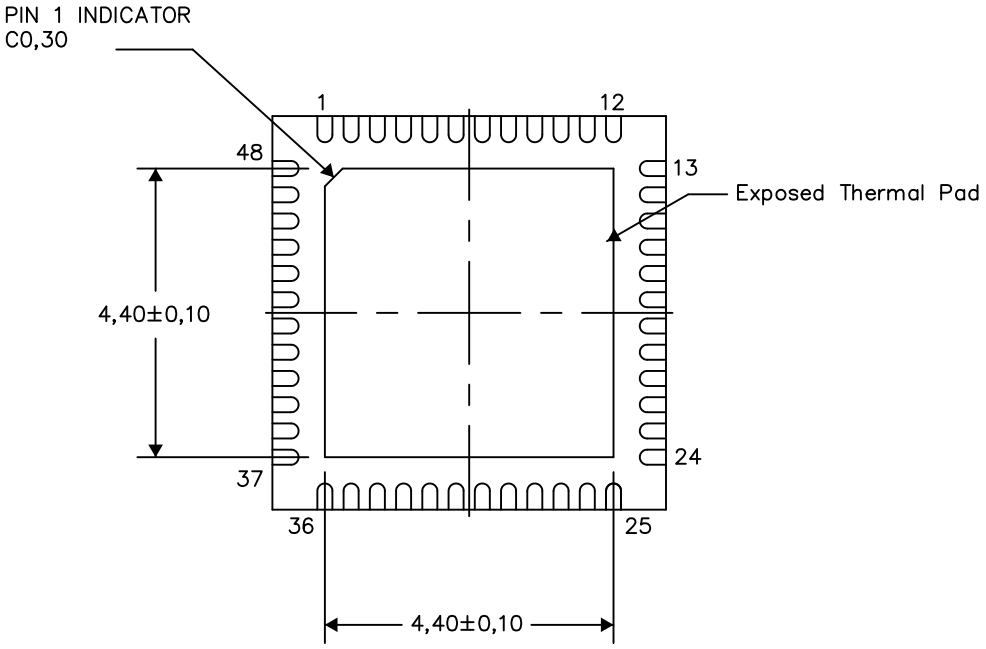
RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



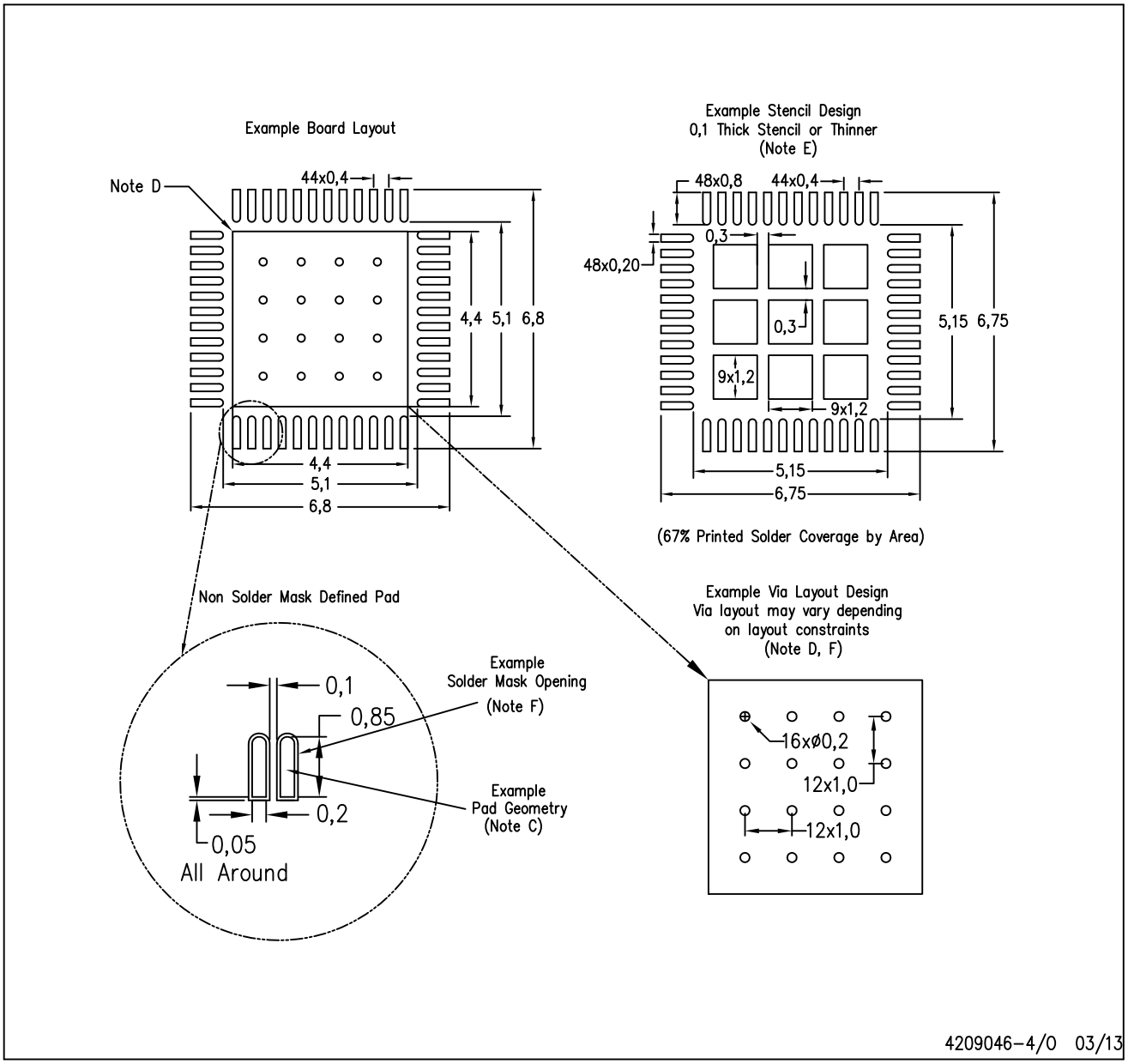
Bottom View

Exposed Thermal Pad Dimensions

4207841–2/P 03/13

NOTE: All linear dimensions are in millimeters

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265