

## 0.14 GHz to 1.5 GHz QUADRATURE MODULATOR

### FEATURES

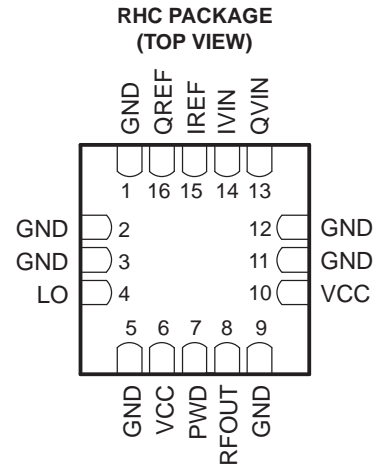
- P1dB of 7 dBm
- –156 dBm/Hz Noise Floor
- –150 dBm/Hz Noise at  $P_{OUT} = 0$  dBm
- Typical Unadjusted Carrier Suppression > 35 dBc at 1 GHz
- Typical Unadjusted Sideband Suppression > 40 dBc at 1 GHz
- Differential or Single-Ended I, Q Inputs
- Convenient Single-Ended LO Input
- Silicon Germanium Technology

### APPLICATIONS

- Cellular Base Transceiver Station Transmit Channel
- IF Sampling Applications
- TDMA: GSM, IS-136, EDGE/UWC-136
- CDMA: IS-95, UMTS, CDMA2000
- Wireless Local Loop
- Wireless LAN IEEE 802.11
- LMDS, MMDS
- Wideband Baseband Transceivers

### DESCRIPTION

The TRF3701 is an ultralow-noise direct quadrature modulator that is capable of converting complex input signals from baseband or IF directly up to RF. An internal analog combiner sums the real and imaginary components of the RF outputs. This combined output can feed the RF preamp directly at frequencies of up to 1.5 GHz. The modulator is implemented as a double-balanced mixer. An internal local oscillator (LO) phase splitter accommodates a single-ended LO input, eliminating the need for a costly external balun.



P0003-01

### AVAILABLE OPTIONS

| $T_A$         | 4-mm × 4-mm 16-Pin RHC (QFN) Package |
|---------------|--------------------------------------|
| –40°C to 85°C | TRF3701IRHC                          |
|               | TRF3701IRHCR (Tape and Reel)         |



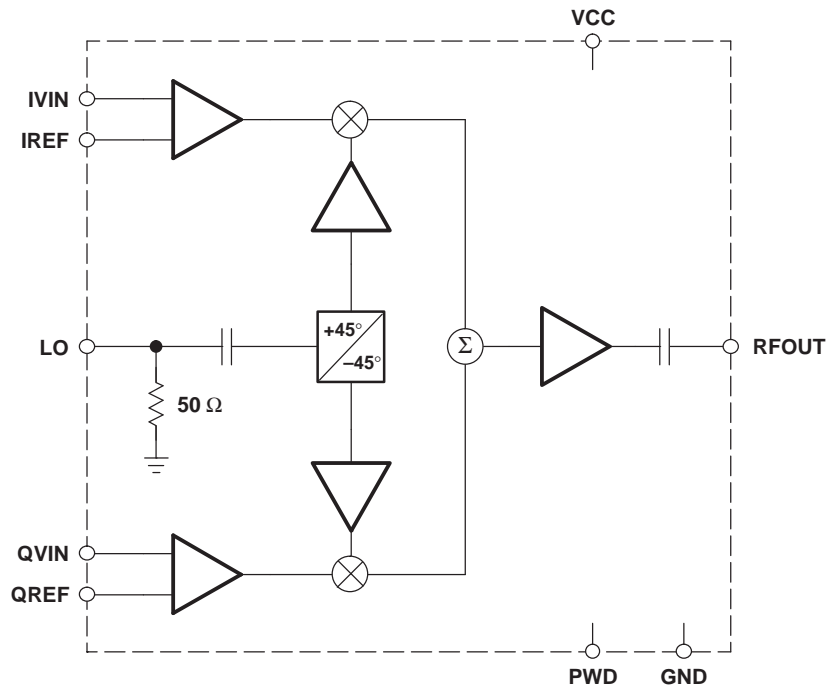
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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**FUNCTIONAL BLOCK DIAGRAM**



B0002-01

**Table 1. TERMINAL FUNCTIONS**

| TERMINAL |                       | I/O | DESCRIPTION   |
|----------|-----------------------|-----|---|
| NAME     | NO.                   |     |   |
| GND      | 1, 2, 3, 5, 9, 11, 12 |     | Ground  |
| IREF     | 15                    | I   | In-phase (I) reference voltage/differential input   |
| IVIN     | 14                    | I   | In-phase (I) signal input                           |
| LO       | 4                     | I   | Local oscillator input                              |
| PWD      | 7                     | I   | Power down  |
| QREF     | 16                    | I   | Quadrature (Q) reference voltage/differential input |
| QVIN     | 13                    | I   | Quadrature (Q) signal input                         |
| RFOUT    | 8                     | O   | RF output   |
| VCC      | 6, 10                 |     | Supply voltage                                      |

## ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

|          |   |               |
|----------|---|---------------|
| $V_{CC}$ | Supply voltage range                        | –0.5 V to 6 V |
|          | LO input power level                        | 10 dBm        |
|          | Baseband input voltage level (single-ended) | 3 Vp-p        |
| $T_A$    | Operating free-air temperature range        | –40°C to 85°C |
|          | Lead temperature for 10 seconds             | 260°C         |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Measured with respect to ground

## RECOMMENDED OPERATING CONDITIONS

|                                    |   | MIN | NOM | MAX  | UNIT |
|------------------------------------|---|-----|-----|------|------|
| <b>Supplies and References</b>     |   |     |     |      |      |
| $V_{CC}$                           | Analog supply voltage                                     | 4.5 | 5   | 5.5  | V    |
|                                    | VCM (IVIN, QVIN, IREF, QREF input common-mode dc voltage) |     | 3.7 |      | V    |
| <b>Local Oscillator Input (LO)</b> |   |     |     |      |      |
|                                    | Input frequency   | 140 |     | 1500 | MHz  |
|                                    | Power level (measured into 50 $\Omega$ )                  | –6  | 0   | 6    | dBm  |
| <b>Signal Inputs (IVIN, QVIN)</b>  |   |     |     |      |      |
|                                    | Input bandwidth   |     | 700 |      | MHz  |
| PWD Operation                      | $V_{IL}$  |     | 0   | 1.2  | V    |
|                                    | $V_{IH}$  | 3.7 | 5   |      |      |

## ELECTRICAL CHARACTERISTICS

 Over recommended operating conditions,  $V_{CC} = 5$  V,  $V_{CM} = 3.7$  V,  $f_{LO} = 942.5$  MHz at 0 dBm,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                     | TEST CONDITIONS            | MIN  | TYP         | MAX | UNIT          |
|---|----------------------------|--|-------------|-----|---------------|
| <b>Power Supply</b>                           |                            |  |             |     |               |
| $I_{CC}$                                      | Total supply current       | $V(\text{PWD}) = 5$ V  | 145         |     | mA            |
|   |                            | $V(\text{PWD}) = 0$ V  | 13          |     |               |
|   | Power-down input impedance |  | 11          |     | $k\Omega$     |
|   | Turnon time                |  | 120         |     | ns            |
|   | Turnoff time               |  | 20          |     | ns            |
| <b>Local Oscillator (LO) Input</b>            |                            |  |             |     |               |
|   | Input impedance            |  | $40 + j4.8$ |     | $\Omega$      |
| <b>Signal Inputs (IVIN, QVIN, IREF, QREF)</b> |                            |  |             |     |               |
|   | Input bias current         | $V(\text{IVIN}) = V(\text{IREF}) = V(\text{QVIN}) = V(\text{QREF}) = V_{CM} = 3.7$ V | 16          |     | $\mu\text{A}$ |
|   | Input impedance            | Single-ended input   | 250         |     | $k\Omega$     |
|   |                            | Differential input   | 125         |     |               |

**RF OUTPUT PERFORMANCE (942.5 MHz)**

Over recommended operating conditions,  $V_{CC} = 5\text{ V}$ ,  $V_{CM} = 3.7\text{ V}$ ,  $f_{LO} = 942.5\text{ MHz}$  at 0 dBm,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

| PARAMETER  |   | TEST CONDITIONS  | MIN     | TYP  | MAX                 | UNIT     |
|--|---|--|---------|------|---------------------|----------|
| <b>Single and Two-Tone Specifications</b>            |   |  |         |      |                     |          |
| Output power   |   |  | -3.5    | -1   |                     | dBm      |
| Second baseband harmonic (USB or LSB) <sup>(3)</sup> | I, Q <sup>(2)</sup> = 1 Vp-p, $f_{BB} = 928\text{ kHz}$ |  |         | -50  | -45                 | dBc      |
| Third baseband harmonic (USB or LSB) <sup>(3)</sup>  |   |  |         | -61  | -55                 | dBc      |
| IMD <sub>3</sub>                                     |   | I, Q <sup>(2)</sup> = 1 Vp-p (two-tone signal, $f_{BB1} = 928\text{ kHz}$ , $f_{BB2} = 992\text{ kHz}$ ) |         | -55  | -45                 | dBc      |
| P1dB (output compression point)                      |   |  |         | 6.5  |                     | dBm      |
| NSD Noise spectral density                           |   | I, Q <sup>(4)</sup> = $V_{CM} = 3.7\text{ VDC}$  |         | -156 |                     | dBm/Hz   |
|  |   | 6-MHz offset from carrier, $P_{out} = -10\text{ dBm}$ , over temperature                                 |         | -153 | -151 <sup>(5)</sup> |          |
|  |   | 6-MHz offset from carrier, $P_{out} = -5\text{ dBm}$ , over temperature                                  |         | -152 | -150 <sup>(5)</sup> |          |
|  |   | 6-MHz offset from carrier, $P_{out} = 0\text{ dBm}$ , over temperature                                   |         | -150 | -148 <sup>(5)</sup> |          |
| RFOUT pin impedance                                  |   |  | 26 + j3 |      |                     | $\Omega$ |
| Carrier suppression                                  |   | I, Q <sup>(2)</sup> = 1 Vp-p, $f_{BB} = 928\text{ kHz}$ , unadjusted                                     | 30      | 35   |                     | dBc      |
|  |   | I, Q <sup>(2)</sup> = 1 Vp-p, $f_{BB} = 928\text{ kHz}$ , optimized                                      |         | 55   |                     |          |
|  |   | I, Q <sup>(2)</sup> = 1 Vp-p, $f_{BB} = 928\text{ kHz}$ , over temperature                               |         | 35   |                     |          |
| Sideband suppression                                 |   | I, Q <sup>(2)</sup> = 1 Vp-p, $f_{BB} = 928\text{ kHz}$ , unadjusted                                     | 37      | 50   |                     | dBc      |
|  |   | I, Q <sup>(2)</sup> = 1 Vp-p, $f_{BB} = 928\text{ kHz}$ , optimized                                      |         | 55   |                     |          |
|  |   | I, Q <sup>(2)</sup> = 1 Vp-p, $f_{BB} = 928\text{ kHz}$ , over temperature                               |         | 38   |                     |          |

(1) Baseband inputs are differential; equivalent performance is attained by using single-ended drive.

(2) I, Q = 1 Vp-p implies that the magnitude of the signal at each input pin IVIN, IREF, QVIN, QREF is equal to 500 mVp-p.

(3) USB = upper sideband. LSB = lower sideband.

(4) All input pins tied to VCM

(5) Maximum noise values are assured by statistical characterization only, not production testing. The values specified are over the entire temperature range,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

## RF OUTPUT PERFORMANCE (340 MHz)

Over recommended operating conditions,  $V_{CC} = 5\text{ V}$ ,  $V_{CM} = 3.7\text{ V}$ ,  $f_{LO} = 340\text{ MHz}$  at 0 dBm,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

| PARAMETER  | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|------|
| <b>Single and Two-Tone Specifications</b>            |  |     |     |     |      |
| Output power   | $I, Q^{(2)} = 1\text{ Vp-p}$ , $f_{BB} = 928\text{ kHz}$   |     | -1  |     | dBm  |
| Second baseband harmonic (USB or LSB) <sup>(3)</sup> |  |     | -52 |     | dBc  |
| Third baseband harmonic (USB or LSB) <sup>(3)</sup>  |  |     | -45 |     | dBc  |
| IMD <sub>3</sub>                                     | $I, Q^{(2)} = 1\text{ Vp-p}$ (two-tone signal, $f_{BB1} = 928\text{ kHz}$ , $f_{BB2} = 992\text{ kHz}$ ) |     | 67  |     | dBc  |
| P1dB (output compression point)                      |  |     | 6   |     | dBm  |
| Carrier suppression                                  | $I, Q^{(2)} = 1\text{ Vp-p}$ , $f_{BB} = 928\text{ kHz}$ , unadjusted                                    | 40  | 51  |     | dBc  |
|  | $I, Q^{(2)} = 1\text{ Vp-p}$ , $f_{BB} = 928\text{ kHz}$ , optimized                                     |     | >60 |     |      |
| Sideband suppression                                 | $I, Q^{(2)} = 1\text{ Vp-p}$ , $f_{BB} = 928\text{ kHz}$ , unadjusted                                    |     | 35  |     | dBc  |
|  | $I, Q^{(2)} = 1\text{ Vp-p}$ , $f_{BB} = 928\text{ kHz}$ , optimized                                     |     | >60 |     |      |

(1) Baseband inputs are differential; equivalent performance is attained by using single-ended drive.

(2)  $I, Q = 1\text{ Vp-p}$  implies that the magnitude of the signal at each input pin  $I_{VIN}$ ,  $I_{REF}$ ,  $Q_{VIN}$ ,  $Q_{REF}$  is equal to 500 mVp-p.

(3) USB = upper sideband. LSB = lower sideband.

## RF OUTPUT PERFORMANCE (140 MHz)

Over recommended operating conditions,  $V_{CC} = 5\text{ V}$ ,  $V_{CM} = 3.7\text{ V}$ ,  $f_{LO} = 140\text{ MHz}$  at 0 dBm,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

| PARAMETER  | TEST CONDITIONS  | MIN | TYP   | MAX | UNIT |
|--|--|-----|-------|-----|------|
| <b>Single and Two-Tone Specifications</b>            |  |     |       |     |      |
| Output power   | $I, Q^{(2)} = 1\text{ Vp-p}$ , $f_{BB} = 928\text{ kHz}$   |     | -1    |     | dBm  |
| Second baseband harmonic (USB or LSB) <sup>(3)</sup> |  |     | -61.5 |     | dBc  |
| Third baseband harmonic (USB or LSB) <sup>(3)</sup>  |  |     | -46   |     | dBc  |
| IMD <sub>3</sub>                                     | $I, Q^{(2)} = 1\text{ Vp-p}$ (two-tone signal, $f_{BB1} = 928\text{ kHz}$ , $f_{BB2} = 992\text{ kHz}$ ) |     | 68    |     | dBc  |
| P1dB (output compression point)                      |  |     | 3.6   |     | dBm  |
| Carrier suppression                                  | $I, Q^{(2)} = 1\text{ Vp-p}$ , $f_{BB} = 928\text{ kHz}$ , unadjusted                                    | 40  | 50    |     | dBc  |
|  | $I, Q^{(2)} = 1\text{ Vp-p}$ , $f_{BB} = 928\text{ kHz}$ , optimized                                     |     | >60   |     |      |
| Sideband suppression                                 | $I, Q^{(2)} = 1\text{ Vp-p}$ , $f_{BB} = 928\text{ kHz}$ , unadjusted                                    |     | 35    |     | dBc  |
|  | $I, Q^{(2)} = 1\text{ Vp-p}$ , $f_{BB} = 928\text{ kHz}$ , optimized                                     |     | >60   |     |      |

(1) Baseband inputs are differential; equivalent performance is attained by using single-ended drive.

(2)  $I, Q = 1\text{ Vp-p}$  implies that the magnitude of the signal at each input pin  $I_{VIN}$ ,  $I_{REF}$ ,  $Q_{VIN}$ ,  $Q_{REF}$  is equal to 500 mVp-p.

(3) USB = upper sideband. LSB = lower sideband.

## DEFINITIONS OF SELECTED SPECIFICATIONS

### Unadjusted Carrier Suppression

This specification measures the amount by which the local oscillator component is attenuated in the output spectrum of the modulator relative to the carrier. It is assumed that the baseband inputs delivered to the pins of the TRF3701 are perfectly matched to have the same dc offset (VCM). This includes all four baseband inputs: IVIN, QVIN, IREF and QREF. Unadjusted carrier suppression is measured in dBc.

### Adjusted (Optimized) Carrier Suppression

This differs from the unadjusted suppression number in that the dc offsets of the baseband inputs are iteratively adjusted around their theoretical value of VCM in order to yield the maximum suppression of the LO component in the output spectrum. Adjusted carrier suppression is measured in dBc.

### Unadjusted Sideband Suppression

This specification measures the amount by which the unwanted sideband of the input signal is attenuated in the output of the modulator, relative to the wanted sideband. It is assumed that the baseband inputs delivered to the modulator input pins are perfectly matched in amplitude and are exactly 90° out of phase. Unadjusted sideband suppression is measured in dBc.

### Adjusted (Optimized) Sideband Suppression

This differs from the unadjusted sideband suppression in that the baseband inputs are iteratively adjusted around their theoretical values to maximize the amount of sideband suppression. Adjusted sideband suppression is measured in dBc.

### Suppressions Over Temperature

This specification assumes that the user has gone through the optimization process for the suppression in question, and set the optimal settings for the I, Q inputs at room temperature. This specification then measures the suppression when temperature conditions change after the initial calibration is done.

**TYPICAL CHARACTERISTICS**

For all the performance plots in this section, the following conditions were used, unless otherwise noted:  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ,  $V_{CM} = 3.7\text{ V}$ ,  $f_{LO} = 942.5\text{ MHz}$  at  $P_{LO} = 0\text{ dBm}$ , I and Q inputs driven differentially at a frequency of  $50\text{ kHz}$  for an output power level  $P_{out} = 0\text{ dBm}$ . In the case of optimized suppressions, the point of optimization is noted and is always at nominal conditions and room temperature. A level of  $>50\text{ dBc}$  is assumed to be optimized.

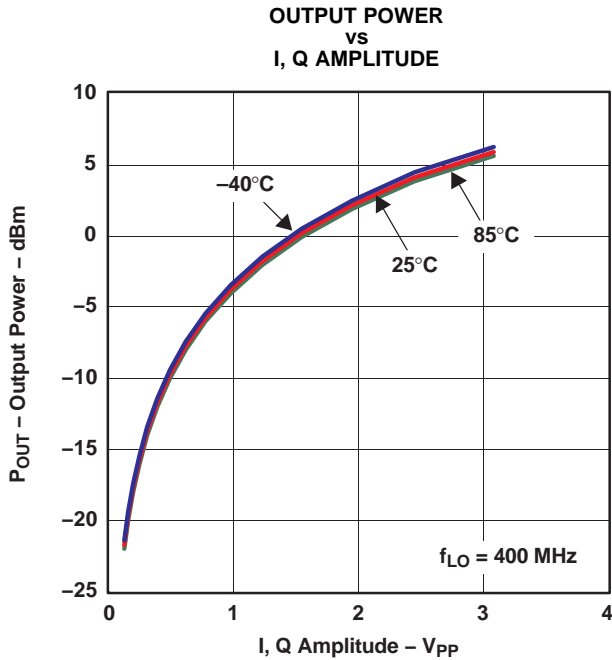


Figure 1.

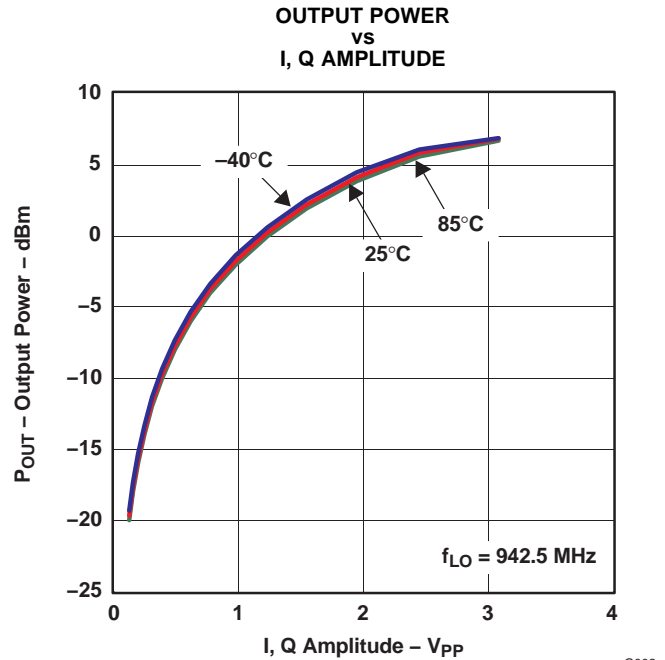


Figure 2.

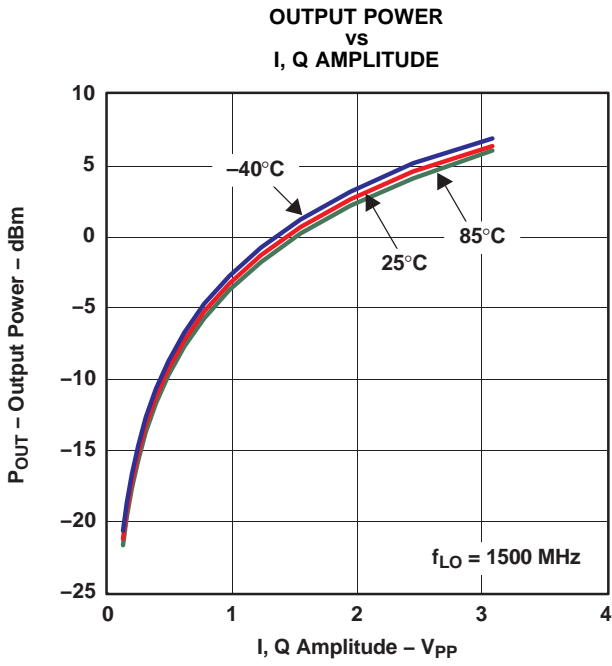


Figure 3.

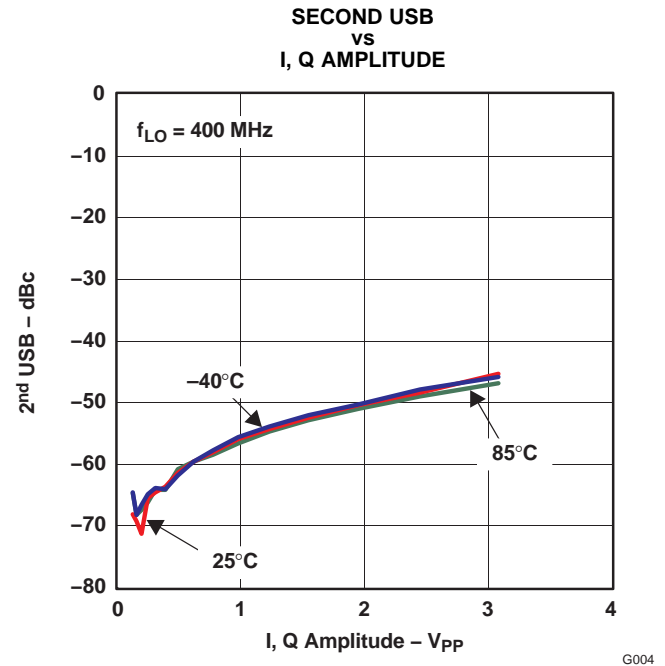
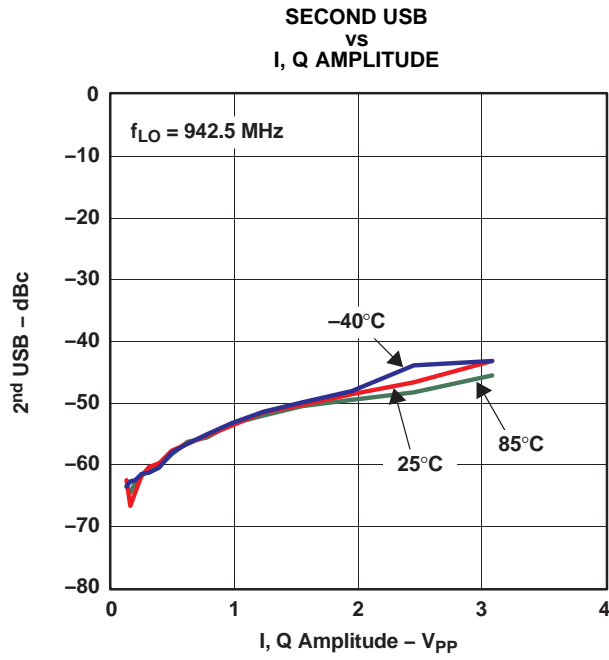


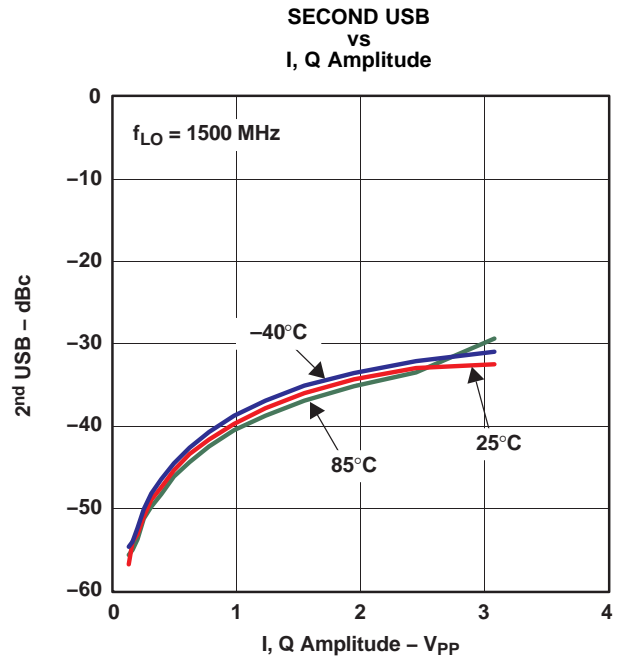
Figure 4.

TYPICAL CHARACTERISTICS (continued)



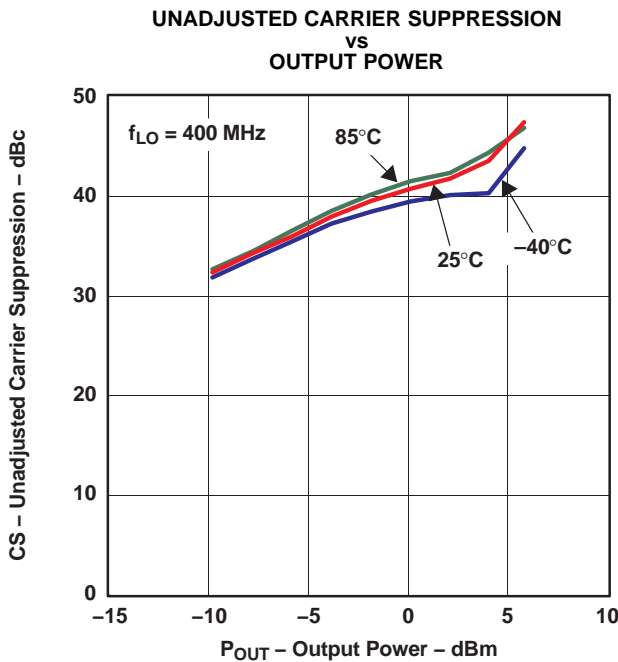
G005

Figure 5.



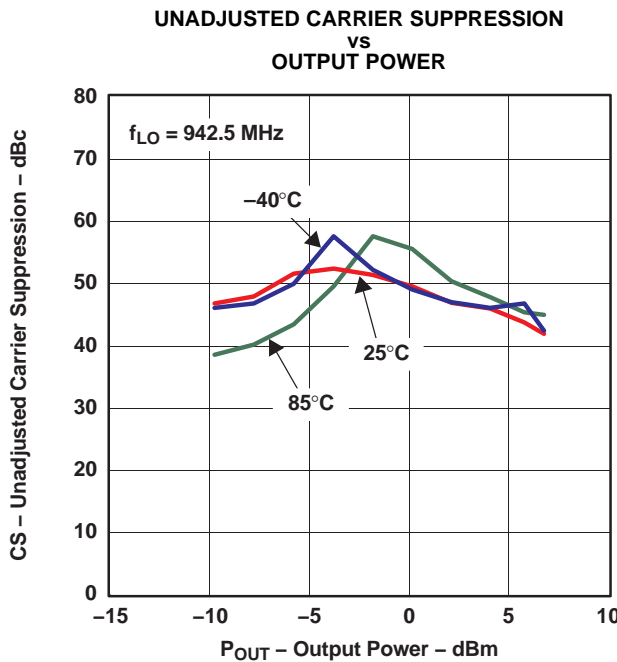
G006

Figure 6.



G007

Figure 7.



G008

Figure 8.



**TYPICAL CHARACTERISTICS (continued)**

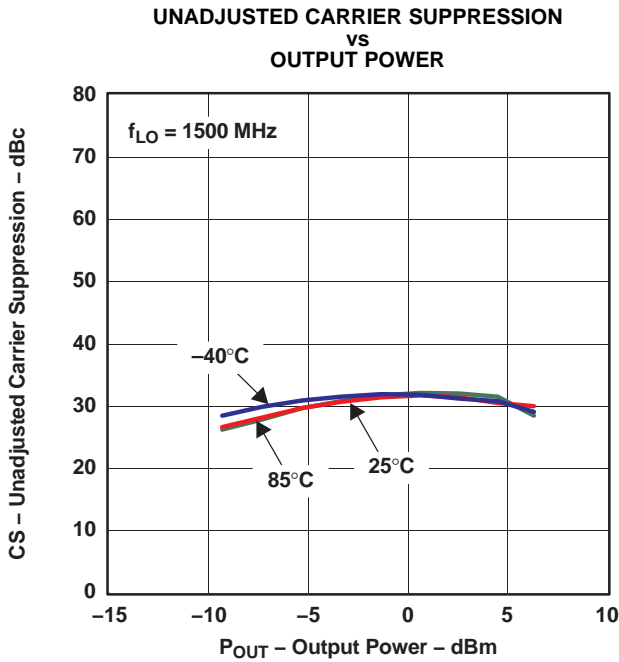


Figure 9.

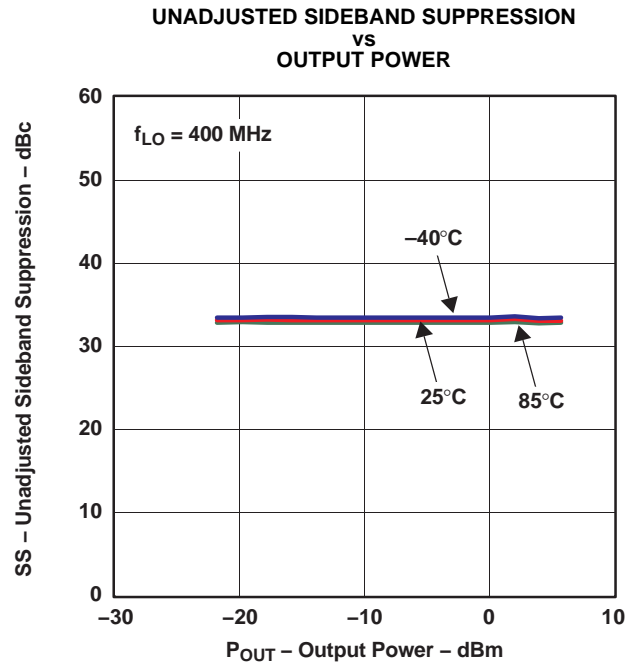


Figure 10.

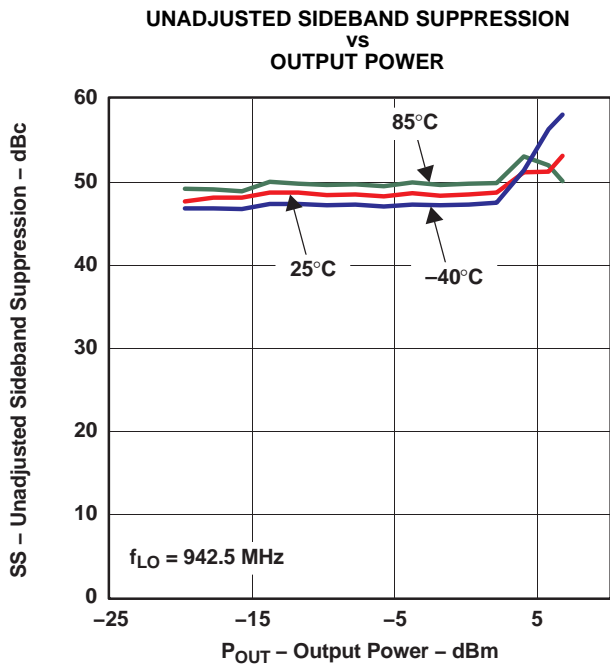


Figure 11.

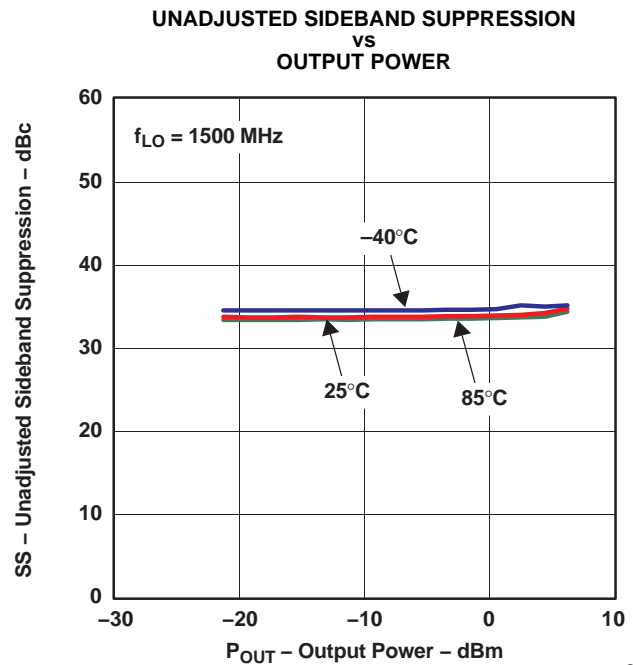
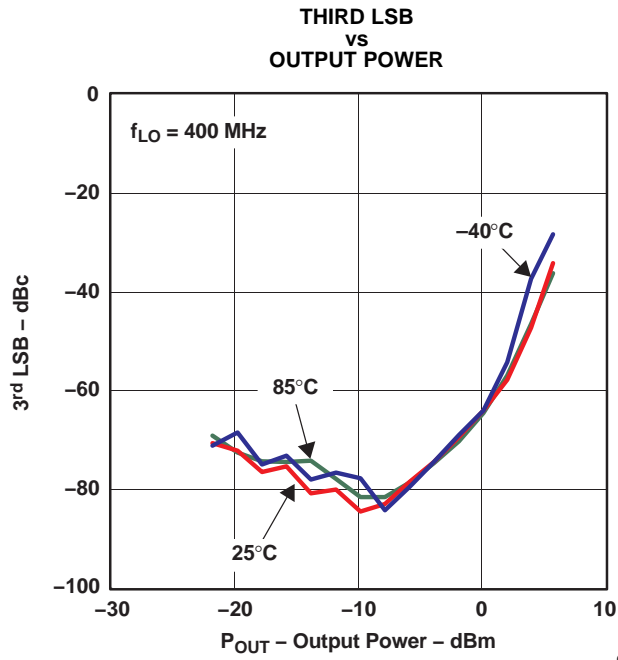


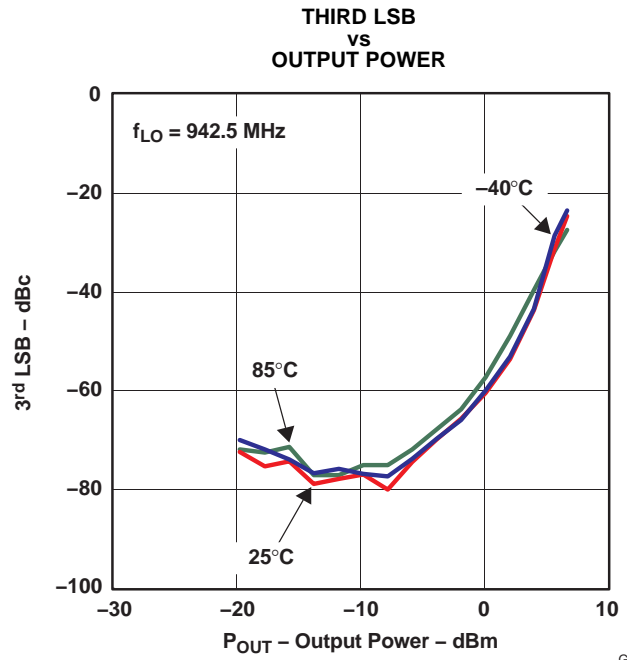
Figure 12.

**TYPICAL CHARACTERISTICS (continued)**



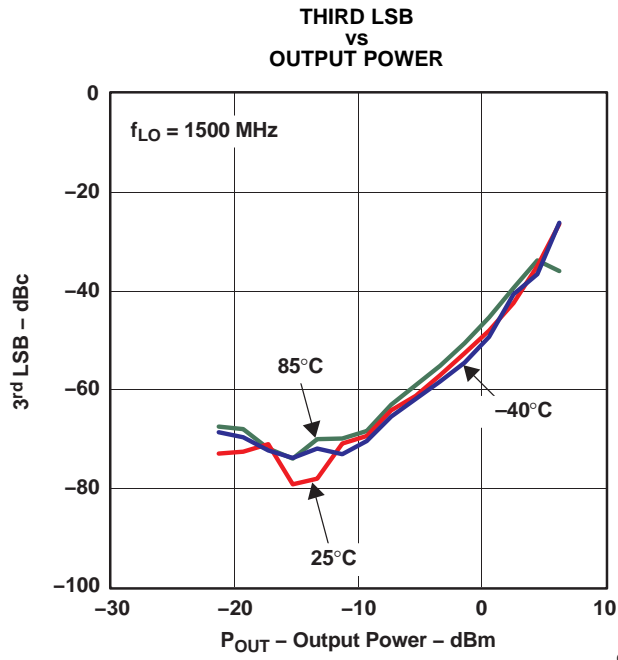
G013

Figure 13.



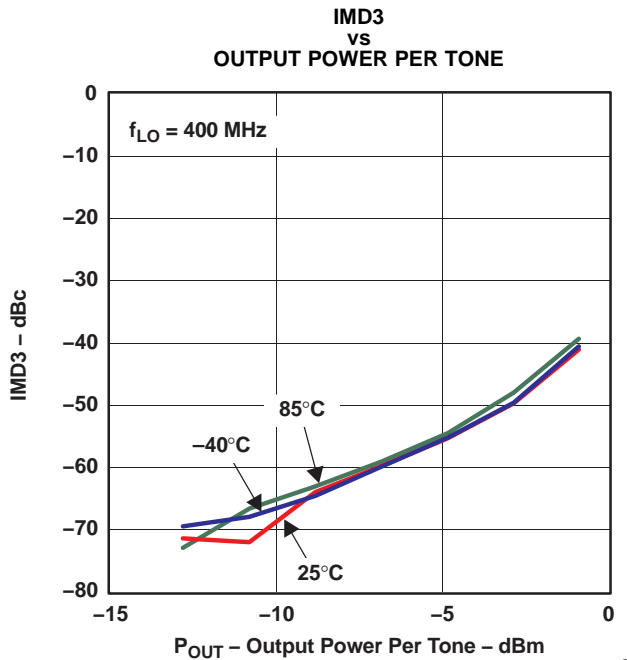
G014

Figure 14.



G015

Figure 15.



G016

Figure 16.

TYPICAL CHARACTERISTICS (continued)

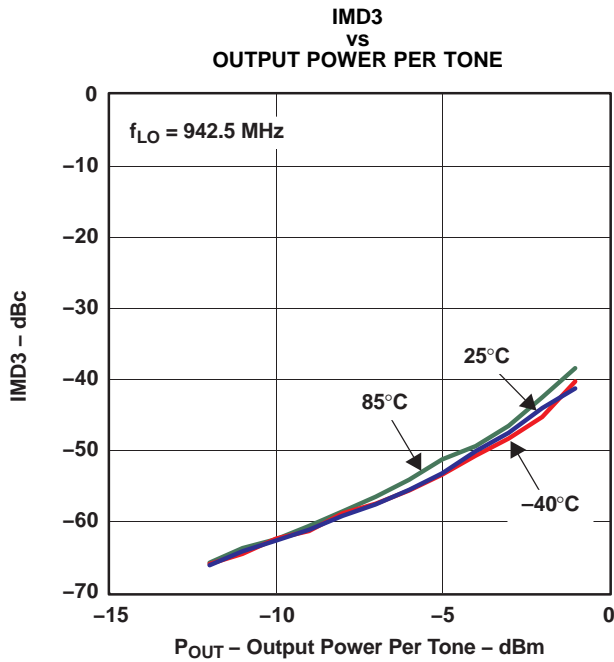


Figure 17.

G017

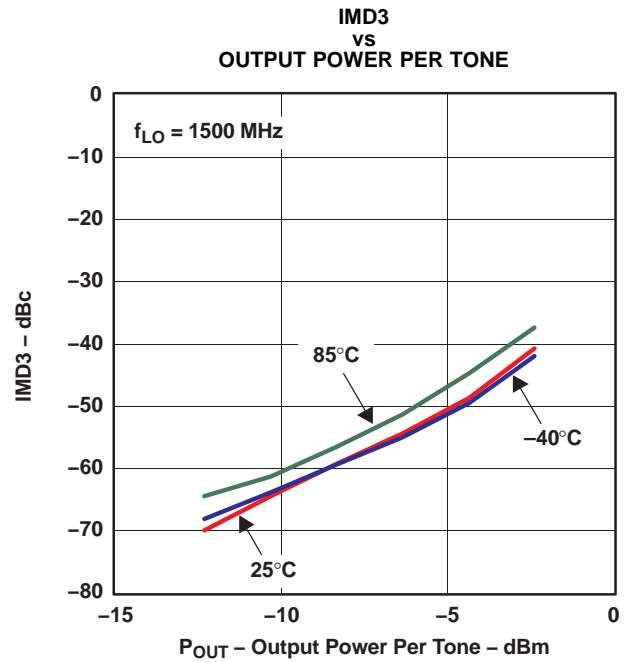


Figure 18.

G018

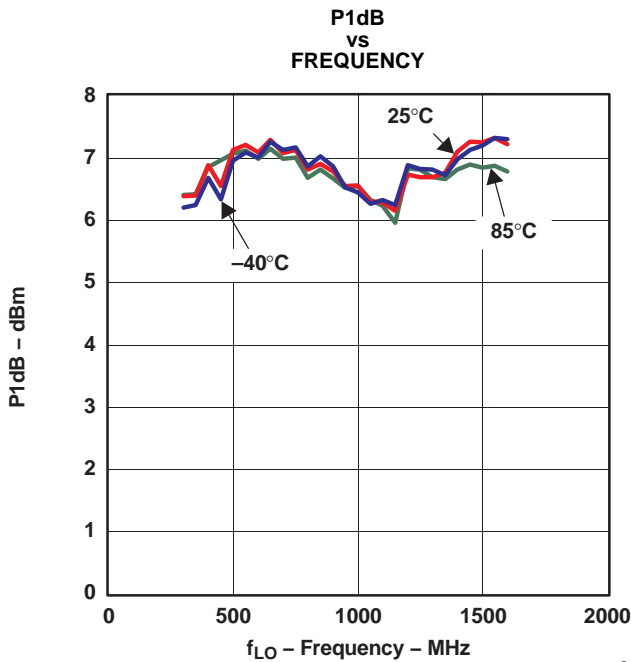


Figure 19.

G019

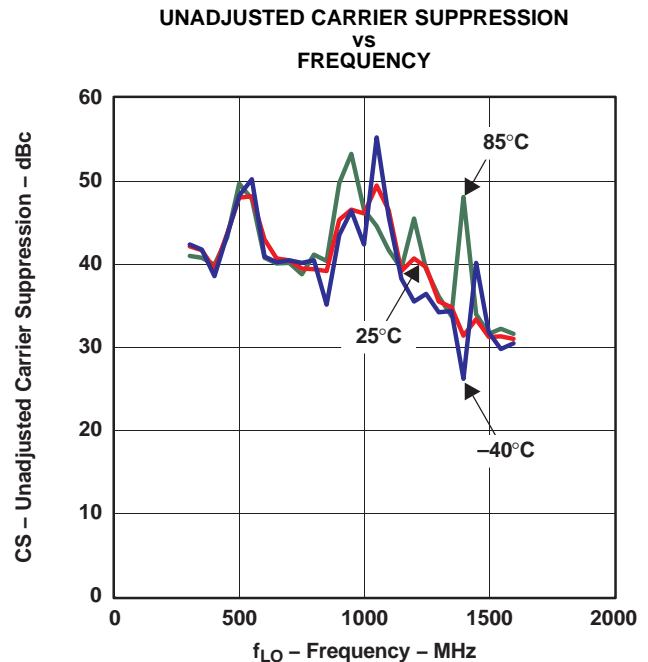


Figure 20.

G020

TYPICAL CHARACTERISTICS (continued)

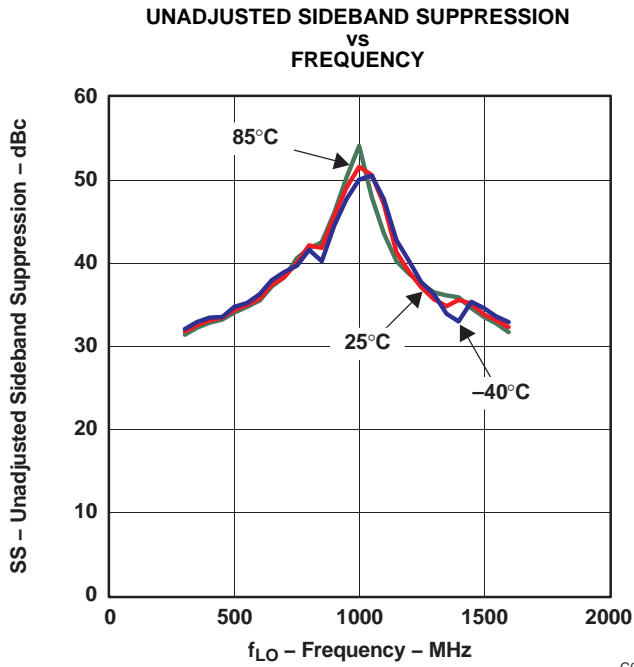


Figure 21.

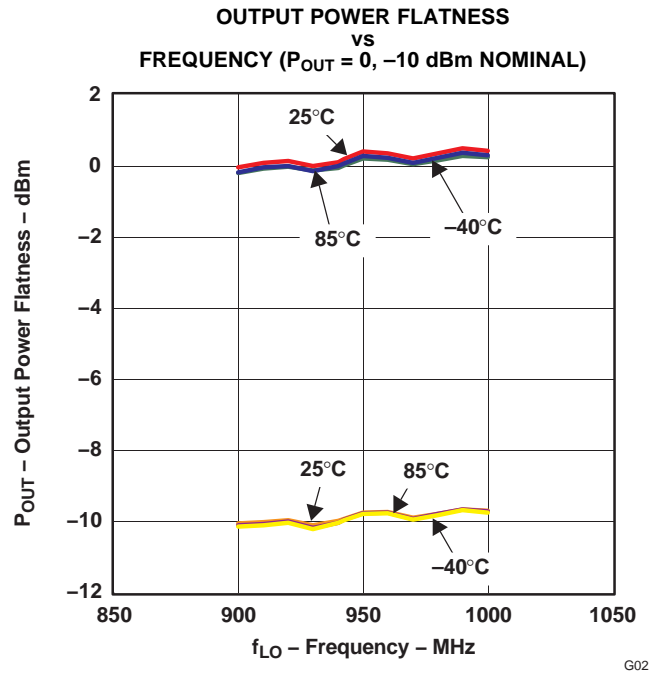


Figure 22.

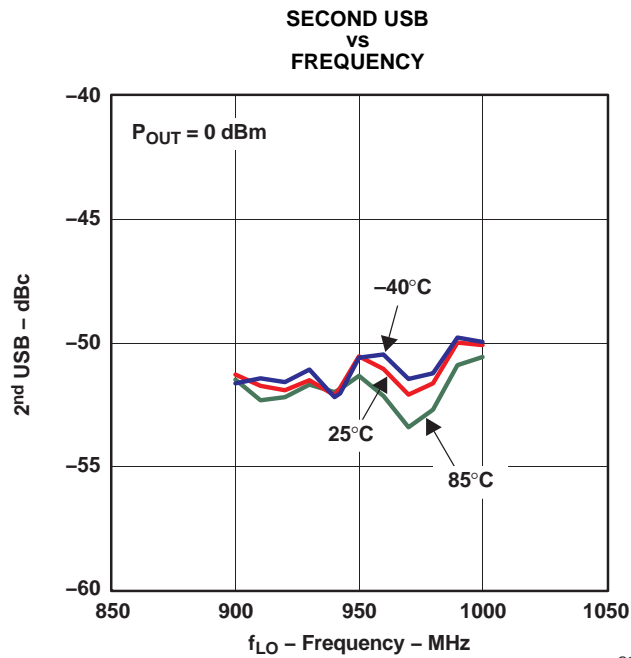


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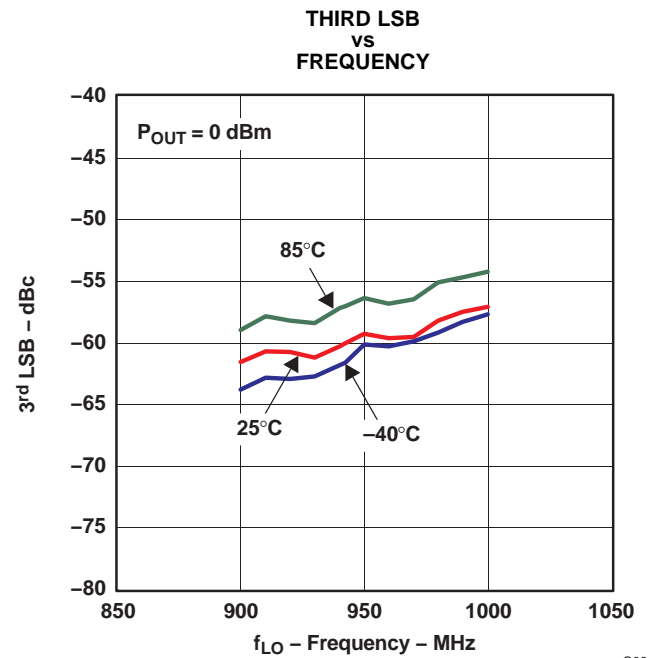


Figure 24.

TYPICAL CHARACTERISTICS (continued)

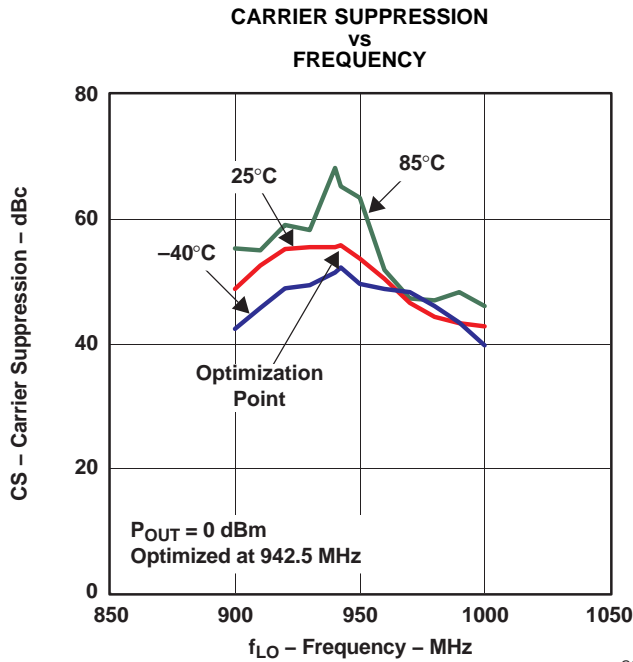


Figure 25.

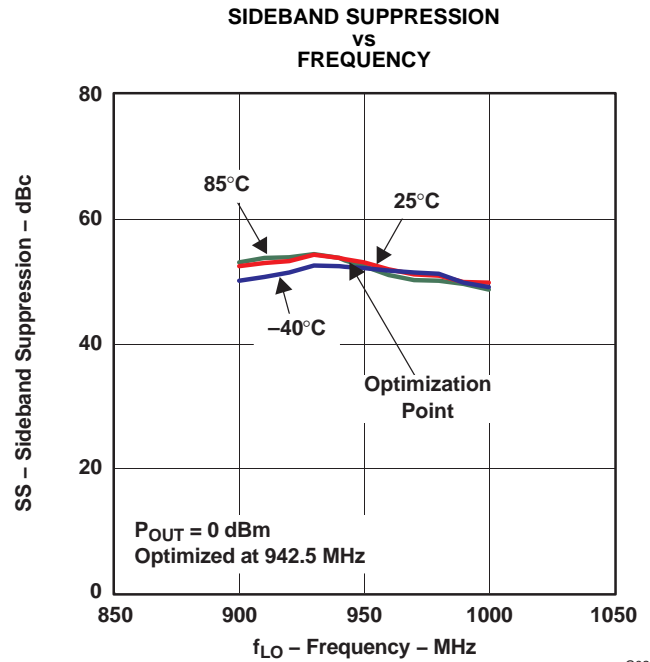


Figure 26.

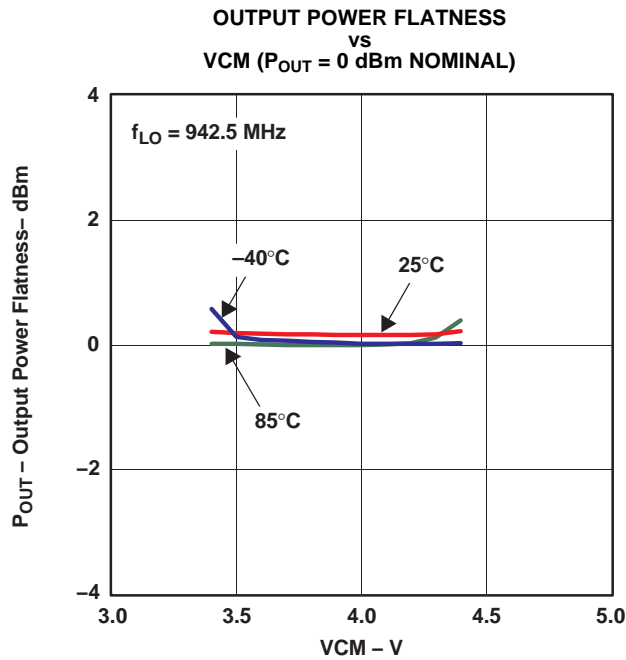


Figure 27.

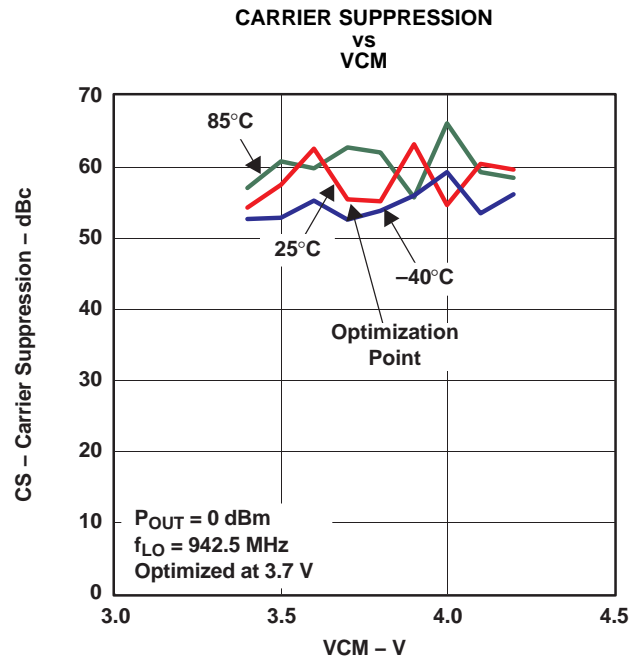


Figure 28.

TYPICAL CHARACTERISTICS (continued)

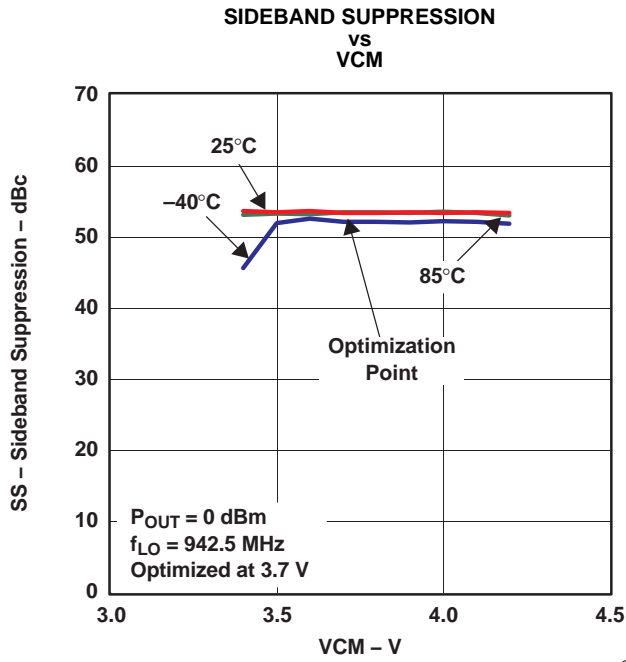


Figure 29.

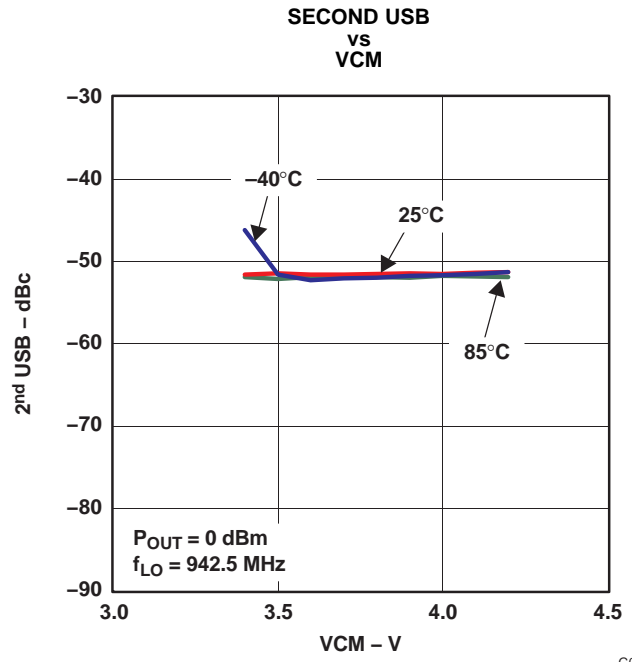


Figure 30.

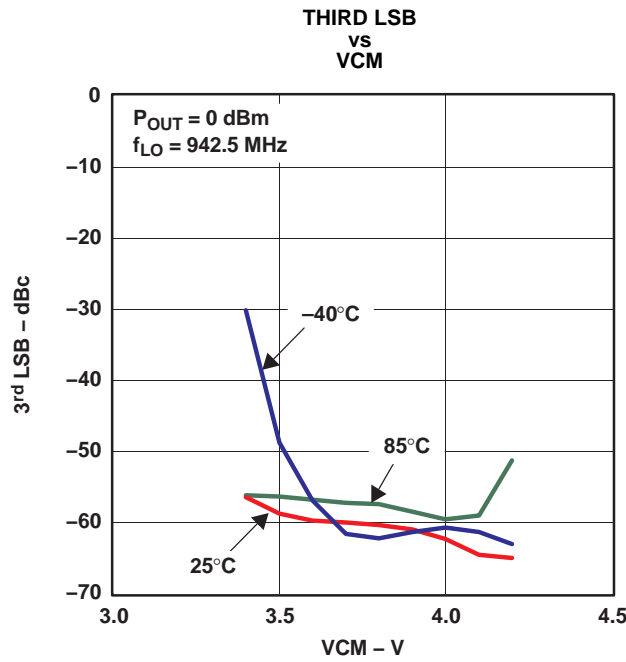


Figure 31.

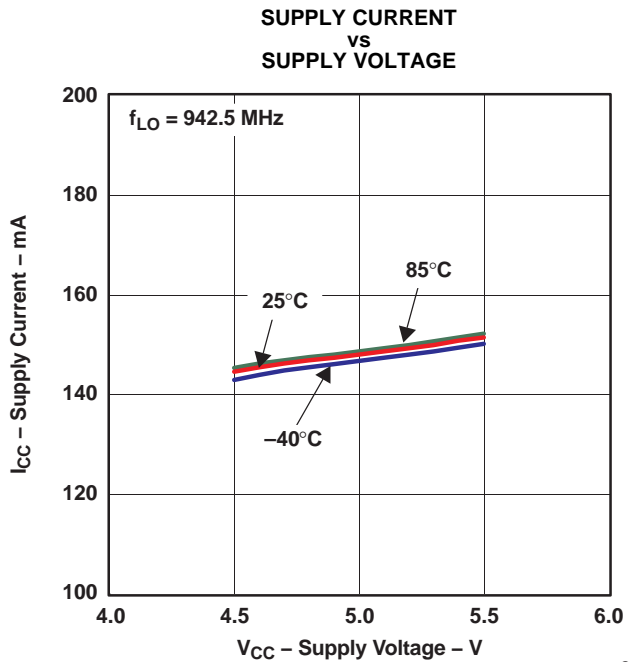


Figure 32.

TYPICAL CHARACTERISTICS (continued)

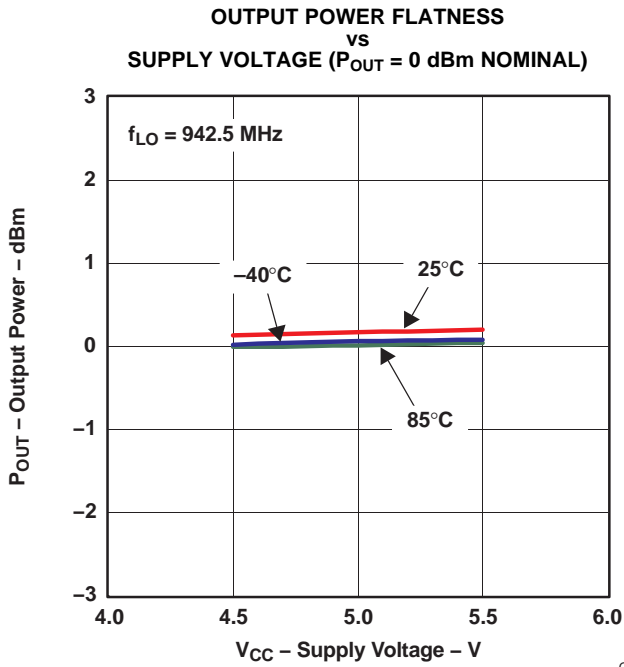


Figure 33.

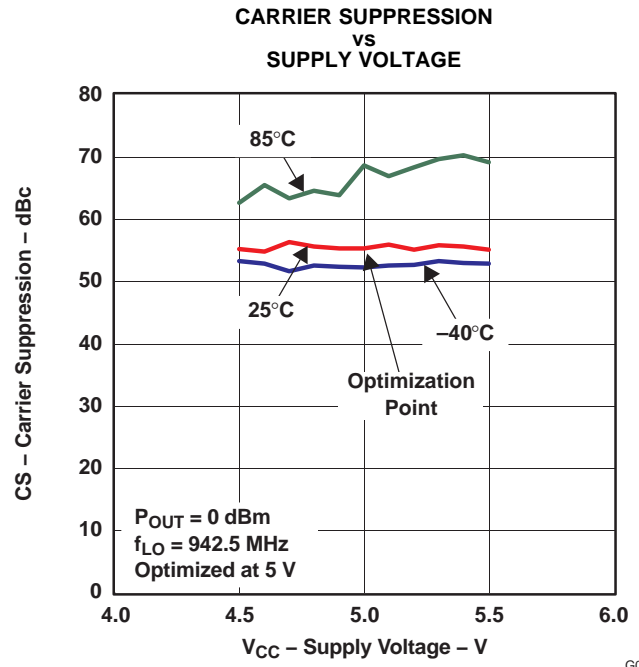


Figure 34.

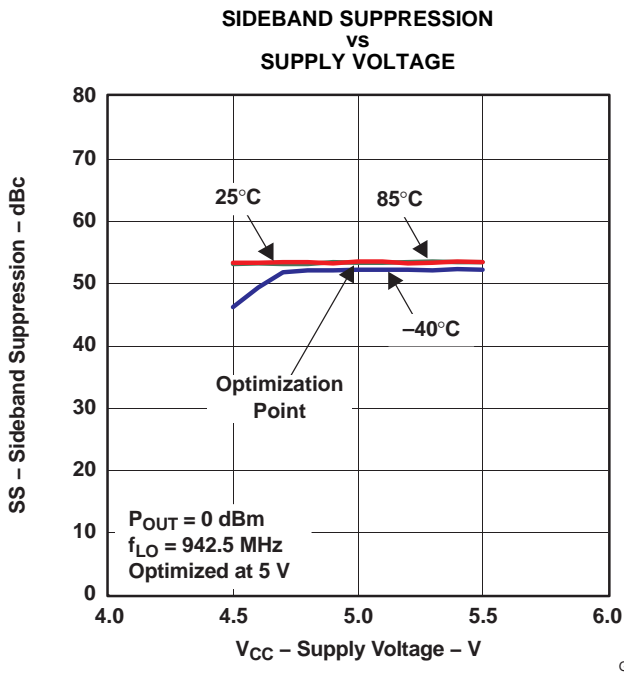


Figure 35.

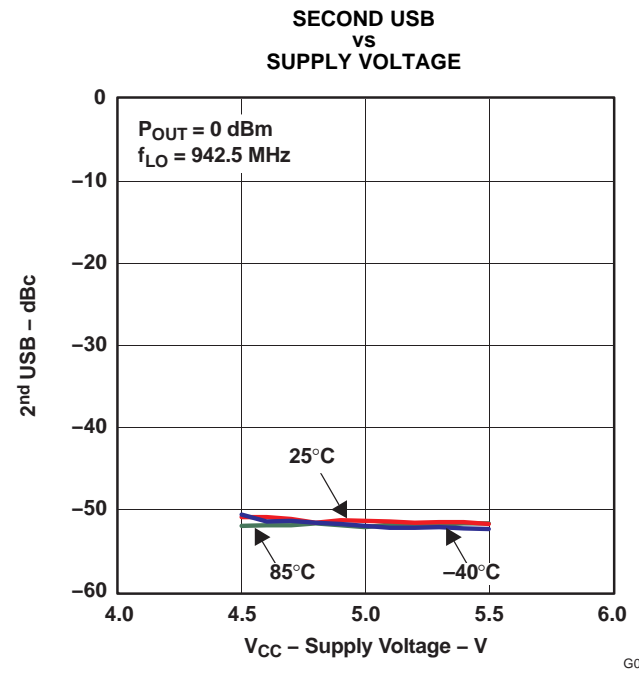


Figure 36.

TYPICAL CHARACTERISTICS (continued)

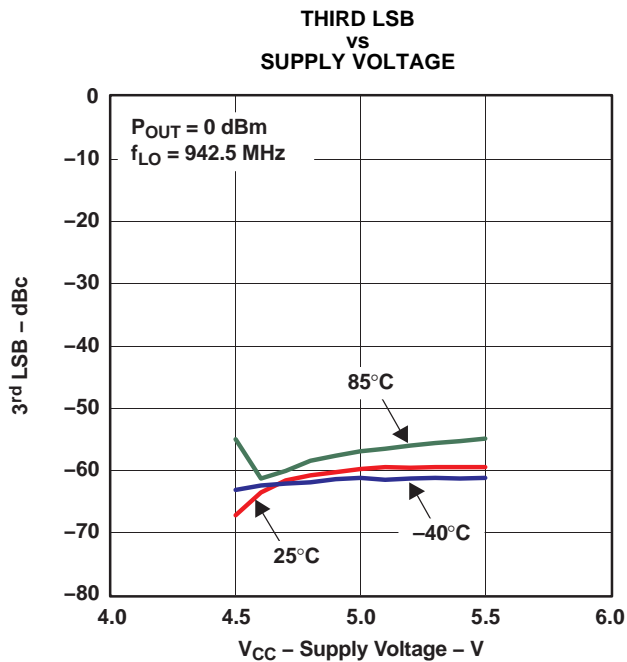


Figure 37.

G037

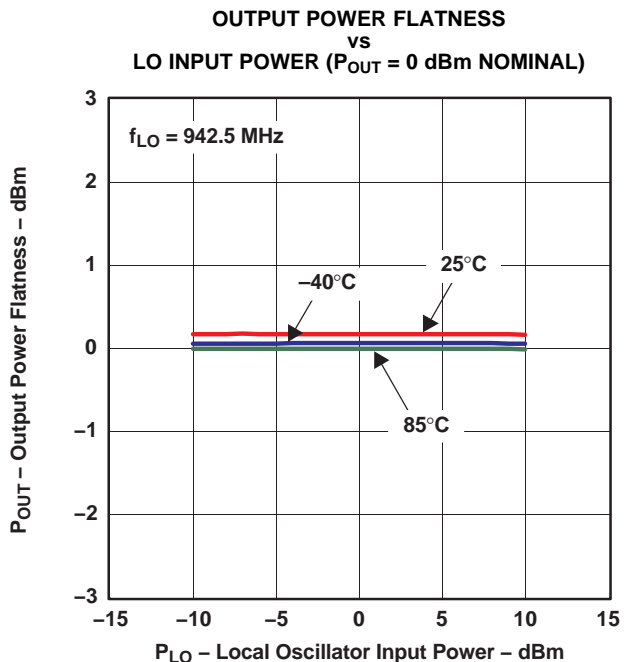


Figure 38.

G038

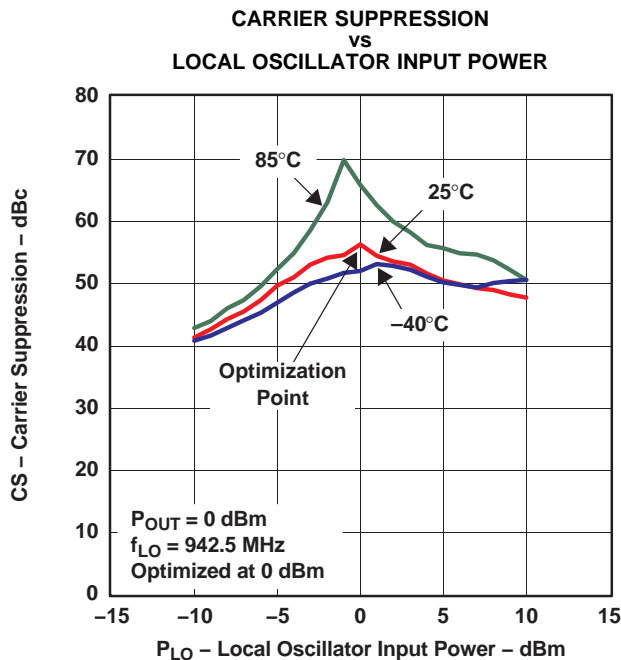


Figure 39.

G039



**Table 2. RFOUT and LO Pin Impedance**

| Frequency (MHz) | Z (RFOUT Pin)   | Z (LO Pin)       |
|-----------------|-----------------|------------------|
| 100             | 8.59 – j 130.2  | 33.95 – j 106.93 |
| 200             | 7.12 – j 61.22  | 29.54 – j 52.57  |
| 300             | 8.52 – j 36.37  | 28.65 – j 31.83  |
| 400             | 10.5 – j 23.72  | 29.371 – j 19.33 |
| 500             | 12.82 – j 15.51 | 30.78 – j 11.42  |
| 600             | 15.26 – j 9.33  | 32.64 – j 6.06   |
| 700             | 187.1 – j 4.77  | 34.99 – j 1.65   |
| 800             | 20.8 – j 1.2    | 36.55 + j 1.65   |
| 900             | 24.2 + j 2.0    | 38.52 + j 3.98   |
| 1000            | 28.7 + j 4.9    | 40.29 + j 5.92   |
| 1100            | 32.35 + j 6.61  | 42.21 + j 6.98   |
| 1200            | 37.15 + j 6.88  | 44.09 + j 7.55   |
| 1300            | 40.55 + j 6.64  | 45.7 + j 7.96    |
| 1400            | 43.76 + j 6.4   | 47 + j 7.76      |
| 1500            | 46.6 + j 6.03   | 48.28 + j 7.39   |

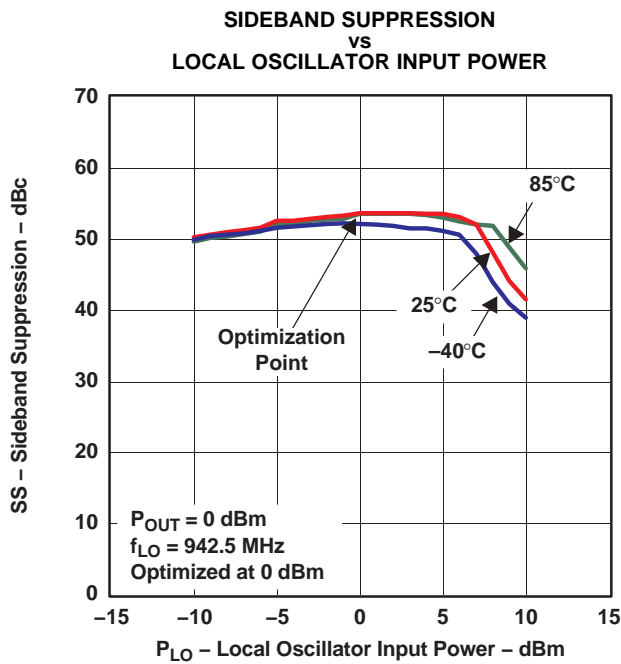


Figure 40.

G040

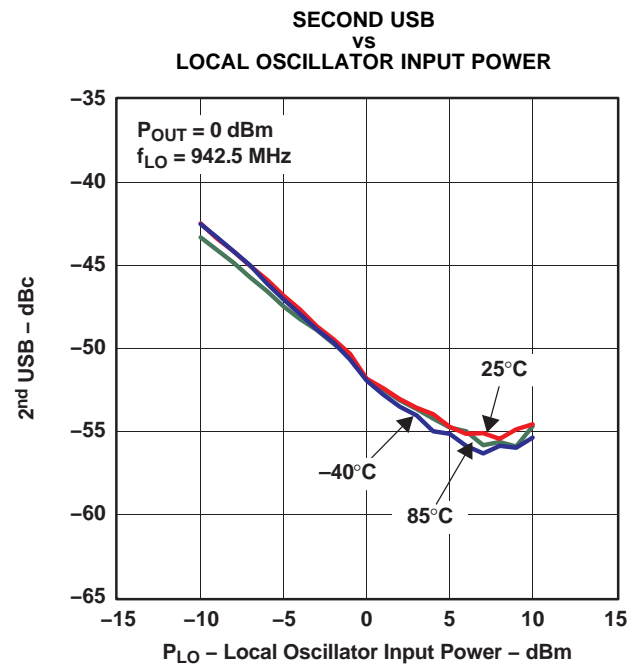


Figure 41.

G041

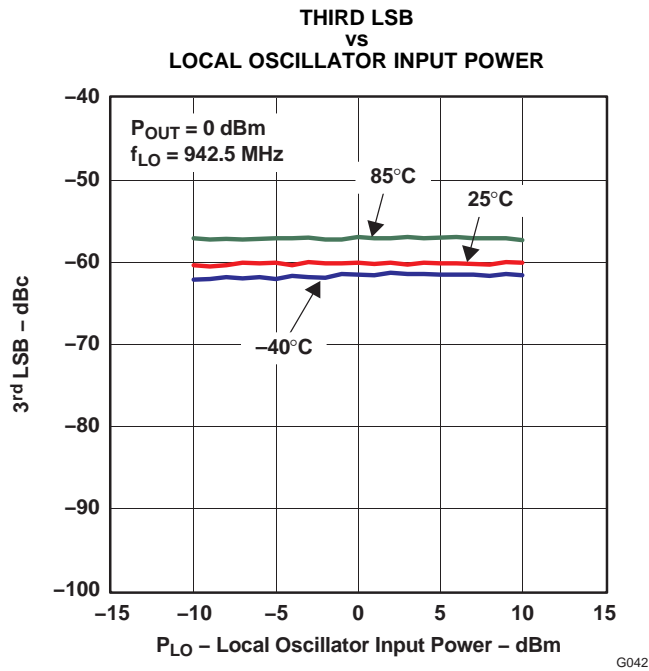


Figure 42.

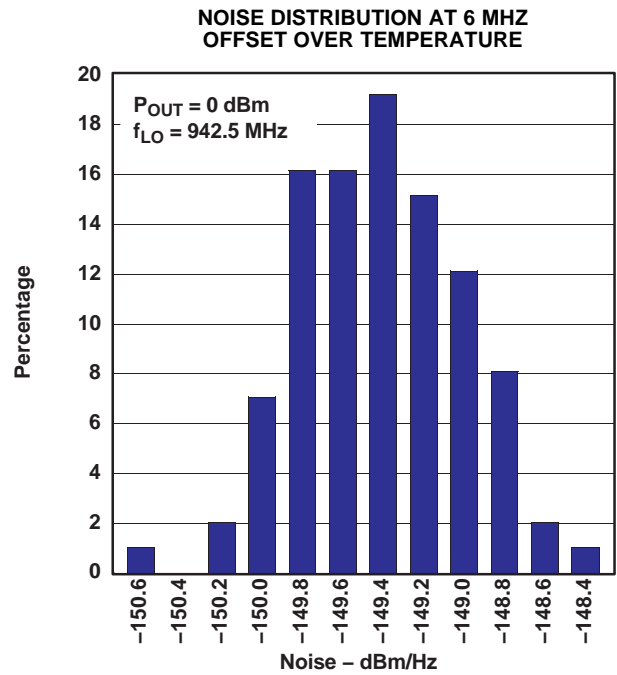


Figure 43.

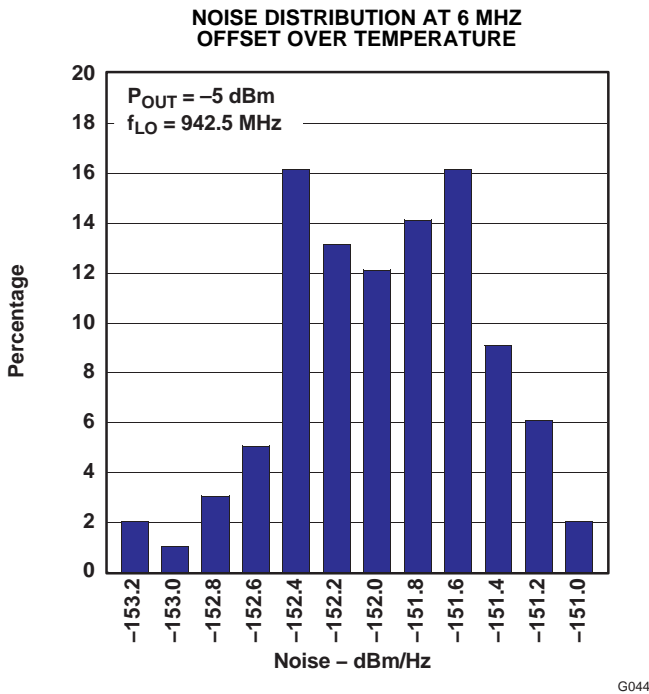


Figure 44.

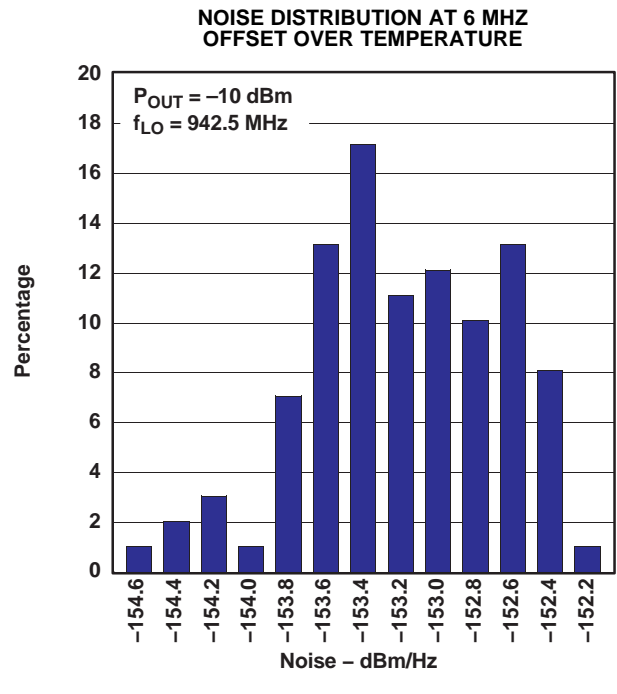


Figure 45.

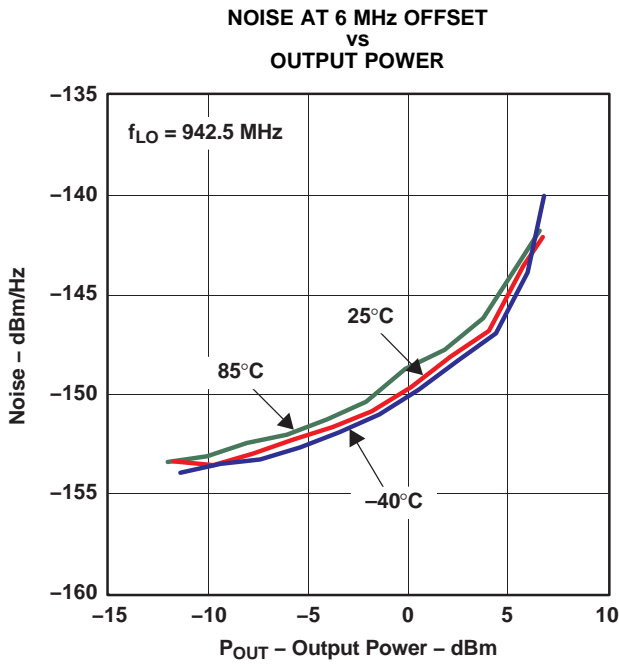


Figure 46.

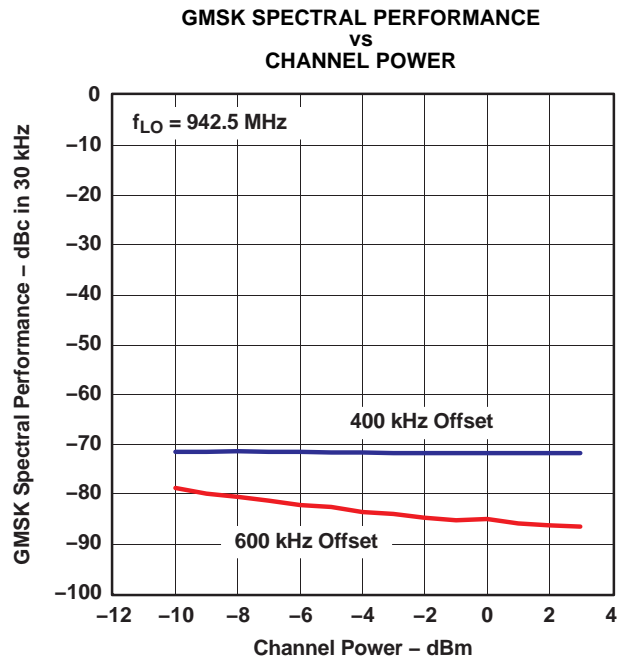


Figure 47.

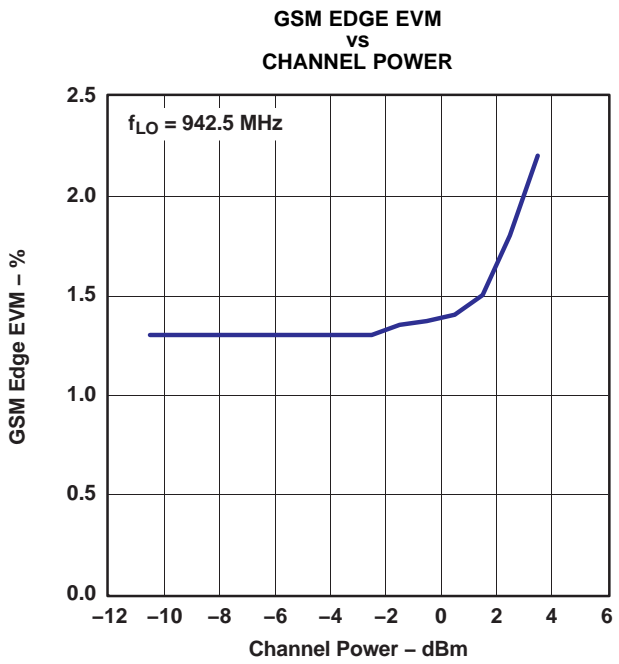


Figure 48.

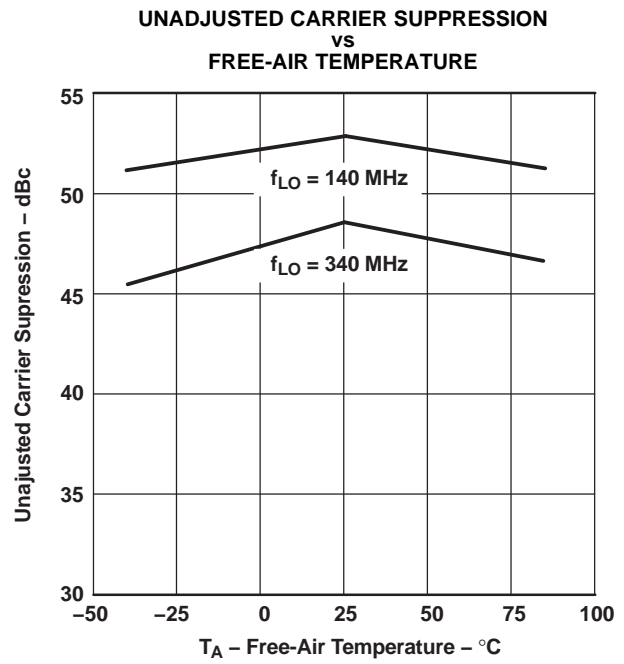


Figure 49.

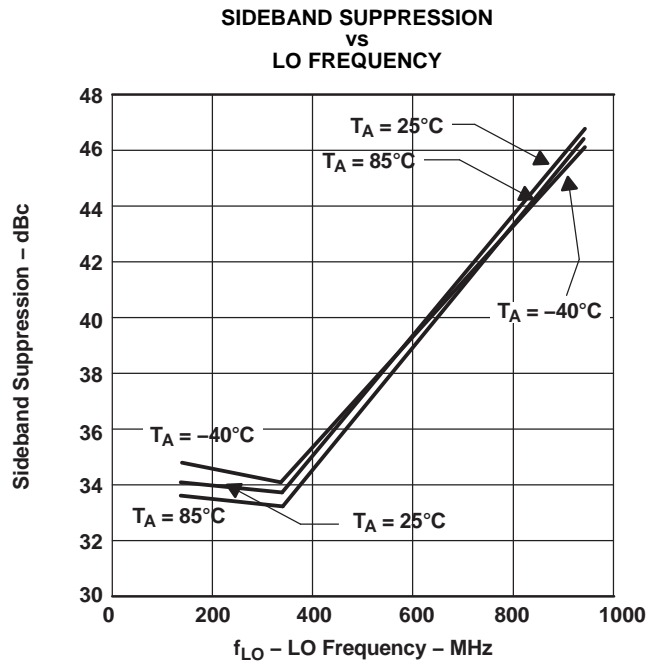


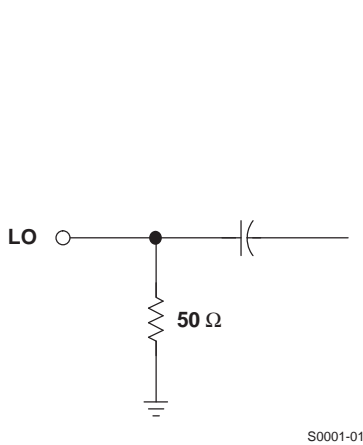
Figure 50.

### THEORY OF OPERATION

The TRF3701 employs a double-balanced mixer architecture in implementing the direct I, Q upconversion. The I, Q inputs can be driven single-endedly or differentially, with comparable performance in both cases. The common mode level (VCM) of the four inputs (IVIN, IREF, QVIN, QREF) is typically set to 3.7 V and needs to be driven externally. These inputs go through a set of differential amplifiers and through a V-I converter feed the double-balanced mixers. The AC-coupled LO input to the device goes through a phase splitter to provide the in-phase and quadrature signals that in turn drive the mixers. The outputs of the mixers are then summed, converted to single-ended signals, and amplified before they are fed to the output port RFOUT. The output of the TRF3701 is ac-coupled and can drive 50-Ω loads.

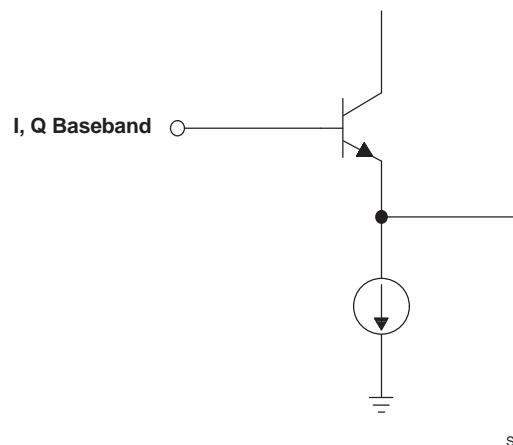
### EQUIVALENT CIRCUITS

Figure 51 through Figure 54 show equivalent schematics for the main inputs and outputs of the device.



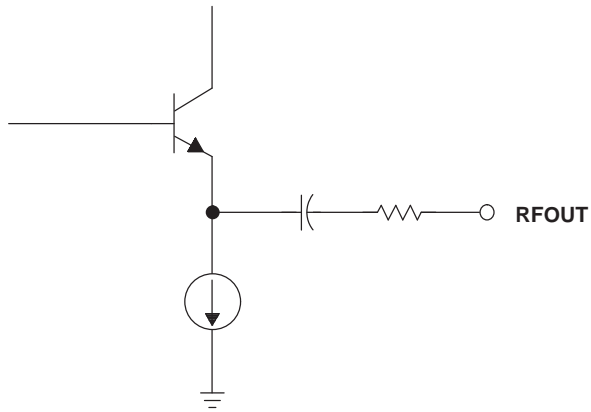
S0001-01

Figure 51. LO Equivalent Input Circuit



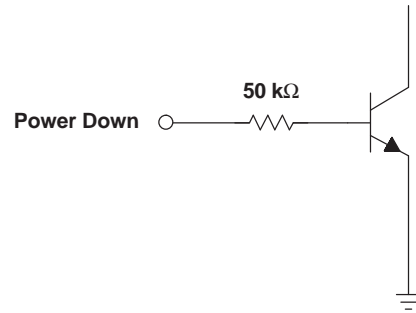
S0002-01

Figure 52. IVIN, QVIN, IREF, QREF Equivalent Circuit



S0003-01

Figure 53. RFOUT Equivalent Circuit



S0004-01

Figure 54. Power-Down (PWD) Equivalent Circuit

## APPLICATION INFORMATION

### DRIVING THE I, Q INPUTS

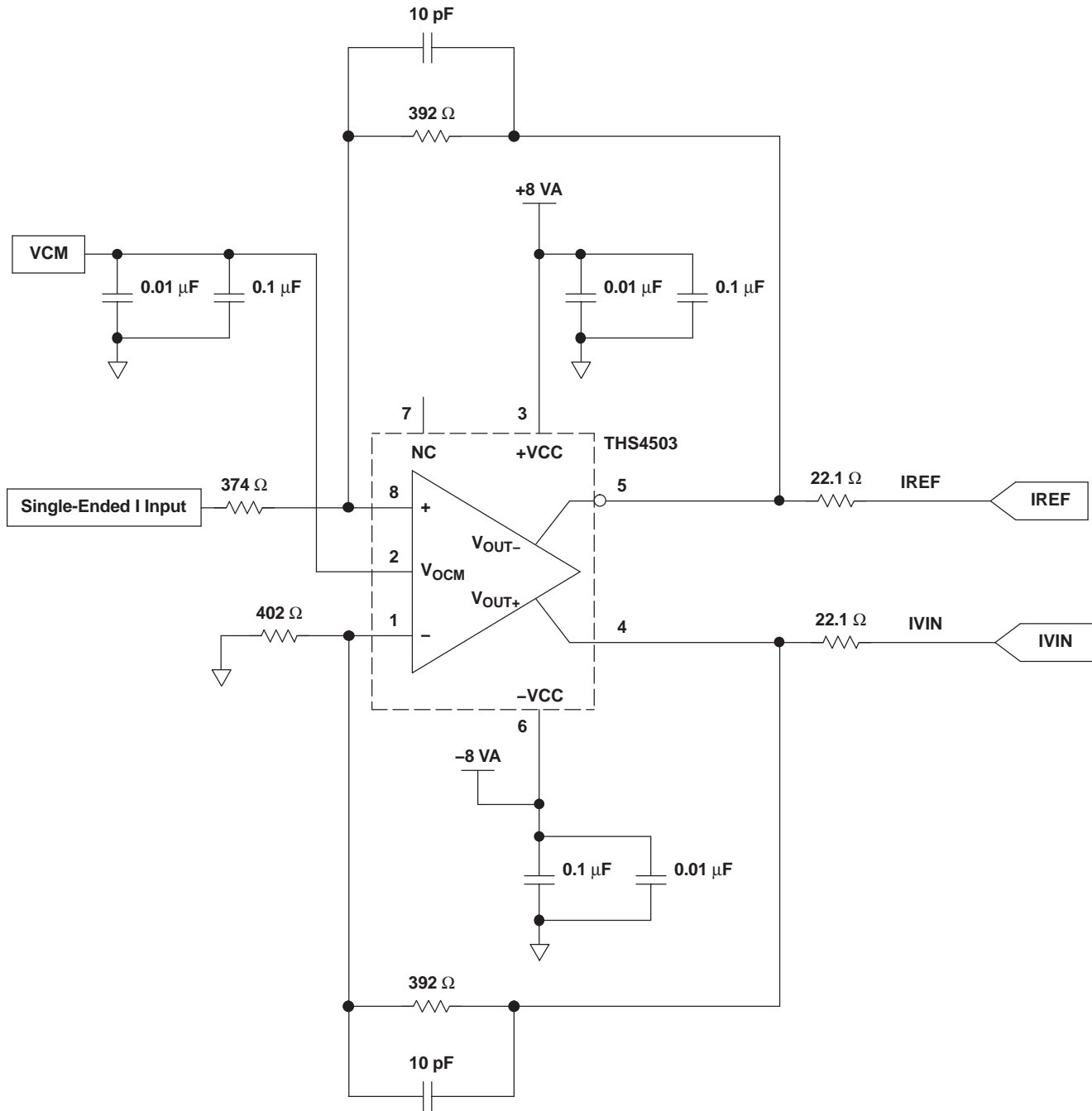
There are several ways to drive the four baseband inputs of the TRF3701 to the required amplitude and dc offset. The optimal configuration depends on the end application requirements and the signal levels desired by the designer.

The TRF3701 is by design a differential part, meaning that ideally the user should provide fully complementary signals. However, similar performance in every respect can be achieved if the user only has single-ended signals available. In this case, the IREF and QREF pins just need to have the VCM dc offset applied.

#### Implementing a Single-to-Differential Conversion for the I, Q inputs

In case differential I, Q signals are desired but not available, the THS4503 family of wideband, low-distortion, fully differential amplifiers can be used to provide a convenient way of performing this conversion. Even if differential signals are available, the THS4503 can provide gain in case a higher voltage swing is required. Besides featuring high bandwidth and high linearity, the THS4503 also provides a convenient way of applying the VCM to all four inputs to the modulator through the VOCM pin (pin 2). The user can further adjust the dc levels for optimum carrier suppression by injecting extra dc at the inputs to the operational amplifier, or by individually adding it to the four outputs. [Figure 55](#) shows a typical implementation of the THS4503 as a driver for the TRF3701. Gain can be easily incorporated in the loop by adjusting the feedback resistors appropriately. For more details, see the THS4503 data sheet at [www.ti.com](http://www.ti.com).

APPLICATION INFORMATION (continued)



S0005-02

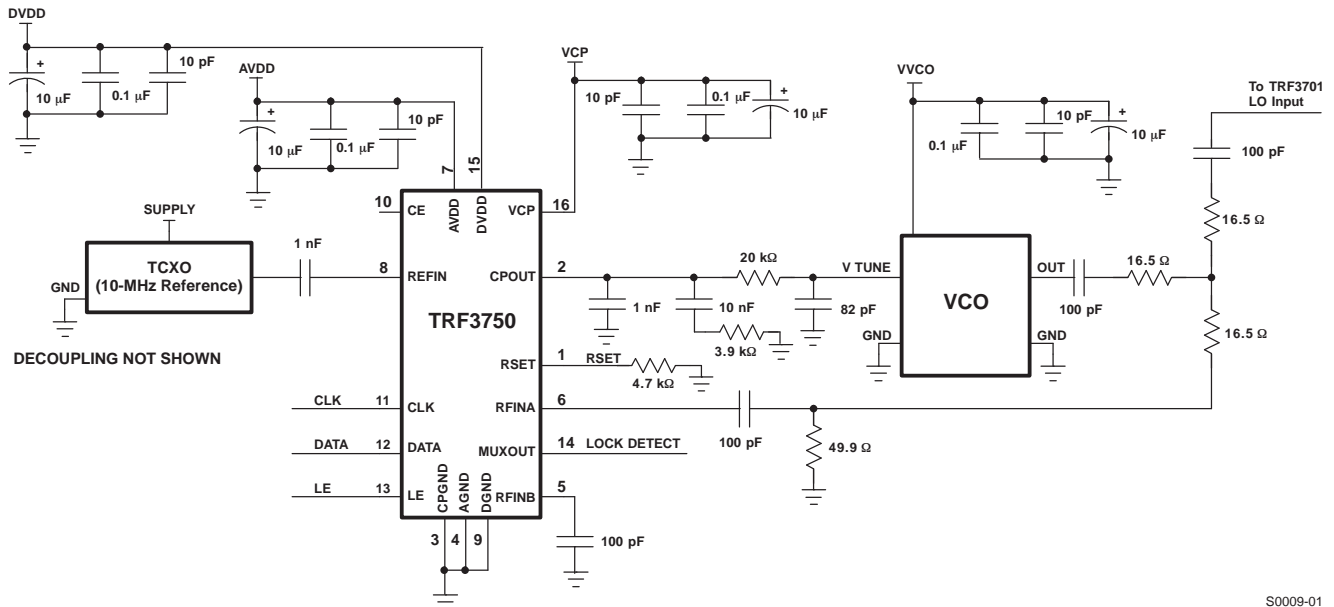
Figure 55. Using the THS4503 to Condition the Baseband Inputs to the TRF3701 (I Channel Shown)

DRIVING THE LOCAL OSCILLATOR INPUT

The LO pin is internally terminated to 50 Ω, thus enabling easy interface to the LO source without the need for external impedance matching. The power level of the LO signal should be in the range of -6 to 6 dBm. For characterization purposes, a power level of 0 dBm was chosen. An ideal way of driving the LO input of the TRF3701 is by using the TRF3750, an ultralow-phase-noise integer-N PLL from Texas Instruments. Combining

### APPLICATION INFORMATION (continued)

the TRF3750 with an external VCO can complete the loop and provide a flexible, convenient and cost-effective solution for the local oscillator of the transmitter. Figure 56 shows a typical application for the LO driver network that incorporates the TRF3750 integer-N PLL synthesizer into the design. Depending on the VCO output and the amount of signal loss, an optional gain stage may be added to the output of the VCO before it is applied to the TRF3701 LO input.



S0009-01

Figure 56. Typical Application Circuit for Generating the LO Signal for the TRF3701 Modulator

### PCB LAYOUT CONSIDERATIONS

The TRF3701 is a high-performance RF device; hence, care should be taken in the layout of the PCB in order to ensure optimum performance. Proper decoupling with low ESR capacitors is needed for the VCC supplies (pins 6 and 10). Typical values used are in the order of 1 pF in parallel to 0.1  $\mu$ F, with the lower-valued capacitors placed closer to the device pins. In addition, a larger tank capacitor in the order of 10  $\mu$ F should be placed on the supply line as layout permits. At least a 4-layer board is recommended for the PCB. If possible, a solid ground plane and a ground pour is also recommended, as is a power plane for the supplies. Because the balance of the four I, Q inputs to the modulator can be critical to device performance, care should be taken to ensure that the trace runs for all four inputs are equidistant. In the case of single-ended drive of the I, Q inputs, the two unused pins IREF and QREF are fed with the VCM dc voltage only, and should be decoupled with a 0.1- $\mu$ F capacitor (or smaller). The LO input trace should be minimized in length and have controlled impedance of 50  $\Omega$ . No external matching components are needed because there is an internal 50- $\Omega$  termination. The RFOUT pin should also have a relatively small trace to minimize parasitics and coupling, and should also be controlled to 50  $\Omega$ . An impedance-matching network can be used to optimize power transfer, but is not critical. All the results shown in the data sheet were taken with no impedance matching network used (RFOUT directly driving an external 50- $\Omega$  load).

The exposed thermal and ground pad on the bottom of the TRF3701 should be soldered to ground to ensure optimum electrical and thermal performance. The landing pattern on the PCB should include a solid pad and 4 thermal vias. These vias typically have 1,2-mm pitch and 0,3-mm diameter. The vias can be arranged in a 2x2 array. The thermal pad on the PCB should be at least 1.65x1.65 mm.

### IMPLEMENTING A DIRECT UPCONVERSION TRANSMITTER USING A TI CommsDAC

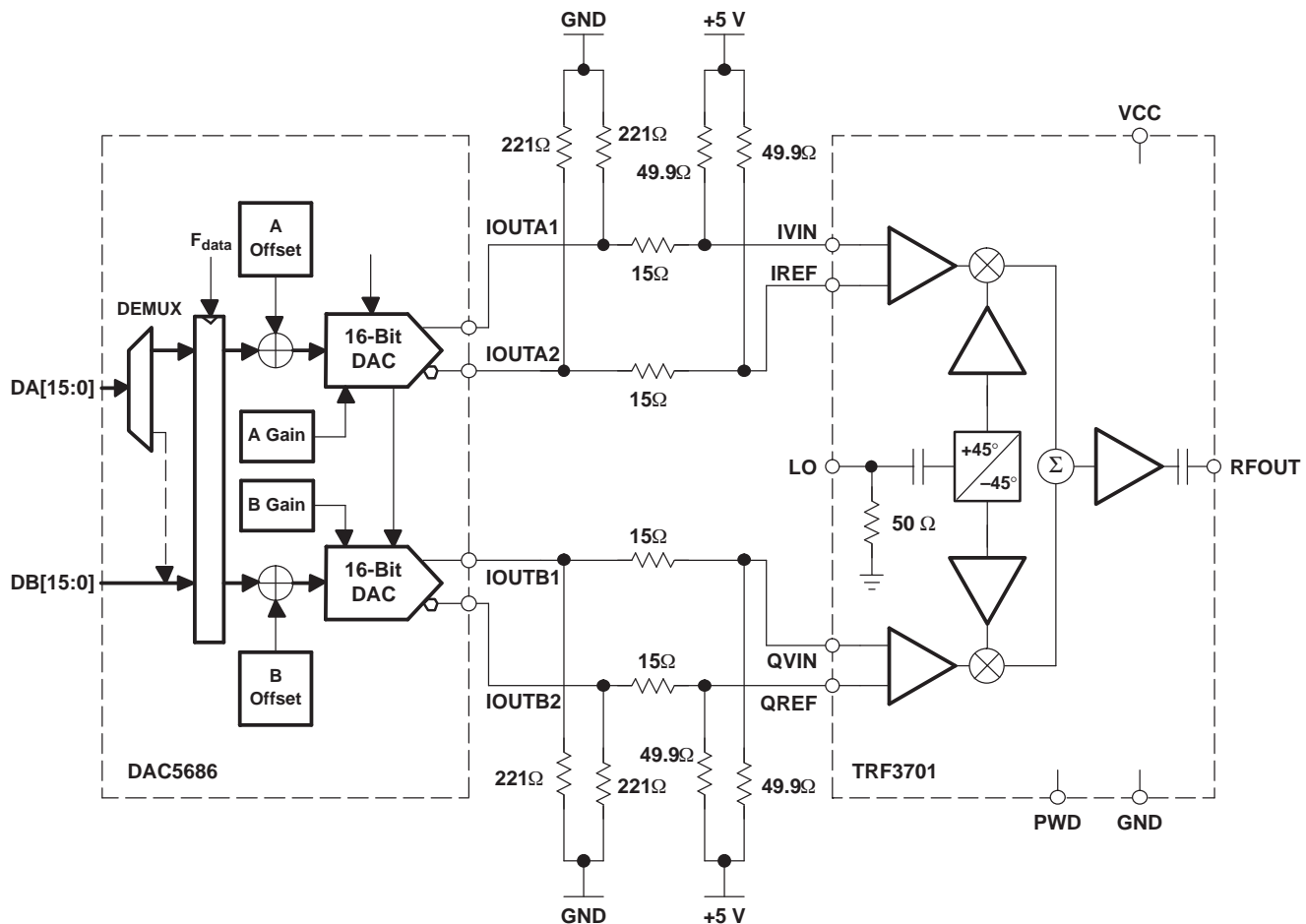
The TRF3701 is ideal for implementing a direct upconversion transmitter, where the input I, Q data can originate from an ASIC or a DAC. Texas Instruments' line of digital-to-analog converters (DAC) is ideally suited for interfacing to the TRF3701. Such DACs include, among others, the DAC290x series, DAC5672, and DAC5686.



APPLICATION INFORMATION (continued)

This section illustrates the use of the DAC5686, which offers a unique set of features that make interfacing to the TRF3701 easy and convenient. The DAC5686 is a 16-bit, 500 MSPS, 2x–16x interpolating dual-channel DAC, and it features I, Q adjustments for optimal interface to the TRF3701. User-selectable, 11-bit offset and 12-bit gain adjustments can optimize the carrier and sideband suppression of the modulator, resulting in enhanced performance and relaxed filtering requirements at RF. The preferred mode of operation of the DAC5686 for direct interface with the TRF3701 at baseband is the dual-DAC mode. The user also has the flexibility of selecting any one of the four possible complex spectral bands to be fed into the TRF3701. For details on the available modes and programming, see the DAC5686 data sheet available at www.ti.com.

Figure 57 shows the DAC5686 in dual-DAC mode, which is best-suited for zero-IF interface to the TRF3701. In this mode, a seamless, passive interface between the DAC output and the input to the modulator is used, so that no extra components are needed between the two devices. The optimum dc offset level for the inputs to the TRF3701 (VCM) is approximately 3.7 V. The output of the DAC should be centered around 3.3 V or less (depending on signal swing), in order to ensure that its output compliance limits are not exceeded. The resistive network shown in Figure 57 allows for this dc offset transition while still providing a dc path between the DAC output and the modulator. This ensures that the dc offset adjustments on the DAC5686 can still be applied to optimize the carrier suppression at the modulator output. The combination of the DAC5686 and the TRF3701 provides a unique signal-chain solution with state-of-the-art performance for wireless infrastructure applications.



S0010-01

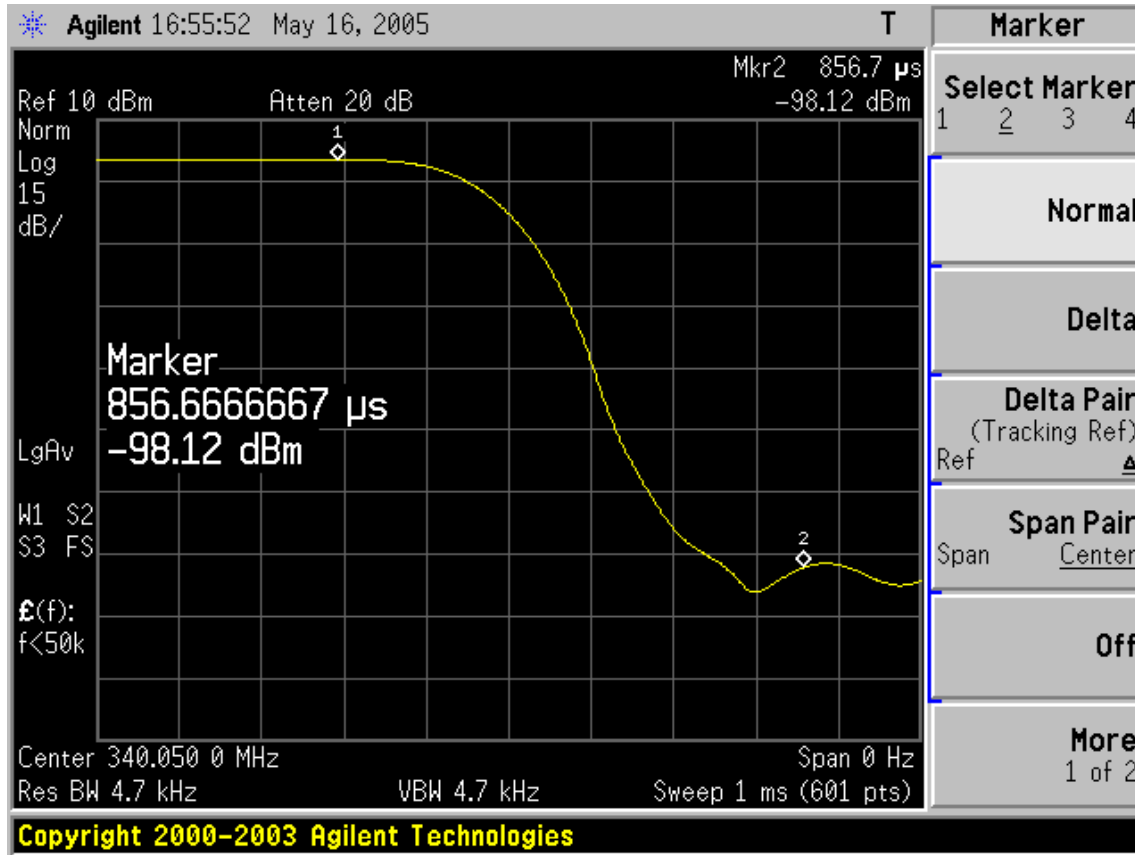
Figure 57. DAC5686 in Dual-DAC Mode with Quadrature Modulator

**APPLICATION INFORMATION (continued)**

**TRF3701 Power Down (PWD) Pin Operation**

The power down pin (PWD) in the TRF3701 powers down the chip when 0V is applied to this pin. The TRF3701 is enabled when 5V is applied to the PWD pin. Figure 58 shows the output power as a function of time when the PWD pin is pulled down from 5V to 0V. Both the I/Q signals and the LO are present during the power down. Figure 59 shows the output power as a function of time when the PWD pin is pulled up from 0V to 5V. In both the power down and power up operation there is a smooth transition with no glitches in output power.

The device will not turn on till a voltage greater than 1.2V is applied at the PWD pin. In addition the device does not turn off till the PWD is pulled below 3.7V. This ensures that the device does not accidentally change state due to glitches on the PWD pin. The turn on time of the device is 120 ns and the turn off time is 20 ns.



**Figure 58. Output power as a Function of Time During a Power-Down Operation (PWD Pin goes from 5V to 0V)**

**APPLICATION INFORMATION (continued)**

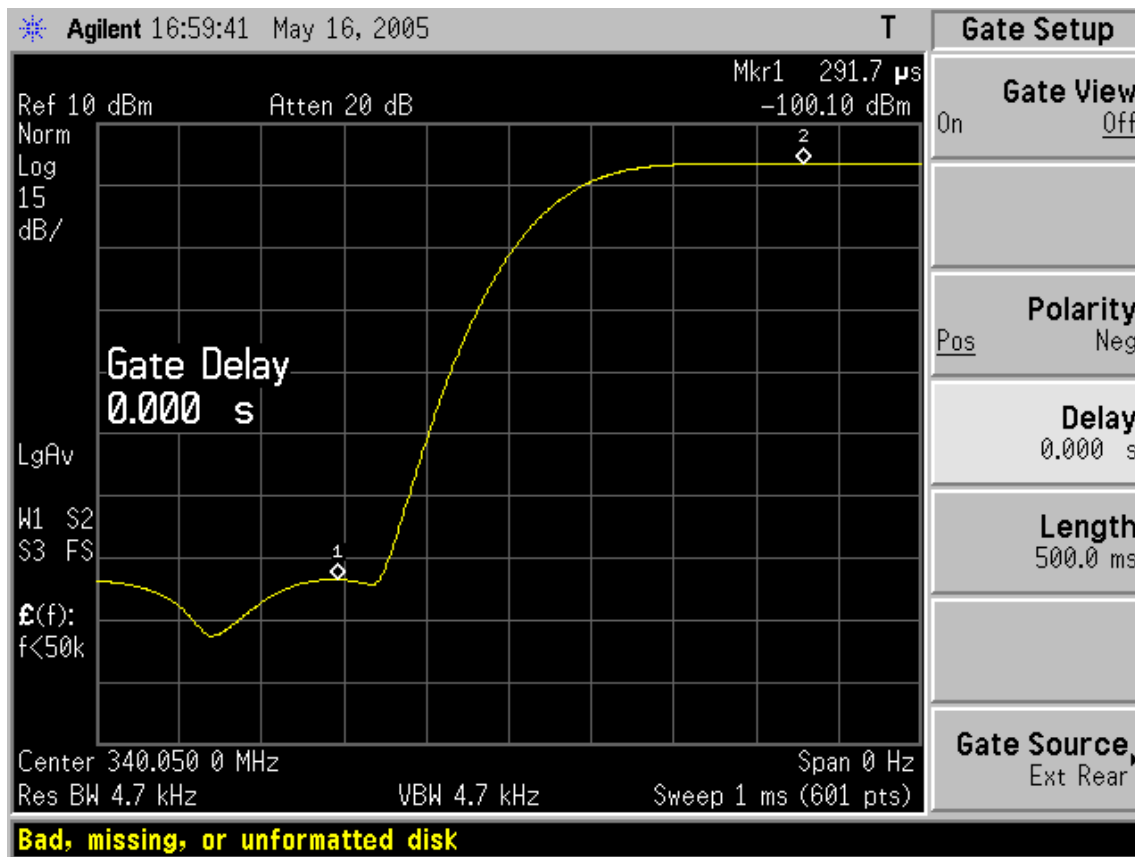


Figure 59. Output Power as a Function of Time During a Power-Up Operation (PWD Pin goes from 0V to 5V)

**Optimizing Carrier and Sideband Suppression**

For more information on optimizing carrier and sideband suppression, please See *Optimizing Carrier and Sideband Suppression (SLWA046)*.

### Revision History

| DATE      | REV                     | PAGE  | SECTION                          | DESCRIPTION  |
|-----------|-------------------------|---|----------------------------------|--|
| 29 JUL 05 | C                       | 1   |                                  | Changed data sheet title from "0.4 GHz" to "0.14 GHz"              |
|           |                         | 2   | ESD                              | Added ESD statement  |
|           |                         | 3   | Recommended Operating Conditions | Changed Input frequency from minimum 400 to minimum 140            |
|           |                         |   |                                  | Added PWD operation specifications                                 |
|           |                         | 4   | RF Output Performance            | Added 942.5 MHz to table title                                     |
|           |                         | 5   | RF Output Performance            | Added RF output performance table for 340 MHz and 140 MHz          |
|           |                         | 19  | Typical Characteristics          | Added Unadjusted Carrier Suppression vs Free-Air Temperature graph |
|           |                         | 20  | Typical Characteristics          | Added Sideband Suppression vs LO Frequency graph                   |
|           |                         | 26  | Application Information          | Added TRF3701 Power Down (PWD) Pin Operation section               |
| 27        | Application Information | Added Optimizing Carrier and Sideband Suppression section |                                  |  |
|           |                         | 28  | Thermal Information              | Added Thermal Information section                                  |
| 23 JUN 04 | B                       | –   | –                                | Changes unknown  |
| 26 MAR 04 | A                       | –   | –                                | Changes unknown  |
| 12 FEB 03 | *                       | –   | –                                | Original version   |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TRF3701IRHC      | ACTIVE        | VQFN         | RHC             | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | 3701<br>TRF             | <a href="#">Samples</a> |
| TRF3701IRHCR     | ACTIVE        | VQFN         | RHC             | 16   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | 3701<br>TRF             | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TRF3701IRHCR | VQFN         | RHC             | 16   | 3000 | 330.0              | 12.4               | 4.3     | 4.3     | 1.5     | 8.0     | 12.0   | Q1            |

TAPE AND REEL BOX DIMENSIONS

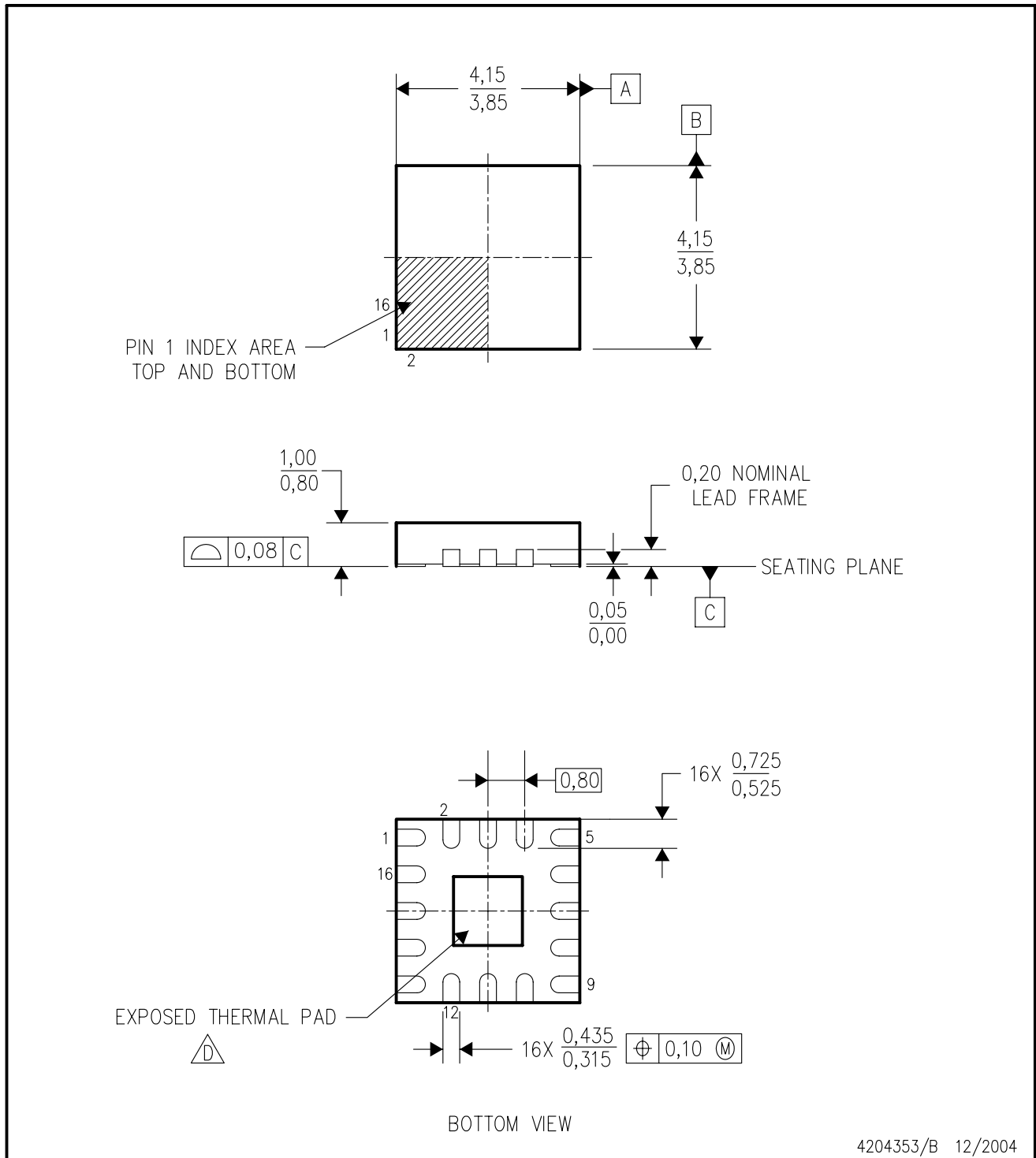


\*All dimensions are nominal


| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TRF3701IRHCR | VQFN         | RHC             | 16   | 3000 | 336.6       | 336.6      | 28.6        |



RHC (S-PQFP-N16) (CUSTOM PACKAGE) PLASTIC QUAD FLATPACK



4204353/B 12/2004

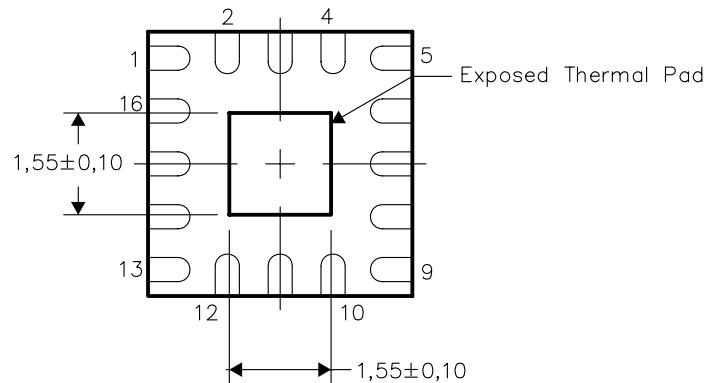
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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