TRS3232 3-V to 5.5-V Multichannel RS-232 Line Driver and Receiver With ±15-kV ESD Protection

1 Features

- RS-232 Bus-Terminal ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU V.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates up to 250 kbps
- Two Drivers and Two Receivers
- Low Supply Current: 300-µA Typical
- External Capacitors: 4 × 0.1 µF
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Terminal-Compatible Devices (1 Mbps)
  - SN65C3232 (–40°C to 85°C)
  - SN75C3232 (0°C to 70°C)

2 Applications

- Battery-Powered Systems
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

3 Description

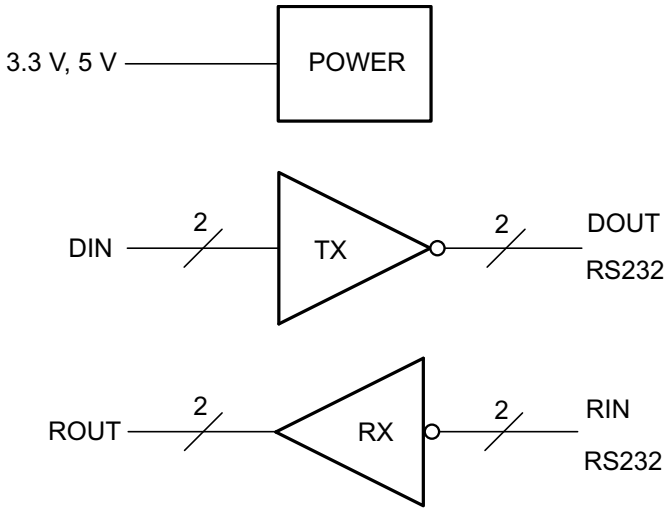
The TRS3232 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection terminal-to-terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from one 3-V to 5.5-V supply. The devices operate at data-signaling rates up to 250 kbps and a maximum of 30-V/µs driver-output slew rate.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TRS3232	SOIC (16)	9.90 mm × 3.91 mm
	SSOP (16)	6.20 mm × 5.30 mm
	SOIC-Wide (16)	10.30 mm × 7.50 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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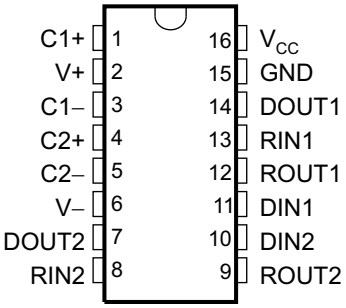
4 Revision History

Changes from Original (July 2007) to Revision A **Page**

- Changed *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics* section, *Detailed Description* section, *Power Supply Recommendations* and *Layout* sections, *Device and Documentation Support* and *Mechanical, Packaging, and Orderable Information* ... 1
- Deleted *Ordering Information* table. ... 3

5 Pin Configuration and Functions

D, DB, DW, PW Packages
16-Pin SOIC, SSOP, SOIC (Wide), TSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
C1–	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2–	5	—	Negative lead of C2 capacitor
DIN1	11	I	Logic data input (from UART)
DIN2	10	I	Logic data input (from UART)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
DOUT2	7	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
RIN1	13	I	RS232 line data input (from remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT1	12	O	Logic data output (to UART)
ROUT2	9	O	Logic data output (to UART)
V+	2	O	Positive charge pump output for storage capacitor only
V–	6	O	Negative charge pump output for storage capacitor only
V_{CC}	16	—	Supply Voltage, Connect to external 3-V to 5.5-V power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.3	6	V
V_+	Positive output supply voltage(2)		–0.3	7	V
V_-	Negative output supply voltage(2)		–7	0.3	V
$V_+ - V_-$	Supply voltage difference(2)			13	V
V_I	Input voltage	Drivers	–0.3	6	V
		Receivers	–25	25	
V_O	Output voltage	Drivers	–13.2	13.2	V
		Receivers	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 RIN , DOUT, and GND pins (1)	±15000	V
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 All other pins(1)	±3000	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(see Figure 6)(1)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver high-level input voltage	DIN	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver low-level input voltage	DIN				0.8	V
V_I	Driver input voltage	DIN		0		5.5	V
	Receiver input voltage	RIN		–25		25	
T_A	Operating free-air temperature		TRS3232C	0		70	°C
			TRS3232I	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.4 Thermal Information

THERMAL METRIC[1]		TRS3232				UNIT
		D (SOIC)	DB (SSOP)	DW (SOIC-wide)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	82	57	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics—Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1] (see Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
I_{CC}	Supply current	No load,	V_{CC} = 3.3 V to 5 V		0.3	1	mA

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.6 Electrical Characteristics—Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1] (see Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	D_{OUT} at R_L = 3 kΩ to GND,	D_{IN} = GND	5	5.4		V
V_{OL}	Low-level output voltage	D_{OUT} at R_L = 3 kΩ to GND,	D_{IN} = V_{CC}	–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}			±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	µA
I_{OS}[3]	Short-circuit output current	V_{CC} = 3.6 V	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V	V_O = 0 V				
r_O	Output resistance	V_{CC} = 0 V, V_+ = 0 V, and $V_–$ = 0 V	V_O = ±2 V	300	10M		Ω

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

6.7 Electrical Characteristics—Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1] (see Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.2		V
		V_{CC} = 5 V	0.8	1.5		
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			0.3		V
r_I	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.8 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
	Maximum data rate	R_L = 3 kΩ, One D_{OUT} switching,	C_L = 1000 pF See Figure 3	150	250		kbps
$t_{sk(p)}$	Driver Pulse skew(3)	R_L = 3 kΩ to 7 kΩ,	C_L = 150 to 2500 pF See Figure 4		300		ns
SR(tr)	Driver Slew rate, transition region (see Figure 3)	R_L = 3 kΩ to 7 kΩ, V_{CC} = 5 V	C_L = 150 to 1000 pF	6		30	V/µs
			C_L = 150 to 2500 pF	4		30	
t_{PLH}	Receiver Propagation delay time, low- to high-level output	C_L = 150 pF			300		ns
t_{PHL}	Receiver Propagation delay time, high- to low-level output				300		ns
$t_{sk(p)}$	Receiver Pulse skew(1)				300		ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6.9 Typical Characteristics

V_{CC} = 3.3 V

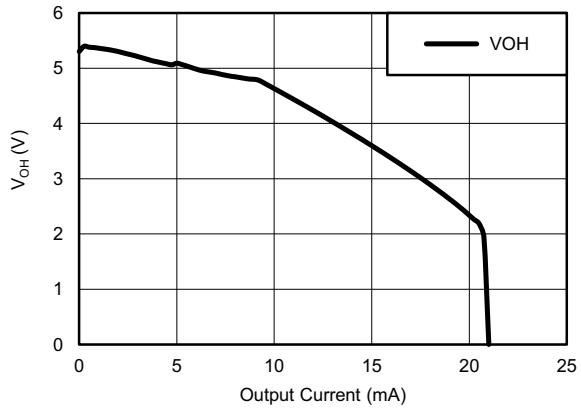


Figure 1. DOUT V_{OH} vs Load Current, Both Drivers Loaded

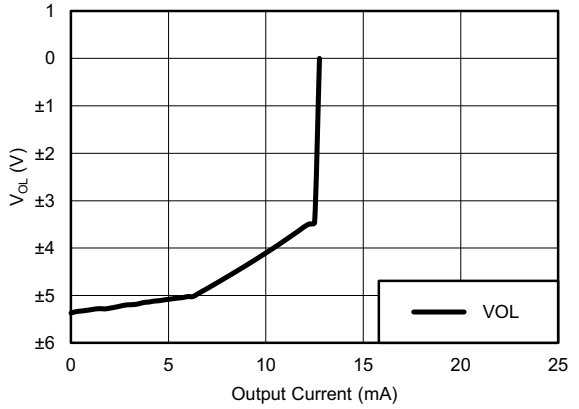
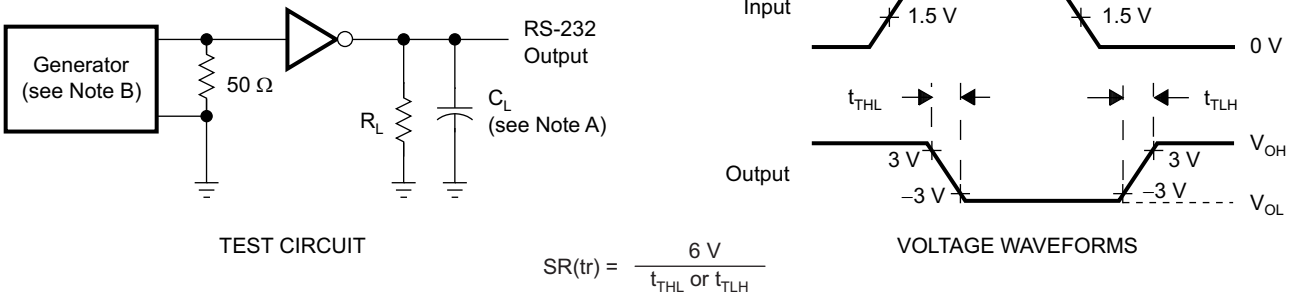


Figure 2. DOUT V_{OL} vs Load Current, Both Drivers Loaded

7 Parameter Measurement Information



TEST CIRCUIT

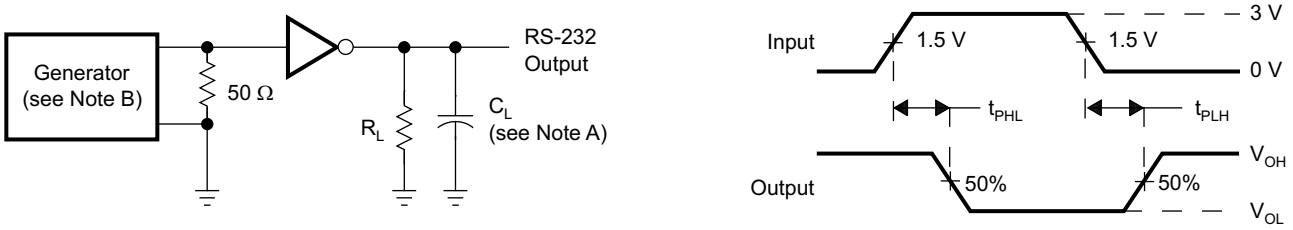
$$SR(tr) = \frac{6\ V}{t_{THL} \text{ or } t_{TLH}}$$

VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbps, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 3. Driver Slew Rate



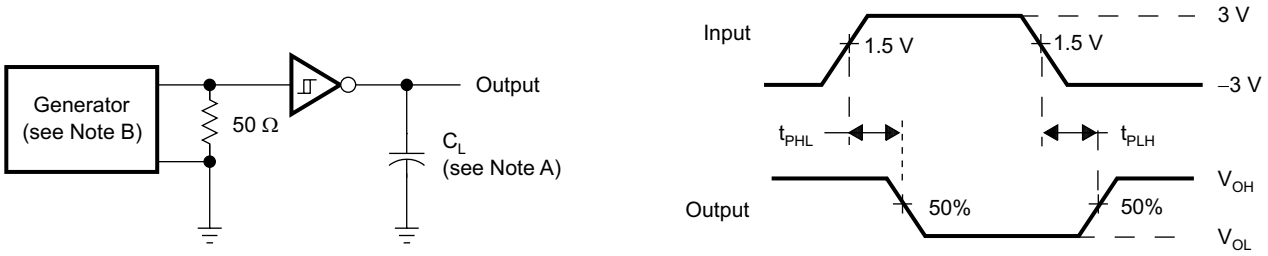
TEST CIRCUIT

VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbps, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 4. Driver Pulse Skew



TEST CIRCUIT

VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

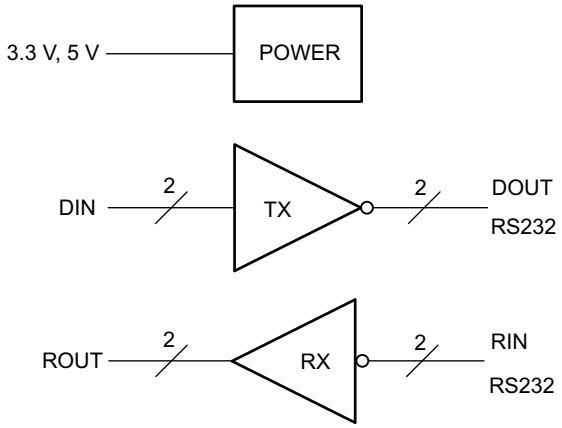
Figure 5. Receiver Propagation Delay Times

8 Detailed Description

8.1 Overview

The TRS3232 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection terminal to terminal (serial-port connection terminals, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from one 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbps and a maximum of 30-V/μs driver output slew rate. Outputs are protected against shorts to ground.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power

The power block increases, inverts, and regulates voltage at V_+ and V_- pins using a charge pump that requires four external capacitors.

8.3.2 RS232 Driver

Two drivers interface the standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

8.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input results in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

8.4 Device Functional Modes

Table 1. Each Driver(1)

INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

Table 2. Each Receiver(1)

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level, Open = input disconnected or connected driver off

8.4.1 V_{CC} Powered by 3 V to 5.5 V

The device is in normal operation.

8.4.2 V_{CC} Unpowered, V_{CC} = 0 V

When the TRS3232 device is unpowered, it can be safely connected to an active remote RS232 device.

9 Application and Implementation

NOTE

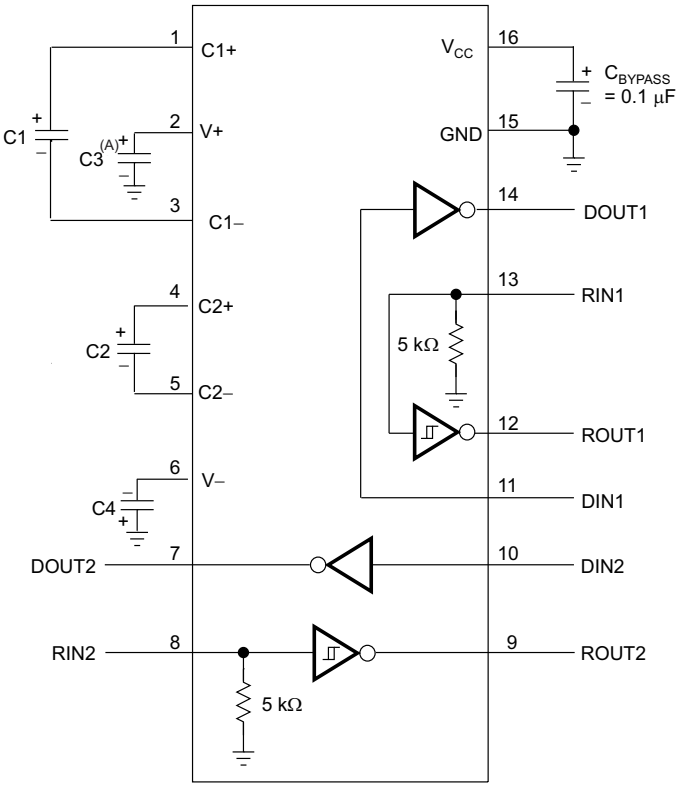
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TRS3232 device is designed to convert single-ended signals into RS232-compatible signals, and vice-versa.

This device can be used in any application where an RS232 line driver or receiver is required. One benefit of this device is its ESD protection, which helps protect other components on the board when the RS232 lines are tied to a physical connector.

9.2 Typical Application



A. C3 can be connected to V_{CC} or GND.

B. Resistor values shown are nominal.

C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.

D. See Table 3 for capacitor values.

Figure 6. Typical Operating Circuit

Typical Application (continued)

9.2.1 Design Requirements

- Recommended V_{CC} is 3.3 V or 5 V
  - 3 V to 5.5 V is also possible
- Maximum recommended bit rate is 250 kbps

Table 3. V_{CC} versus Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

9.2.2 Detailed Design Procedure

For proper operation, add capacitors as shown in Figure 6 and Table 3.

All DIN inputs must be connected to valid low or high logic levels.

Select capacitor values based on V_{CC} level for best performance.

9.2.3 Application Curve

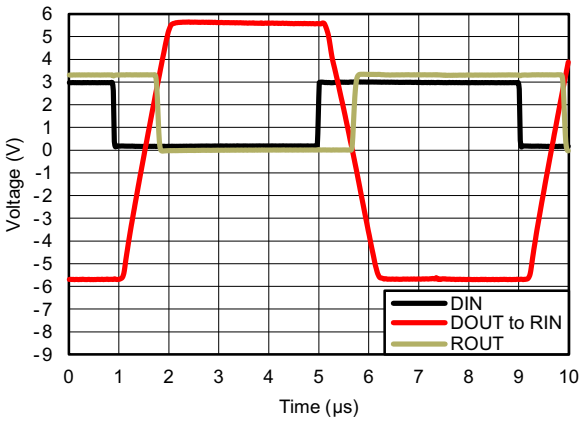


Figure 7. 250 kbps Driver to Receiver Loopback Timing Waveform, V_{CC}= 3.3 V

10 Power Supply Recommendations

V_{CC} must be between 3 V and 5.5 V. Charge pump capacitors must be chosen using Table 3.

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

11.2 Layout Example

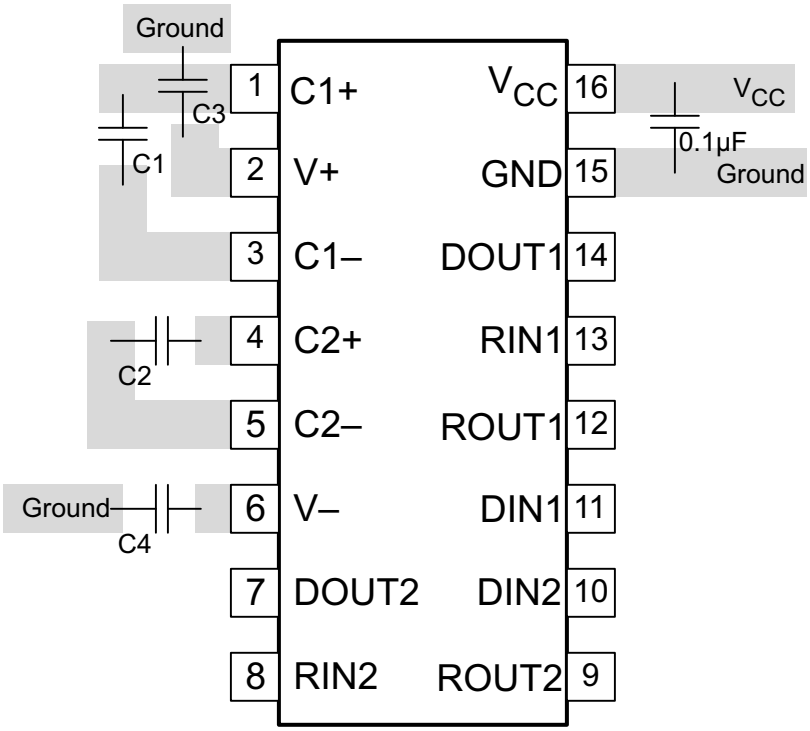


Figure 8. Layout Diagram

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3232CDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS32C	Samples
TRS3232CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232C	Samples
TRS3232CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3232C	Samples
TRS3232CPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS32C	Samples
TRS3232CPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS32C	Samples
TRS3232IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3232I	Samples
TRS3232IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32I	Samples
TRS3232IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS32I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

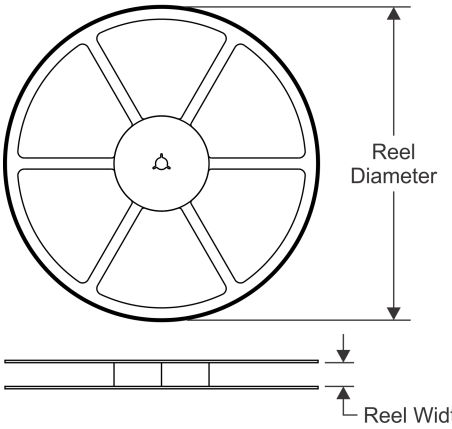
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

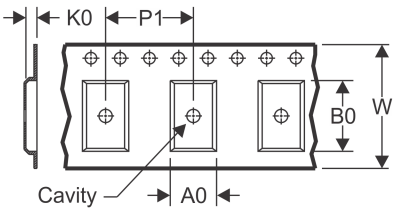
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

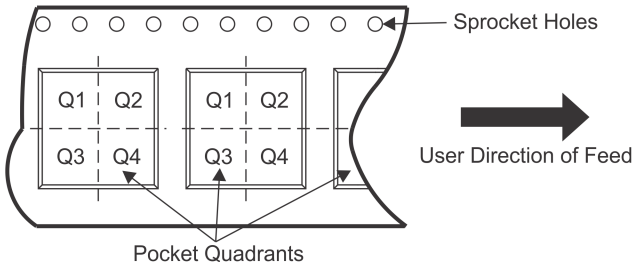


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

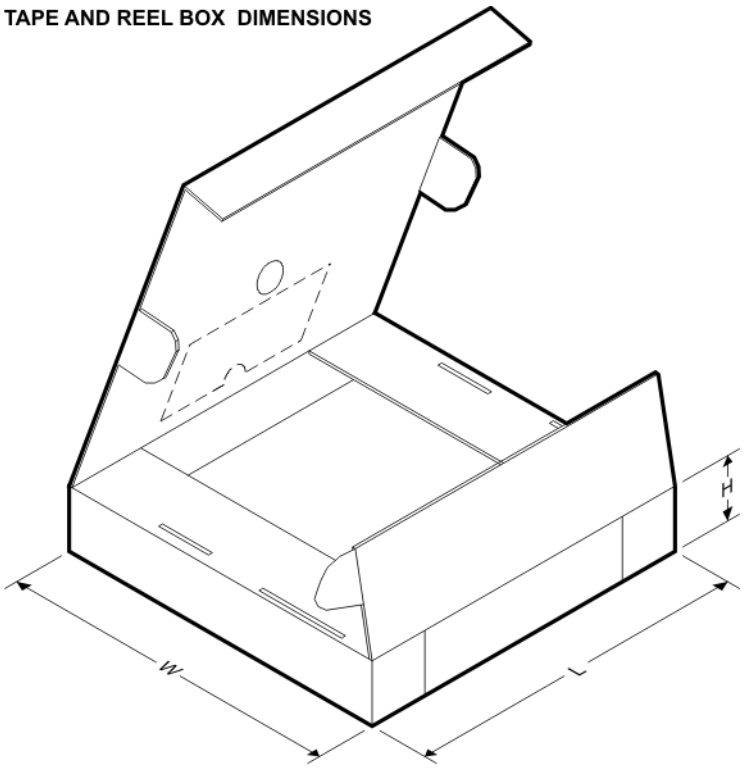
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3232CDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TRS3232CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS3232IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

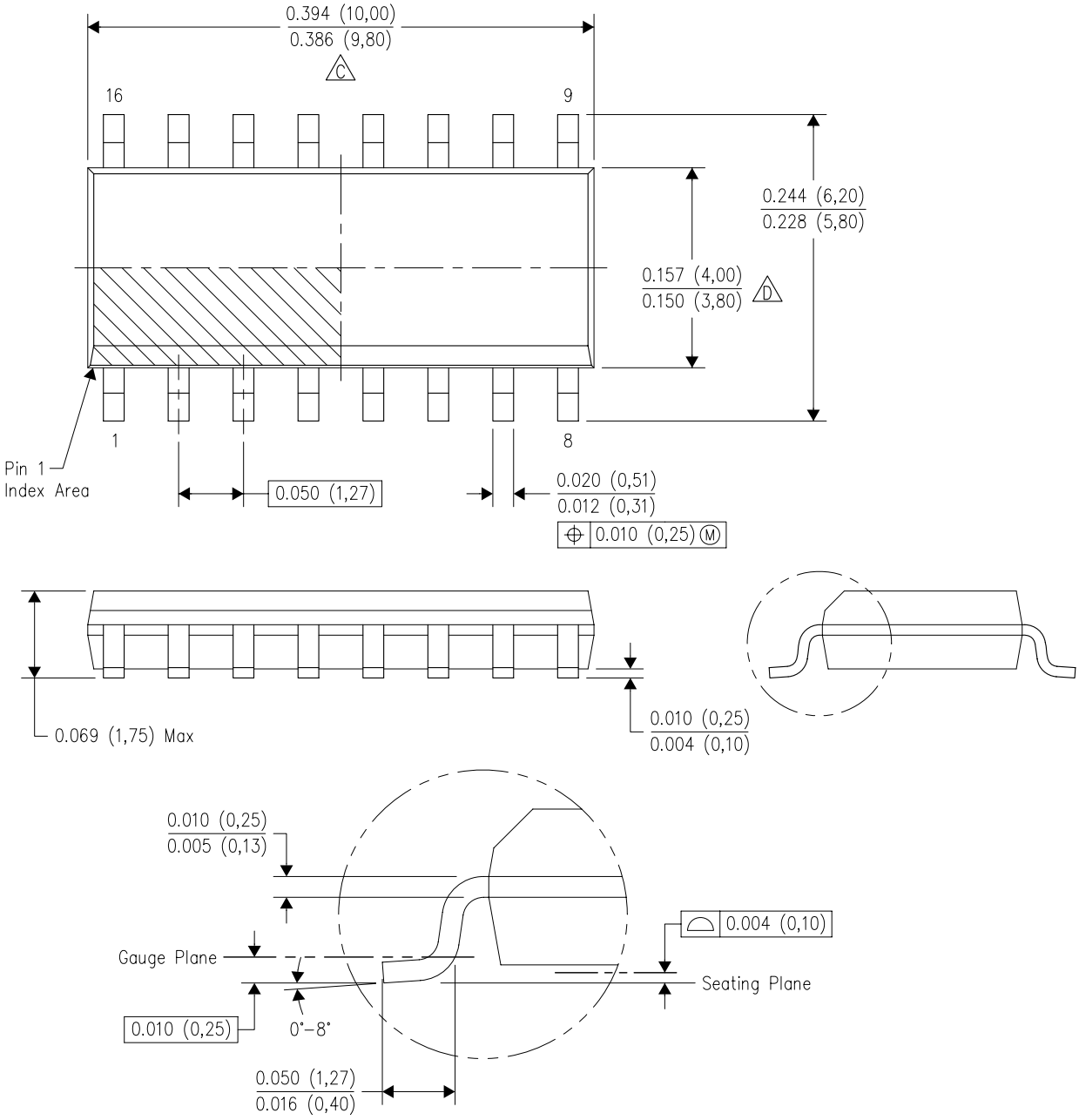
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

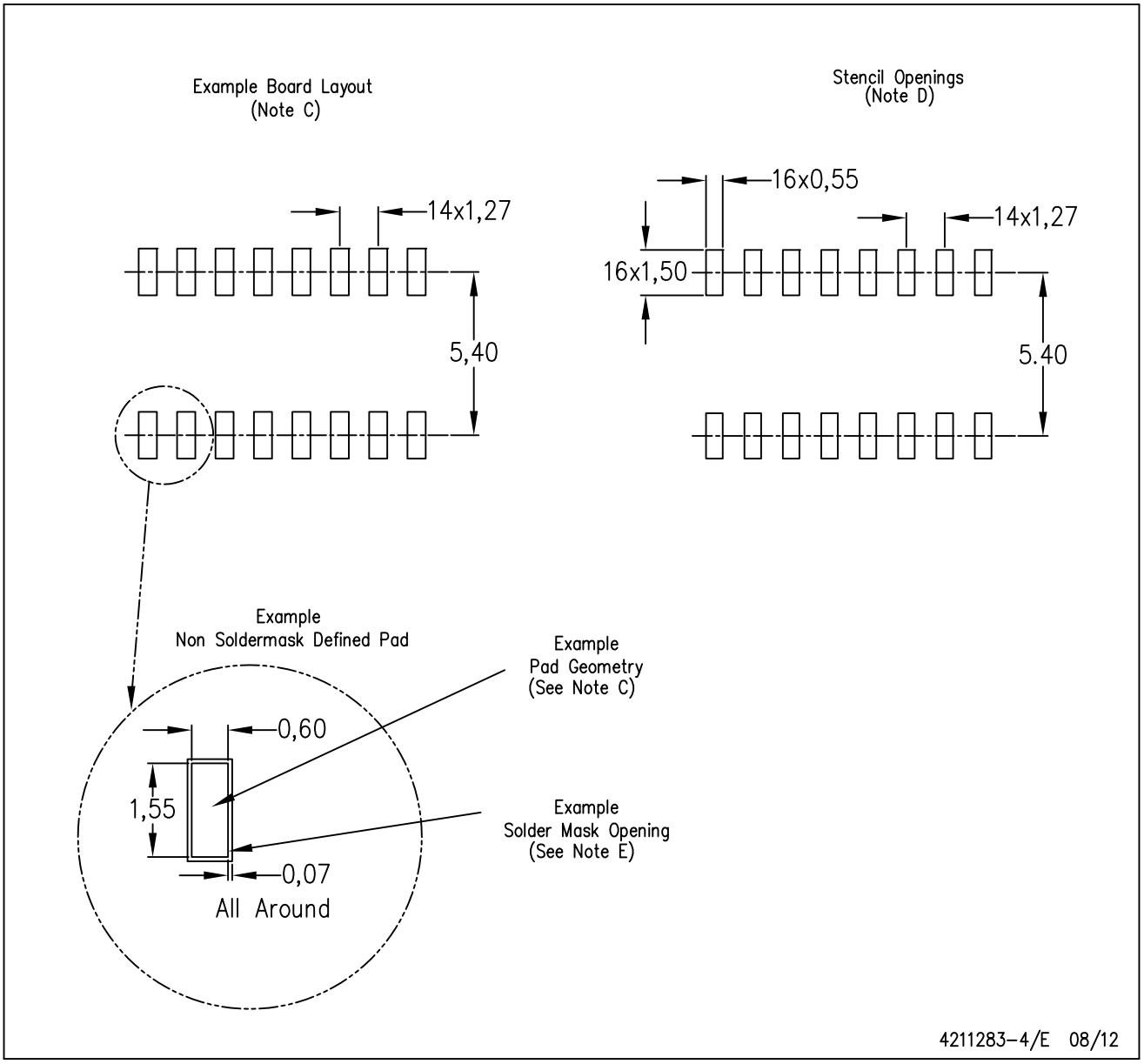
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3232CDBR	SSOP	DB	16	2000	367.0	367.0	38.0
TRS3232CDR	SOIC	D	16	2500	333.2	345.9	28.6
TRS3232CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
TRS3232IDR	SOIC	D	16	2500	333.2	345.9	28.6
TRS3232IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



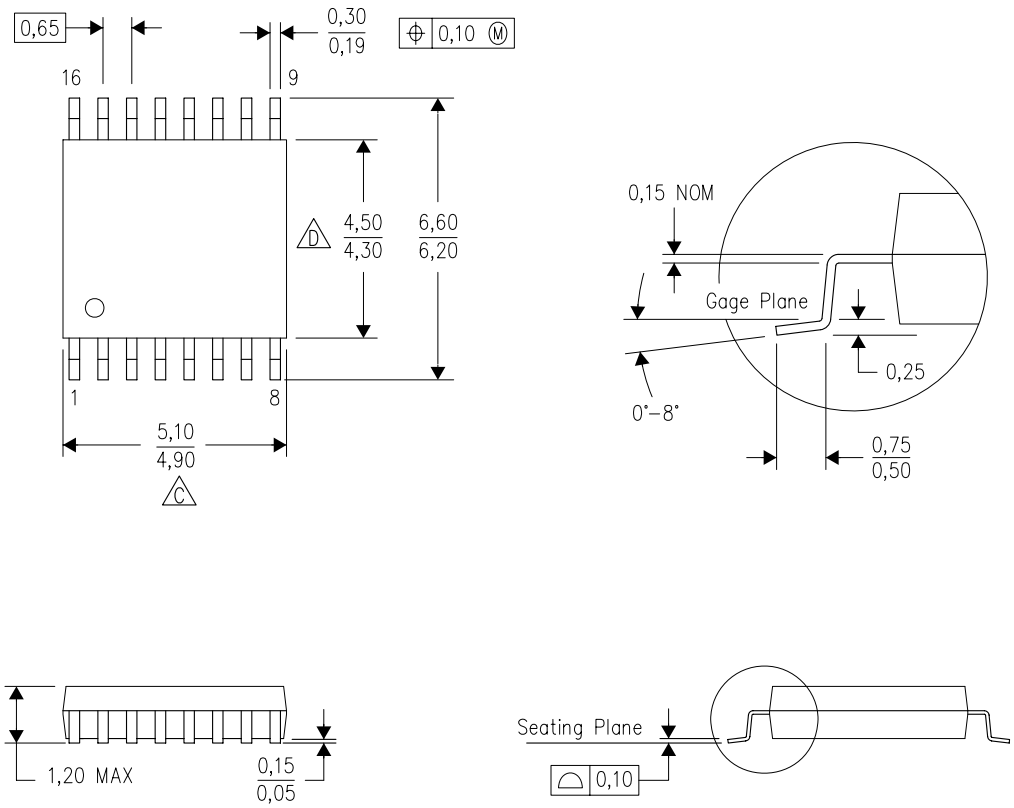
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

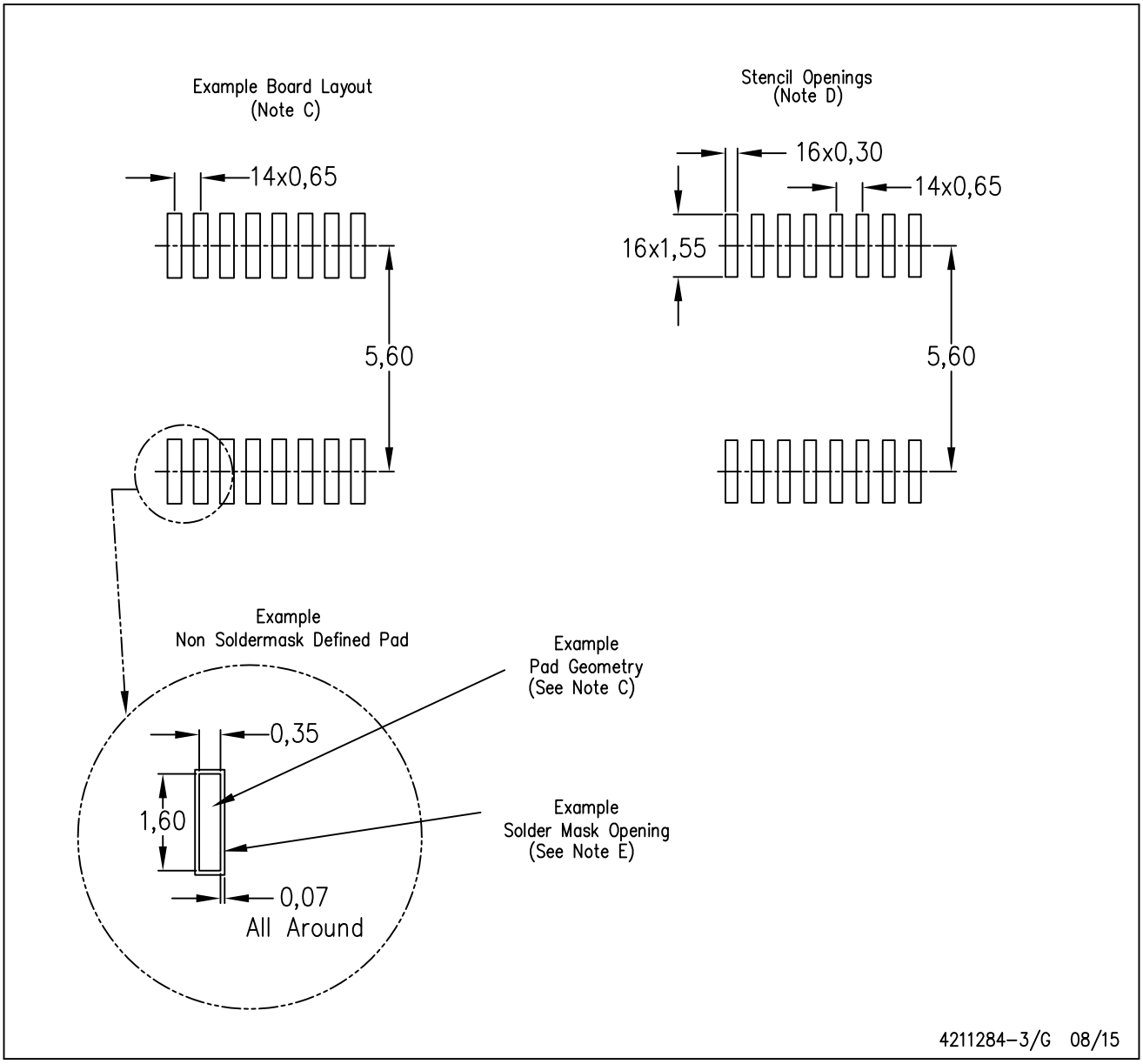
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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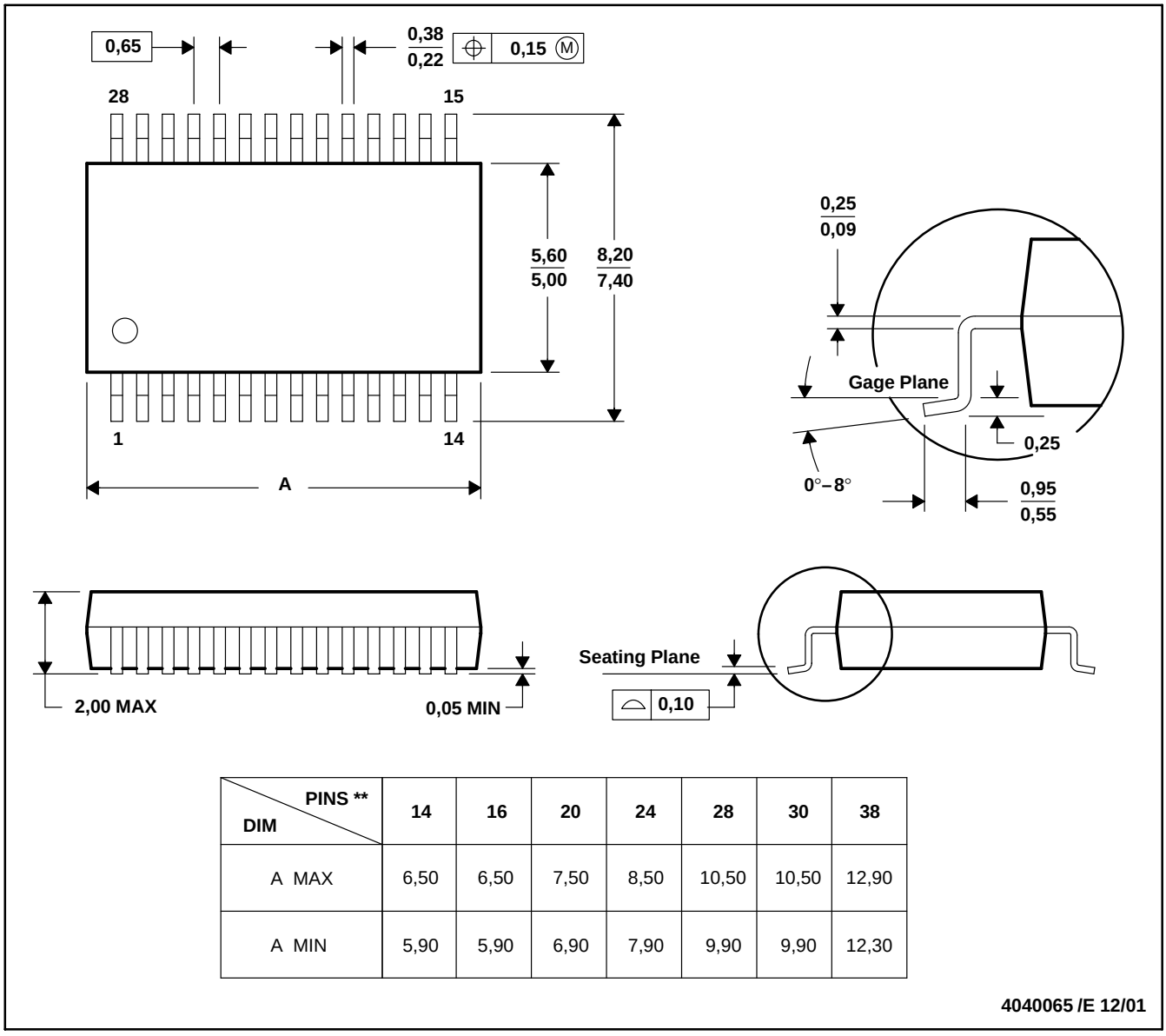
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

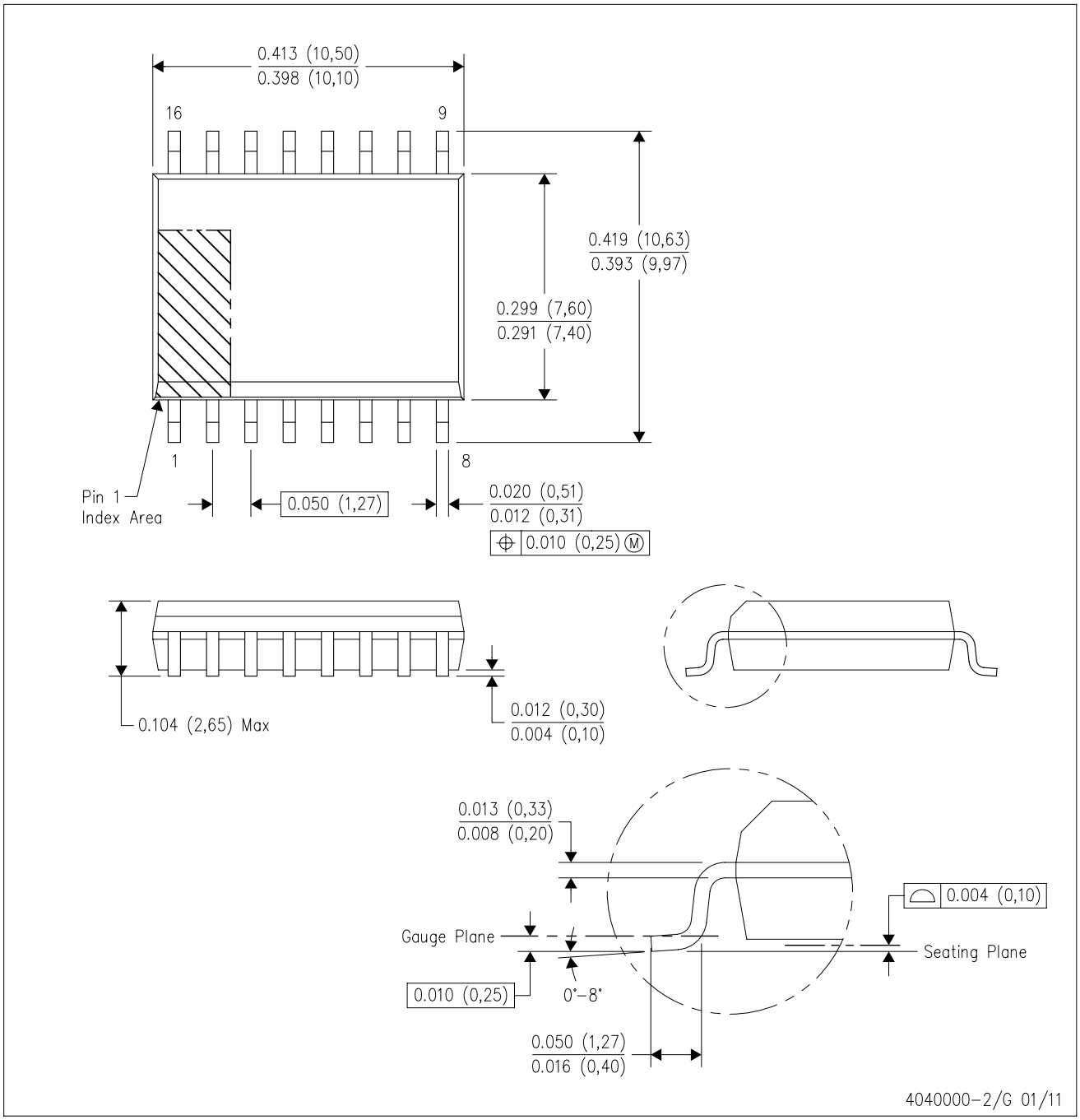


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

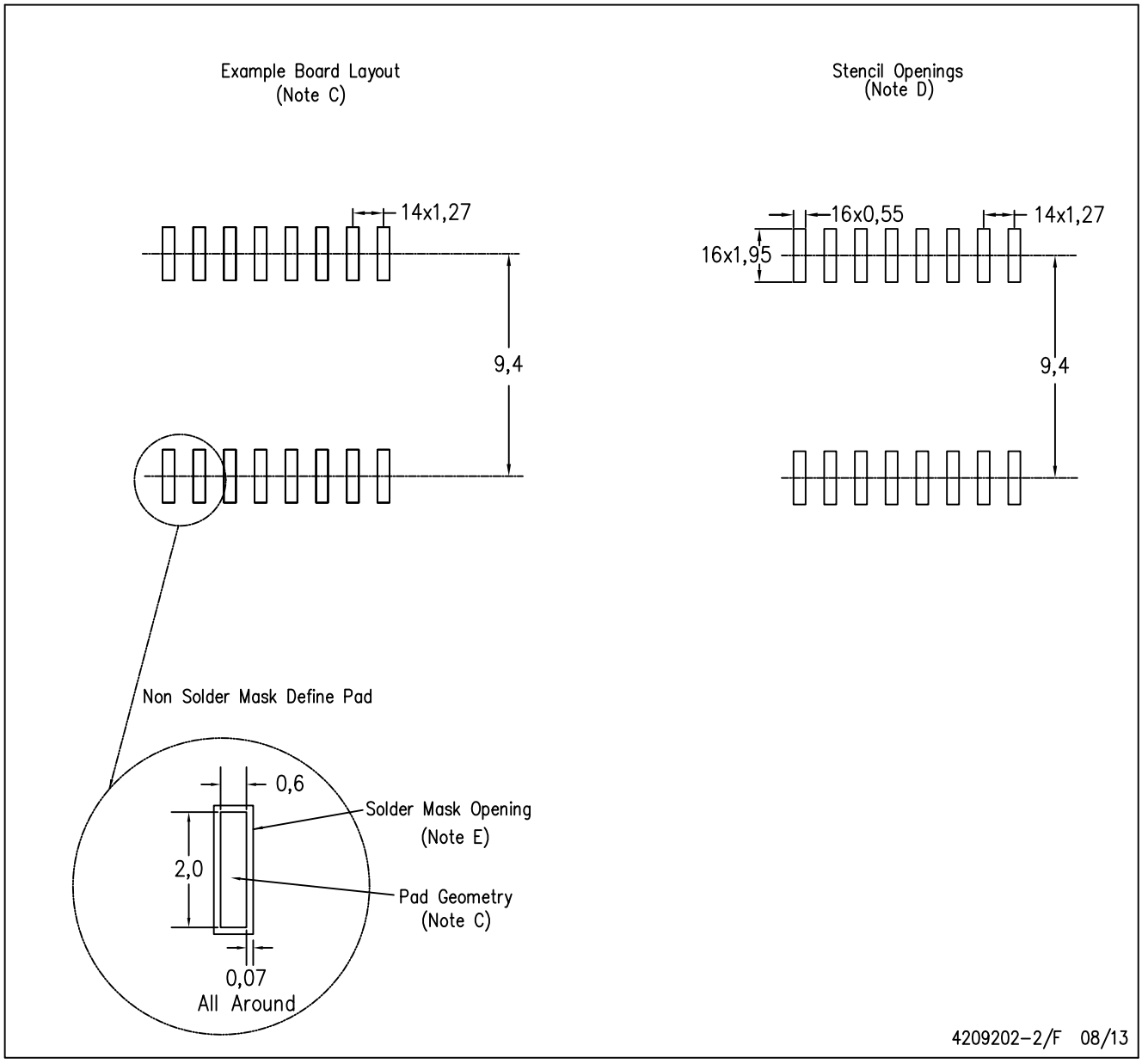
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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