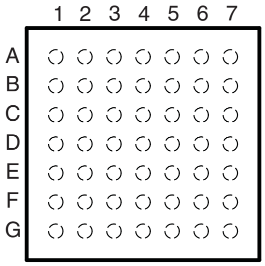
SDIO, UART, AND AUDIO VOLTAGE-TRANSLATION TRANSCEIVER

Check for Samples: TWL1200

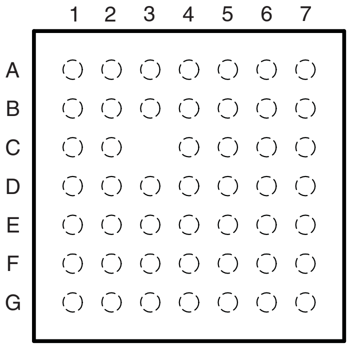
FEATURES

- **Level Translator**
  - **V_{CCA} and V_{CCB} Range of 1.1 V to 3.6 V**
- **Seamlessly Bridges 1.8-V/2.6-V Digital-Switching Compatibility Gap Between 2.6-V processors and TI's Wi-Link (WL1271 and WL1273)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2500-V Human-Body Model (A114-B)**
  - **250-V Machine Model (A115-A)**
  - **1500-V Charged-Device Model (C101)**

YFF PACKAGE
(TOP VIEW)



ZQC PACKAGE
(TOP VIEW)



BGA PACKAGE TERMINAL ASSIGNMENTS

	1	2	3	4	5	6	7
A	SDIO_CLK(A)	SDIO_CMD(A)	AUDIO_CLK(A)	AUD_DIR	AUDIO_CLK(B)	SDIO_CMD(B)	SDIO_CLK(B)
B	SDIO_DATA3(A)	SDIO_DATA0(A)	AUDIO_F-SYN(A)	$\overline{OE}$	AUDIO_F-SYN(B)	SDIO_DATA0(B)	SDIO_DATA3(B)
C	SDIO_DATA2(A)	SDIO_DATA1(A)		V_{CCA}	V_{CCB}	SDIO_DATA1(B)	SDIO_DATA2(B)
D	WLAN_EN(A)	WLAN_IRQ(A)	GND	V_{CCA}	V_{CCB}	WLAN_EN(B)	WLAN_IRQ(B)
E	CLK_REQ(A)	BT_EN(A)	GND	GND	GND	BT_EN(B)	CLK_REQ(B)
F	BT_UART_CTS(A)	BT_UART_RTS(A)	AUDIO_IN(A)	SLOW_CLK(B)	AUDIO_IN(B)	BT_UART_RTS(B)	BT_UART_CTS(B)
G	BT_UART_RX(A)	BT_UART_TX(A)	AUDIO_OUT(A)	SLOW_CLK(A)	AUDIO_OUT(B)	BT_UART_TX(B)	BT_UART_RX(B)

WCS PACKAGE TERMINAL ASSIGNMENTS

	1	2	3	4	5	6	7
A	SDIO_CLK(A)	SDIO_CMD(A)	AUDIO_CLK(A)	AUD_DIR	AUDIO_CLK(B)	SDIO_CMD(B)	SDIO_CLK(B)
B	SDIO_DATA3(A)	SDIO_DATA0(A)	AUDIO_F-SYN(A)	$\overline{OE}$	AUDIO_F-SYN(B)	SDIO_DATA0(B)	SDIO_DATA3(B)
C	SDIO_DATA2(A)	SDIO_DATA1(A)	NC(1)	V_{CCA}	V_{CCB}	SDIO_DATA1(B)	SDIO_DATA2(B)
D	WLAN_EN(A)	WLAN_IRQ(A)	GND	V_{CCA}	V_{CCB}	WLAN_EN(B)	WLAN_IRQ(B)
E	CLK_REQ(A)	BT_EN(A)	GND	GND	GND	BT_EN(B)	CLK_REQ(B)
F	BT_UART_CTS(A)	BT_UART_RTS(A)	AUDIO_IN(A)	SLOW_CLK(B)	AUDIO_IN(B)	BT_UART_RTS(B)	BT_UART_CTS(B)
G	BT_UART_RX(A)	BT_UART_TX(A)	AUDIO_OUT(A)	SLOW_CLK(A)	AUDIO_OUT(B)	BT_UART_TX(B)	BT_UART_RX(B)

(1) NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The TWL1200 is an 19-bit voltage translator specifically designed to seamlessly bridge the 1.8-V/2.6-V digital-switching compatibility gap between 2.6-V baseband and the TI Wi-Link-6 (WL1271/3). It is optimized for SDIO, UART, and audio functions. The TWL1200 has two supply-voltage pins, V_{CCA} and V_{CCB}, that can be operated over the full range of 1.1 V to 3.6 V. The TWL1200 enables system designers to easily interface applications processors or digital basebands to peripherals operating at a different I/O voltage levels, such as the TI Wi-Link-6 (WL1271/3) or other SDIO/memory cards.

The TWL1200 is offered in both 48-ball 0.5-mm ball grid array (BGA) and 49-bump 0.4-mm wafer chip scale package (WCSP) packages. Low static power consumption and small package size make the TWL1200 an ideal choice for mobile-phone applications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	BGA MicroStar Junior™ – ZQC (Pb-free)	Tape and reel	TWL1200ZQCR	YW200
	WCSP ™ – YFF (Pb-free)	Tape and reel	TWL1200YFFR	YW200

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

TERMINAL FUNCTIONS

TERMINAL			TYPE	DESCRIPTION
ZQC BALL NO.	YFF BUMP NO.	NAME		
C4, D4	C4, D4	V_{CCA}	Power	A-side supply voltage (1.1 V to 3.6 V)
B2	B2	SDIO_DATA0(A)	I/O	Data bit 1 connected to baseband SDIO controller
C2	C2	SDIO_DATA1(A)	I/O	Data bit 2 connected to baseband SDIO controller
C1	C1	SDIO_DATA2(A)	I/O	Data bit 3 connected to baseband SDIO controller
B1	B1	SDIO_DATA3(A)	I/O	Data bit 4 connected to baseband SDIO controller
A2	A2	SDIO_CMD(A)	I/O	Command bit connected to baseband SDIO controller. Referenced to V_{CCA}.
A6	A6	SDIO_CMD(B)	I/O	Command bit connected to SD/SDIO peripheral. Includes a 15-kΩ pullup resistor to V_{CCB}.
D3, E3, E4, E5	D3, E3, E4, E5	GND		Ground
B6	B6	SDIO_DATA0(B)	I/O	Data bit 1 connected to SD/SDIO peripheral
C6	C6	SDIO_DATA1(B)	I/O	Data bit 2 connected to SD/SDIO peripheral
C7	C7	SDIO_DATA2(B)	I/O	Data bit 3 connected to SD/SDIO peripheral
B7	B7	SDIO_DATA3(B)	I/O	Data bit 4 connected to SD/SDIO peripheral
A1	A1	SDIO_CLK(A)	I	Clock signal connected to baseband SDIO controller. Referenced to V_{CCA}.
A7	A7	SDIO_CLK(B)	O	Clock signal connected to SD/SDIO peripheral. Referenced to V_{CCB}; drive strength = 8 mA
C5, D5	C5, D5	V_{CCB}	Pwr	B-side supply voltage (1.1 V to 3.6 V)
C3	C3	–	–	No ball (for ZQC) and No-Connect (for YFF)
B4	B4	$\overline{OE}$	I	Output enable (active low)
A4	A4	AUD_DIR	I	Direction control signal for AUDIO_CLK and AUDIO_F-SYNC signals
G3	G3	AUDIO_OUT(A)	O	Connected to baseband audio subsystem; drive strength = 4 mA
G5	G5	AUDIO_OUT(B)	I	Connected to Wi-Link-6 PCM subsystem
D1	D1	WLAN_EN(A)	I	Connected to baseband SDIO controller
D6	D6	WLAN_EN(B)	O	Connected to SD/SDIO peripheral; drive strength = 2 mA
G2	G2	BT_UART_TX(A)	O	Connected to baseband UART subsystem; drive strength = 8 mA
G6	G6	BT_UART_TX(B)	I	Connected to BT UART subsystem of Wi-Link-6
D2	D2	WLAN_IRQ(A)	O	Connected to baseband SDIO controller; drive strength = 4 mA

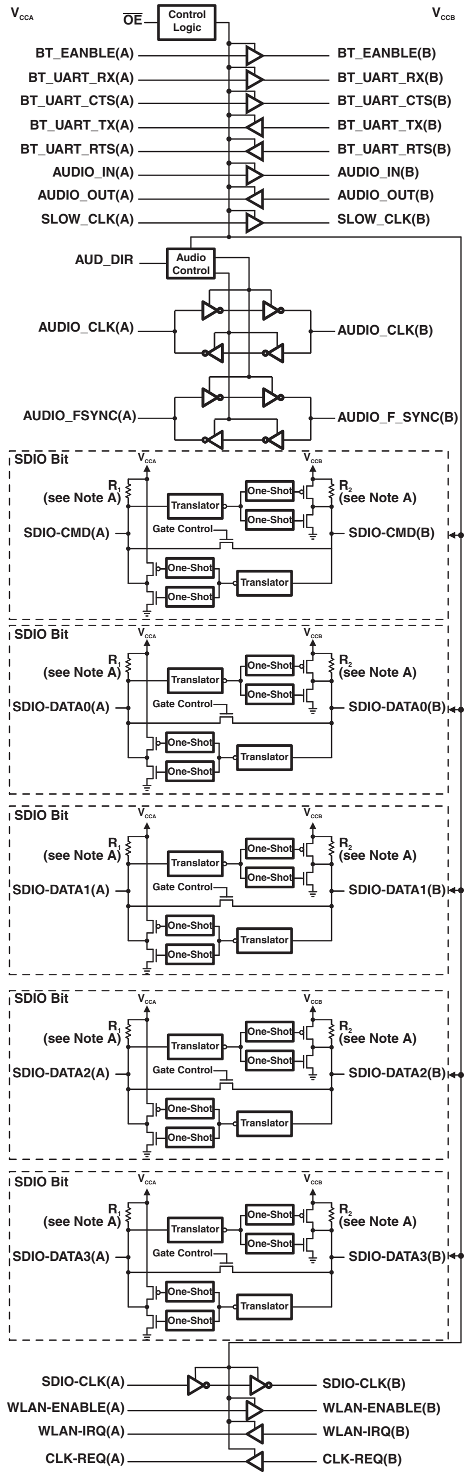
TERMINAL FUNCTIONS (continued)

TERMINAL			TYPE	DESCRIPTION
ZQC BALL NO.	YFF BUMP NO.	NAME		
D7	D7	WLAN_IRQ(B)	I	Connected to SD/SDIO peripheral
G4	G4	SLOW_CLK(A)	I	Low frequency 32-kHz clock connected to baseband device
F4	F4	SLOW_CLK(B)	O	Low frequency 32-kHz clock connected to Wi-Link-6 device; drive strength = 2 mA
G1	G1	BT_UART_RX(A)	I	Connected to baseband UART subsystem
G7	G7	BT_UART_RX(B)	O	Connected to BT UART subsystem of Wi-Link-6; drive strength = 8 mA
E1	E1	CLK_REQ(A)	O	Connected to baseband SDIO controller; drive strength = 4 mA
E7	E7	CLK_REQ(B)	I	Connected to SD/SDIO peripheral
F1	F1	BT_UART_CTS(A)	I	Connected to baseband UART subsystem
F3	F3	AUDIO_IN(A)	I	Connected to baseband audio subsystem
F5	F5	AUDIO_IN(B)	O	Connected to Wi-Link-6 PCM subsystem; drive strength = 4 mA
A3	A3	AUDIO_CLK(A)	I/O	Connected to baseband audio subsystem; drive strength = 4 mA
A5	A5	AUDIO_CLK(B)	I/O	Connected to Wi-Link-6 PCM subsystem; drive strength = 4 mA
E2	E2	BT_EN(A)	I	Connected to baseband UART subsystem
E6	E6	BT_EN(B)	O	Connected to BT UART subsystem of Wi-Link-6; drive strength = 2 mA
F7	F7	BT_UART CTS(B)	O	Connected to BT UART subsystem of Wi-Link-6; drive strength = 4 mA
F2	F2	BT_UART RTS(A)	O	Connected to baseband UART subsystem; drive strength = 4 mA
F6	F6	BT_UART RTS(B)	I	Connected to BT UART subsystem of Wi-Link-6
B3	B3	AUDIO_F-SYN(A)	I/O	Connected to baseband audio subsystem; drive strength = 4 mA
B5	B5	AUDIO_F-SYN(B)	I/O	Connected to Wi-Link-6 PCM subsystem; drive strength = 4 mA

Table 1. FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{\text{OE}}$	AUD_DIR	
H	X	All outputs are Hi-Z
L	H	AUDIO_CLK(A) to AUDIO_CLK(B) and AUDIO_F-SYNC(A) to AUDIO_F-SYNC(B)
L	L	AUDIO_CLK(B) to AUDIO_CLK(A) and AUDIO_F-SYNC(B) to AUDIO_F-SYNC(A)

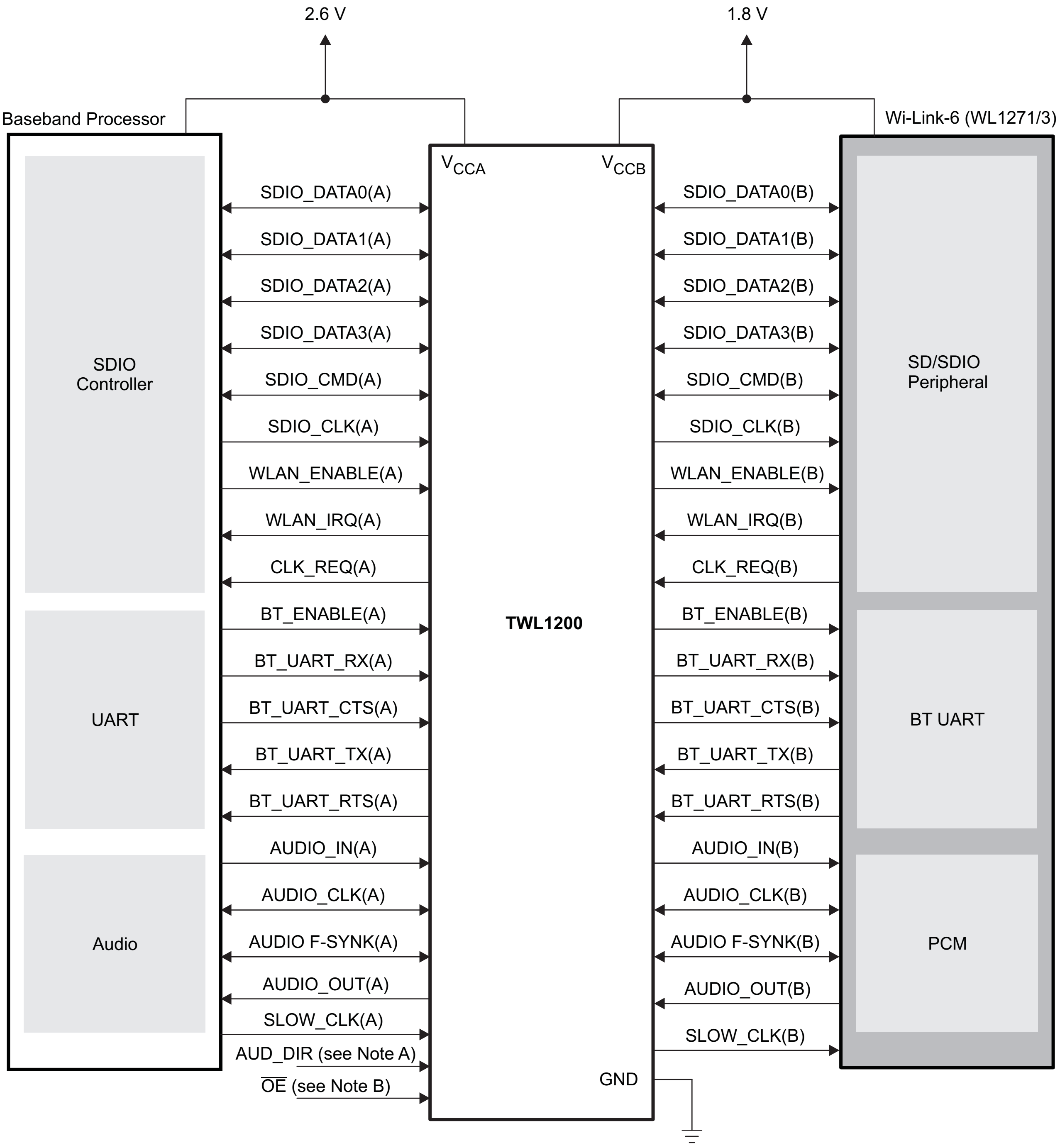
LOGIC DIAGRAM



A. R_1 and R_2 resistor values are determined based upon the logic level applied to the A port or B port as follows:
R_1 and R_2 = 25 kΩ when a logic level low is applied to the A port or B port.
R_1 and R_2 = 4 kΩ when a logic level high is applied to the A port or B port.
R_1 and R_2 = 70 kΩ when the port is deselected (or in High-Z or 3-state).

B. $\overline{\text{OE}}$ controls all output buffers. When $\overline{\text{OE}}$ = high, all outputs are Hi-Z.

TYPICAL APPLICATION BLOCK DIAGRAM



A. AUD_DIR must be biased to determine audio direction (see Function Table for properly establishing the bias).

B. $\overline{\text{OE}}$ is an active-low pin that must be grounded to 0 V to enable operation of the TWL1200 device.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4.6	V
V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state[2]	A port	–0.5	4.6	V
		B port	–0.5	4.6	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

THERMAL IMPEDANCE RATINGS

				UNIT
θ_{JA}	Package thermal impedance[1]	ZQC package	171.6	°C/W
		YFF package	75	

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.1	3.6	V
V_{CCB}	Supply voltage				1.1	3.6	V
V_{IH}	High-level input voltage	Buffer type	1.1 V to 3.6 V	1.1 V to 3.6 V	$V_{CCI} \times 0.65$	3.6	V
		$\overline{OE}$ and AUD_DIR			$V_{CCA} \times 0.65$	3.6	
V_{IH}	High-level input voltage	Switch type	1.1 V to 3.6 V	1.1 V to 3.6 V	$V_{CCI} - 0.2$	V_{CCI}	V
V_{IL}	Low-level input voltage	Buffer type and Control Logic	1.1 V to 3.6 V	1.1 V to 3.6 V	0	$V_{CCI} \times 0.35$	V
		$\overline{OE}$ and AUD_DIR			0	$V_{CCA} \times 0.35$	
V_{IL} (2)	Low-level input voltage	Switch type	1.1 V to 3.6 V	1.1 V to 3.6 V	0	0.15	V
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.1 V to 1.3 V		–0.5	mA
				1.4 V to 1.6 V		–1	
				1.65 V to 1.95 V		–2	
				2.3 V to 2.7 V		–4	
				3 V to 3.6 V		–8	
I_{OL}	Low-level output current			1.1 V to 1.3 V		0.5	mA
				1.4 V to 1.6 V		1	
				1.65 V to 1.95 V		2	
				2.3 V to 2.7 V		4	
				3 V to 3.6 V		8	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Note, the max V_{IL} value is provided to ensure that a valid V_{OL} is maintained. The V_{OL} value is the V_{IL} + the voltage-drop across the pass-gate transistor.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP(1)	MAX	UNIT
V_{OH}	A port (Buffer-type output, 8-mA drive)	I_{OH} = –100 µA	1.1 V to 3.6 V	1.1 V to 3.6 V	V_{CCO} – 0.2			V
		I_{OH} = –8 mA	1.65 V	1.65 V	1.2			
			2.5 V	2.5 V	1.97			
	A port (Buffer-type output, 4-mA drive)	I_{OH} = –100 µA	1.1 V to 3.6 V	1.1 V to 3.6 V	V_{CCO} – 0.2			
		I_{OH} = –4 mA	1.65 V	1.65 V	1.2			
			2.5 V	2.5 V	1.97			
V_{OH}	A port (Switch-type outputs)	I_{OH} = –20 µA	1.65 V	1.65 V	1.5			V
			2.5 V	2.5 V	2.3			
V_{OL}	A port (Buffer-type output, 8-mA drive)	I_{OL} = 100 µA	1.1 V to 3.6 V	1.1 V to 3.6 V			0.2	V
		I_{OL} = 8 mA	1.65 V	1.65 V			0.45	
			2.5 V	2.5 V			0.55	
	A port (Buffer-type output, 4-mA drive)	I_{OL} = 100 µA	1.1 V to 3.6 V	1.1 V to 3.6 V			0.2	
		I_{OL} = 4 mA	1.65 V	1.65 V			0.45	
			2.5 V	2.5 V			0.55	
V_{OL}	A port (Switch-type outputs)	I_{OL} = 220 µA, V_{IN} = 0.15 V	1.65 V	1.65 V			0.45	V
		I_{OL} = 300 µA, V_{IN} = 0.15 V	2.5 V	2.5 V			0.55	
V_{OH}	B port (Buffer-type output, 8-mA drive)	I_{OH} = –100 µA	1.1 V to 3.6 V	1.1 V to 3.6 V	V_{CC0} – 0.2			V
		I_{OH} = –8 mA	1.65 V	1.65 V	1.2			
			2.5 V	2.5 V	1.97			
	B port (Buffer-type output, 4-mA drive)	I_{OH} = –100 µA	1.1 V to 3.6 V	1.1 V to 3.6 V	V_{CC0} – 0.2			
		I_{OH} = –4 mA	1.65 V	1.65 V	1.2			
			2.5 V	2.5 V	1.97			
	B port (Buffer-type output, 2-mA drive)	I_{OH} = –100 µA	1.1 V to 3.6 V	1.1 V to 3.6 V	V_{CC0} – 0.2			
		I_{OH} = –2 mA	1.65 V	1.65 V	1.2			
			2.5 V	2.5 V	1.97			
	B port (Switch-type outputs)	I_{OH} = –20 µA	1.65 V	1.65 V	1.5			
			2.5 V	2.5 V	2.3			
V_{OL}	B port (Buffer-type output, 8-mA drive)	I_{OL} = 100 µA	1.1 V to 3.6 V	1.1 V to 3.6 V			0.2	V
		I_{OL} = 8 mA	1.65 V	1.65 V			0.45	
			2.5 V	2.5 V			0.55	
	B port (Buffer-type output, 4-mA drive)	I_{OL} = 100 µA	1.1 V to 3.6 V	1.1 V to 3.6 V			0.2	
		I_{OL} = 4 mA	1.65 V	1.65 V			0.45	
			2.5 V	2.5 V			0.55	
	B port (Buffer-type output, 2-mA drive)	I_{OL} = 100 µA	1.1 V to 3.6 V	1.1 V to 3.6 V			0.2	
		I_{OL} = 2 mA	1.65 V	1.65 V			0.45	
			2.5 V	2.5 V			0.55	
	B port (Switch-type outputs)	I_{OL} = 220 µA, V_{IN} = 0.15 V	1.65 V	1.65 V			0.45	
		I_{OL} = 300 µA, V_{IN} = 0.15 V	2.5 V	2.5 V			0.55	
I_I		V_I = V_{CCA} or GND	1.1 V to 3.6 V	1.1 V to 3.6 V			±1	µA
I_{CCA}		Switch-type I/O are open and all other inputs are biased at either V_{CC} or GND	1.1 V to 3.6 V	1.1 V to 3.6 V			15	µA
			3.6 V	0 V			14	
			0 V	3.6 V			–12	

---

(1) All typical values are at T_A = 25°C.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP (1)	MAX	UNIT
I_{CCB}		Switch-type I/O are open and all other inputs are biased at either V_{CC} or GND	1.1 V to 3.6 V	1.1 V to 3.6 V			15	μA
			3.6 V	0 V			–12	
			0 V	3.6 V			14	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.1 V to 3.6 V	1.1 V to 3.6 V			30	μA
C_{io}	Auto-Dir (SDIO lines)	$V_I = V_{CCI}$					5.5	pF
	Bi-Dir buffer	$V_I = V_{CCX}$ or GND					4.5	
C_i	AUD_DIR / $\overline{OE}$	$V_I = V_{CCA}$ or GND					4	pF
	Buffer	$V_I = V_{CCX}$ or GND					4	
C_o	2-mA buffer	$V_I = V_{CCX}$ or GND					5	pF
	4-mA buffer	$V_I = V_{CCX}$ or GND					5	
	8-mA buffer	$V_I = V_{CCX}$ or GND					6	

OUTPUT DRIVE STRENGTH

2 mA	4 mA	8 mA
WLAN_EN(B)	AUDIO_OUT(A)	SDIO_CLK(B)
SLOW_CLK(B)	WLAN_IRQ(A)	BT_UART_TX(A)
BT_EN(B)	CLK_REQ(A)	BT_UART_RX(B)
	AUDIO_IN(B)	
	AUDIO_CLK(A)	
	BT_UART CTS(B)	
	BT_UART RTS(A)	
	AUDIO_F-SYNC(A)	

TIMING REQUIREMENTS
V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted)

				V_{CCB} = 1.8 V ± 0.15 V		UNIT
				MIN	MAX	
	Data rate	SDIO_CMD	Push-pull driving		60	Mbps
			Open-drain driving		1	
		SDIO_CLK	Push-pull driving		50	MHz
		SDIO_DATAx			60	Mbps
t_W	Pulse duration	SDIO_CMD	Push-pull driving	17		ns
			Open-drain driving	1		μs
		SDIO_CLK	Push-pull driving	10		ns
		SDIO_DATAx		17		ns

TIMING REQUIREMENTS
V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

				V_{CCB} = 1.8 V ± 0.15 V		UNIT
				MIN	MAX	
	Data rate	SDIO_CMD	Push-pull driving		60	Mbps
			Open-drain driving		1	
		SDIO_CLK	Push-pull driving		50	MHz
		SDIO_DATAx			60	Mbps
t_W	Pulse duration	SDIO_CMD	Push-pull driving	17		ns
			Open-drain driving	1		μs
		SDIO_CLK	Push-pull driving	10		ns
		SDIO_DATAx		17		ns

SWITCHING CHARACTERISTICS
V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 1.8 V ± 0.15 V		UNIT
				MIN	MAX	
t_{pd}	SDIO_CMD(A)	SDIO_CMD(B)	Push-pull driving		7	ns
			Open-drain driving (H-to-L)	1.1	7	
			Open-drain driving (L-to-H)	30	510	
	SDIO_CMD(B)	SDIO_CMD(A)	Push-pull driving		7	
			Open-drain driving (H-to-L)	1	7.5	
			Open-drain driving (L-to-H)	30	515	
	SDIO_CLK(A)	SDIO_CLK(B)	Push-pull driving	1	6.5	
	SDIO_DATAx(A)	SDIO_DATAx(B)	Push-pull driving	1	7	
	SDIO_DATAx(B)	SDIO_DATAx(A)		1	7	
	Buffered input	2-mA drive strength output	Push-pull driving	1	7.6	
	Buffered input	4-mA drive strength output	Push-pull driving	1	7	
	Buffered input	8-mA drive strength output	Push-pull driving	1	6.5	
t_{en}	OE	2-mA drive strength output	Push-pull driving		16	ns
		4-mA drive strength output	Push-pull driving		19	
		8-mA drive strength output	Push-pull driving		18	
		Switch-type output	Push-pull driving		1	µs
t_{dis}	OE	2-mA drive strength output	Push-pull driving		17	ns
		4-mA drive strength output	Push-pull driving		16.5	
		8-mA drive strength output	Push-pull driving		16	
		Switch-type outputs	Push-pull driving		1	µs
t_{rA}	SDIO_CMD(A) rise time		Push-pull driving	1	5	ns
			Open-drain driving	15	420	
	SDIO_DATAx(A) rise time		Push-pull driving	1	4.7	
t_{rB}	SDIO_CMD(B) rise time		Push-pull driving	1	9.7	ns
			Open-drain driving	15	420	
	SDIO_CLK(B) rise time		Push-pull driving	0.5	6	
	SDIO_DATAx(B) rise time			1	9.7	
t_{fA}	SDIO_CMD(A) fall time		Push-pull driving	0.7	8.3	ns
			Open-drain driving	1.6	8.3	
	SDIO_DATAx(A) fall time		Push-pull driving	1	8.3	
t_{fB}	SDIO_CMD(B) fall time		Push-pull driving	1	9.9	ns
			Open-drain driving	1.6	10.9	
	SDIO_CLK(B) fall time		Push-pull driving	0.5	5.3	
	SDIO_DATAx(B) fall time			1	9.9	
$t_{sk(O)}$	SDIO Ch-A to Ch-B skew		Push-pull driving		0.4	ns
	SDIO Ch-B to Ch-A skew		Push-pull driving		0.4	
	SDIO channel-to-clock skew		Push-pull driving		1.3	
Max data rate	SDIO_CMD		Push-pull driving		60	Mbps
			Open-drain driving		1	
	SDIO_CLK		Push-pull driving		50	MHz
	SDIO_DATAx				60	Mbps

SWITCHING CHARACTERISTICS

V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 1.8 V ± 0.15 V		UNIT
				MIN	MAX	
t_{pd}	SDIO_CMD(A)	SDIO_CMD(B)	Push-pull driving		7	ns
			Open-drain driving (H-to-L)	1.1	7	
			Open-drain driving (L-to-H)	30	510	
	SDIO_CMD(B)	SDIO_CMD(A)	Push-pull driving		7	
			Open-drain driving (H-to-L)	1	7.5	
			Open-drain driving (L-to-H)	30	515	
	SDIO_CLK(A)	SDIO_CLK(B)	Push-pull driving	1	6.5	
	SDIO_DATAx(A)	SDIO_DATAx(B)	Push-pull driving	1	7	
	SDIO_DATAx(B)	SDIO_DATAx(A)		1	7	
	Buffered input	2-mA drive strength output	Push-pull driving	1	7.6	
	Buffered input	4-mA drive strength output	Push-pull driving	1	7	
	Buffered -nput	8-mA drive strength output	Push-pull driving	1	6.5	
t_{en}	OE	2-mA drive strength output	Push-pull driving		16	ns
		4-mA drive strength output	Push-pull driving		19	
		8-mA drive strength output	Push-pull driving		19	
		Switch-type output	Push-pull driving		1	μs
t_{dis}	OE	2-mA drive strength output	Push-pull driving		17	ns
		4-mA drive strength output	Push-pull driving		16	
		8-mA drive strength output	Push-pull driving		16	
		Switch-type output	Push-pull driving		1	μs
t_{rA}	SDIO_CMD(A) rise time		Push-pull driving	1	4.25	ns
			Open-drain driving	15	420	
	SDIO_DATAx(A) rise time		Push-pull driving	1	4.25	
t_{rB}	SDIO_CMD(B) rise time		Push-pull driving	1	9.5	ns
			Open-drain driving	15	420	
	SDIO_CLK(B) rise time		Push-pull driving	0.5	5.9	
	SDIO_DATAx(B) rise time			1	9.6	
t_{fA}	SDIO_CMD(A) fall time		Push-pull driving	0.7	8.2	ns
			Open-drain driving	1.6	8.2	
	SDIO_DATAx(A) fall time		Push-pull driving	1	8.2	
t_{fB}	SDIO_CMD(B) fall time		Push-pull driving	1	9.2	ns
			Open-drain driving	1.6	10.8	
	SDIO_CLK(B) fall time		Push-pull driving	0.5	5.2	
	SDIO_DATAx(B) fall time			1	9.8	
$t_{sk(O)}$	SDIO Ch-A to Ch-B skew		Push-pull driving		0.4	ns
	SDIO Ch-B to Ch-A skew		Push-pull driving		0.4	
	SDIO Channel-to-Clock skew		Push-pull driving		1.3	
Max data rate	SDIO_CMD		Push-pull driving		60	Mbps
			Open-drain driving		1	
	SDIO_CLK		Push-pull driving		50	MHz
	SDIO_DATAx				60	Mbps

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER			TEST CONDITIONS	$V_{CCA} = V_{CCB}$ = 1.8 V	$V_{CCA} = V_{CCB}$ = 2.5 V	UNIT
DATAx and CMD	Enabled	C_{pd} input side	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	18.3	20.3	pF
		C_{pd} output side		18.25	19.52	
	Disabled	C_{pd} input side		0.8	0.8	
		C_{pd} output side		0.1	0.1	
Clock	Enabled	C_{pd} input side	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	0.6	0.9	pF
		C_{pd} output side		8.8	10.1	
	Disabled	C_{pd} input side		0.1	0.1	
		C_{pd} output side		0.1	0.1	
2-mA buffer	Enabled	C_{pd} input side	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	0.6	1.0	pF
		C_{pd} output side		7.1	7.9	
	Disabled	C_{pd} input side		0.1	0.1	
		C_{pd} output side		0.1	0.1	
4-mA buffer	Enabled	C_{pd} input side	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	0.6	1.0	pF
		C_{pd} output side		7.6	8.6	
	Disabled	C_{pd} input side		0.1	0.1	
		C_{pd} output side		0.1	0.1	
8-mA buffer	Enabled	C_{pd} input side	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	0.6	1.0	pF
		C_{pd} output side		8.8	10.1	
	Disabled	C_{pd} input side		0.1	0.1	
		C_{pd} output side		0.1	0.1	
4-mA I/O	Enabled	C_{pd} input side	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	0.6	0.95	pF
		C_{pd} output side		8.2	9.1	
	Disabled	C_{pd} input side		0.1	0.1	
		C_{pd} output side		0.1	0.1	

TYPICAL CHARACTERISTICS

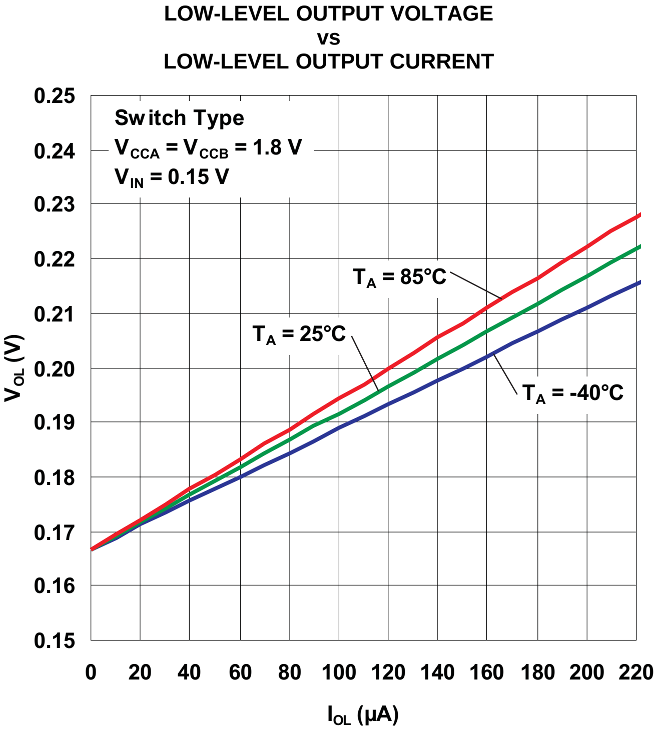


Figure 1.

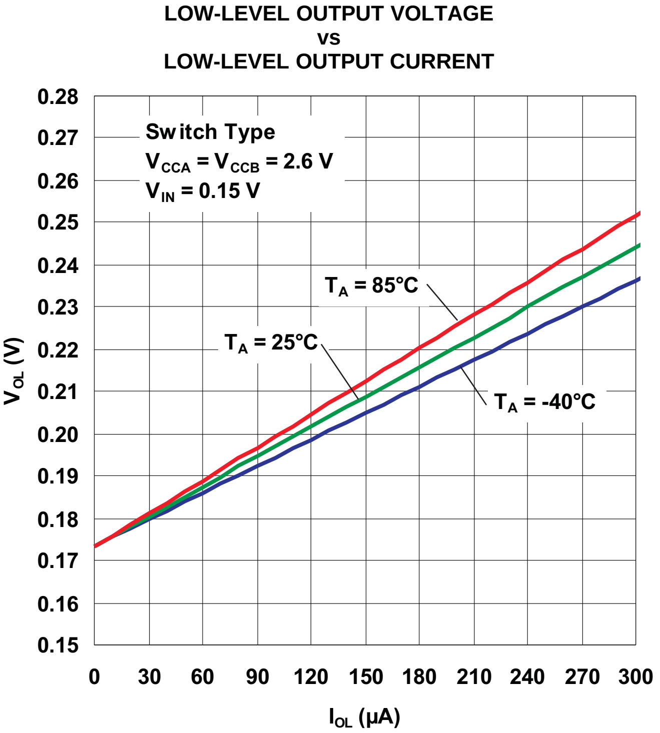


Figure 2.

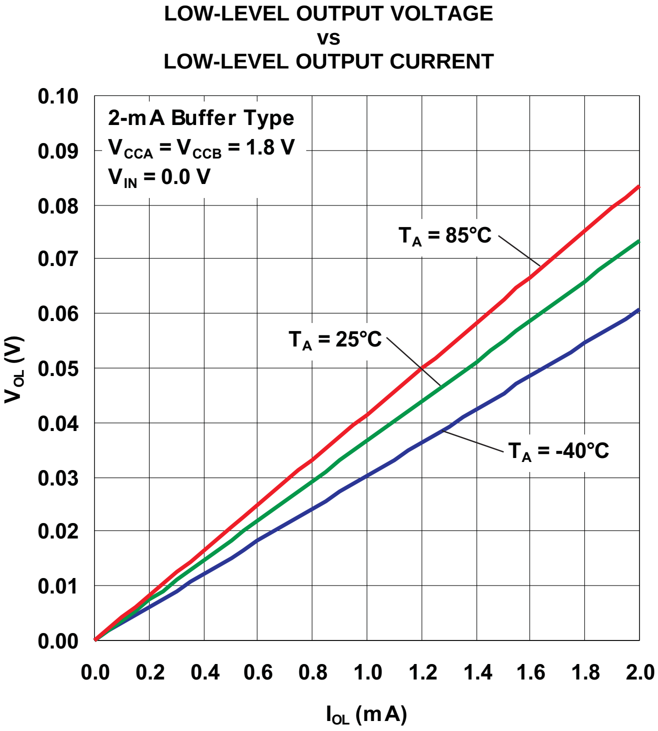


Figure 3.

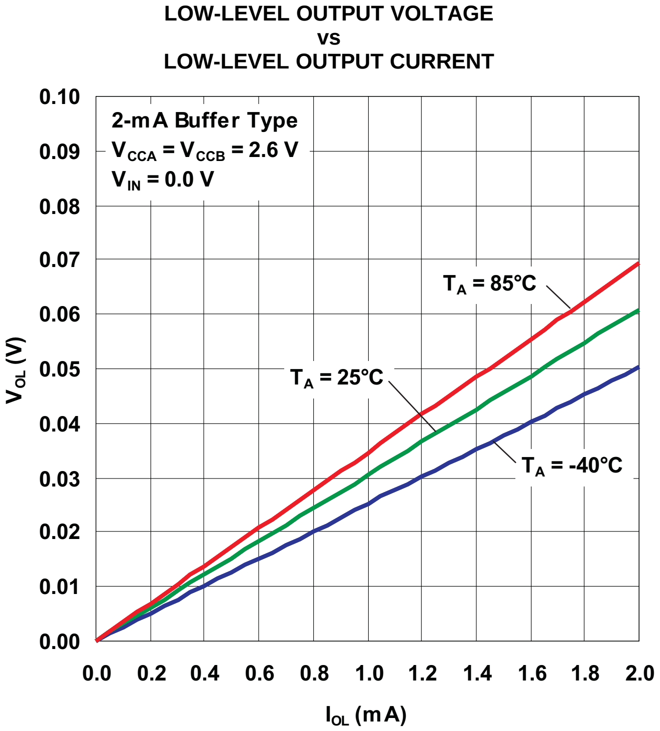


Figure 4.

TYPICAL CHARACTERISTICS (continued)

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

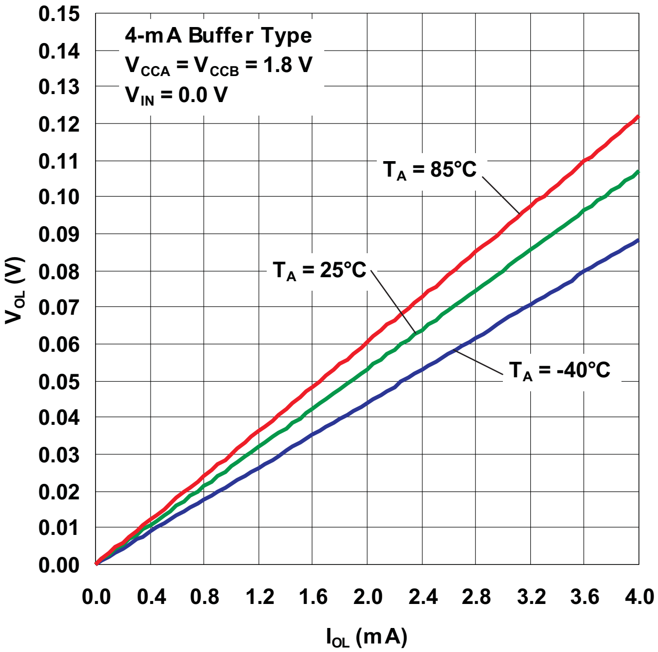


Figure 5.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

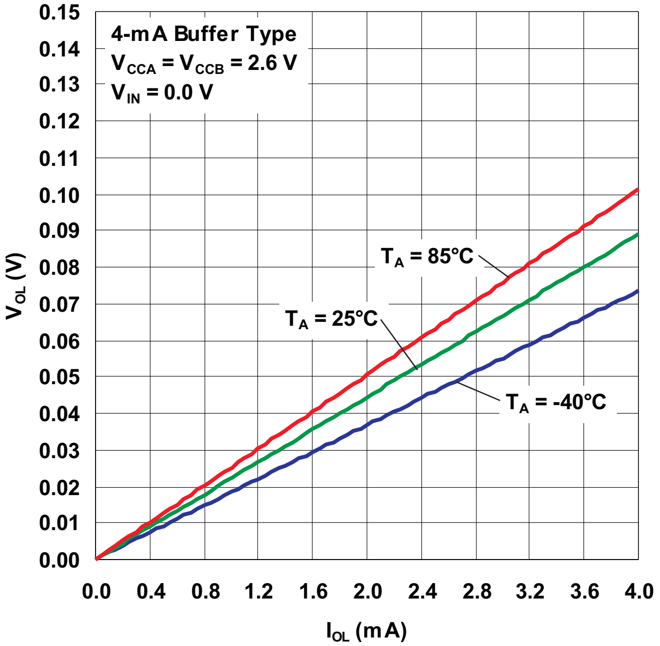


Figure 6.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

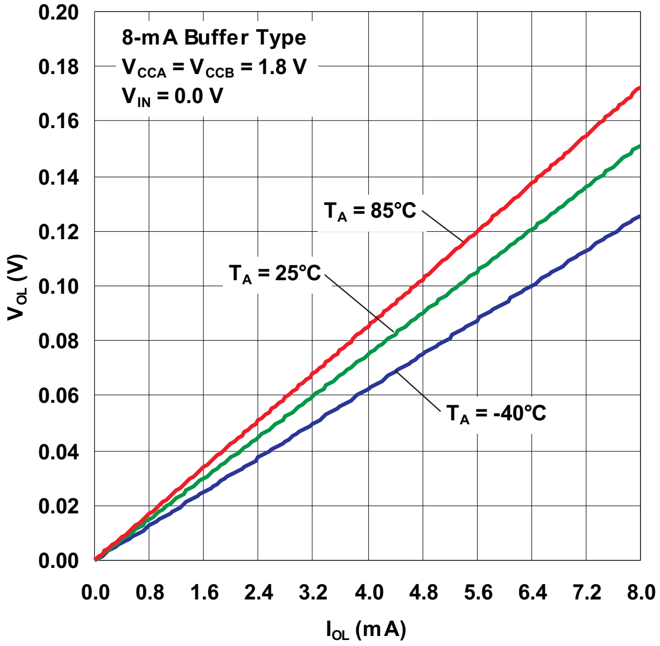


Figure 7.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

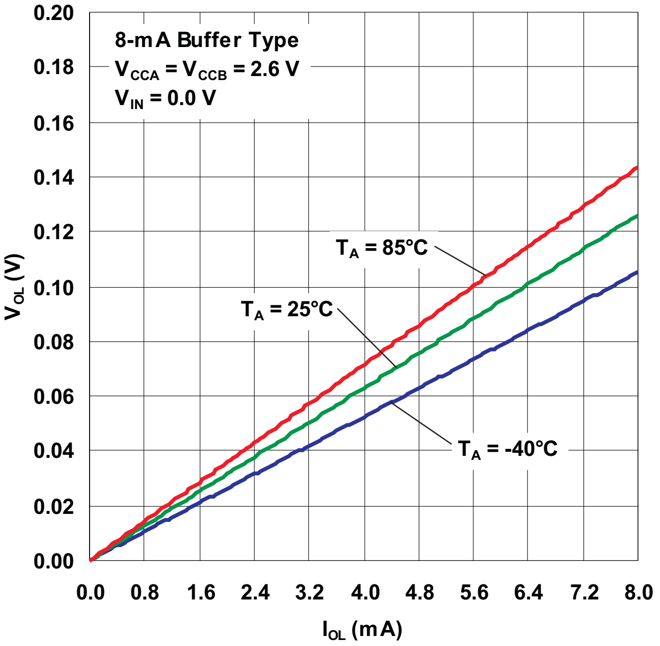


Figure 8.

TYPICAL CHARACTERISTICS (continued)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

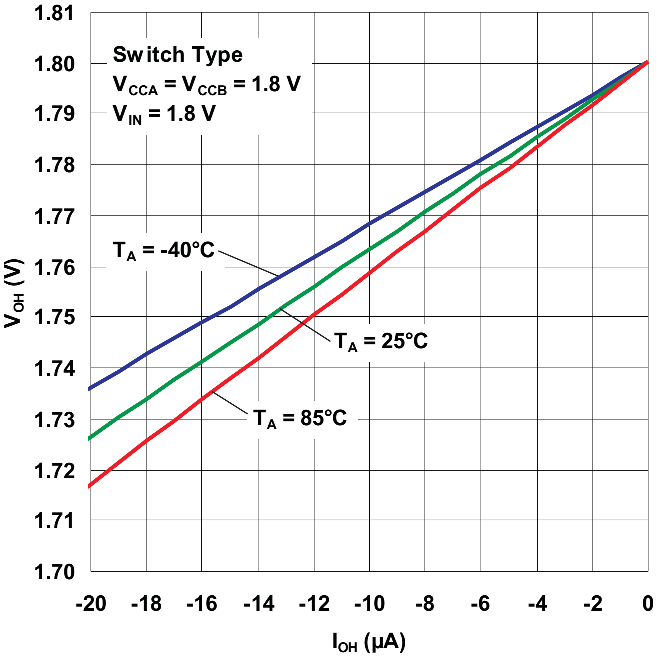


Figure 9.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

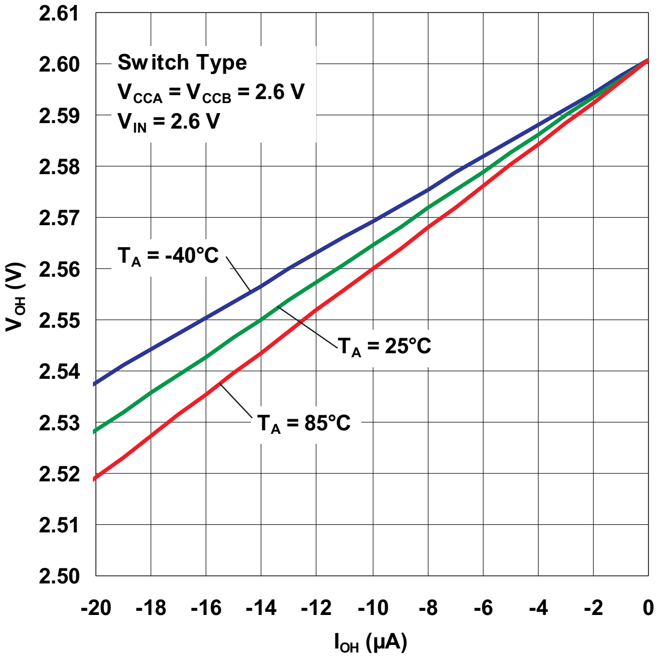


Figure 10.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

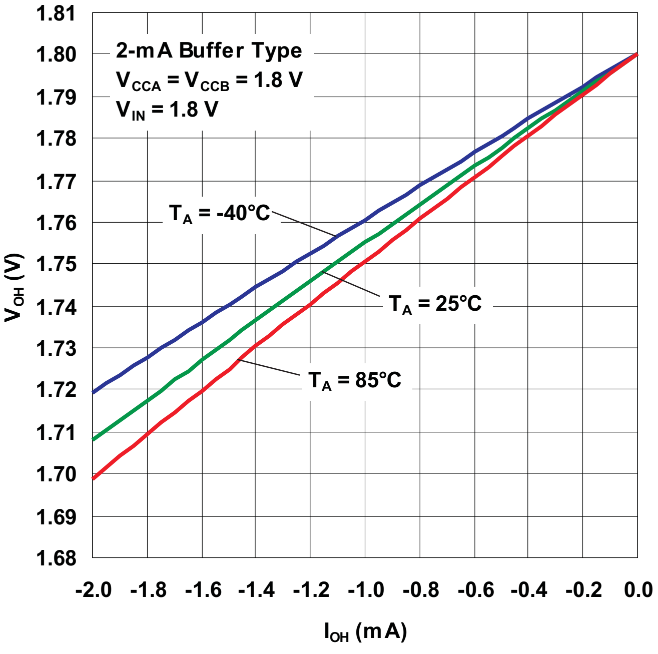


Figure 11.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

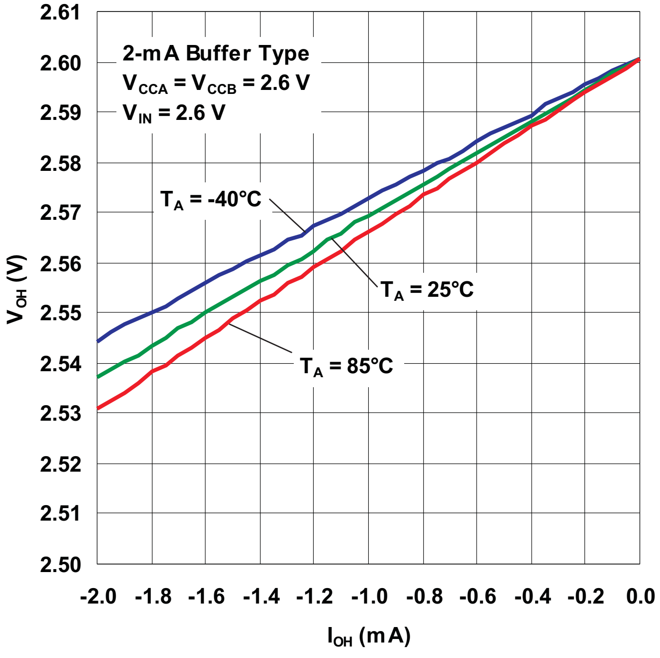


Figure 12.

TYPICAL CHARACTERISTICS (continued)

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

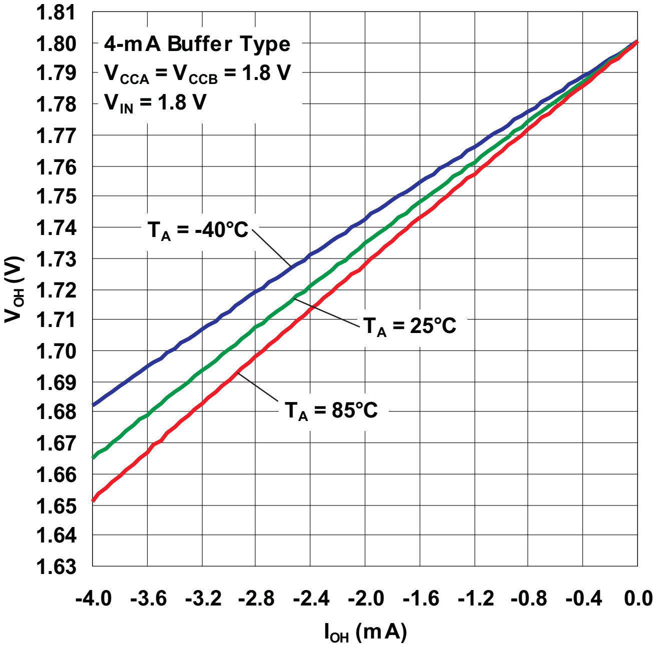


Figure 13.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

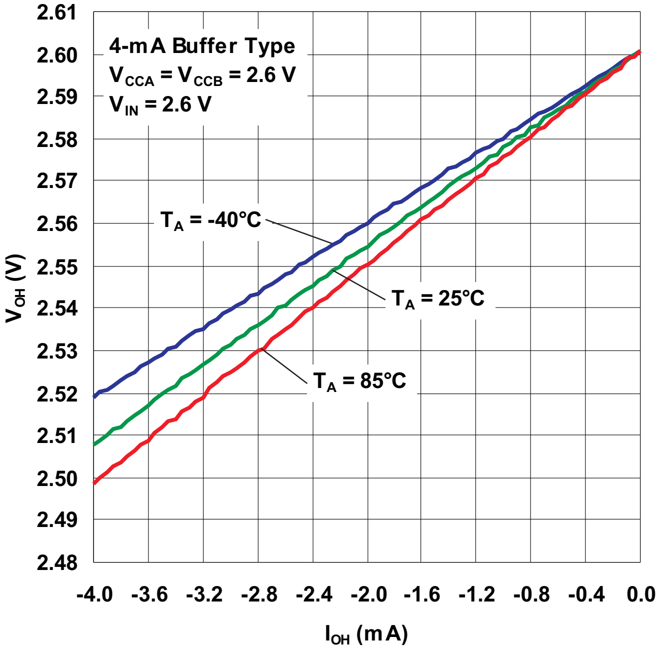


Figure 14.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

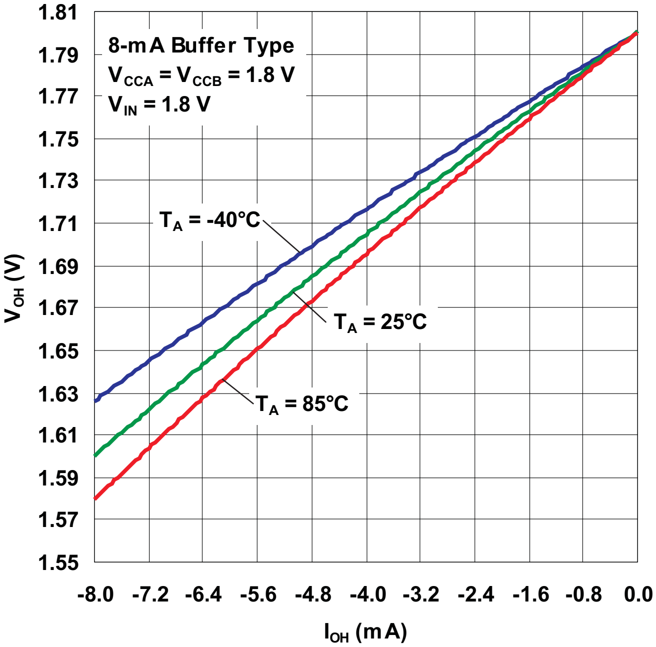


Figure 15.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

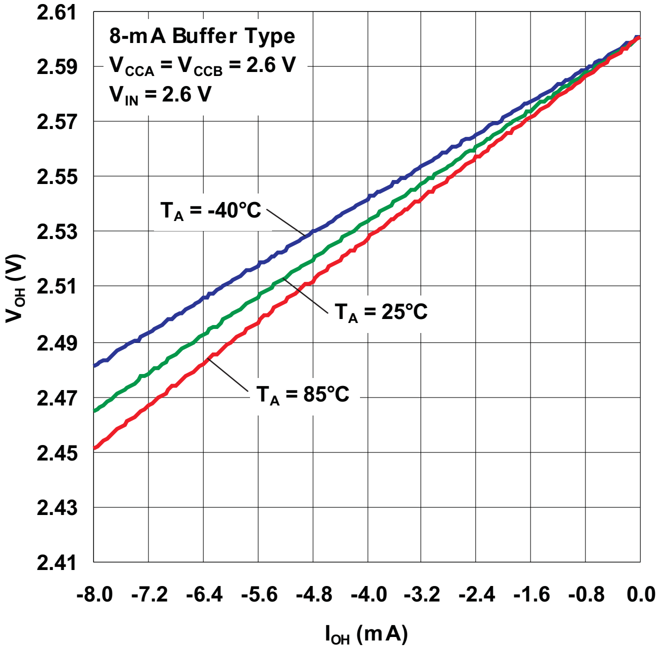


Figure 16.

TYPICAL CHARACTERISTICS (continued)

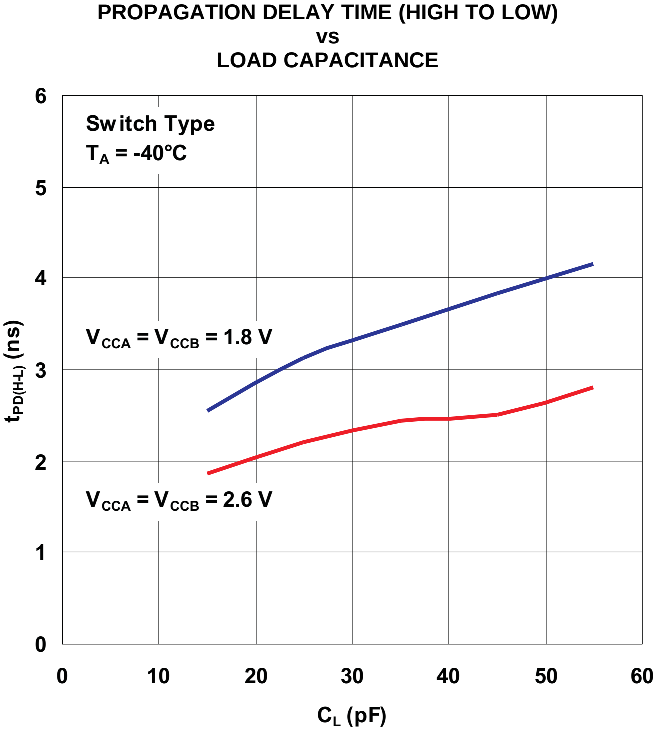


Figure 17.

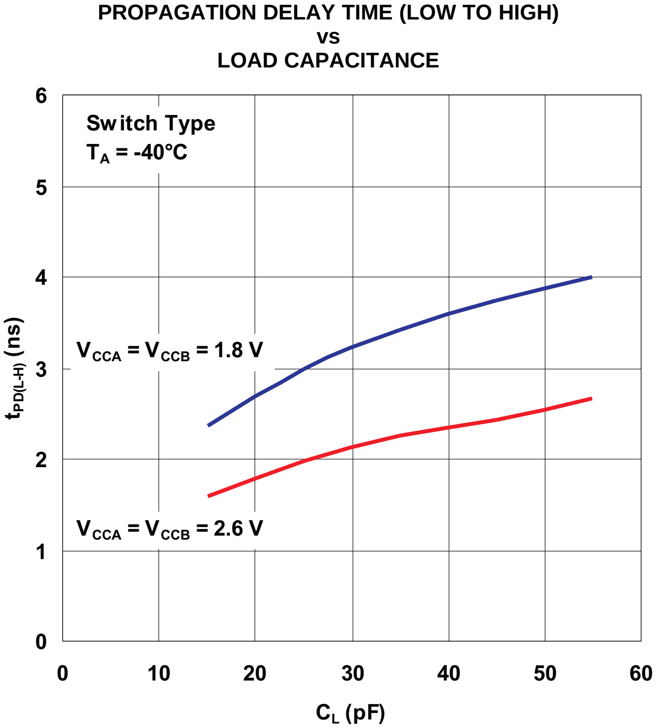


Figure 18.

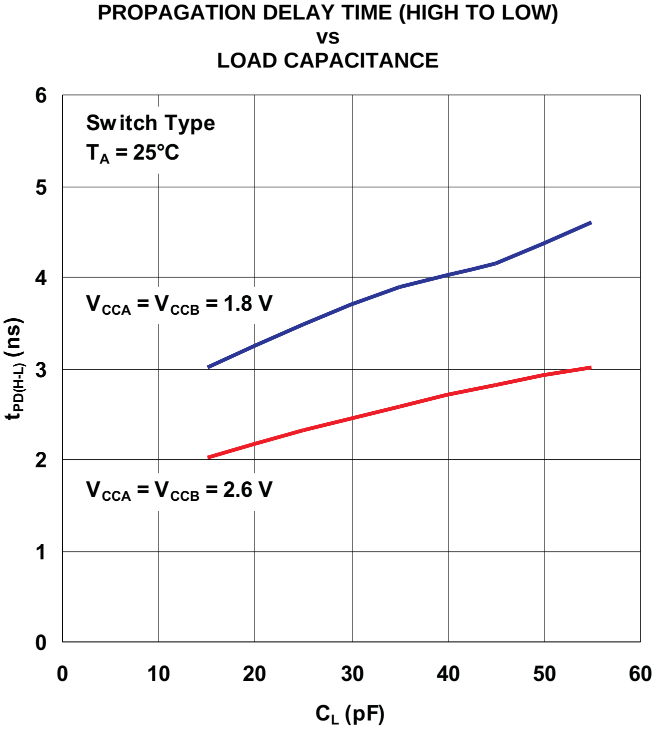


Figure 19.

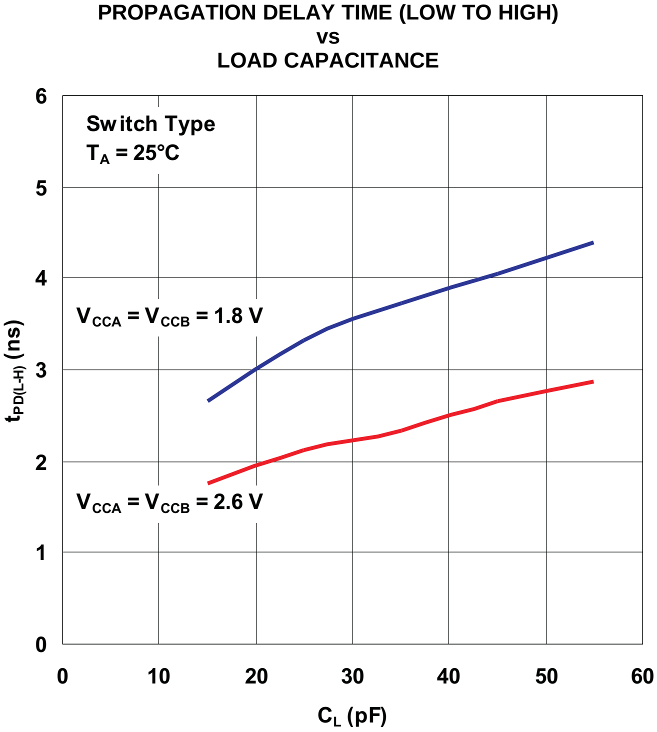


Figure 20.

TYPICAL CHARACTERISTICS (continued)

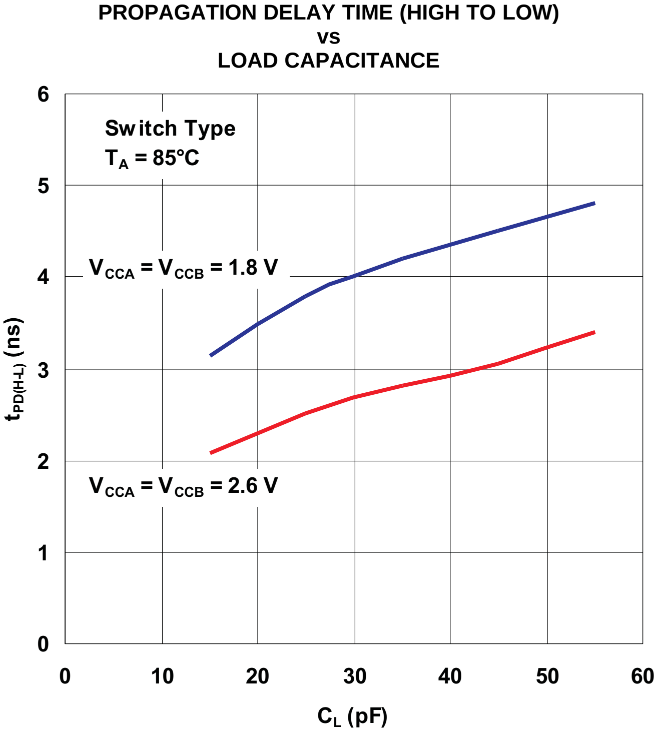


Figure 21.

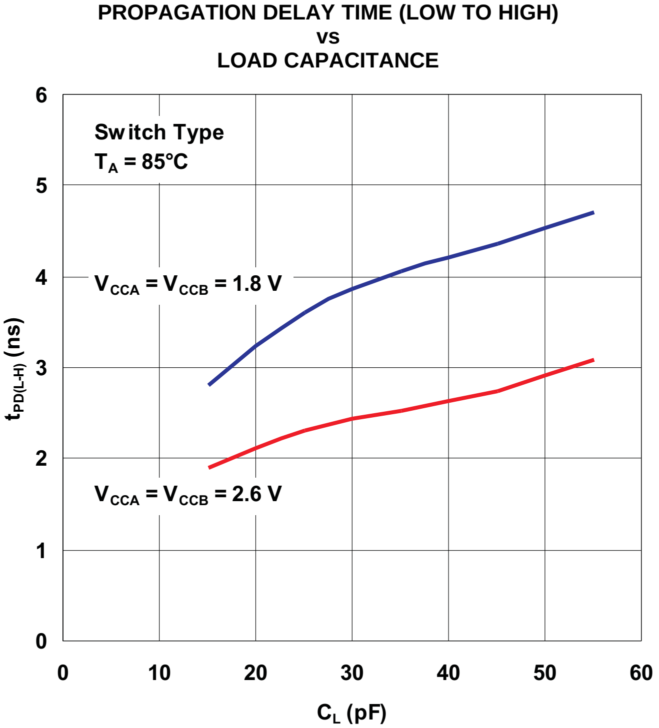


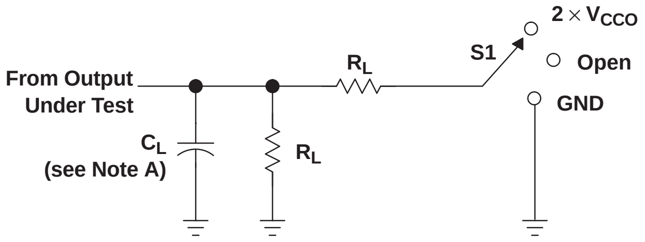
Figure 22.

Typical Application Wiring for TWL1200 When Connecting to the WL1271

Table 2. WL1271+TWL1200 Interface

HOST (MSM)	PIN NAME	BALL NO.	TYPE		TYPE	BALL NO.	PIN NAME	WL1271 COB
	VCCA	C4	Power (3.0 V)	TWL1200	Power (1.8 V)	C5	VCCB	
	VCCA	D4	Power (3.0 V)		Power (1.8 V)	D5	VCCB	
	SDIO_DATA0(A)	B2	I/O ↔		I/O ↔	B6	SDIO_DATA0(B)	K4
	SDIO_DATA1(A)	C2	I/O ↔		I/O ↔	C6	SDIO_DATA1(B)	J4
	SDIO_DATA2(A)	C1	I/O ↔		I/O ↔	C7	SDIO_DATA2(B)	J3
	SDIO_DATA3(A)	B1	I/O ↔		I/O ↔	B7	SDIO_DATA3(B)	J5
	SDIO_CMD(A)	A2	I/O ↔		I/O ↔	A6	SDIO_CMD(B)	L3
	SDIO_CLK(A)	A1	I →		O →	A7	SDIO_CLK(B)	M3
	WLAN_EN(A)	D1	I →		O →	D6	WLAN_EN(B)	J2
	WLAN_IRQ(A)	D2	O ←		I ←	D7	WLAN_IRQ(B)	G4
	CLK_REQ(A)	E1	O ←		I ←	E7	CLK_REQ(B)	F5
	BT_EN(A)	E2	I →		O →	E6	BT_EN(B)	G5
	BT_UART_RX(A)	G1	I →		O →	G7	BT_UART_RX(B)	G7
	BT_UART_CTS(A)	F1	I →		O →	F7	BT_UART_CTS(B)	E11
	BT_UART_TX(A)	G2	O ←		I ←	G6	BT_UART_TX(B)	G8
	BT_UART_RTS(A)	F2	O ←		I ←	F6	BT_UART_RTS(B)	G11
	AUDIO_IN(A)	F3	I →		I/O ↔	F5	AUDIO_IN(B)	F6
	AUDIO_CLK(A)	A3	I/O ↔		I/O ↔	A5	AUDIO_CLK(B)	F8
	AUDIO_F-SYN(A)	B3	I/O ↔		I/O ↔	B5	AUDIO_F-SYN(B)	H11
	AUDIO_OUT(A)	G3	O ←		I ←	G5	AUDIO_OUT(B)	F7
	SLOW_CLK(A)	G4	I →		O →	F4	SLOW_CLK(B)	K9
	AUD_DIR	A4	I →		GND	D3	GND	
	$\overline{OE}$	B4	active low			E3	GND	
						E4	GND	
						E5	GND	

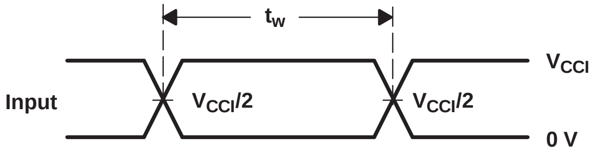
PARAMETER MEASUREMENT INFORMATION



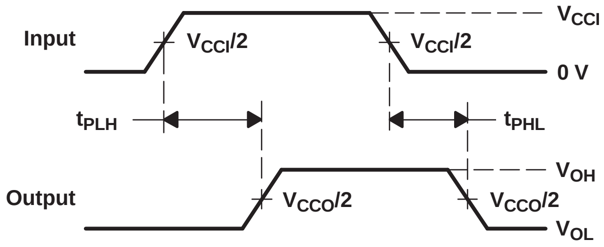
LOAD CIRCUIT FOR BUFFER-TYPE OUTPUTS

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

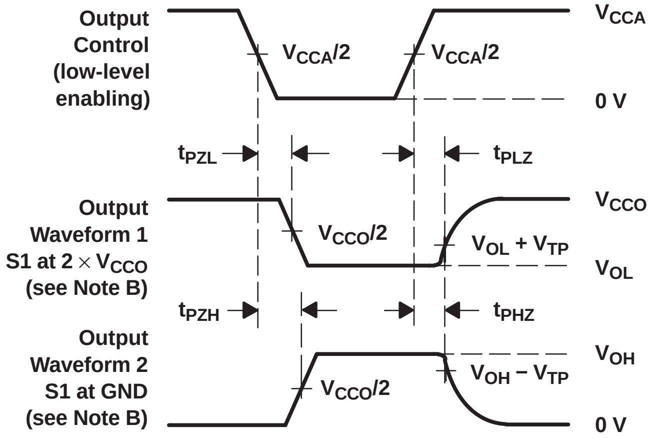
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

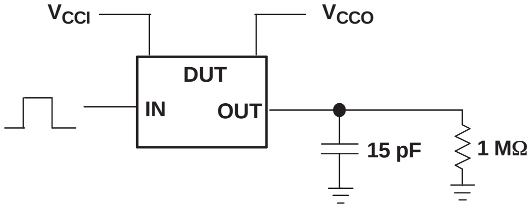


VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

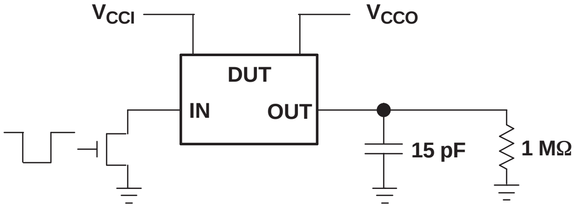
NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

Figure 23. Push-Pull Buffered Direction Control Load Circuit and Voltage Waveform

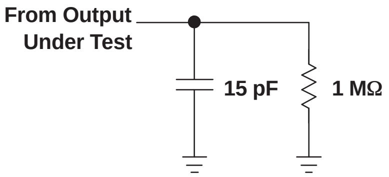
PARAMETER MEASUREMENT INFORMATION (continued)



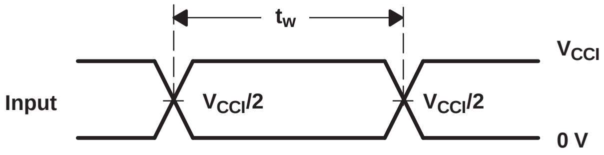
DATA RATE, PULSE DURATION, PROPAGATION DELAY, OUTPUT RISE AND FALL TIME MEASUREMENT USING A PUSH-PULL DRIVER



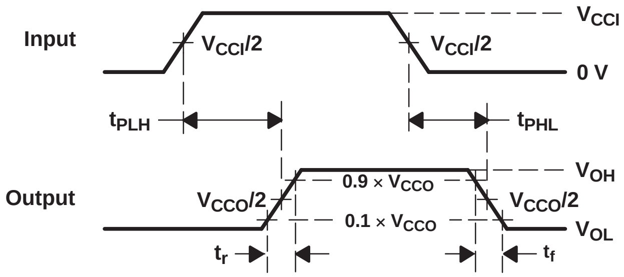
DATA RATE, PULSE DURATION, PROPAGATION DELAY, OUTPUT RISE AND FALL TIME MEASUREMENT USING AN OPEN-DRAIN DRIVER



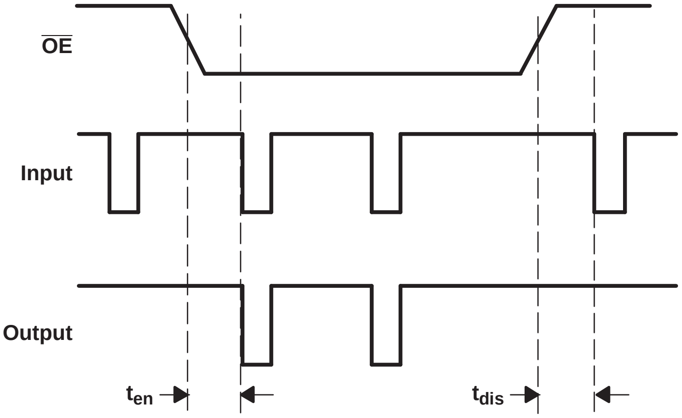
LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT – SWITCH-TYPE SDIOs



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

Figure 24. Auto-Direction Control Load Circuit and Voltage Waveform

APPLICATION CIRCUIT EXAMPLES

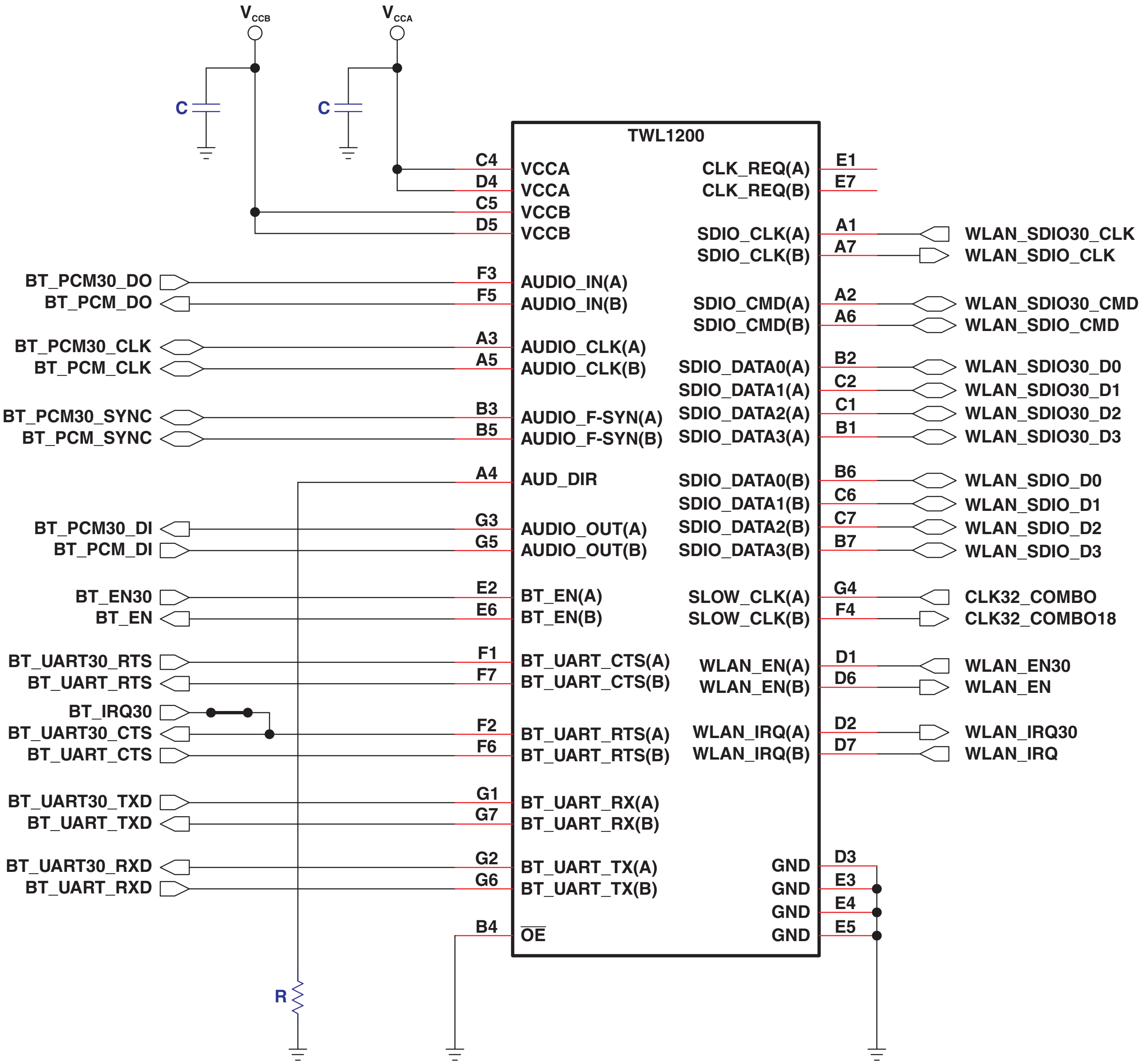


Figure 25. Application Circuit Example, $\overline{\text{OE}}$ Connection With Audio_CLK and Audio_F-SYNC Channels Established From B Side to A Side

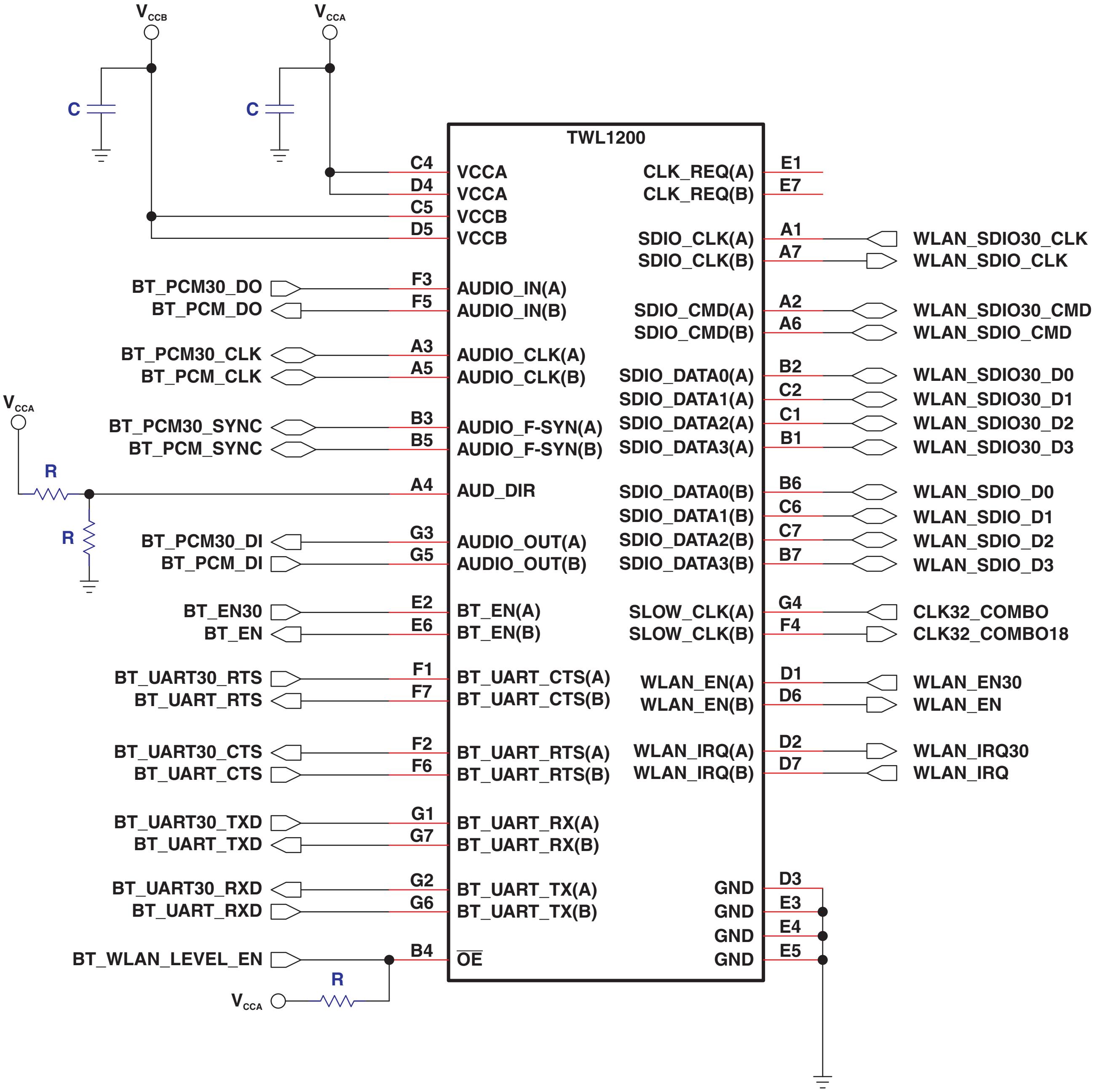


Figure 26. Application Circuit Example, With Voltage Divider for AUD_DIR Connection

PRINCIPLES OF OPERATION

Applications

The TWL1200 device has been designed to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels between a host processor and the Texas Instruments Wi-Link-6 WLAN/BT/FM products. It is intended to be used in a point-to-point topology when interfacing these devices that may or may not be operating at different interface voltages.

Architecture

The BT/UART and PCM/Audio subsystem interfaces consist of a fully-buffered voltage translator design that has its output transistors to source and sink current optimized for drive strength.

The SDIO lines comprise a semi-buffered auto-direction-sensing based translator architecture (see Figure 27) that does not require a direction-control signal to control the direction of data flow of the A to B ports (or from B to A ports).

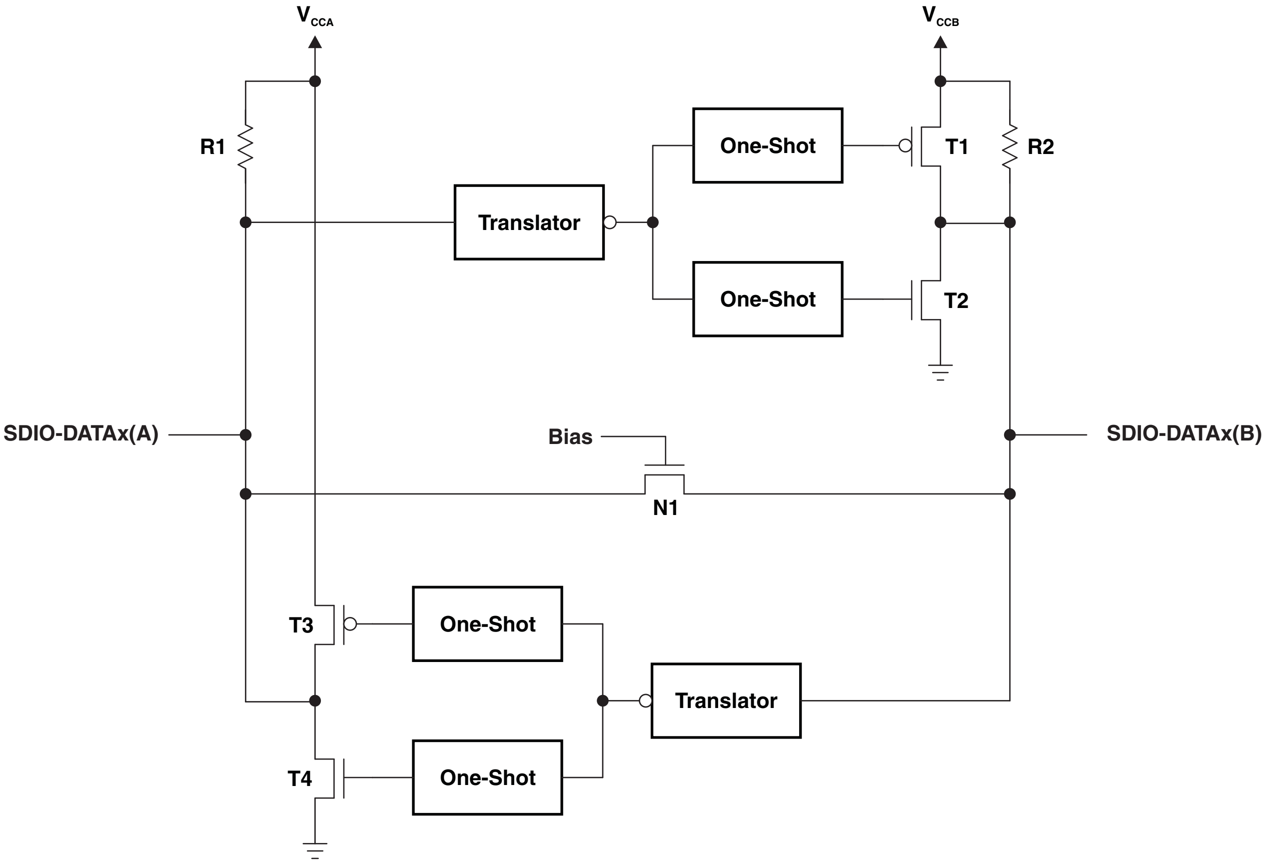


Figure 27. Architecture of an SDIO Switch-Type Cell

Each of these bidirectional SDIO channels independently determines the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The following two key circuits are employed to facilitate the "switch-type" voltage translation function:

1. Integrated pullup resistors to provide dc-bias and drive capabilities
2. An N-channel pass-gate transistor topology (with a high R_{ON} of ~300 Ω) that ties the A-port to the B-port
3. Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports

For bidirectional voltage translation, pullup resistors are included on the device for dc current sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set at a level that optimizes the switch characteristics for maximum data rate as well as minimal static supply leakage. Data can flow in either direction without guidance from a control signal.

The edge-rate acceleration circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device.

During a low-to-high signal rising-edge, the O.S. circuits turn on the PMOS transistors (T_1, T_3) and its associated driver output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first. This edge-rate acceleration provides high ac drive by bypassing the internal pullup resistors during the low-to-high transition to speed up the rising-edge signal.

During a high-to-low signal falling-edge, the O.S. circuits turn on the NMOS transistors (T_2, T_4) and its associated driver output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first.

To minimize dynamic I_{CC} and the possibility of signal contention, the user should wait for the O.S. circuit to turn-off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number provided in the *Timing Requirements* section of this data sheet.

Once the O.S. is triggered and switched off, both the A and B ports must go to the same state (i.e. both High or both Low) for the one-shot to trigger again. In a DC state, the output drivers maintain a Low state through the pass transistor. The output drivers maintain a High through the "smart pullup resistors" that dynamically change value based on whether a Low or a High is being passed through the SDIO lines, as follows:

- R_{PU1} and R_{PU2} values are 25 kΩ when the output is driving a low
- R_{PU1} and R_{PU2} values are 4 kΩ when the output is driving a high
- R_{PU1} and R_{PU2} values are 70 kΩ when the device is disabled via the $\overline{OE}$ pin or by pulling the either V_{CCA} or V_{CCB} to 0 V.

The reason for using these "smart" pullup resistors is to allow the TWL1200 to realize a lower static power consumption (when the I/Os are low), support lower V_{OL} values for the same size pass-gate transistor, and improved simultaneous switching performance.

Input Driver Requirements

The continuous dc-current "sinking" capability is determined by the external system-level driver interfaced to the SDIO pins. Since the high bandwidth of these bidirectional SDIO circuits necessitates the need for a port to quickly change from an input to an output (and vice-vera), they have a modest dc-current "sourcing" capability of hundreds of micro-Amps, as determined by the smart pullup resistor values.

The fall time (t_{fA}, t_{fB}) of a signal depends on the edge rate and output impedance of the external device driving the SDIO I/Os, as well as the capacitive loading on these lines.

Similarly, the t_{pd} and max data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{pd}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω.

Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TWL1200 SDIO output sees, so it is recommended that this lumped-load capacitance be considered and kept below 75 pF to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

Package Dimensions

The dimensions for the YFF package are shown in Table 3. See the package drawing at the end of this data sheet.

Table 3. YFF Package Dimensions

Packaged Device	D	E
TWL1200YFFR	2.76 ± 0.03 mm	2.76 ± 0.03 mm

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TWL1200YFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	YW200	Samples
TWL1200ZQCR	ACTIVE	BGA MICROSTAR JUNIOR	ZQC	48	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	YW200	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TWL1200 :

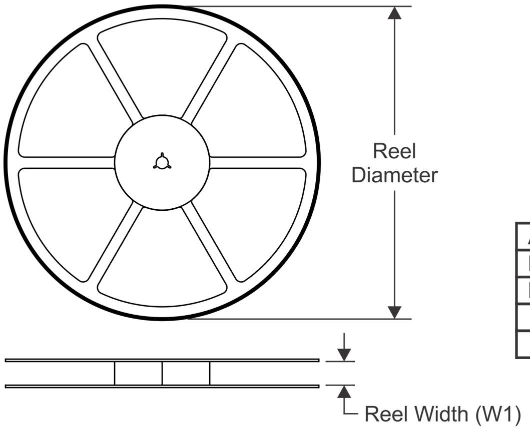
- Automotive: TWL1200-Q1

NOTE: Qualified Version Definitions:

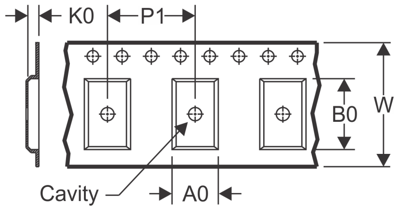
  - Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

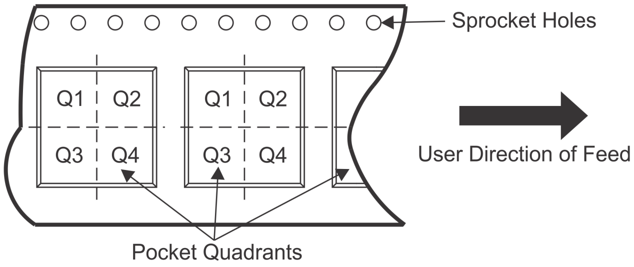


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

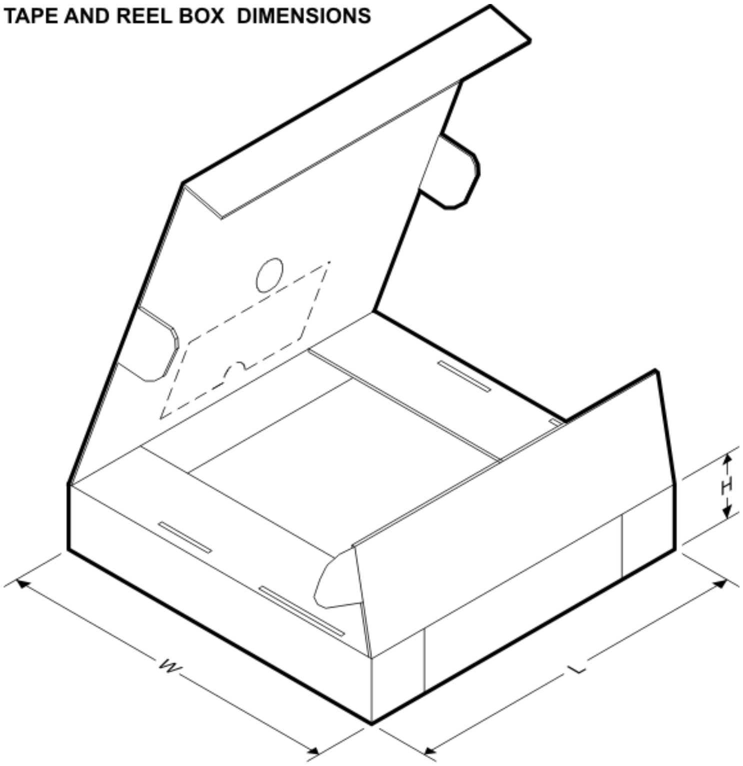
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TWL1200YFFR	DSBGA	YFF	49	3000	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
TWL1200ZQCR	BGA MICROSTAR JUNIOR	ZQC	48	2500	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q1

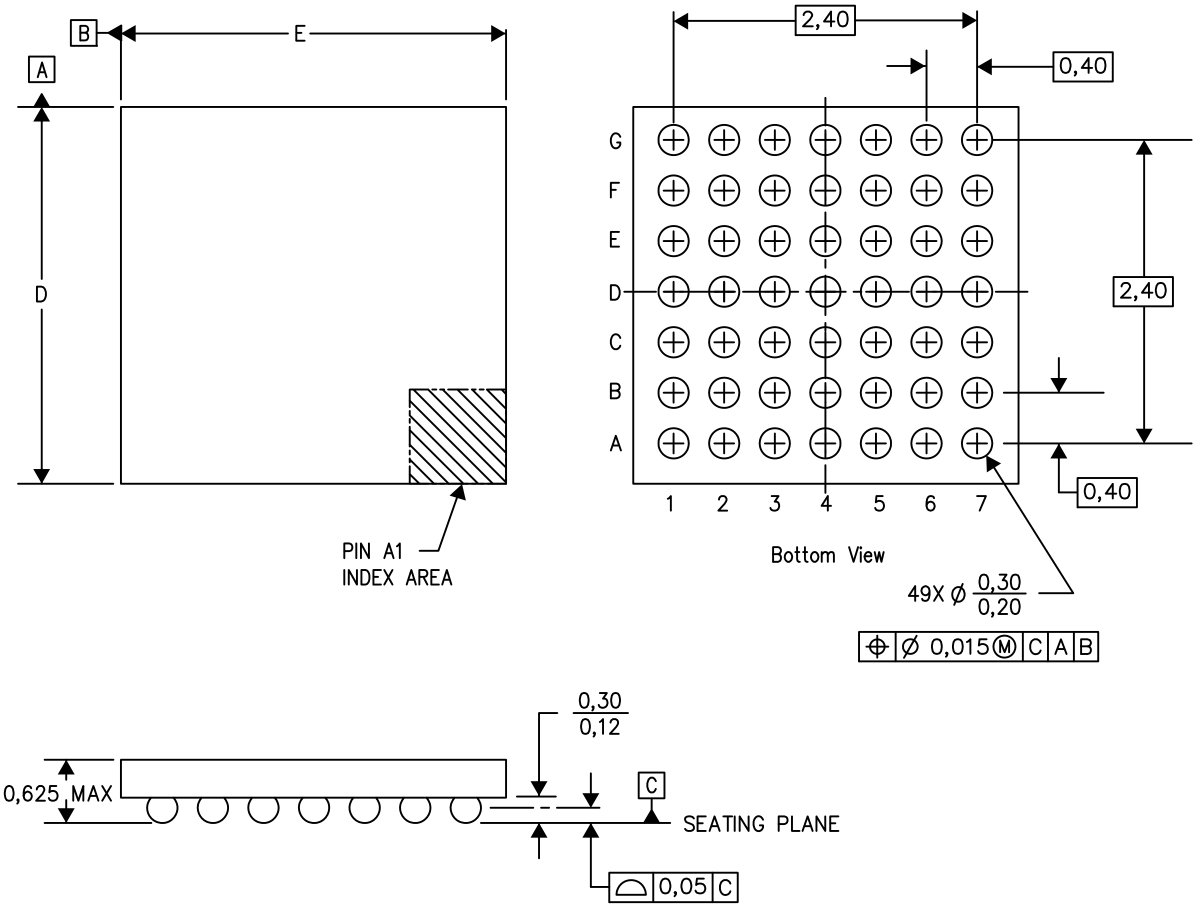
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TWL1200YFFR	DSBGA	YFF	49	3000	182.0	182.0	20.0
TWL1200ZQCR	BGA MICROSTAR JUNIOR	ZQC	48	2500	336.6	336.6	28.6

YFF (R–XBGA–N49) DIE–SIZE BALL GRID ARRAY

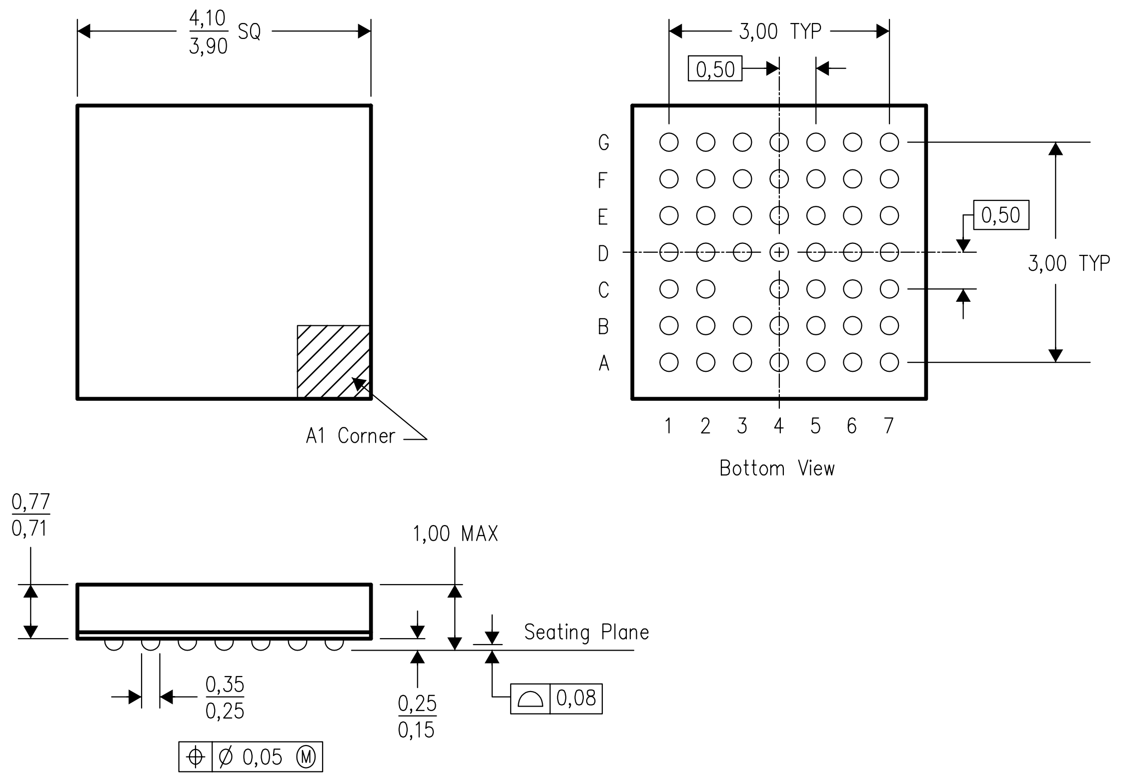


4207625–16/A0 12/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

ZQC (S–PBGA–N48) PLASTIC BALL GRID ARRAY



4204659/A 09/02

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar Junior™ BGA configuration
- D. Falls within JEDEC MO–225
- E. This package is lead–free.

MicroStar Junior is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2016, Texas Instruments Incorporated