

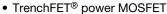
www.vishay.com

Vishay Siliconix

# N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (TYP.)			
100	0.0260 at V <sub>GS</sub> = 10 V	35	31 nC			
100	0.0375 at V <sub>GS</sub> = 7 V	31	31110			

# **FEATURES**



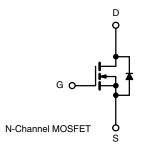


• Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



# **APPLICATIONS**

· Primary side switch





TO-252

#### **Ordering Information:**

SUD35N10-26P-E3 (lead (Pb)-free)

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V <sub>DS</sub>	100	v		
Gate-Source Voltage	V <sub>GS</sub>	± 20			
	T <sub>C</sub> = 25 °C		35		
Continuous Drain Current /T 175 °C)	T <sub>C</sub> = 70 °C		32		
Continuous Drain Current (T <sub>J</sub> = 175 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	12 <sup>b, c</sup>	1	
	T <sub>A</sub> = 70 °C		10 <sup>b, c</sup>		
Pulsed Drain Current	I <sub>DM</sub>	40	A		
Continuous Courses Dunis Diada Coursest	T <sub>C</sub> = 25 °C		50 e		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	l <sub>S</sub> —	6.9 b, c		
Avalanche Current Pulse	. 0.1	I <sub>AS</sub>	33		
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	55	mJ	
	T <sub>C</sub> = 25 °C		83		
Manian on David Disaination	T <sub>C</sub> = 70 °C		58	10/	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	8.3 b, c	W	
	T <sub>A</sub> = 70 °C		5.8 b, c		
Operating Junction and Storage Temperature R	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C		

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum Junction-to-Ambient b, d	t ≤ 10 s	$R_{thJA}$	15	18	°C/W		
Maximum Junction-to-Case	Steady State	$R_{thJC}$	1.5	1.8	0/00		

#### **Notes**

- a. Based on  $T_C$  = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- d. Maximum under steady state conditions is 50 °C/W.
- e. Calculated based on maximum junction temperature. Package limitation current is 50 A.



# Vishay Siliconix

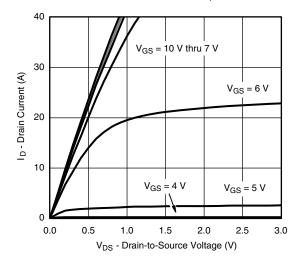
PARAMETER	SYMBOL TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100	-	-	V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 A	-	165	-	m\//°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-11	-	mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.5	-	4.4	٧	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μA	
Zero date voltage Drain Gunerit	DSS	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$	-	-	10	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	Α	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$	- 0.0210 0.026		0.0260	Ω	
2.4 354.00 011 014.0 1100.014.100	$V_{GS} = 7 \text{ V, } I_D = 8 \text{ A}$		-	0.0285	0.0375		
Forward Transconductance a	9fs	$V_{DS} = 15 \text{ V}, I_D = 12 \text{ A}$	-	25	-	S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			2000	-	pF	
Output Capacitance	Coss	$V_{DS} = 12 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	180	-		
Reverse Transfer Capacitance	C <sub>rss</sub>		-	60	-		
Total Gate Charge	$Q_g$		-	31	47	nC	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$	-	10	-		
Gate-Drain Charge	$Q_{gd}$		-	9	-		
Gate Resistance	$R_g$	f = 1 MHz	-	1.5	-	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>		-	10	15		
Rise Time	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, R_L = 5 \Omega$	-	10	15	ns	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	15	25		
Fall Time	t <sub>f</sub>		-	10	15		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	Is	T <sub>C</sub> = 25 °C	-	_	50		
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>		-	-	40	Α	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 10 A	-	0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>		-	50	75	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	100	150	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 10 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$		38	-		
Reverse Recovery Rise Time	t <sub>b</sub>		_	12	_	ns	

#### Note

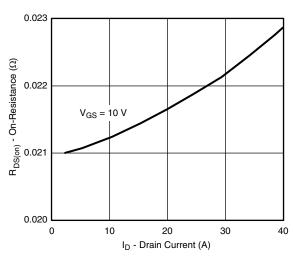
- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

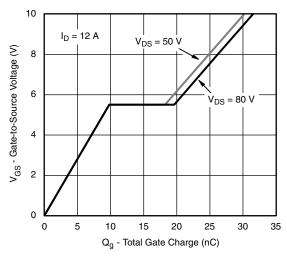




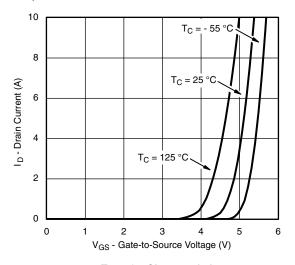
### **Output Characteristics**



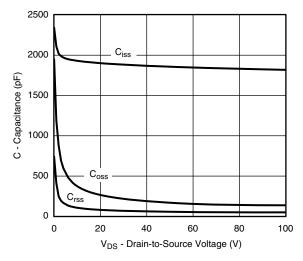
On-Resistance vs. Drain Current



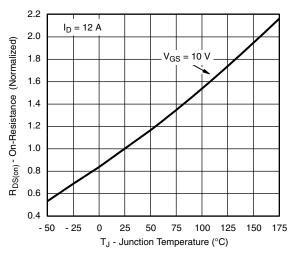
**Gate Charge** 



**Transfer Characteristics** 

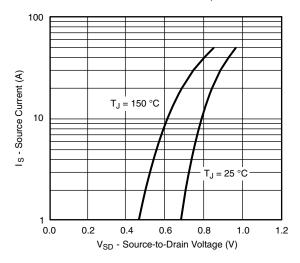


Capacitance

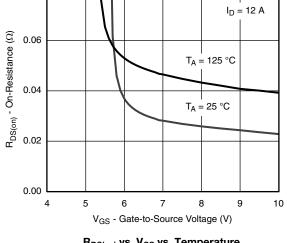


On-Resistance vs. Junction Temperature

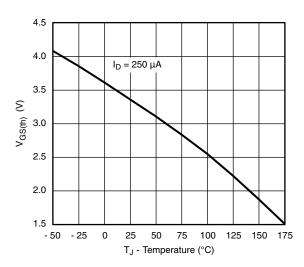




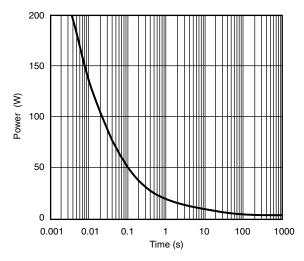
#### Source-Drain Diode Forward Voltage



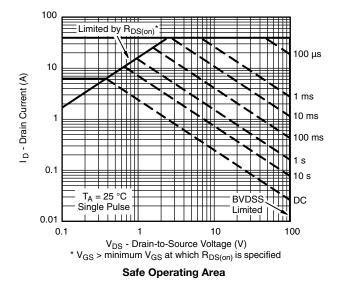
 $R_{DS(on)}$  vs.  $V_{GS}$  vs. Temperature



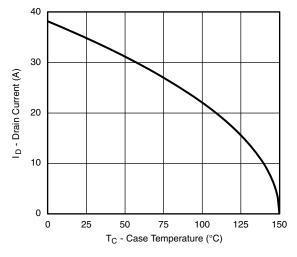
**Threshold Voltage** 

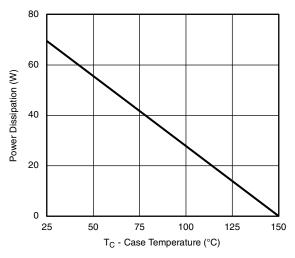


Single Pulse Power, Junction-to-Ambient









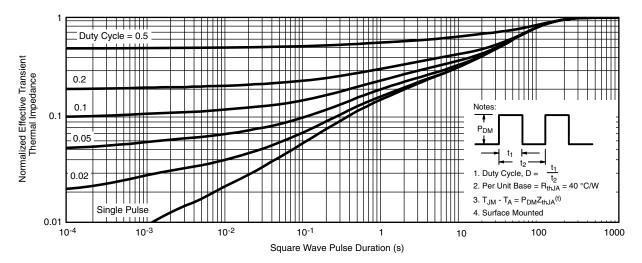
#### **Power Derating**

Current Derating a

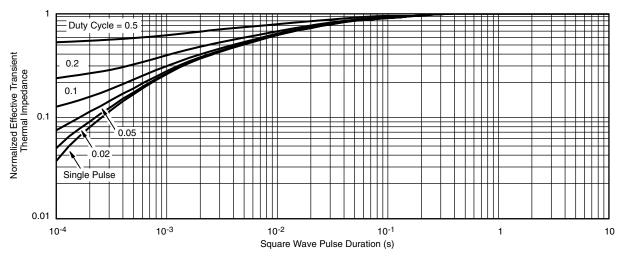
#### Note

a. The power dissipation  $P_D$  is based on  $T_J$  (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



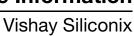


Normalized Thermal Transient Impedance, Junction-to-Ambient



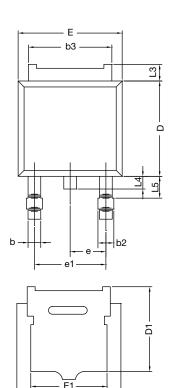
Normalized Thermal Transient Impedance, Junction-to-Case

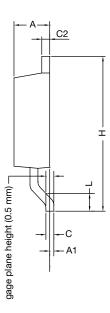
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?69796">www.vishay.com/ppg?69796</a>.





# **TO-252AA Case Outline**





	MILLIMETERS		INC	HES		
DIM.	MIN.	MAX.	MIN.	MAX.		
Α	2.18	2.38	0.086	0.094		
A1	-	0.127	-	0.005		
b	0.64	0.88	0.025	0.035		
b2	0.76	1.14	0.030	0.045		
b3	4.95	5.46	0.195	0.215		
С	0.46	0.61	0.018	0.024		
C2	0.46	0.89	0.018	0.035		
D	5.97	6.22	0.235	0.245		
D1	4.10	-	0.161	-		
Е	6.35	6.73	0.250	0.265		
E1	4.32	-	0.170	-		
Н	9.40	10.41	0.370	0.410		
е	2.28	BSC	0.090	BSC		
e1	4.56	BSC	0.180 BSC			
L	1.40	1.78	0.055	0.070		
L3	0.89	1.27	0.035	0.050		
L4	-	1.02	-	0.040		
L5	1.01	1.52	0.040	0.060		
ECN: T16-0236-Rev. P, 16-May-16						

ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347

# Notes

• Dimension L3 is for reference only.



# **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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