DATASHEET

Low Power Ambient Light-to-Voltage Nonlinear Converter

ISL29102

The ISL29102 is a low cost, light-to-voltage silicon optical sensor combining a photodiode array, a nonlinear current amplifier, and a micro-power op amp on a single monolithic IC. Similar to human eyes, the photodiode array has peak sensitivity at 550nm and spans from 400nm to 600nm, rejecting UV light and IR light. The input luminance range is from 0.3 lux to 10,000 lux.

The integrated nonlinear current amplifier boosts and converts the photodiode signal in a square root fashion, extending the light input dynamic range, while maintaining excellent sensitivity at dim conditions with low lux levels. The device consumes minimal power over a wide range of ambient lux levels because the current consumption ramps at a square root fashion. A dark-current compensation circuit minimizes the effect of temperature-dependent leakage currents in the absence of light, improving the light sensitivity at low lux levels while maintaining excellent sensitivity at low lux levels. The built-in 1µA op amp gives the ISL29102 an output voltage driving advantage for heavier loads.

The ISL29102 is housed in an ultra compact 2mmx2.1mm ODFN plastic case surface mount package. Operation is rated from -40°C to +85°C.

Related Literature

- For a full list of related documents, visit our website
  - ISL29102 product page

Features

- Square root voltage output
- 0.3 lux to 10,000 lux range
- 1.8V to 3.3V supply range
- Close to human eye spectral response
- Fast response time
- Internal temperature compensation
- Good IR rejection
- Low supply current
- Operating temperature range -40°C to +85°C
- 6 Ld ODFN: 2mmx2.1mmx0.7mm
- Pb-free (RoHS compliant)

Applications

- Display and keypad dimming for:
  - Mobile devices: smart phone, PDA, GPS
  - Computing devices: notebook PC, webpod
  - Consumer devices: LCD-TV, digital picture frame, digital camera
- Industrial and medical light sensing

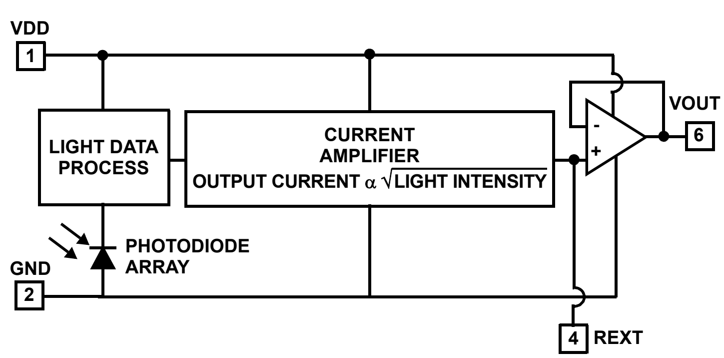


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM

Ordering Information

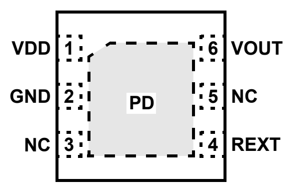
PART NUMBER (Notes 1, 2, 3)	TEMP RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL29102IROZ-T7	-40 to +85	3k	6 Ld ODFN	L6.2x2.1
ISL29102IROZ-T7A	-40 to +85	250	6 Ld ODFN	L6.2x2.1
ISL29102IROZ-EVALZ		Evaluation Board		

NOTES:

1. Refer to TB347 or details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see device information page for ISL29102. For more information on MSL, see techbrief TB363.

Pin Configuration

ISL29102
(6 LD ODFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VDD	Supply (1.8V to 3.3V).
2	GND	Ground
3	NC	No connect
4	REXT	Connected to an external resistor to GND setting the light-to-voltage scaling constant.
5	NC	No connect
6	VOUT	Voltage Output
-	PD	Thermal pad. Thermal pad can be connected to GND or electrically isolated.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage Between VDD and GND 3.6V
R_{EXT} . . . . (-0.5V + GND) to (0.5V + V_{DD})
V_{OUT} . . . . (-0.5V + GND) to (0.5V + V_{DD})
V_{OUT} Short-Circuit Current . . . . <10mA
ESD Rating
Human Body Model 3kV
Machine Model 300V

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W)
6 Ld ODFN (Note 4) 88
Maximum Die Temperature . . . . +90°C
Storage Temperature . . . . -40°C to +100°C
Operating Temperature . . . . -40°C to +85°C
Pb-Free Reflow Profile (*) . . . . see TB477
*Peak temperature during solder reflow +235°C max

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

Electrical Specifications V_{DD} = 3V, T_A = +25°C, R_{EXT} = 100kΩ, no load at V_{OUT}, green LED light, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITION	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
E	Range of Input Light Intensity for Square Root Relationship to be Held			0.3 - 10k		Lux
V_{DD}	Operating Supply Voltage		1.8		3.3	V
I_{DD}	Supply Current	E = 0 lux		0.65		µA
		E = 100 lux		3.5		µA
		E = 1,000 lux		10	15	µA
V_{OUT0}	Light-to-Voltage Accuracy	E = 100 lux		0.185		V
V_{OUT1}	Light-to-Voltage Accuracy	E = 1000 lux	0.460	0.580	0.680	V
V_{DARK}	Voltage Output in the Absence of Light	E = 0 lux, R_{EXT} = 10MΩ		20	50	mV
ΔV_{OUT}	Output Voltage Variation Over Three Light Sources: Fluorescent, Incandescent, and Halogen			10		%
PSRR	Power Supply Rejection Ratio	E = 100 lux, VDD = 1.8V to 3.6V		2.5		mV/V
$V_{O\text{-}CMPL}$	Maximum Output Compliance Voltage at 95% of Nominal Output			V_{DD} - 0.7V		V
$V_{O\text{-}MAX}$	Maximum Output Voltage Swing				V_{DD}	V
t_R	Rise Time	E = 0 lux to 300 lux		68		µs
		E = 0 lux to 1000 lux		68		µs
t_F	Fall Time	E = 300 lux to 0 lux		1830		µs
		E = 1000 lux to 0 lux		970		us
t_D	Delay Time for Rising Edge	E = 0 lux to 300 lux		352		µs
		E = 0 lux to 1000 lux		145		µs
t_S	Delay Time for Falling Edge	E = 300 lux to 0 lux		22		µs
		E = 1000 lux to 0 lux		22		µs
ISC	Short Circuit Current of Op Amp			±11		mA
SR	Slew Rate of Op Amp			±10		V/ms
VOS	Offset Voltage of Op Amp			±1.2		mV

NOTE:

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

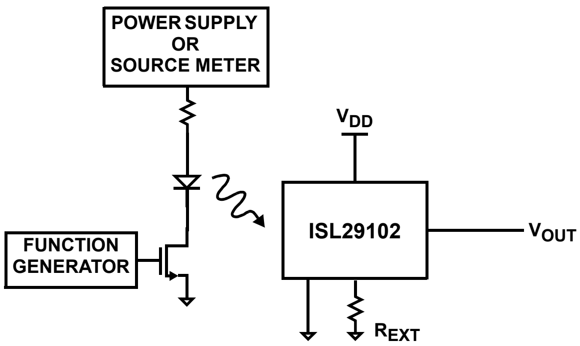


FIGURE 2. TEST CIRCUIT FOR RISE/FALL TIME MEASUREMENT

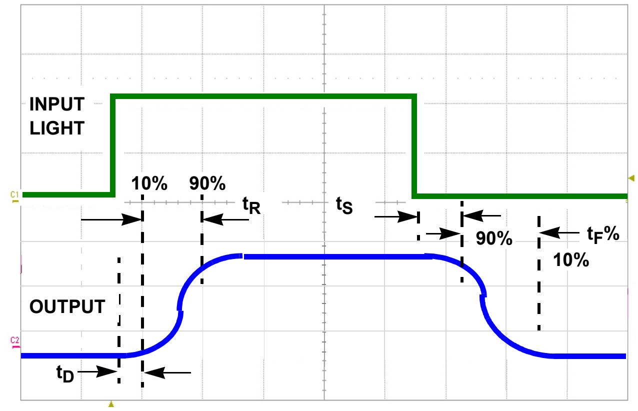


FIGURE 3. TIMING DIAGRAM

Typical Performance Curves

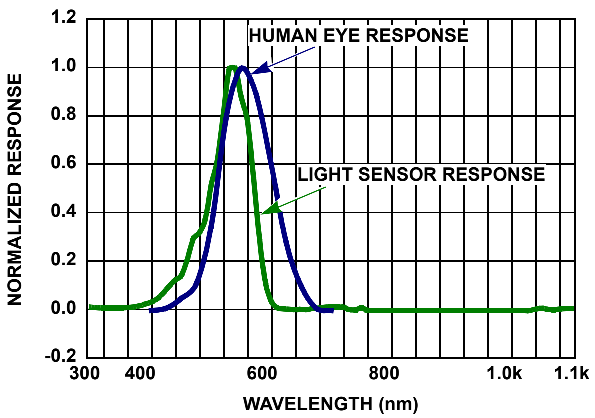


FIGURE 4. SPECTRAL RESPONSE

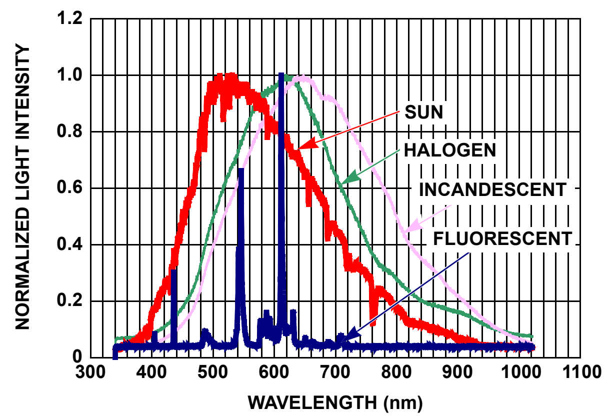


FIGURE 5. SPECTRUM OF LIGHT SOURCES

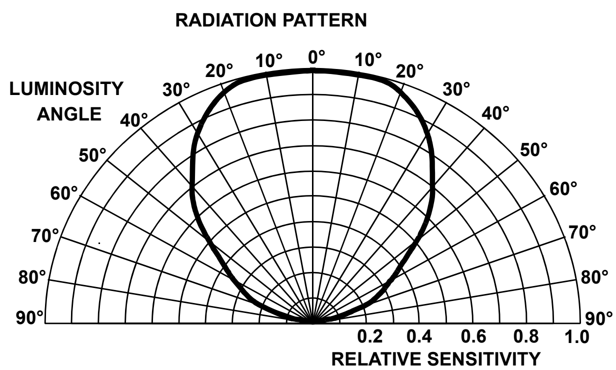


FIGURE 6. RADIATION PATTERN

Typical Performance Curves (Continued)

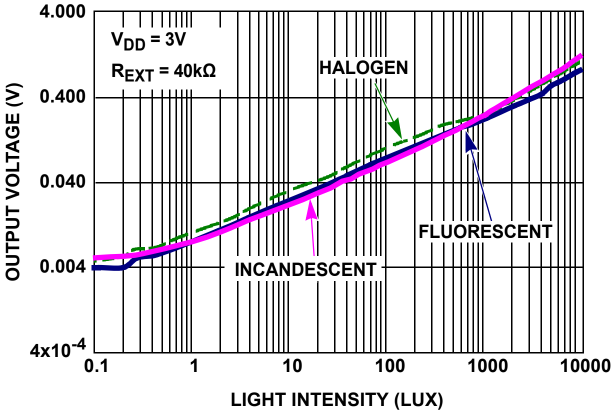


FIGURE 7. OUTPUT VOLTAGE vs LIGHT INTENSITY

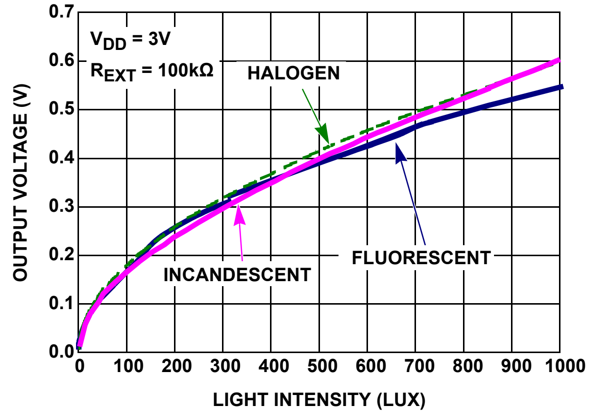


FIGURE 8. OUTPUT VOLTAGE vs LIGHT INTENSITY

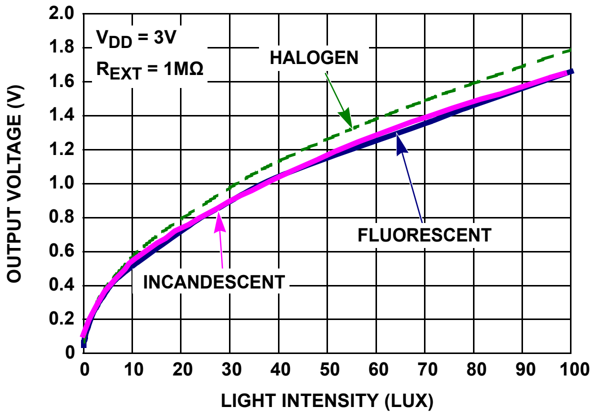


FIGURE 9. OUTPUT VOLTAGE vs LIGHT INTENSITY

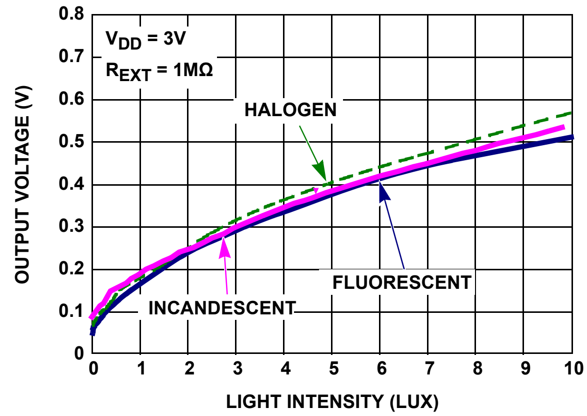


FIGURE 10. OUTPUT VOLTAGE vs LIGHT INTENSITY

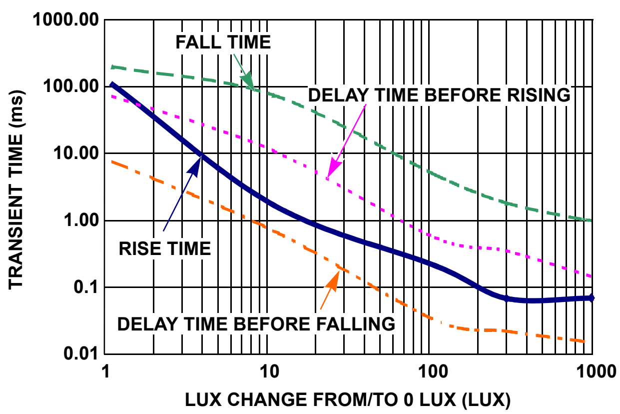


FIGURE 11. TRANSIENT TIME vs LUX CHANGE FROM/TO 0 LUX

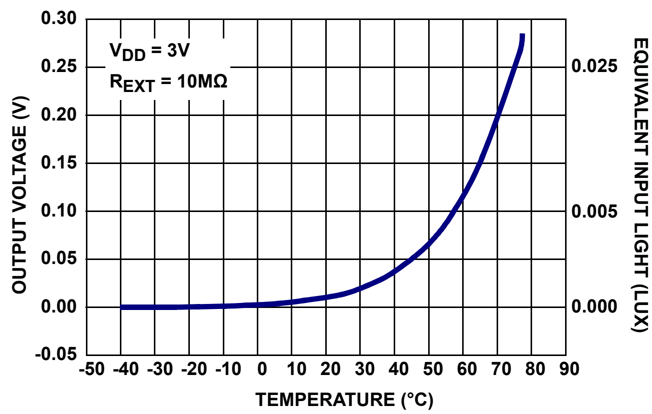


FIGURE 12. OUTPUT VOLTAGE vs TEMPERATURE AT 0 LUX

Typical Performance Curves (Continued)

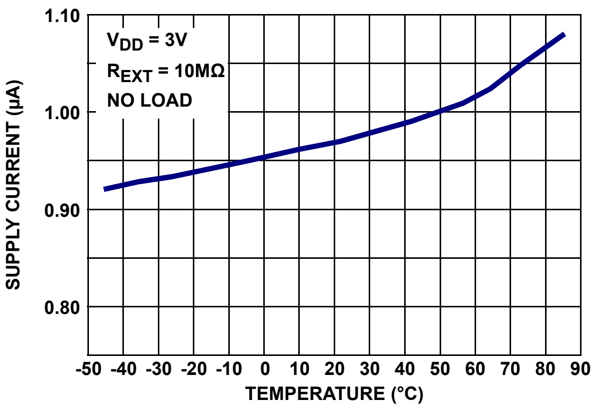


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE AT 0 LUX

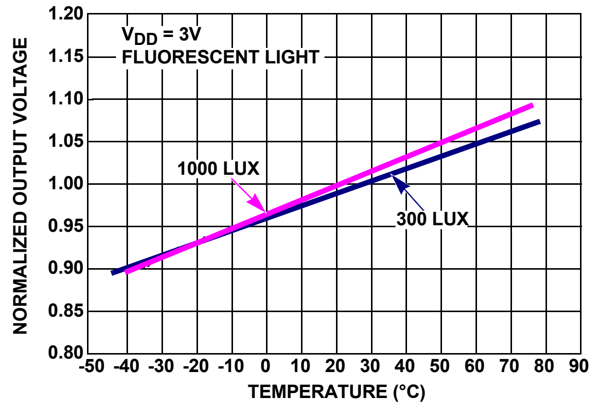


FIGURE 14. NORMALIZED OUTPUT VOLTAGE vs TEMPERATURE

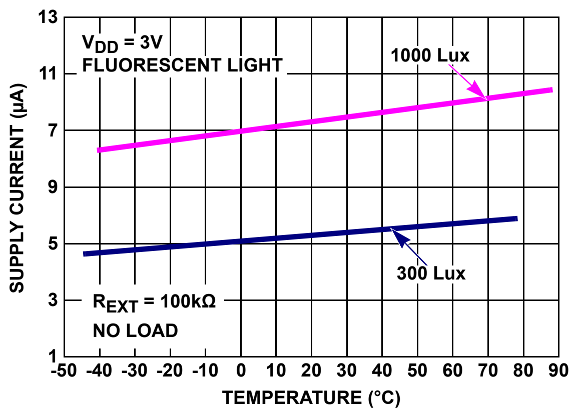


FIGURE 15. SUPPLY CURRENT vs TEMPERATURE

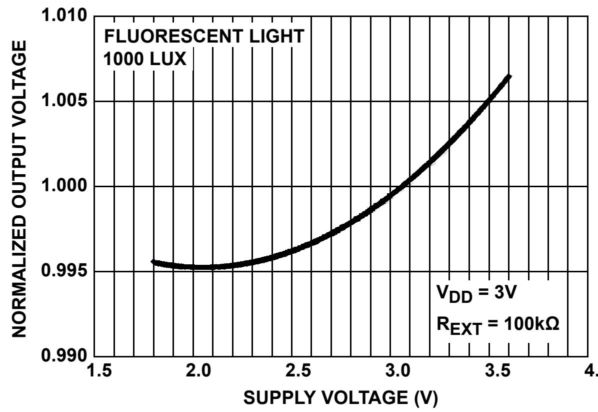


FIGURE 16. NORMALIZED OUTPUT VOLTAGE vs SUPPLY VOLTAGE

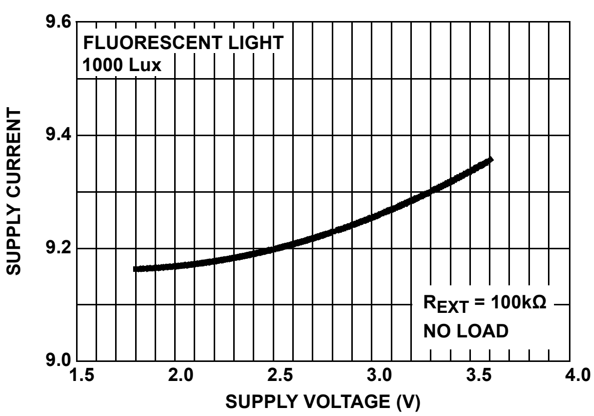


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

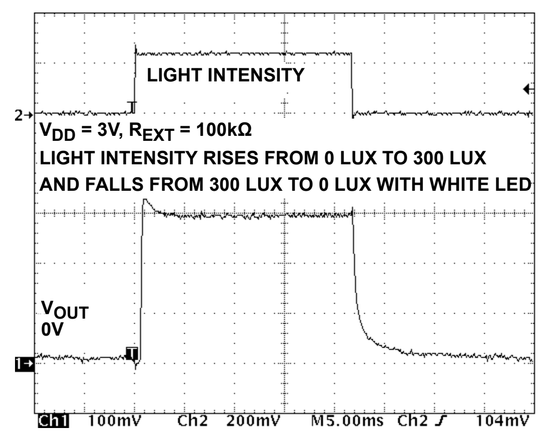


FIGURE 18. TRANSIENT RESPONSE OF ISL29102 TO CHANGE IN LIGHT INTENSITY

Application Information

Light-to-Voltage Conversion

The ISL29102 has responsiveness that is a square-root function of the light intensity intercepted by the photodiode in lux. Because the photodiode has a responsivity that resembles the human eye, conversion rate is independent of the light source (fluorescent light, incandescent light, or direct sunlight).

$$V_{OUT} = \frac{1.8\mu A}{\sqrt{100lux}}\sqrt{E} \times R_{EXT} \quad \text{(EQ. 1)}$$

In Equation 1, V_{OUT} is the output voltage, E is the light intensity, and R_{EXT} is the value of the external resistor. The R_{EXT} is used to set the light-to-voltage scaling constant. The compliance of the ISL29102's output circuit may result in premature saturation when an excessively large R_{EXT} is used. The output compliance voltage is 700mV below the supply voltage as listed in $V_{O\text{-}MAX}$ of the “Electrical Specifications” table on page 3.

Optical Sensor Location Outline

The green area in Figure 19 shows the optical sensor location outline of ISL29102. Along the pinout direction, the center line (CL) of the sensor coincides with that of the packaging. The sensor width in this direction is 0.39mm. Perpendicular to the pinout direction, the CL of the sensor has an 0.19mm offset from the CL of packaging away from pin 1. The sensor width in this direction is 0.46mm.

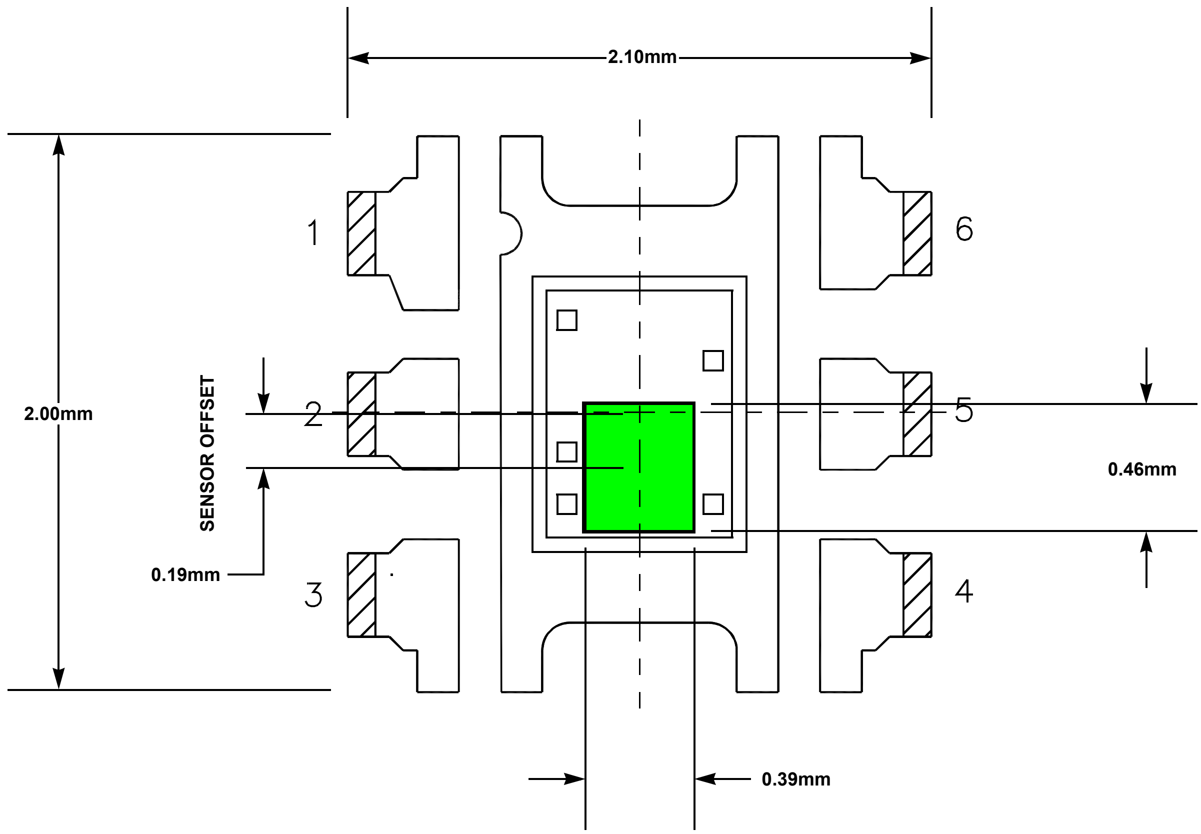


FIGURE 19. 6 LD ODFN SENSOR LOCATION OUTLINE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
November 17, 2016	FN6483.2	• Updated datasheet to new standards. • Moved Ordering Information table to page 2. Added ISL29102IROZ-T7A. • Removed Important note above Electrical spec table and added Note 5. • Updated POD from rev 2 to rev 4. Changes were: Added “MAX 0.75” dimension to Side View Changed Note 5 From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and maybe located on any of the 4 sides (or ends). Updated Arrows to correct arrow type.
December 12, 2008	FN6483.1	Added MSL Note 3 to “Ordering Information” to page 2. Corrected Eval board name from ISL29102IROZEVALZ to ISL29102IROZ-EVALZ in “Ordering Information” on page 2. Added “Related Literature” on page 1 per new data sheet standards. Updated Theta JA in “Thermal Information” on page 3 from 90C/W to 88C/W per ASYD in Intrepid. Added Note 4. Revised VO-MAX spec in “Electrical Specifications” table on page 3 from: Description: Maximum Output Compliance voltage at 95% of nominal output TYP: VDD - 0.7V To: Description: Maximum Output Voltage Swing TYP: removed (was VDD - 0.7V) MAX: added "VDD" Added new spec to “Electrical Specifications” table on page 3 as follows: VO-CMPL Description: Maximum Output Compliance voltage at 95% of nominal output TYP: VDD - 0.7V Updated package outline drawing L6.2x2.1 on page 9 to most recent revision. Changes to POD were: Changing the way we dimension the solder pad recommendation on the PODs. Changes inc: Bottom View: Added dimension callouts for solder pad Land Pattern: Added package outline and package outline dimensions. Added lead width of 6x0.30±0.05 and note 4 callout to bottom view Increased the size of the pin 1 shaded area Added “Revision History” on page 8 & “Products” on page 8 per new data sheet standards.
July 1, 2008	FN6483.0	Initial release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

For additional products, see www.intersil.com/en/products.html

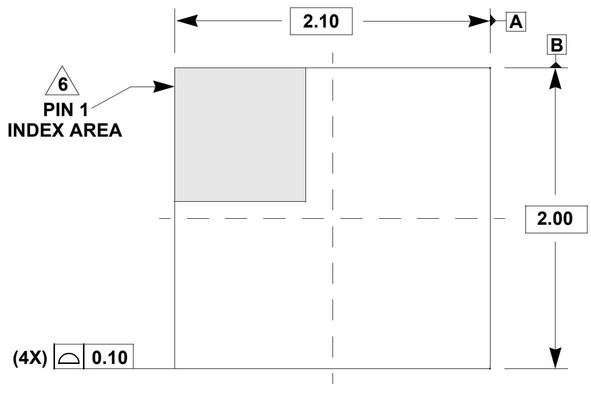
Package Outline Drawing

For the most recent package outline drawing, see L6.2x2.1.

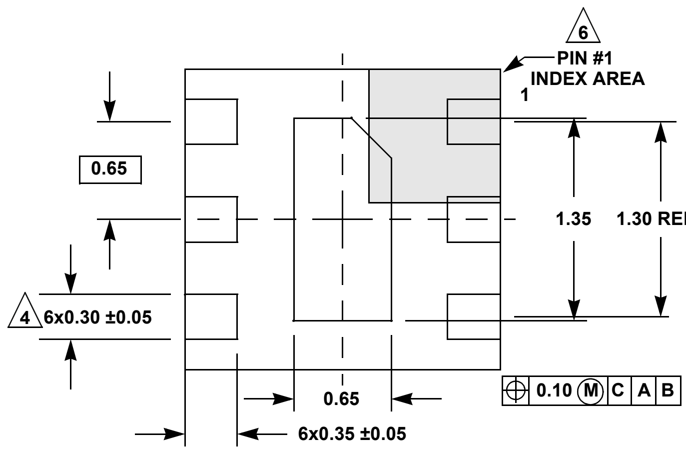
L6.2x2.1

6 LEAD OPTICAL DUAL FLAT NO-LEAD PLASTIC PACKAGE (ODFN)

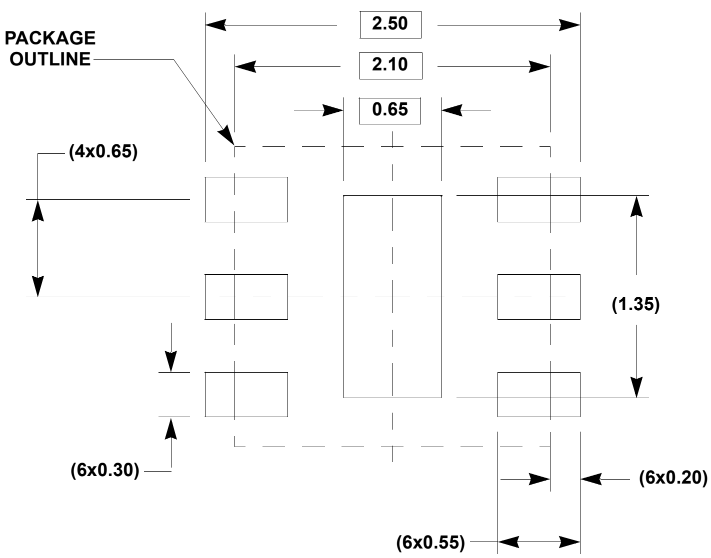
Rev 4, 2/15



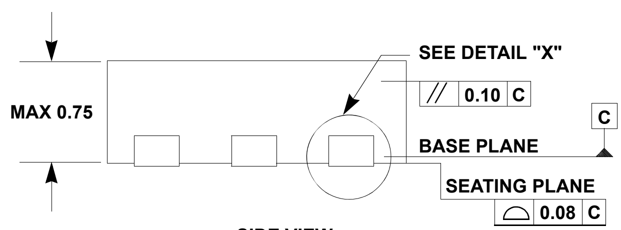
TOP VIEW



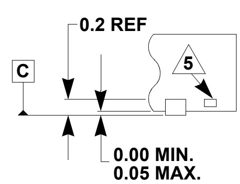
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and maybe located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.