PCA24S08A

1024 × 8-bit CMOS EEPROM with access protection

Rev. 01 — 19 January 2010 Product data sheet

1. General description

The PCA24S08A provides 8192 bits of serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 1024 words of 8 bits each. Data bytes are received and transmitted via the serial I^2C-bus.

Access permissions limiting reads or writes are set via the I^2C-bus to isolate blocks of memory from improper access.

The PCA24S08A is intended to be pin compatible with standard 24C08 serial EEPROM devices except for pins 1, 2, and 3, which are address pins in the standard part. Other exceptions to the PCA24S08A serial EEPROM data sheet are noted in Section 6.6.

All bits are sent to or read from the device, most significant bit first, in a manner consistent with the 24C08 serial EEPROM. The bit fields in this document are correspondingly listed with the MSB on the left and the LSB on the right.

The EEPROM memory is broken up into 8 blocks of 1 kbit (128 bytes) each. Within each block, the memory is physically organized in to 8 pages of 128 bits (16 bytes) each. In addition to these 8 kbits, there are two more 128-bit pages that are used to store the access protection and ID information. There are a total of 8448 bits of EEPROM memory available in the PCA24S08A.

Access protection (both read and write) is organized on a block basis for block 1 through block 7 and on a page and a block basis for block 0. Protection information for these blocks and pages is stored in one of the additional pages of EEPROM memory that is addressed separately from the main data storage array. SeeSection 6.4 for more details.

The ID value is located in the ID page of the EEPROM, the second of the additional 16 byte pages.

Writes from the serial interface may include from one byte to 16 bytes at a time, depending on the protocol followed by the bus master. All page accesses must be properly aligned to the internal EEPROM page.

The EEPROM memory offers an endurance of 100,000 write cycles per byte, with 10 year data retention. Writes to the EEPROM take less than 5 ms to complete.

After manufacturing, all EEPROM bits will be set to a value of ‘1’.

2. Features

- Non-volatile storage of 8 kbits organized as 8 blocks of 128 bytes each
- I^2C-bus interface logic
- Compatible with 24C08 serial EEPROM, and alternate source of Atmel AT24RF08C without the RF interface
- Write operation:
  - Byte write mode
  - 16-byte page write mode
- Read operation:
  - Sequential read
  - Random read
- Programmable access protection to limit reads and writes
- Lock/unlock function
- Write protect feature protecting the full memory array against write operations
- Self timed write cycle
- Internal power-on reset
- High reliability:
  - Ten years non-volatile data retention time
  - 100,000 write cycle endurance
- Low power CMOS technology
- Operating power supply voltage range of 2.5 V to 3.6 V
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8

3. Ordering information

Table 1. Ordering information

T_{amb} = −40 °C to +85 °C

Type number	Topside mark	Package		
		Name	Description	Version
PCA24S08AD	P24S08A	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA24S08ADP	PS08A	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

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4. Block diagram

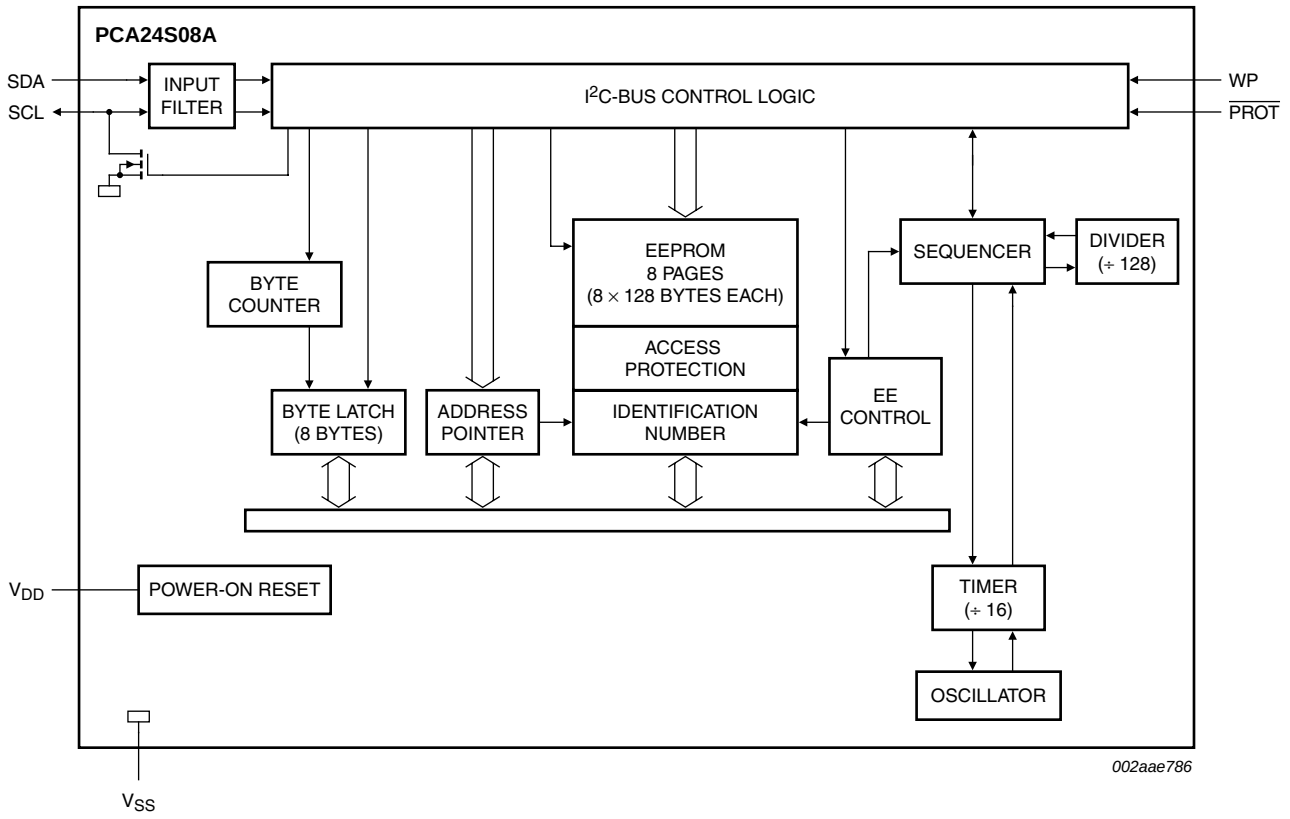

Fig 1. Block diagram

5. Pinning information

5.1 Pinning

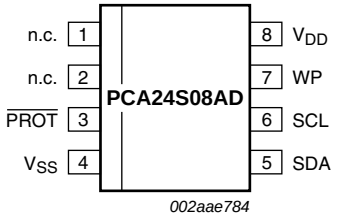

Fig 2. Pin configuration for SO8

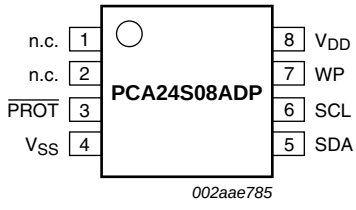

Fig 3. Pin configuration for TSSOP8

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5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
n.c.	1, 2	not connected
$\overline{PROT}$	3	active LOW protect reset input
V_{SS}	4	ground supply voltage
SDA	5	serial data; open-drain I/O
SCL	6	serial clock; open-drain input
WP	7	active HIGH write protect input
V_{DD}	8	supply voltage

6. Functional description

Refer to Figure 1 “Block diagram”.

6.1 Device addressing

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA24S08A is shown in Figure 4.

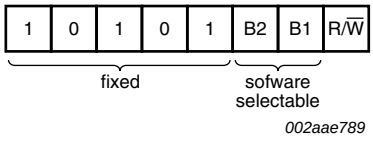

Fig 4. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected, while logic 0 selects a write operation. Bits B2 and B1 in the slave address represent the 2 most significant bits of the word to be addressed. The third device address bit in the I^2C-bus protocol that is usually matched to A2 (pin 3) on a standard 24C08 serial EEPROM is internally connected HIGH, so device addresses A8h through AFh (hex) are used to access the memory on the chip.

6.2 Write operations

Write operations on the device can be performed only when WP is held LOW. When the WP pin is held HIGH, content of the full memory is protected (Block 0 to Block 7, APP registers, ID Page), and no write operation is allowed.

6.2.1 Byte/word write

Write command may be used to set the address for a subsequent Read command. For a write operation, the PCA24S08A requires a second address field. The address field associated with the two software selectable bits in the slave address is a word address providing access to the 1024 bytes of memory, as shown in Figure 5. Upon receipt of the word address, the PCA24S08A responds with an acknowledge and awaits the next 8 bits of data, again responding with an acknowledge. Word address is automatically incremented.

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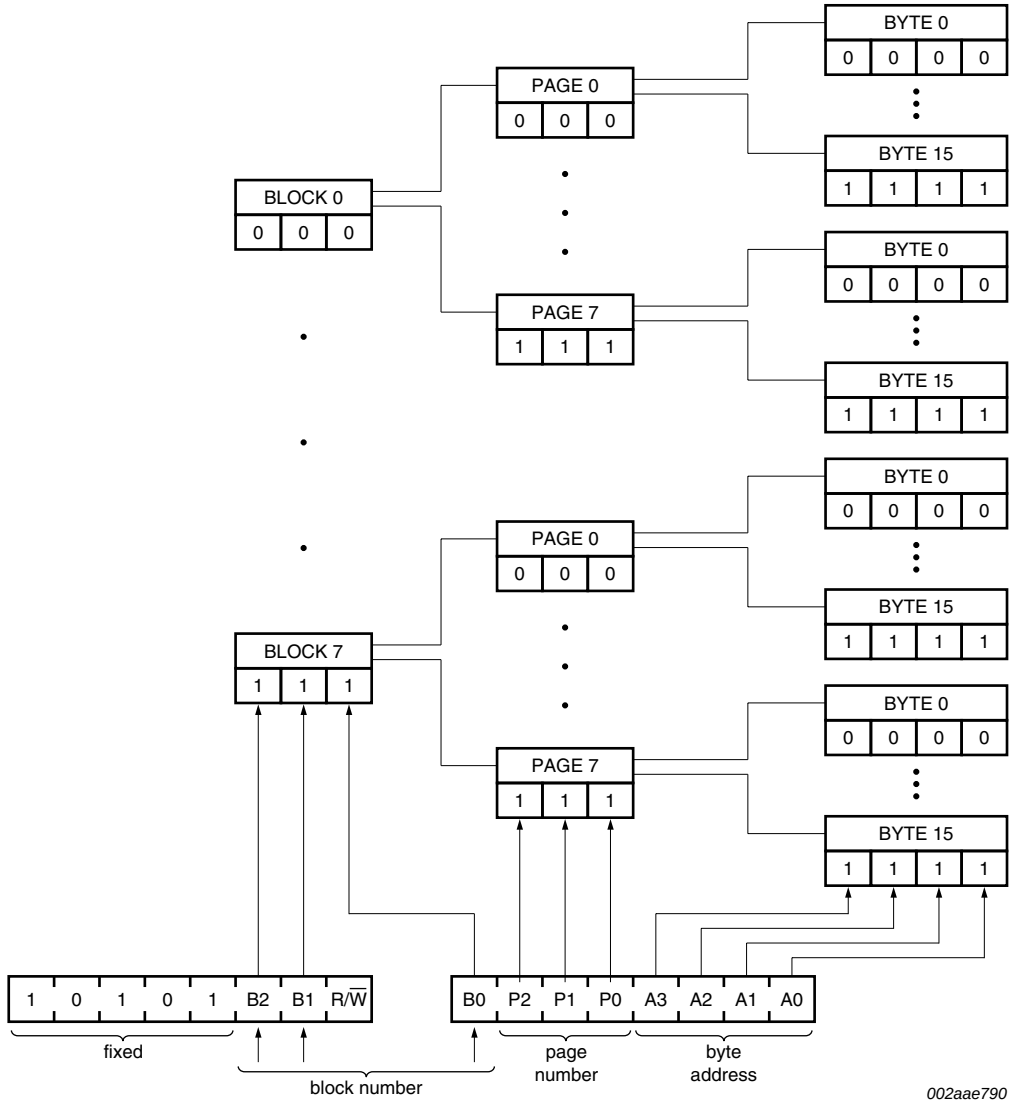

Fig 5. Memory addressing

Figure 6 shows how the memory array is addressed when the slave address byte and address field byte are sent. The master terminates the transfer by generating a STOP condition. After this STOP condition, the Erase/Write (E/W) cycle starts and the I^2C-bus is free for another transmission. Up to 16 bytes of data can be written in the slave writing sequence (E/W cycle).

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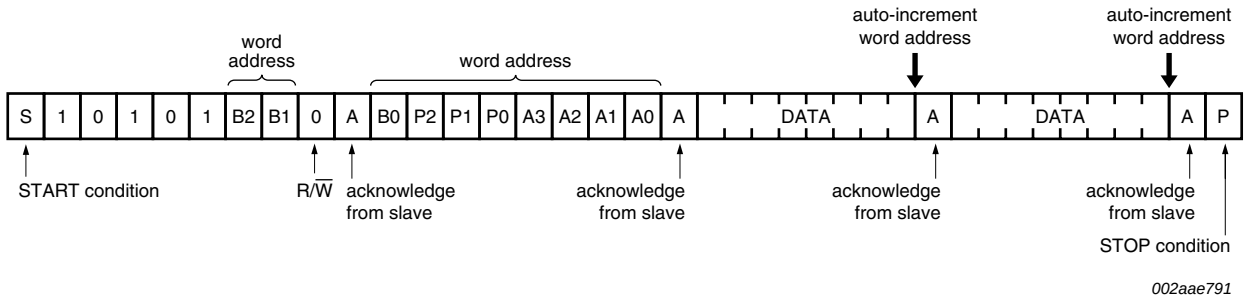

Fig 6. Auto-increment memory word address (2 byte write)

The general command encoding used by the serial port for EEPROM accesses is shown in Figure 11, where B[2:0] is the block number, P[2:0] is the page number within the block and A[3:0] is the byte address within the page. Bits denoted as 'X' are ignored by the device.

6.2.2 Page write

The PCA24S08A is capable of a 16-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transit 16 data bytes within one transmission. After receipt of each byte, the PCA24S08A will respond with an acknowledge. The typical E/W time in this mode is 5 ms.

After the receipt of each data byte, the four low-order bits of the word address are internally incremented. The six high-order bits of the address remain unchanged. The slave acknowledges the reception of each data byte with an ACK. The I^2C-bus data transfer is terminated by the master after the 16^{th} byte of data with a STOP condition. After a write to the last byte in a page, the internal address is wrapped around to point to the beginning of that page. If the master transmits more than 16 bytes prior to generating the STOP condition, no acknowledge will be given on the 17^{th} (and following) data bytes and the whole transmission will be ignored and no programming will be done. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

After this STOP condition, the E/W cycle starts and the I^2C-bus is free for another transmission.

During the E/W cycle the slave receiver does not acknowledge if addressed via the I^2C-bus.

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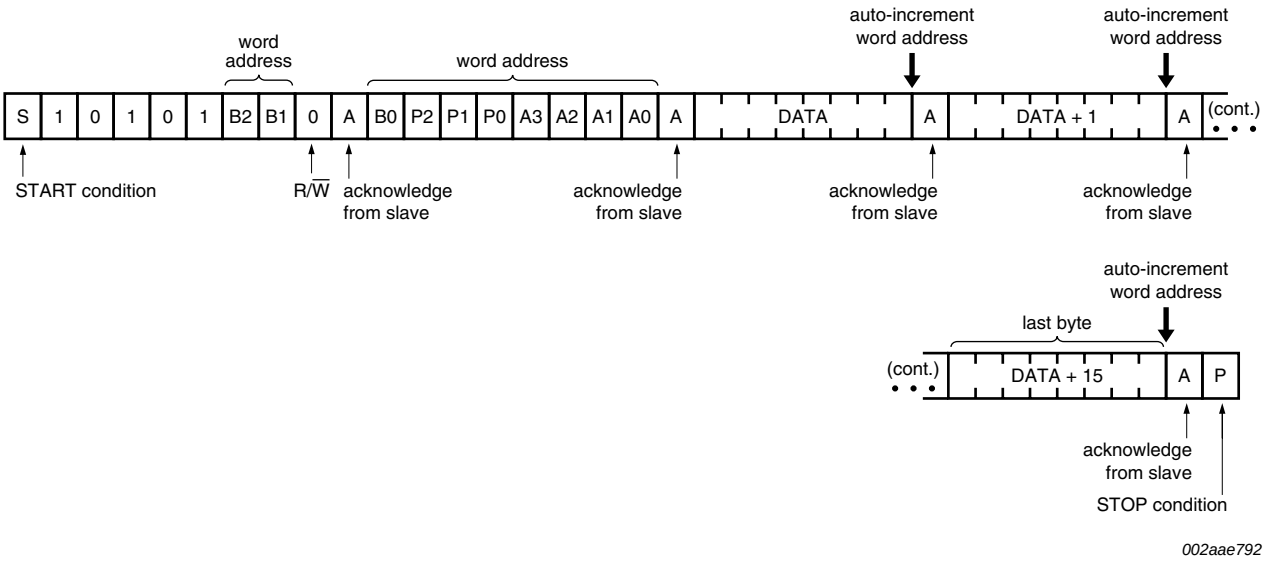

Fig 7. Page write operation (16 bytes)

6.3 Read operations

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1.

The lower 7 bits of the word address are incremented after each transmission of a data byte during a read. The three MSBs of the word address are not changed when the word counter overflows. Thus, the word address overflows from 127 to 0, and from 255 to 128.

After the read of the last byte within a block, the internal serial address wraps around to point at the beginning of that block.

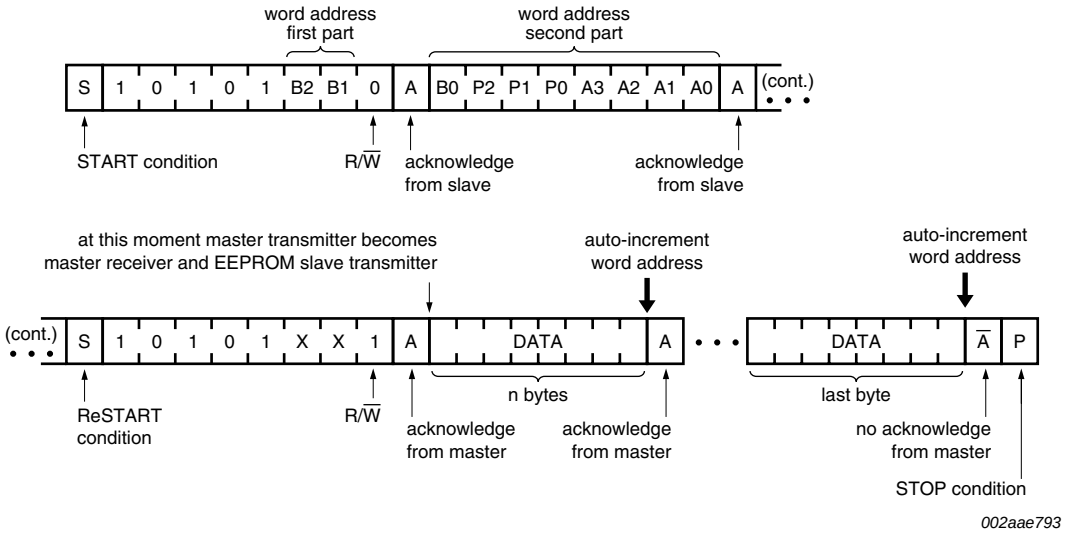

Fig 8. Master reads PCA24S08A slave after setting word address (write word address: read data); sequential read

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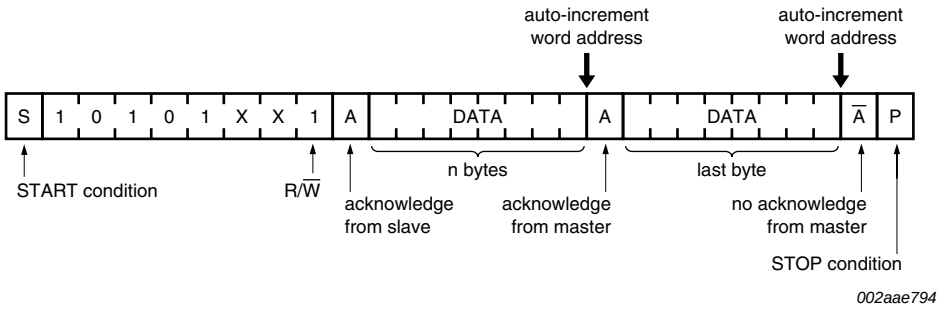

Fig 9. Master read PCA24S08A immediately after first byte (read mode); current address read

6.4 Access protection

Write operation on the Access protection registers can be performed when WP pin is LOW. If the WP pin is HIGH, all write operations are prohibited from the serial port, although write commands may be used to set the address for a subsequent read command.

All access protection bits are stored on a separate page of the EEPROM that is not accessed using the normal commands of a PCA24S08A memory. See Section 6.4.2.2 "Access Protection Page (APP)" for more detail on this information.

6.4.1 RFID access fields (RF)

Even though the PCA24S08A does not have the RFID capability, RFID access fields (RF) can be stored in order to keep existing software compatibility. The fields are stored in the EEPROM and organized as shown in Table 3.

Table 3. RFID access field organization

MSB	LSB	Function
0	0	no accesses permitted from RFID port
0	1	no accesses permitted from RFID port
1	0	read only from RFID port
1	1	no restrictions for RFID accesses

6.4.2 Protection bits (PB)

The protection bits fields in the Access Protection Page determine what type of accesses will be permitted via the serial port for each of the blocks on the chip. If an illegal access is attempted, the command will be NACKed. The MSB (if clear) prohibits all access to the block, and the LSB (if clear) prohibits writes. The fields are stored in the EEPROM and are organized as shown in Table 4.

Table 4. PB organization

MSB	LSB	Function
0	0	no accesses permitted in the block
0	1	no accesses permitted in the block
1	0	read only; writes cause a NACK
1	1	read/write; no access constraints for data within this block

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Accessed within the Access Protection Page is an individual CMOS Sticky Bit (SB) for each of the 8 blocks on the device. When the value of the sticky bit is '0', the Protection Bits (PB) for the corresponding block may not be changed via the software. These bits are all set to logic 1 when power is initially applied or when the $\overline{\text{PROT}}$ pin is LOW. These sticky bits may be written only to a '0' via the serial interface using the standard serial write operations. Reading the sticky bits does not affect their state.

Because permissions are set individually for each of the blocks, all reads via serial port will only read bytes within the block that was specified when the current address was latched in the device (with a write command). The block address bits (B2 or B1) that are sent with the write command are ignored on a read command.

When a sticky bit is cleared (programmed at 0), the byte containing the sticky bit cannot be changed anymore. If a write operation to this byte is attempted, it will be normally acknowledged but no change will happen in the byte value. The device does not go to an E/W cycle and can be accessed immediately.

If a block is protected and only read operation is allowed (the corresponding APP register has its PB bits programmed to 10b), a write operation to this block is not acknowledged (Slave Address and Register pointer only are acknowledged). The device does not go to an E/W cycle and can be accessed immediately.

S – Addr+W – ACK – Reg Pointer – ACK – Data – NACK

This applies to:

- EEPROM block 0 to block 7, controlled by PB0 to PB7.
- The last 7 bytes of the APP block (09h to 0Fh) and the ID page (10h to 1Fh) controlled by PBAP.

If a block is protected and neither read operation nor write operation is allowed (the corresponding APP register has its PB bits programmed to 00b or 01b), a write operation to this block is not acknowledged (Slave Address and Register pointer only are acknowledged).

S – Addr+W – ACK – Reg Pointer – ACK – Data – NACK

A read operation to this block is not allowed.

S – Addr+W – ACK – Reg Pointer – ACK – Sr – Addr+R – NACK

S – Addr+W – ACK – Reg Pointer – ACK – P – S – Addr+R – NACK

This applies to:

- EEPROM block 0 to block 7, controlled by PB0 to PB7.
- The last 7 bytes of the APP block (09h to 0Fh) and the ID page (10h to 1Fh) controlled by PBAP.

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6.4.2.1 Block 0 write protection bits

The PCA24S08A provides a mechanism to divide block 0 into eight 128-bit (16-byte) pages that can be individually protected against writes. These eight write protection (WPN) bits are stored within a byte of the access protection page and are organized such that the LSB protects the first 128 bits, and so on. If a bit in this byte is set to a one and the PB0 field is set to 11b, then writes are permitted on the page corresponding to the WPN bit. If the WPN bit is set to a logic 0 or the PB0 is any value other than 11b, then writes are not permitted in that page.

The Write Protection hierarchy for serial accesses is shown in Figure 10. In this drawing the bits within the boxes to the left of the arrows are the only thing that determine whether or not the bit in the box to the right of the arrow can be written. Read access control is not shown in this diagram. Addresses listed in this diagram are for the serial port assuming that the R/$\overline{W}$ bit in the command byte is set to '0'.

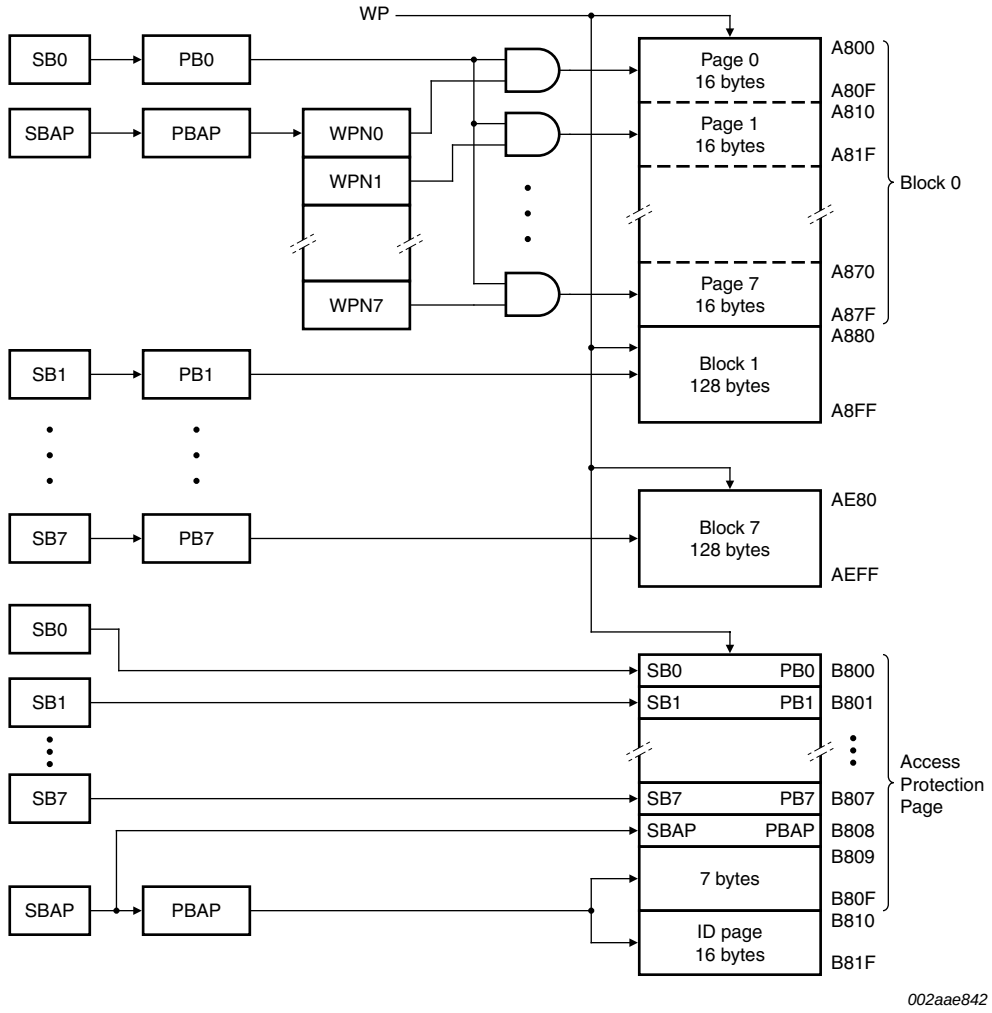

Fig 10. Write protection example

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For example, when SB1 is a 1, the PB1 field can be written to any value by the system. When the PB1 field is 11b, Block 1 can be written to by the system. Note that the state of the SB1 bit does not affect whether or not Block 1 can be written.

There is no individual page Write Protection for any other block other than block 0 within the device. Within the remaining blocks on the chip, access permissions are controlled on a block basis (BP bits) or full chip basis (WP pin) only.

6.4.2.2 Access Protection Page (APP)

The serial port may be used to read and write the Access Protection Page (APP) and ID Page using device access codes B8h and B9h instead of the normal value of A8h through AFh (hex) that are used to access the rest of the EEPROM memory. The second byte of write commands (the word address) should be in the range of 00h through 0Fh for the APP page and 10h through 1Fh for the ID page. This coding is shown in Figure 11.

Reads and writes to these two pages may take place on a single byte basis only. Multi-byte operations will be NACKed.

As an example, the bit encoding for a single byte read and write command are shown in Figure 11.

The PCA24S08A will acknowledge all device addresses of B8h or B9h. If the most significant three its of the word address are not all 0 (indicating an address outside the Access protection and ID pages), the chip will NACK the access.

Byte 0 through byte 7 of the APP contain 8 identical sets of access control fields (PBx and SBx) for each of the eight blocks of memory on the chip, which operate according to Table 4. When the sticky bit in one of these bytes is set, that byte can be written by the system. Once a sticky bit is reset (written to zero) by the software, the byte containing it can no longer be modified by the software until the next power cycle. These bytes can always be read by the system.

Byte 8 contains another PB field (PBAP) as bit 0 and bit 1, and an additional sticky bit (SBAP) as bit 7. The value of the PBAP bits controls read and write access to the last 7 bytes (byte 9 through byte 15) of the APP and all 16 bytes of the ID page according to the encoding listed in Section 6.4. The value of the PBAP bits can only be changed, a write from the serial port, when SBAP is HIGH. This byte can always be read by the system. Bit 0 through bit 6 of this byte are stored in EEPROM memory and do not change when the power is cycled or the $\overline{\text{PROT}}$ pin changes state.

Byte 9 contains the eight block 0 write protection bits (WPN) for each page within block 0.

Byte 10 emulates a coil detection feature to keep compatibility with existing software controlling device.

Even though the PCA24S08A does not have the RFID capability of the AT24RF03C, it gives a ‘coil non-detected’ information when the detection feature is initiated.

The detection feature uses the Detection Enable bit (DE) and the Detect Coil bit (DC). At power-up, DE = 0 and DC = 1. Detection is enabled by setting DE bit at 1. Since no coil is detected, DC is then automatically reset and equal to 0.

DE is a read/write bit; DC is a read-only bit. Attempts to write to this bit will be ignored.

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Bit 0 in the same byte emulates a TAMPER bit and is always equal to 0. TAMPER is a read-only bit. Attempt to write a ‘1’ to this bit will be ignored.

Byte 11 through byte 14 are currently reserved and should not be used by the system. Byte 14 may not be written by the device at any time.

Byte 11 to byte 13 are read/write bytes that are stored in the EEPROM.

Byte 14 is a read-only byte and the returned value during a read operation is FFh. A write on it is acknowledged, but the write will be ignored.

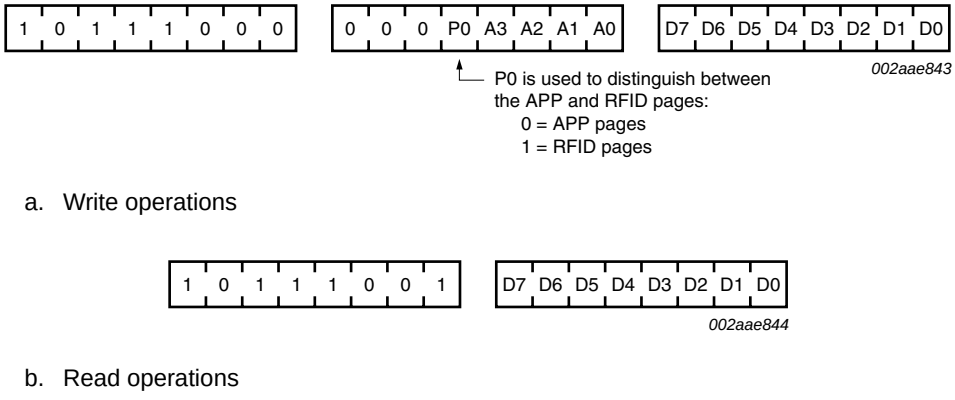

Fig 11. Device access examples

Byte 15 contains device revision information stored in the EEPROM. It is set at the wafer production facility and cannot be changed in the field, so any write to this byte will be ignored but acknowledged. The value of this byte is 10h.

The memory map for the Access Protection Page is shown in Table 5 “APP memory map”. In this table, an ‘X’ means that the value is a ‘Don’t care’ upon writing, and that it is undefined upon reading. The PB fields are all 2 bits wide, and the Device Revision field is 8 bits wide. All other fields are 1 bit wide.

With the exception of the 9 Sticky Bits (SB), the two coil detect bits (DE and DC), the tamper bit (TAMPER), and bytes 14 and 15, all bits within the Access Protection Page are stored in EEPROM memory. Their state does not change if power is removed or when the $\overline{\text{PROT}}$ pin is held LOW.

The following page of memory (accessed with A4 = 1) emulate the ID field that would be transmitted by the device from the RFID port. Bytes within it are accessed with the address byte at B8h or B9h (write/read). Reading and writing to this page is permitted when PBAP is 11.

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Table 5. APP memory map

X = 'Don't care' upon writing and undefined upon reading.

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SB0	X	RF0		X	X	PB0	
1	SB1	X	RF1		X	X	PB1	
2	SB2	X	RF2		X	X	PB2	
3	SB3	X	RF3		X	X	PB3	
4	SB4	X	RF4		X	X	PB4	
5	SB5	X	RF5		X	X	PB5	
6	SB6	X	RF6		X	X	PB6	
7	SB7	X	RF7		X	X	PB7	
8	SBAP	X	X	X	X	X	PBAP	
9	WPN7	WPN6	WPN5	WPN4	WPN3	WPN2	WPN1	WPN0
10	DE	DC	X	X	X	X	X	TAMPER
11	reserved; R/W							
12	reserved; R/W							
13	reserved; R/W							
14	reserved; read-only							
15	device revision							

6.5 $\overline{\text{PROT}}$ pin

The $\overline{\text{PROT}}$ pin is used as a power good signal. When this pin is held LOW, the serial port is held in reset and all sticky bits are set to one. When HIGH, activity on the serial bus is permitted and sticky bits can be set to their values.

6.6 Serial EEPROM exceptions

In general, the two-wire serial interface on the PCA24S08A functions identically to the 24C08. The following exceptions exist, as noted elsewhere in this document.

- Pins 1, 2, and 3 have different usage.
- Access to various blocks may be restricted via the access protection circuitry.
- The two block address bits (B2 and B1) in the command byte are ignored with all read commands. They are set only via the write command.
- Multi-byte reads do not cross block boundaries, but instead wrap to the beginning of the block.
- The serial port will be reset whenever the $\overline{\text{PROT}}$ pin is LOW.
- If more than 16 bytes are written to the EEPROM with a page write, overlapping bytes will have their values corrupted.
- If V_{DD} is 0 V, the device draws current on the SDA, SCL, WP, and $\overline{\text{PROT}}$ pins when they are brought above 0 V.

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7. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Functional operation under these conditions is not implied.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	with respect to ground	-	4.6	V
V_I	input voltage	SDA, SCL, $\overline{PROT}$, WP pins	–0.1 to V_{DD}	+0.3	V
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature		–40	+85	°C

8. Static characteristics

Table 7. Static characteristics

V_{DD} = 2.5 V to 3.6 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		2.5	-	3.6	V
I_{DD}	supply current	V_{DD} = 3.6 V; f_{SCL} = 100 kHz				
		EEPROM read	-	50	100	μA
		EEPROM write	-	0.325	1.0	mA
I_{stb}	standby current	V_{DD} = 3.6 V; SDA, SCL = V_{SS}	-	11.4	18	μA
$I_{I/O}$	input/output current	$\overline{PROT}$, SDA, SCL pins; $V_I = V_{DD}$ or V_{SS}	-	0.25	3.0	μA
I_I	input current	WP pin; $V_I = V_{DD}$ = 5.5 V	-	-	20	μA
V_{IL}	LOW-level input voltage		–0.1	-	$V_{DD} \times 0.3$	V
V_{IH}	HIGH-level input voltage		$V_{DD} \times 0.7$	-	V_{DD}	V
V_{OL}	LOW-level output voltage	I_{OL} = 2.1 mA	-	-	0.4	V
C_i	input capacitance	SCL, $\overline{PROT}$, WP not tested	-	-	6	pF
C_{io}	input/output capacitance	SDA not tested	-	-	8	pF

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9. Dynamic characteristics

Table 8. Dynamic characteristics

C_L = 1 TTL gate and 100 pF, except as noted. V_{DD} = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time			0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time		[1]	-	600	-	600	ns
$t_{VD;DAT}$	data valid time	LOW level	[2]	-	600	-	600	ns
		HIGH level	[2]	-	1500	-	600	ns
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals			-	300	$20 + 0.1C_b$ [3]	300	ns
t_r	rise time of both SDA and SCL signals			-	1000	$20 + 0.1C_b$ [3]	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.

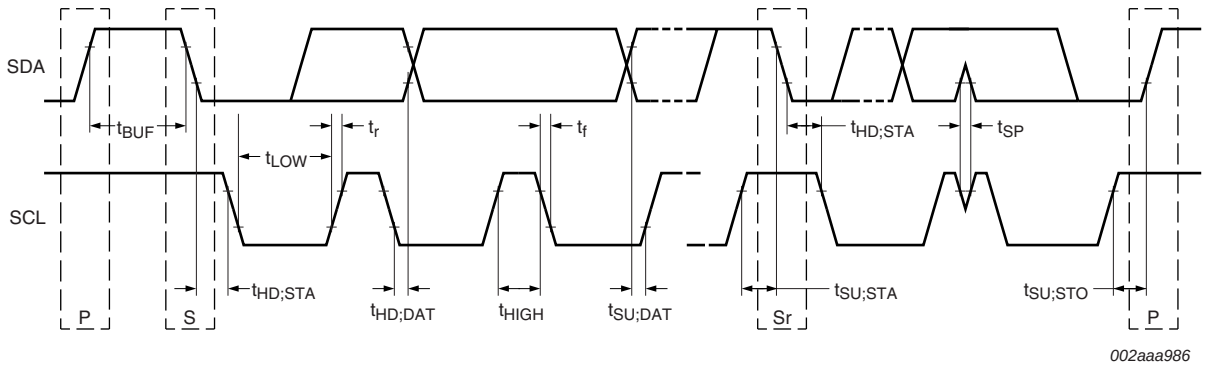

Fig 12. Timing diagram for serial interface

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10. EEPROM memory

Table 9. EEPROM memory specifications

Parameter	Specification
data retention at operating temperature	10 years (minimum)
endurance per byte	100,000 cycles (minimum)

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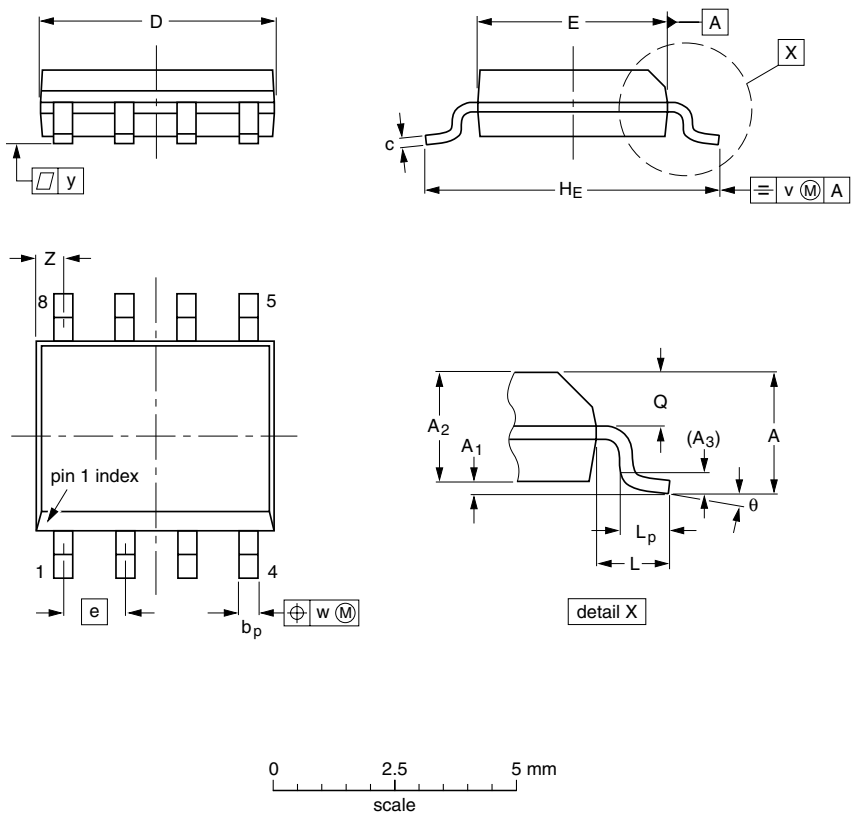
11. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 13. Package outline SOT96-1 (SO8)

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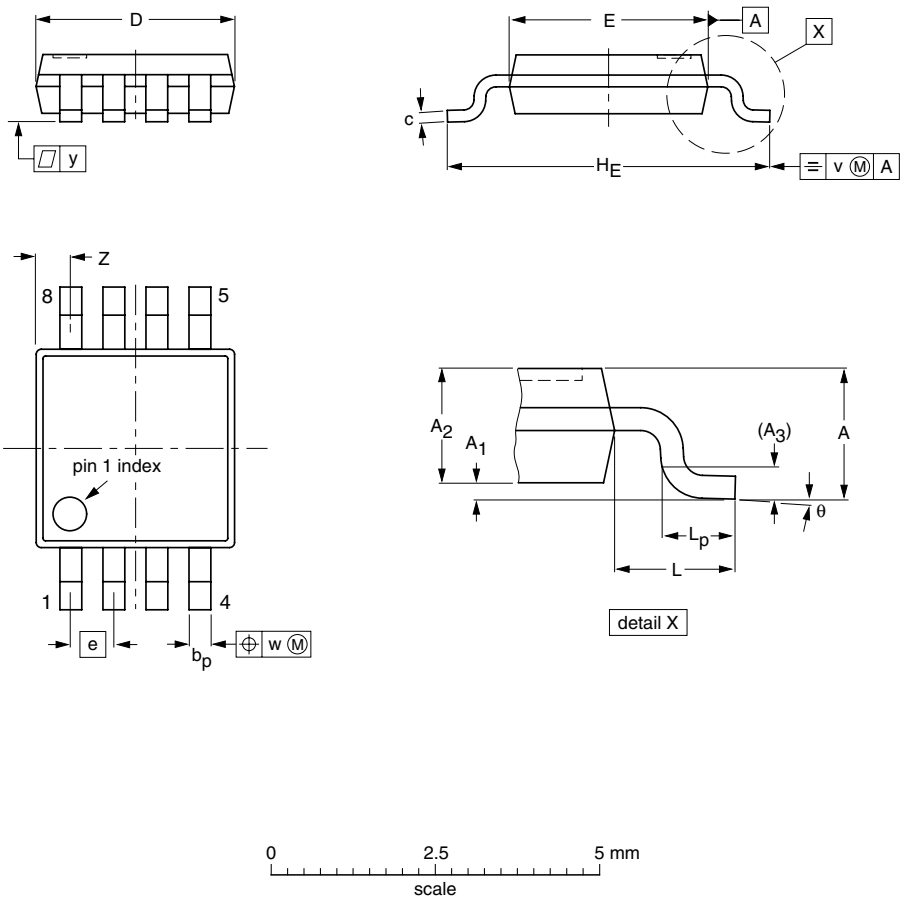
TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 14. Package outline SOT505-1 (TSSOP8)

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12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 15) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 15.

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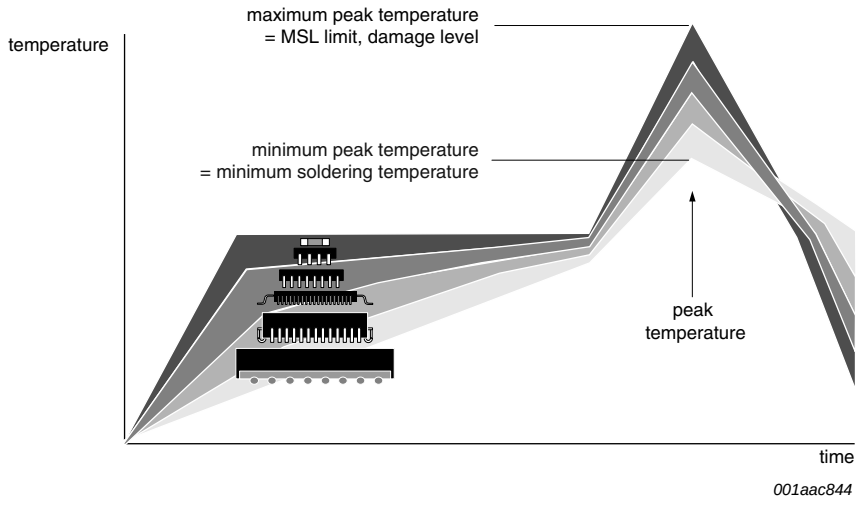

MSL: Moisture Sensitivity Level

Fig 15. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
ACK	Acknowledge
APP	Access Protection Page
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
E/W	Erase/Write
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
NACK	Not Acknowledge
PB	Protection Bit
RF	Radio Frequency
RFID	Radio Frequency Identification
SB	Sticky Bit

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14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA24S08A_1	20100119	Product data sheet	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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17. Contents

1 General description 1
2 Features 2
3 Ordering information 2
4 Block diagram 3
5 Pinning information 3
5.1 Pinning 3
5.2 Pin description 4
6 Functional description 4
6.1 Device addressing 4
6.2 Write operations 4
6.2.1 Byte/word write 4
6.2.2 Page write 6
6.3 Read operations 7
6.4 Access protection 8
6.4.1 RFID access fields (RF) 8
6.4.2 Protection bits (PB) 8
6.4.2.1 Block 0 write protection bits 10
6.4.2.2 Access Protection Page (APP) 11
6.5 PROT pin 13
6.6 Serial EEPROM exceptions 13
7 Limiting values 14
8 Static characteristics 14
9 Dynamic characteristics 15
10 EEPROM memory 16
11 Package outline 17
12 Soldering of SMD packages 19
12.1 Introduction to soldering 19
12.2 Wave and reflow soldering 19
12.3 Wave soldering 19
12.4 Reflow soldering 20
13 Abbreviations 21
14 Revision history 22
15 Legal information 23
15.1 Data sheet status 23
15.2 Definitions 23
15.3 Disclaimers 23
15.4 Trademarks 23
16 Contact information 23
17 Contents 24

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