AMC1304x High-Precision, Reinforced Isolated Delta-Sigma Modulators with LDO

1 Features

- Pin-Compatible Family Optimized for Shunt-Resistor-Based Current Measurements:
  - ±50-mV or ±250-mV Input Voltage Ranges
  - CMOS or LVDS Digital Interface Options
- Excellent DC Performance Supporting High-Precision Sensing on System Level:
  - Offset Error: ±50 µV or ±100 µV (max)
  - Offset Drift: 1.3 µV/°C (max)
  - Gain Error: ±0.2% or ±0.3% (max)
  - Gain Drift: ±40 ppm/°C (max)
- Safety-Related Certifications:
  - 7000-V_{PK} Reinforced Isolation per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
  - 5000-V_{RMS} Isolation for 1 Miinute per UL1577
  - CAN/CSA No. 5A-Component Acceptance Service Notice, IEC 60950-1: 2005, and IEC60065: 2014 End Equipment Standards
- Transient Immunity: 15 kV/µs (min)
- High Electromagnetic Field Immunity (see Application Note SLLA181A)
- External 5-MHz to 20-MHz Clock Input for Easier System-Level Synchronization
- On-Chip 18-V LDO Regulator
- Fully Specified Over the Extended Industrial Temperature Range

2 Applications

- Shunt-Resistor-Based Current Sensing In:
  - Industrial Motor Drives
  - Photovoltaic Inverters
  - Uninterruptible Power Supplies
- Isolated Voltage Measurements

3 Description

The AMC1304 is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PEAK} according to the DIN V VDE V 0884-10, UL1577 and CSA standards. Used in conjunction with isolated power supplies, the device prevents noise currents on a high common-mode voltage line from entering the local system ground and interfering with or damaging low voltage circuitry.

The input of the AMC1304 is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The unique low input voltage range of the ±50-mV device allows significant reduction of the power dissipation through the shunt while supporting excellent ac and dc performance. By using an appropriate digital filter (that is, as integrated on the TMS320F2807x or TMS320F2837x families) to decimate the bit stream, the device can achieve 16 bits of resolution with a dynamic range of 81 dB (13.2 ENOB) at a data rate of 78 kSPS.

On the high-side, the modulator is supplied by an integrated low-dropout (LDO) regulator that allows an unregulated input voltage between 4 V and 18 V (LDOIN). The isolated digital interface operates from a 3.3-V or 5-V power supply (DVDD).

The AMC1304 is available in a wide-body SOIC-16 (DW) package and is specified from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1304x	SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

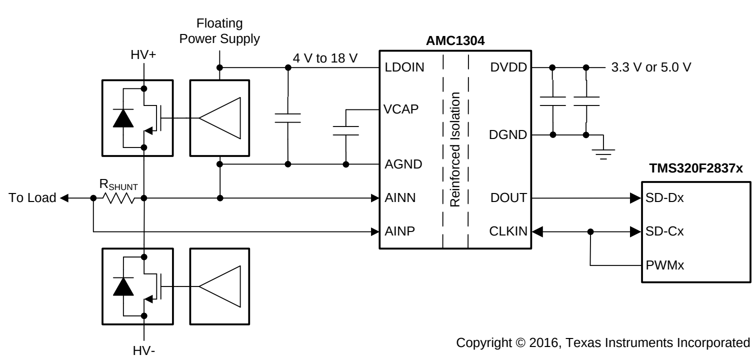


Table of Contents

4 Revision History

Changes from Revision C (September 2015) to Revision D — **Page**

- Changed *Features* section: deleted *Certified Isolation Barrier* bullet, added *Safety-Related Certifications* and *Transient Immunity* bullets ... 1
- Changed *Simplified Schematic* ... 1
- Changed Specifications section to comply with ISO data sheet format ... 5
- Changed *Maximum virtual junction* parameter to *Junction temperature* in *Absolute Maximum Ratings* table ... 5
- Moved *Power Rating*, *Insulation Specifications*, *Safety-Related Certifications*, and *Safety Limiting Values* tables, changed to current standards ... 5
- Changed *Insulation Specifications* table as per ISO standard ... 6
- Added *Safety and Insulation Characteristics* section ... 13
- Changed Figure 54 (*The AMC1304 in a Frequency Inverter Application*) ... 26
- Changed Figure 58 (*Decoupling the AMC1304*) ... 30

Changes from Revision B (July 2015) to Revision C — **Page**

- Changed document status to full Production Data: released AMC1304Mx5 to production ... 1
- Changed status of AMC1304Mx5 rows to *Production* in *Device Comparison Table* ... 4
- Changed title of *AMC1304x05 Electrical Characteristics* table from AMC1304L05 to AMC1304x05 ... 8
- Changed typical specification in second row of DC Accuracy, *PSRR* parameter of *AMC1304x05 Electrical Characteristics* table ... 8
- Added CMOS Logic Family (AMC1304M05) section to *AMC1304x05 Electrical Characteristics* table ... 9
- Added last two rows to the Power Supply, I_{DVDD} and P_{DVDD} parameters of *AMC1304x05 Electrical Characteristics* table ... 9
- Changed title of *AMC1304x25 Electrical Characteristics* table from AMC1304L25 to AMC1304x25 ... 10
- Changed typical specification in second row of DC Accuracy, *PSRR* parameter of *AMC1304x25 Electrical Characteristics* table ... 10

- Added CMOS Logic Family (AMC1304M05) section to *AMC1304x25 Electrical Characteristics* table 11
- Added footnote 4 to *AMC1304x25 Electrical Characteristics* table 11
- Added last two rows to the Power Supply, I_{DVDD} and P_{DVDD} parameters of *AMC1304x25 Electrical Characteristics* table 11
- Changed legends of Figure 6 and Figure 7 to include all devices, changed conditions of Figure 10 and Figure 11 14
- Changed conditions of Figure 12, Figure 13, and Figure 14 15
- Changed legends of Figure 19 to Figure 22, changed conditions of Figure 23 16
- Changed conditions of Figure 24 and Figure 29 17
- Changed conditions of Figure 30 and Figure 35 18
- Changed conditions of Figure 36 to Figure 40 19
- Added CMOS curve to Figure 44 to Figure 47 20
- Changed legend of Figure 57 29

Changes from Revision A (May 2015) to Revision B **Page**

- AMC1304L25 released to production 1
- Changed *Offset Error* and *Gain Error* sub-bullets of second Features bullet to include AMC1304L25 specifications 1
- Changed status of second row to *Production* 4
- Changed table order in *Specifications* section to match correct SDS flow 8
- Added AMC1304L25 *Electrical Characteristics* table 10
- Changed Typical Characteristics section: changed condition statement to reflect AINP difference between device, added AMC1304L25 related curves 14
- Added AMC1304L25 plot to Figure 6 and Figure 7 14
- Changed Figure 10 14
- Added Figure 11 14
- Added Figure 12 and condition to Figure 13 15
- Changed Figure 14 15
- Added AMC1304L25 plot to Figure 19, Figure 20, Figure 21, and Figure 22 16
- Added Figure 23 16
- Added Figure 29 and condition to Figure 24 17
- Added condition to Figure 30 18
- Added Figure 35 18
- Added condition to Figure 36 19
- Added device name to conditions of Figure 37 and Figure 38 19
- Added Figure 39 and Figure 40 19

Changes from Original (September 2014) to Revision A **Page**

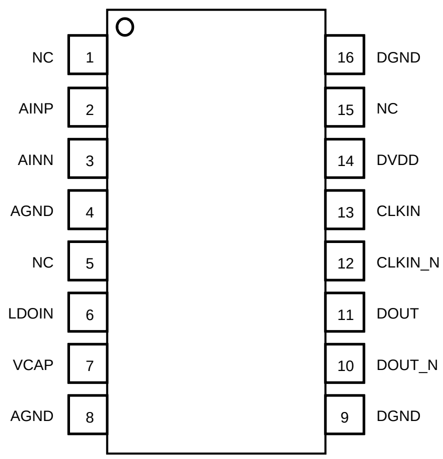
- Made changes to product preview document; AMC1304L05 released to production 1

5 Device Comparison Table

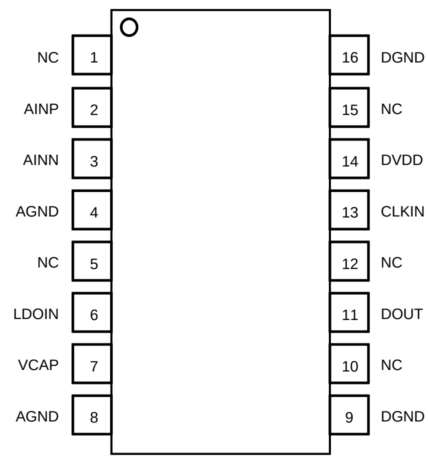
ORDER NUMBER	STATUS	INPUT VOLTAGE RANGE	DIFFERENTIAL INPUT RESISTANCE	DIGITAL OUTPUT INTERFACE
AMC1304L05DW, AMC1304L05DWR	Production	±50 mV	5 kΩ	LVDS
AMC1304L25DW, AMC1304L25DWR	Production	±250 mV	25 kΩ	LVDS
AMC1304M05DW, AMC1304M05DWR	Production	±50 mV	5 kΩ	CMOS
AMC1304M25DW, AMC1304M25DWR	Production	±250 mV	25 kΩ	CMOS

6 Pin Configurations and Functions

DW Package: LVDS Interface Versions (AMC1304Lx)
16-Pin SOIC
Top View



DW Package: CMOS Interface Versions (AMC1304Mx)
16-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO. AMC1304Lx (LVDS)	NO. AMC1304Mx (CMOS)		
AGND	4	4	—	This pin is internally connected to pin 8 and can be left unconnected or tied to high-side ground
	8	8	—	High-side ground reference
AINN	3	3	I	Inverting analog input
AINP	2	2	I	Noninverting analog input
CLKIN	13	13	I	Modulator clock input, 5 MHz to 20.1 MHz
CLKIN_N	12	—	I	Inverted modulator clock input
DGND	9, 16	9, 16	—	Controller-side ground reference
DOUT	11	11	O	Modulator data output
DOUT_N	10	—	O	Inverted modulator data output
DVDD	14	14	—	Controller-side power supply, 3.0 V to 5.5 V. See the *Power-Supply Recommendations* section for decoupling recommendations.
LDOIN	6	6	—	Low dropout regulator input, 4 V to 18 V
NC	1	1	—	This pin can be connected to VCAP or left unconnected
	5	5	—	This pin can be left unconnected or tied to AGND only
	—	10, 12	—	These pins have no internal connection
	15	15	—	This pin can be left unconnected or tied to DVDD only
VCAP	7	7	—	LDO output. See the *Power-Supply Recommendations* section for decoupling recommendations.

7 Specifications

7.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	DVDD to DGND	–0.3	6.5	V
LDO input voltage	LDOIN to AGND	–0.3	26	V
Analog input voltage at AINP, AINN		AGND – 6	3.7	V
Digital input voltage at CLKIN, CLKIN_N		DGND – 0.3	DVDD + 0.3	V
Input current to any pin except supply pins		–10	10	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
LDOIN	LDO input supply voltage (LDOIN pin)	4.0	15.0	18.0	V
DVDD	Digital (controller-side) supply voltage (DVDD pin)	3.0	3.3	5.5	V
T_A	Operating ambient temperature range	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		AMC1304x DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	LDOIN = 18 V, DVDD = 5.5 V	161	mW
P_{D1}	Maximum power dissipation (high-side supply)	LDOIN = 18 V	117	mW
P_{D2}	Maximum power dissipation (low-side supply)	DVDD = 5.5 V, LVDS, R_{LOAD} = 100 Ω	44	mW

7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	Minimum air gap (clearance)(1)	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	Minimum external tracking (creepage)(1)	Shortest pin-to-pin distance across the package surface	≥ 8	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 0.0135 mm)	0.027	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At ac voltage (bipolar or unipolar)	1414	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At ac voltage (sine wave)	1000	V_{RMS}
		At dc voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7000	V_{PK}
		V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production test)	8400	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, V_{TEST} = 1.6 x V_{IOSM} = 10000 V_{PK} (qualification)	6250	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)}$ = 1.2 x V_{IORM} = 1697 V_{PK}, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)}$ = 1.6 x V_{IORM} = 2263 V_{PK}, t_m = 10 s	≤ 5	pC
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)}$ = 1.875 x V_{IORM} = 2652 V_{PK}, t_m = 1 s	≤ 5	pC
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 V_{PP} at 1 MHz	1.2	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_S = 150°C	> 10^9	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS} or 7000 V_{DC}, t = 60 s (qualification test), V_{TEST} = 1.2 x V_{ISO} = 6000 V_{RMS}, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves or ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

7.7 Safety-Related Certifications

VDE	UL
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60095 (VDE 0860): 2005-11	Recognized under UL1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
File number: 40040142	File number: E181974

7.8 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O circuitry may allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 80.2°C/W, LDOIN = 18 V, T_J = 150°C, T_A = 25°C, see Figure 3			86.5	mA
P_S	Safety input, output, or total power	θ_{JA} = 80.2°C/W, T_J = 150°C, T_A = 25°C, see Figure 4			1558 (1)	mW
T_S	Maximum safety temperature				150	°C

(1) Input, output, or the sum of input and output power must not exceed this value.

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

7.9 Electrical Characteristics: AMC1304x05

All minimum and maximum specifications are at T_A = –40°C to 125°C, LDOIN = 4.0 V to 18.0 V, DVDD = 3.0 V to 5.5 V, AINP = –50 mV to 50 mV, AINN = 0 V, and $sinc^3$ filter with OSR = 256, unless otherwise noted.
Typical values are at T_A = 25°C, CLKIN = 20 MHz, LDOIN = 15.0 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
$V_{Clipping}$	Maximum differential voltage input range (AINP-AINN)			±62.5		mV
FSR	Specified linear full-scale range (AINP-AINN)		–50		50	mV
V_{CM}	Operating common-mode input range		–0.032		1.2	V
C_{ID}	Differential input capacitance			2		pF
I_{IB}	Input bias current	Inputs shorted to AGND	–97	–72	–57	µA
R_{ID}	Differential input resistance			5		kΩ
I_{IO}	Input offset current			±5		nA
CMTI	Common-mode transient immunity		15			kV/µs
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–98		dB
		f_{IN} from 0.1 Hz to 50 kHz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–85		
BW	Input bandwidth			800		kHz
DC ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity (1)	Resolution: 16 bits	–4	±1.5	4	LSB
E_O	Offset error	Initial, at 25°C	–50	±2.5	50	µV
TCE_O	Offset error thermal drift (2)		–1.3		1.3	µV/°C
E_G	Gain error	Initial, at 25°C	–0.3%	–0.02%	0.3%	
TCE_G	Gain error thermal drift (3)		–40	±20	40	ppm/°C
PSRR	Power-supply rejection ratio	LDOIN from 4 V to 18 V, at dc		–110		dB
		LDOIN from 4 V to 18 V, from 0.1 Hz to 50 kHz		–110		
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz	76	81.5		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1 kHz	76	81		dB
THD	Total harmonic distortion	f_{IN} = 1 kHz		–90	–81	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz	81	90		dB
DIGITAL INPUTS/OUTPUTS						
External Clock						
f_{CLKIN}	Input clock frequency		5	20	20.1	MHz
$Duty_{CLKIN}$	Duty cycle	5 MHz ≤ f_{CLKIN} ≤ 20.1 MHz	40%	50%	60%	

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as a number of LSBs or as a percent of the specified linear full-scale range (FSR).
(2) Offset error drift is calculated using the box method, as described by the following equation:
$$TCE_O = \frac{value_{MAX} - value_{MIN}}{TempRange}$$
(3) Gain error drift is calculated using the box method, as described by the following equation:
$$TCE_G(ppm) = \left(\frac{value_{MAX} - value_{MIN}}{value \times TempRange}\right) \times 10^6$$

Electrical Characteristics: AMC1304x05 (continued)

All minimum and maximum specifications are at T_A = –40°C to 125°C, LDOIN = 4.0 V to 18.0 V, DVDD = 3.0 V to 5.5 V, AINP = –50 mV to 50 mV, AINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.
Typical values are at T_A = 25°C, CLKIN = 20 MHz, LDOIN = 15.0 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS Logic Family (AMC1304M05, CMOS with Schmitt Trigger)						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD	–1		1	µA
C_{IN}	Input capacitance			5		pF
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × DVDD	V
C_{LOAD}	Output load capacitance	f_{CLKIN} = 20 MHz		30		pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	DVDD – 0.1			V
		I_{OH} = –4 mA	DVDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	
LVDS Logic Family (AMC1304L05)(4)						
V_T	Differential output voltage	R_{LOAD} = 100 Ω	250	350	450	mV
V_{OC}	Common-mode output voltage		1.125	1.23	1.375	V
V_{ID}	Differential input voltage		100	350	600	mV
V_{IC}	Common-mode input voltage	V_{ID} = 100 mV	0.05	1.25	3.25	V
I_I	Receiver input current	DGND ≤ V_{IN} ≤ 3.3 V	–24	0	20	µA
POWER SUPPLY						
LDOIN	LDOIN pin input voltage		4.0	15.0	18.0	V
VCAP	VCAP pin voltage			3.45		V
I_{LDOIN}	LDOIN pin input current			5.3	6.5	mA
DVDD	Controller-side supply voltage		3.0	3.3	5.5	V
I_{DVDD}	Controller-side supply current	LVDS, R_{LOAD} = 100 Ω		6.1	8	mA
		CMOS, 3.0 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 5 pF		2.7	4.0	
		CMOS, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 5 pF		3.2	5.5	

(4) For further information on electrical characteristics of LVDS interface circuits, see the TIA-644-A standard and the *Interface Circuits for TIA/EIA-644 (LVDS)* design note (SLLA038).

7.10 Electrical Characteristics: AMC1304x25

All minimum and maximum specifications are at T_A = –40°C to 125°C, LDOIN = 4.0 V to 18.0 V, DVDD = 3.0 V to 5.5 V, AINP = –250 mV to 250 mV, AINN = 0 V, and $sinc^3$ filter with OSR = 256, unless otherwise noted.
Typical values are at T_A = 25°C, CLKIN = 20 MHz, LDOIN = 15.0 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
$V_{Clipping}$	Maximum differential voltage input range (AINP-AINN)			±312.5		mV
FSR	Specified linear full-scale range (AINP-AINN)		–250		250	mV
V_{CM}	Operating common-mode input range		–0.16		1.2	V
C_{ID}	Differential input capacitance			1		pF
I_{IB}	Input bias current	Inputs shorted to AGND	–82	–60	–48	µA
R_{ID}	Differential input resistance			25		kΩ
I_{IO}	Input offset current			±5		nA
CMTI	Common-mode transient immunity		15			kV/µs
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–98		dB
		f_{IN} from 0.1 Hz to 50 kHz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–98		
BW	Input bandwidth			1000		kHz
DC ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity(1)	Resolution: 16 bits	–4	±1.5	4	LSB
E_O	Offset error	Initial, at 25°C	–100	±25	100	µV
TCE_O	Offset error thermal drift(2)		–1.3		1.3	µV/°C
E_G	Gain error	Initial, at 25°C	–0.2%	–0.05%	0.2%	
TCE_G	Gain error thermal drift(3)		–40	±20	40	ppm/°C
PSRR	Power-supply rejection ratio	LDOIN from 4 V to 18 V, at dc		–110		dB
		LDOIN from 4 V to 18 V, from 0.1 Hz to 50 kHz		–110		
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz	82	85		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1 kHz	80	84		dB
THD	Total harmonic distortion	f_{IN} = 1 kHz		–90	–81	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz	81	90		dB
DIGITAL INPUTS/OUTPUTS						
External Clock						
f_{CLKIN}	Input clock frequency		5	20	20.1	MHz
$Duty_{CLKIN}$	Duty cycle	5 MHz ≤ f_{CLKIN} ≤ 20.1 MHz	40%	50%	60%	

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
(2) Offset error drift is calculated using the box method as described by the following equation:
$$TCE_O = \frac{value_{MAX} - value_{MIN}}{TempRange}$$
(3) Gain error drift is calculated using the box method as described by the following equation:
$$TCE_G(ppm) = \left(\frac{value_{MAX} - value_{MIN}}{value \times TempRange}\right) \times 10^6$$

Electrical Characteristics: AMC1304x25 (continued)

All minimum and maximum specifications are at T_A = –40°C to 125°C, LDOIN = 4.0 V to 18.0 V, DVDD = 3.0 V to 5.5 V, AINP = –250 mV to 250 mV, AINN = 0 V, and $sinc^3$ filter with OSR = 256, unless otherwise noted.
Typical values are at T_A = 25°C, CLKIN = 20 MHz, LDOIN = 15.0 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS Logic Family (AMC1304M25, CMOS with Schmitt Trigger)						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD	–1		1	µA
C_{IN}	Input capacitance			5		pF
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × DVDD	V
C_{LOAD}	Output load capacitance	f_{CLKIN} = 20 MHz		30		pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	DVDD – 0.1			V
		I_{OH} = –4 mA	DVDD – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	V
LVDS Logic Family (AMC1304L25)(4)						
V_T	Differential output voltage	R_{LOAD} = 100 Ω	250	350	450	mV
V_{OC}	Common-mode output voltage		1.125	1.23	1.375	V
V_{ID}	Differential input voltage		100	350	600	mV
V_{IC}	Common-mode input voltage	V_{ID} = 100 mV	0.05	1.25	3.25	V
I_I	Receiver input current	DGND ≤ V_{IN} ≤ 3.3 V	–24	0	20	µA
POWER SUPPLY						
LDOIN	LDOIN pin input voltage		4.0	15.0	18.0	V
VCAP	VCAP pin voltage			3.45		V
I_{LDOIN}	LDOIN pin input current			5.3	6.5	mA
DVDD	Controller-side supply voltage		3.0	3.3	5.5	V
I_{DVDD}	Controller-side supply current	LVDS, R_{LOAD} = 100 Ω		6.1	8.0	mA
		CMOS, 3.0 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 5 pF		2.7	4.0	
		CMOS, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 5 pF		3.2	5.5	

(4) For further information on electrical characteristics of LVDS interface circuits, see the TIA-644-A standard and design note *Interface Circuits for TIA/EIA-644 (LVDS)* .

7.11 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CLK}	CLKIN, CLKIN_N clock period		49.75	50	200	ns
t_{HIGH}	CLKIN, CLKIN_N clock high time		19.9	25	120	ns
t_{LOW}	CLKIN, CLKIN_N clock low time		19.9	25	120	ns
t_D	Falling edge of CLKIN, CLKIN_N to DOUT, DOUT_N valid delay		0		15	ns
t_{ISTART}	Interface startup time	DVDD at 3.0 V (min) to DOUT, DOUT_N valid with LDO_IN > 4 V	32		32	CLKIN cycles
t_{ASTART}	Analog startup time	LDOIN step to 4 V with DVDD ≥ 3.0 V, and 0.1 µF at VCAP pin		1		ms

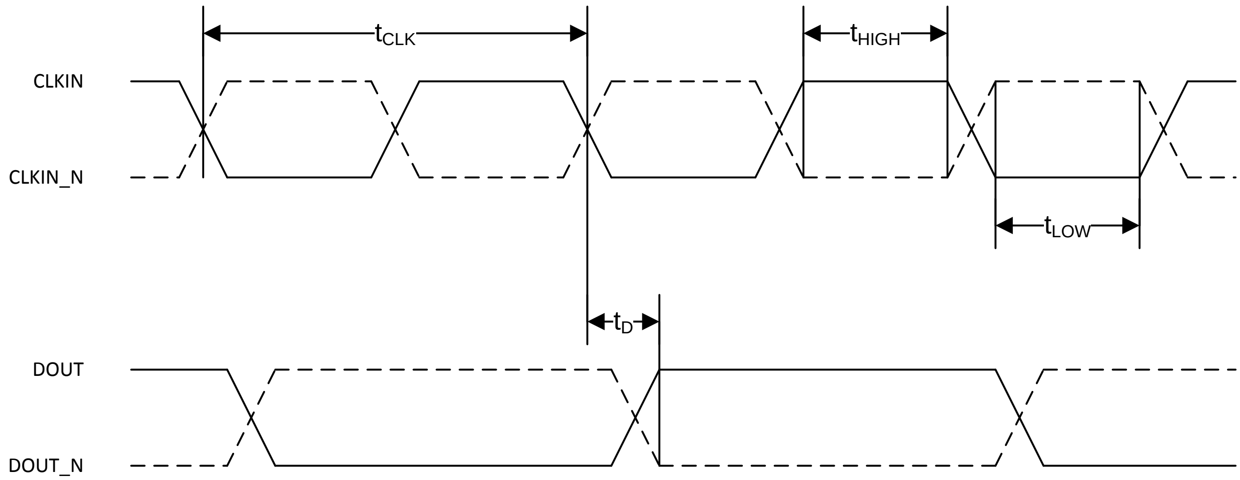


Figure 1. Digital Interface Timing

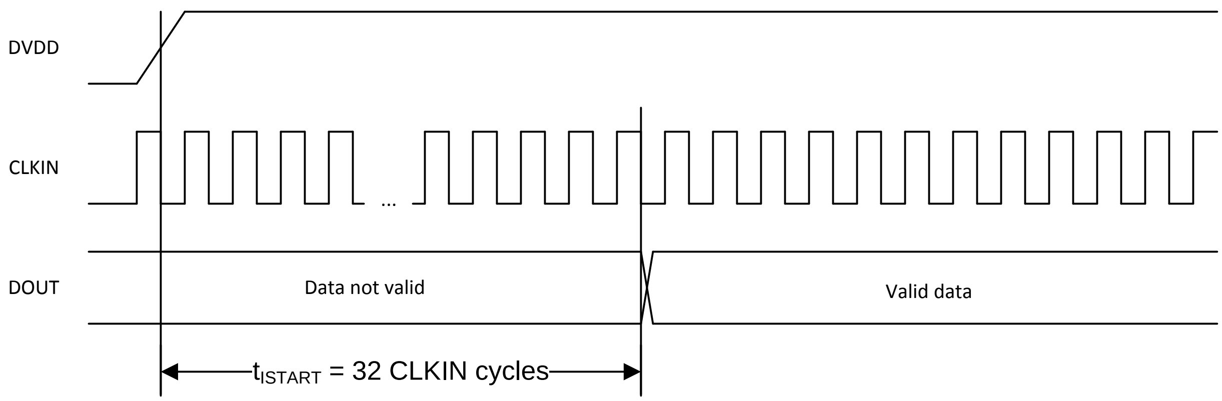
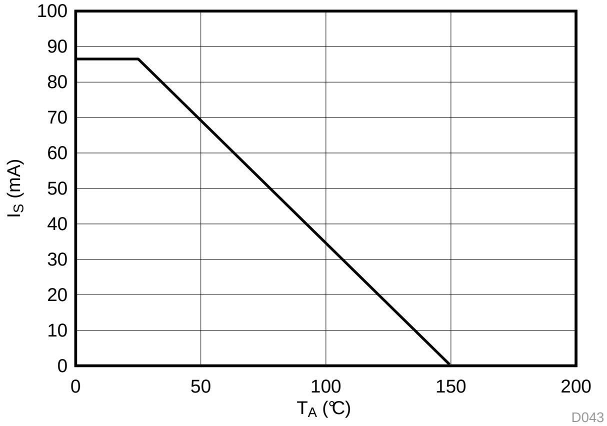


Figure 2. Digital Interface Startup Timing

7.12 Insulation Characteristics Curves



LDOIN = 18 V (worst case)

Figure 3. Thermal Derating Curve for Safety Limiting Current per VDE

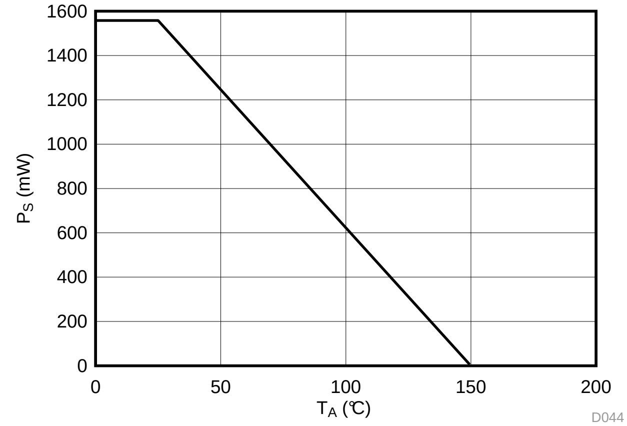
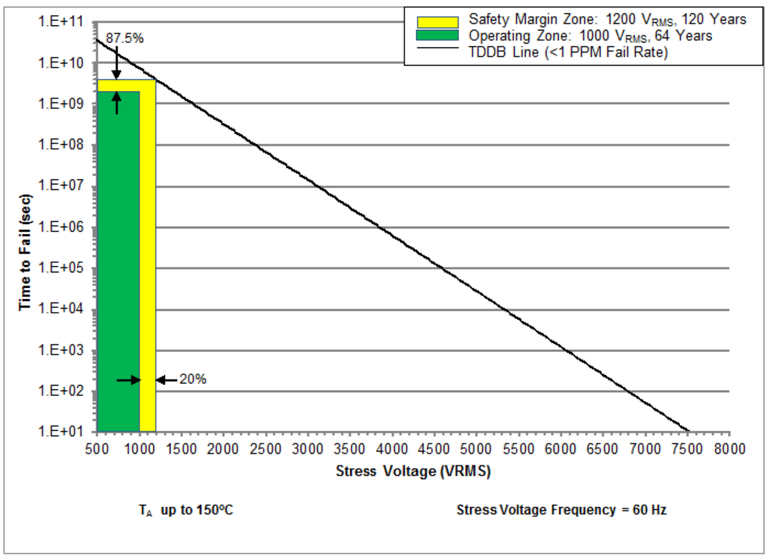


Figure 4. Thermal Derating Curve for Safety Limiting Power per VDE



T_A up to 150°C, stress voltage frequency = 60 Hz

Figure 5. Reinforced Isolation Capacitor Lifetime Projection

7.13 Typical Characteristics

At LDOIN = 15.0 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1304x05) or –250 mV to 250 mV (AMC1304x25), AINN = 0 V, f_{CLKIN} = 20 MHz, and sinc[3] filter with OSR = 256, unless otherwise noted.

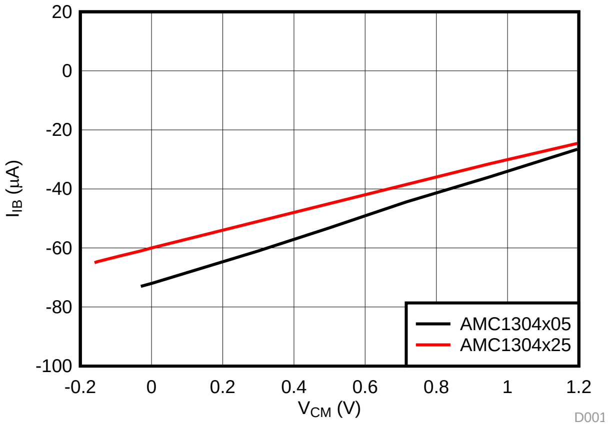


Figure 6. Input Current vs Input Common-Mode Voltage

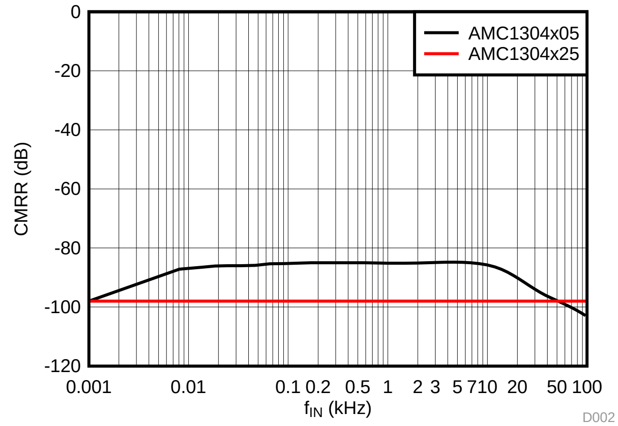


Figure 7. Common-Mode Rejection Ratio vs Input Signal Frequency

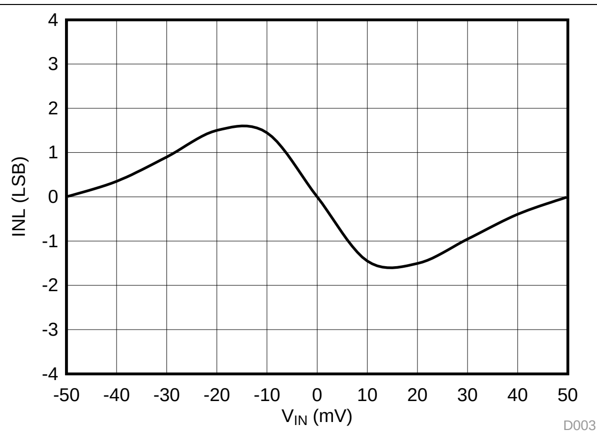


Figure 8. Integral Nonlinearity vs Input Signal Amplitude

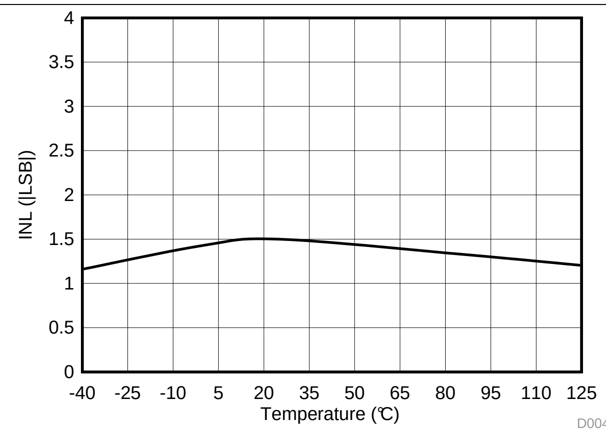
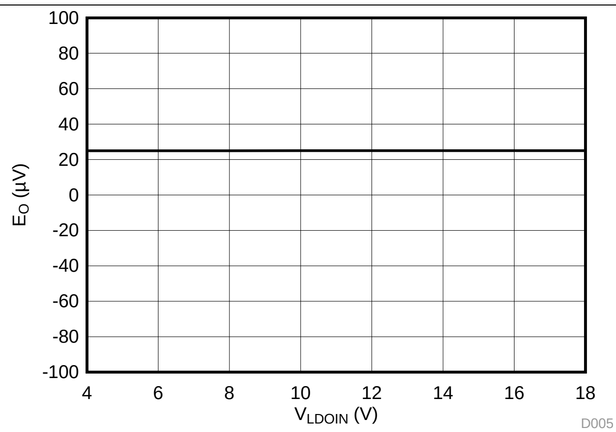
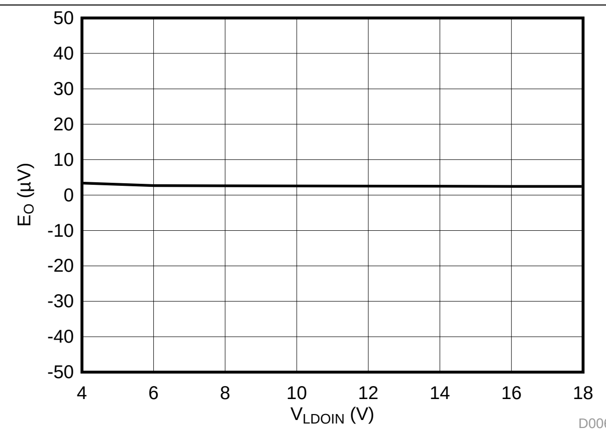


Figure 9. Integral Nonlinearity vs Temperature



AMC1304x25

Figure 10. Offset Error vs LDO Input Supply Voltage



AMC1304x05

Figure 11. Offset Error vs LDO Input Supply Voltage

Typical Characteristics (continued)

At LDOIN = 15.0 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1304x05) or –250 mV to 250 mV (AMC1304x25), AINN = 0 V, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, unless otherwise noted.

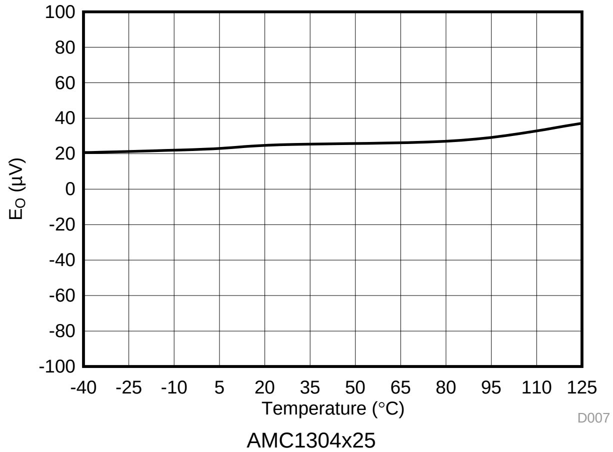


Figure 12. Offset Error vs Temperature

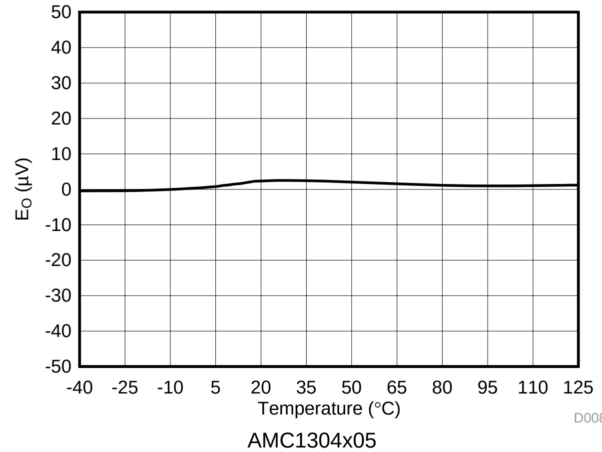


Figure 13. Offset Error vs Temperature

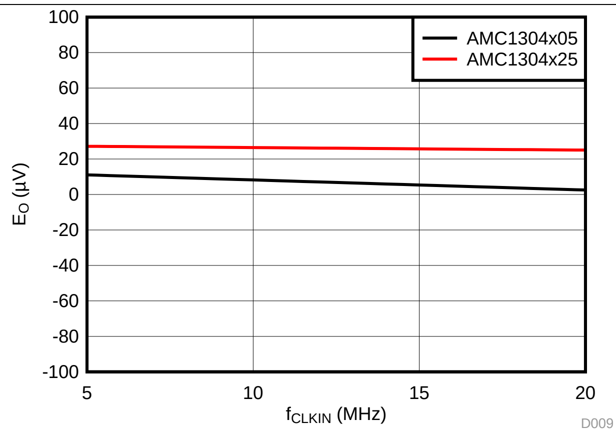


Figure 14. Offset Error vs Clock Frequency

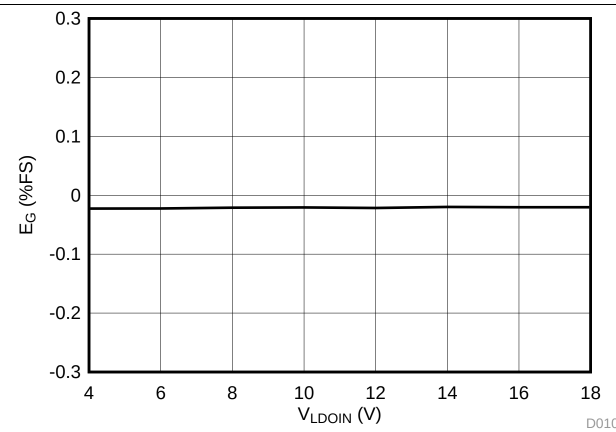


Figure 15. Gain Error vs LDO Input Supply Voltage

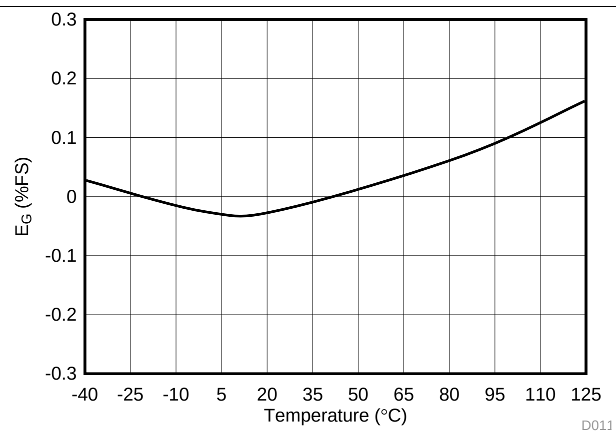


Figure 16. Gain Error vs Temperature

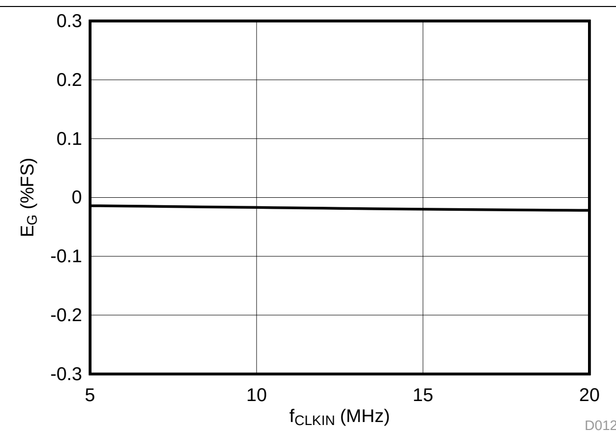


Figure 17. Gain Error vs Clock Frequency

Typical Characteristics (continued)

At LDOIN = 15.0 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1304x05) or –250 mV to 250 mV (AMC1304x25), AINN = 0 V, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256, unless otherwise noted.

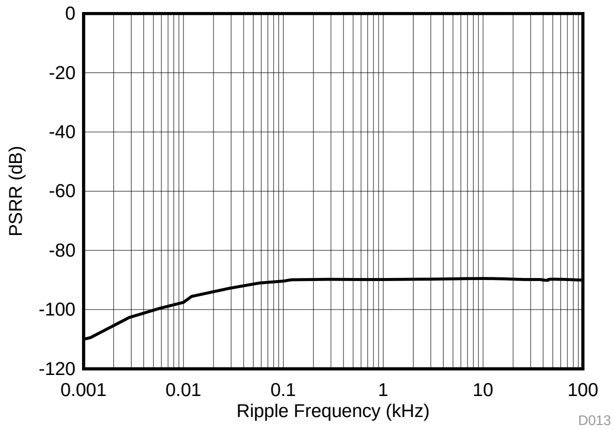


Figure 18. Power-Supply Rejection Ratio vs Ripple Frequency

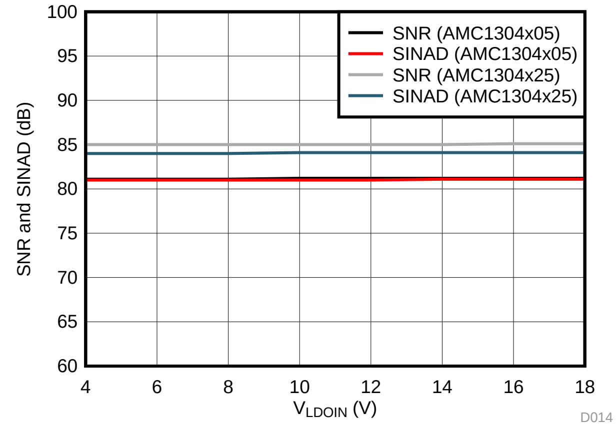


Figure 19. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs LDO Input Supply Voltage

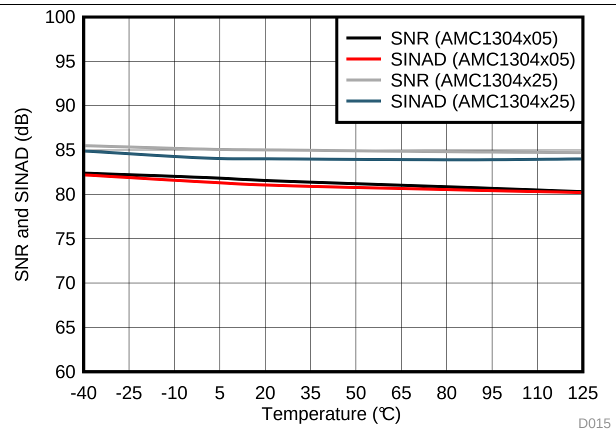


Figure 20. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature

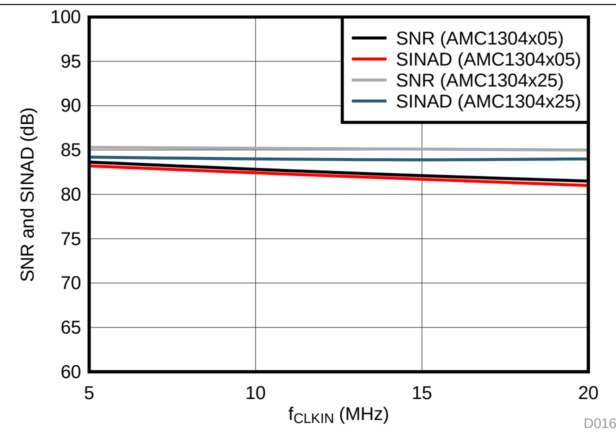


Figure 21. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Clock Frequency

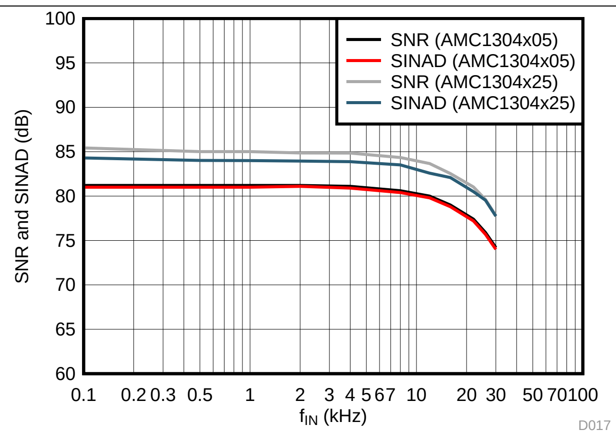


Figure 22. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency

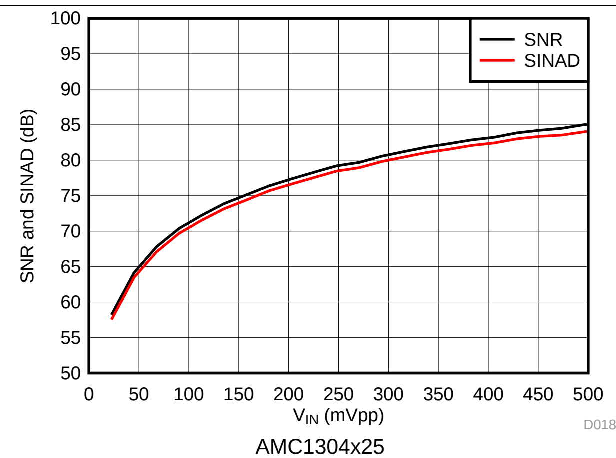


Figure 23. SNR and SINAD vs Input Signal Amplitude

Typical Characteristics (continued)

At LDOIN = 15.0 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1304x05) or –250 mV to 250 mV (AMC1304x25), AINN = 0 V, f_{CLKIN} = 20 MHz, and sinc[3] filter with OSR = 256, unless otherwise noted.

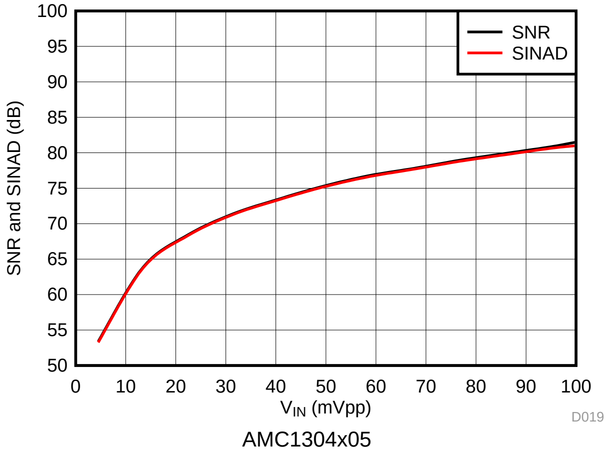


Figure 24. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude

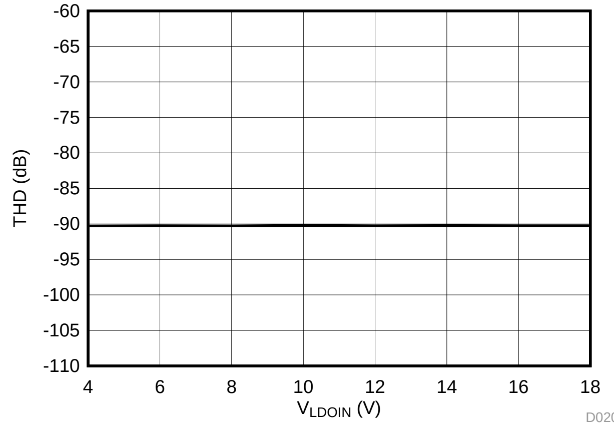


Figure 25. Total Harmonic Distortion vs LDO Input Supply Voltage

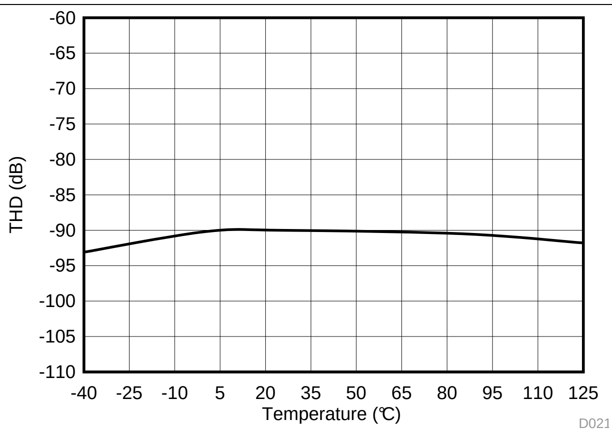


Figure 26. Total Harmonic Distortion vs Temperature

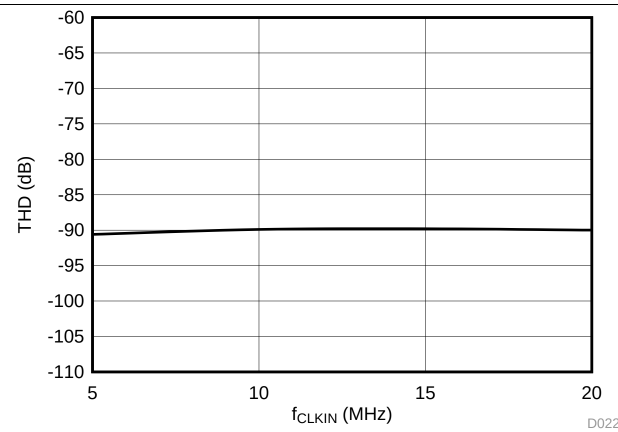


Figure 27. Total Harmonic Distortion vs Clock Frequency

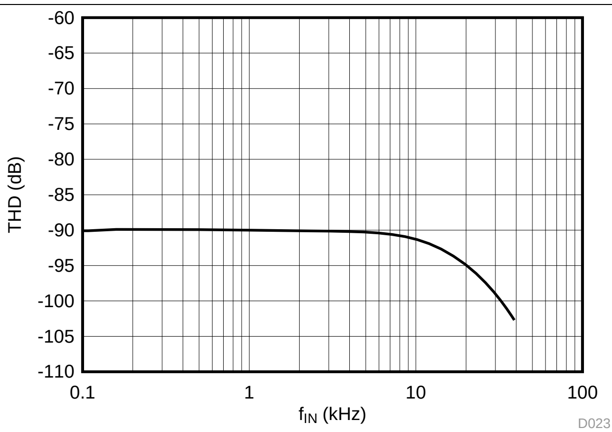


Figure 28. Total Harmonic Distortion vs Input Signal Frequency

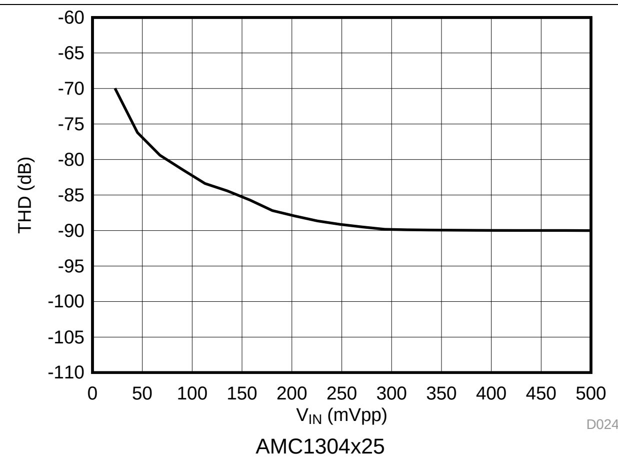


Figure 29. Total Harmonic Distortion vs Input Signal Amplitude

Typical Characteristics (continued)

At LDOIN = 15.0 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1304x05) or –250 mV to 250 mV (AMC1304x25), AINN = 0 V, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, unless otherwise noted.

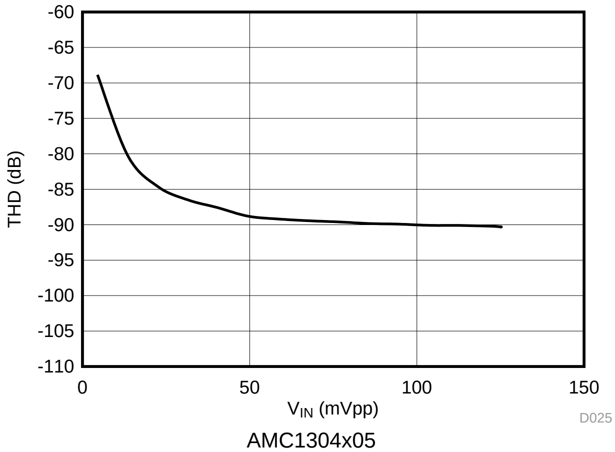


Figure 30. Total Harmonic Distortion vs Input Signal Amplitude

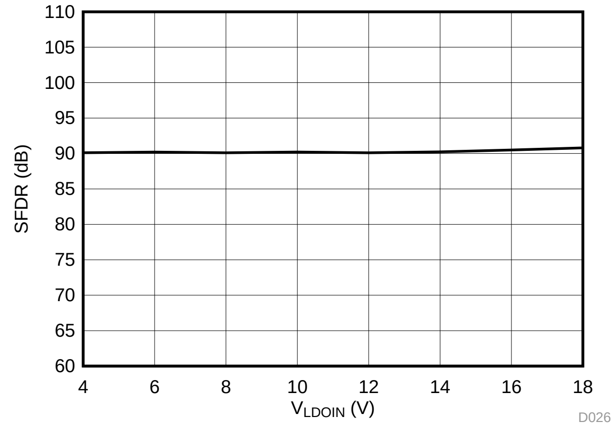


Figure 31. Spurious-Free Dynamic Range vs LDO Input Supply Voltage

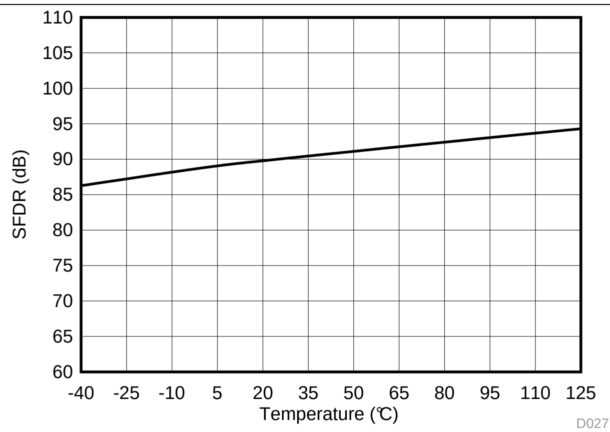


Figure 32. Spurious-Free Dynamic Range vs Temperature

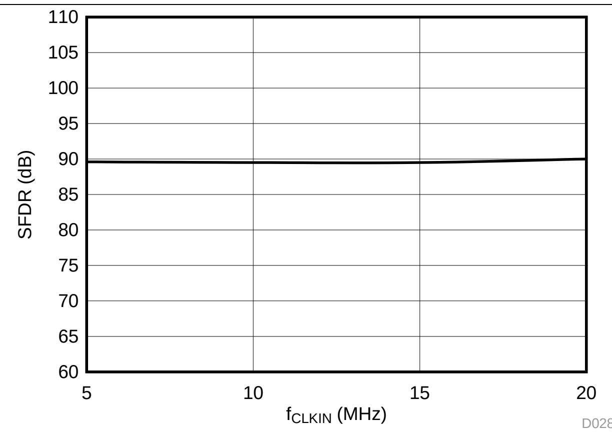


Figure 33. Spurious-Free Dynamic Range vs Clock Frequency

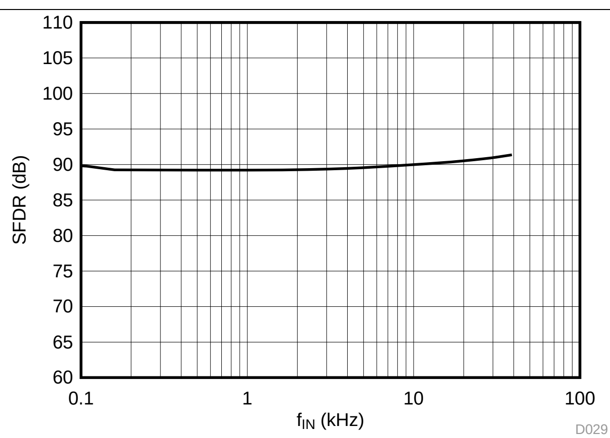


Figure 34. Spurious-Free Dynamic Range vs Input Signal Frequency

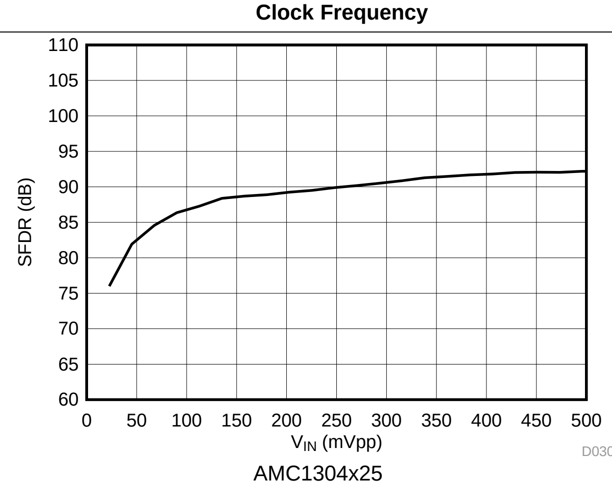
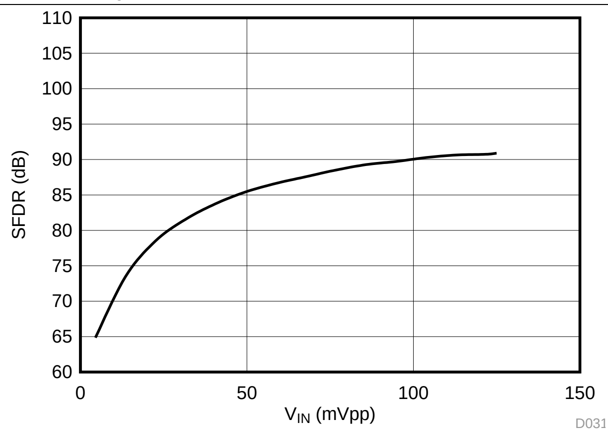


Figure 35. Spurious-Free Dynamic Range vs Input Signal Amplitude

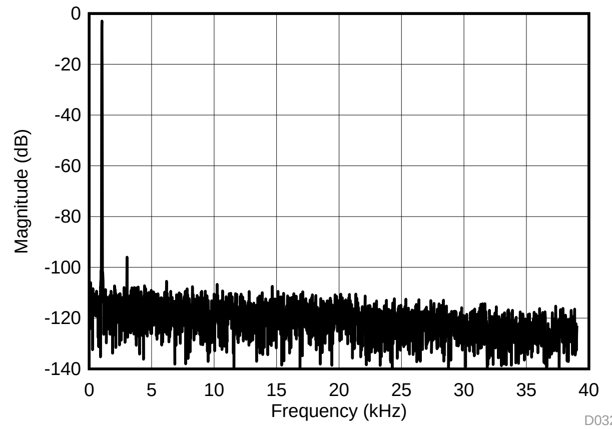
Typical Characteristics (continued)

At LDOIN = 15.0 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1304x05) or –250 mV to 250 mV (AMC1304x25), AINN = 0 V, f_{CLKIN} = 20 MHz, and sinc[3] filter with OSR = 256, unless otherwise noted.



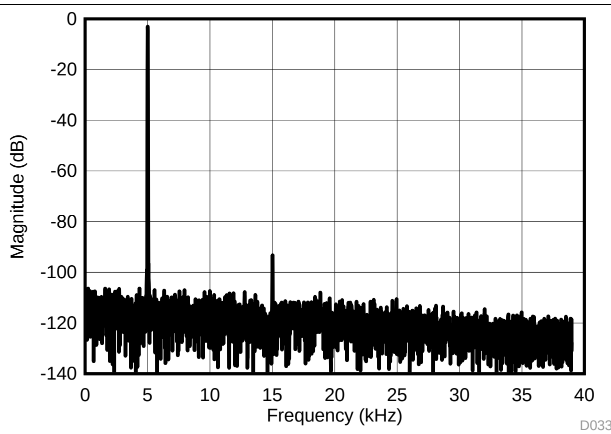
AMC1304x05

Figure 36. Spurious-Free Dynamic Range vs Input Signal Amplitude



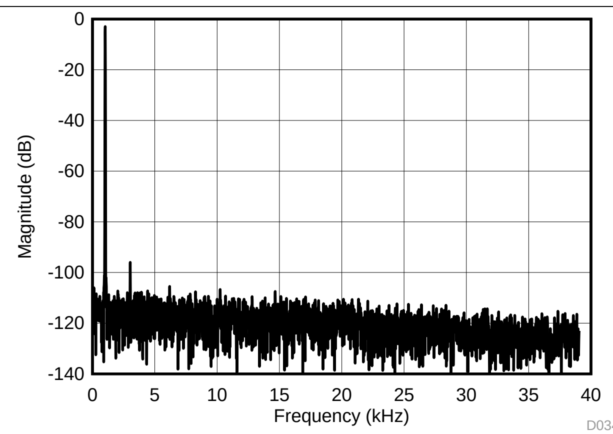
AMC1304x05, 4096-point FFT, V_{IN} = 100 mV_{PP}

Figure 37. Frequency Spectrum with 1-kHz Input Signal



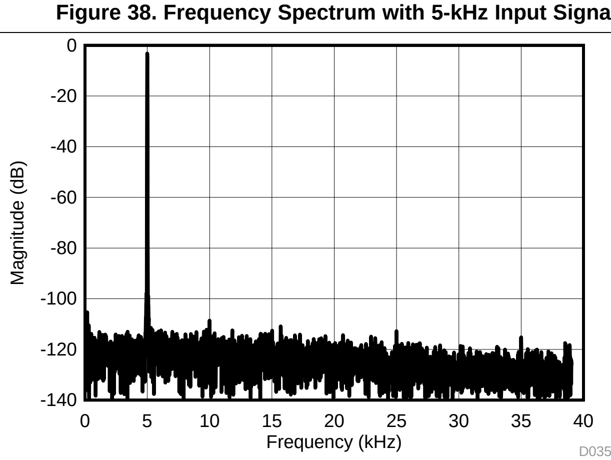
AMC1304x05, 4096-point FFT, V_{IN} = 100 mV_{PP}

Figure 38. Frequency Spectrum with 5-kHz Input Signal



AMC1304x25, 4096-point FFT, V_{IN} = 500 mV_{PP}

Figure 39. Frequency Spectrum with 1-kHz Input Signal



AMC1304x25, 4096-point FFT, V_{IN} = 500 mV_{PP}

Figure 40. Frequency Spectrum with 5-kHz Input Signal

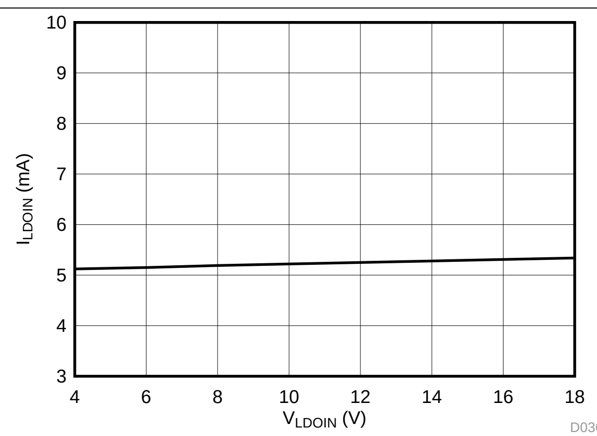


Figure 41. LDO Input Supply Current vs LDO Input Supply Voltage

Typical Characteristics (continued)

At LDOIN = 15.0 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1304x05) or –250 mV to 250 mV (AMC1304x25), AINN = 0 V, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, unless otherwise noted.

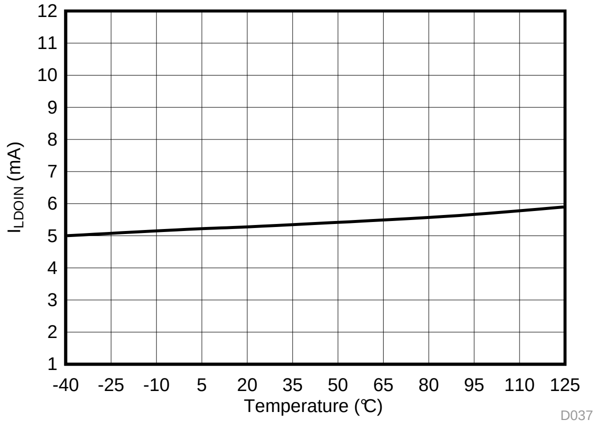


Figure 42. LDO Input Supply Current vs Temperature

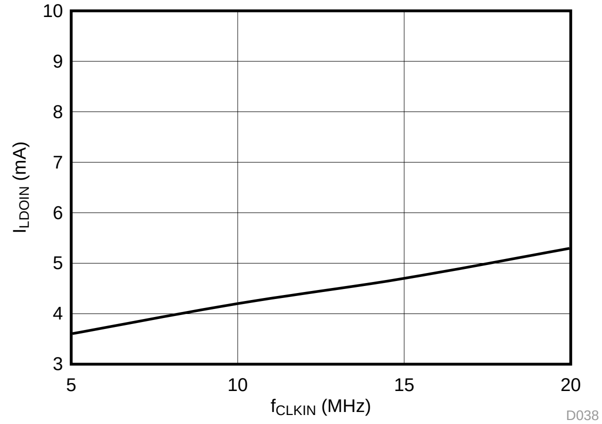


Figure 43. LDO Input Supply Current vs Clock Frequency

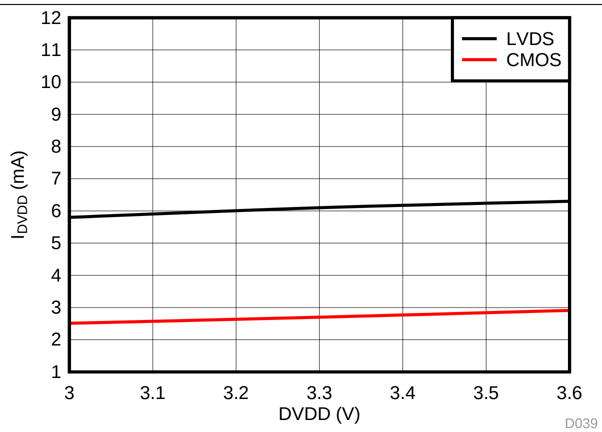


Figure 44. Controller-Side Supply Current vs Controller-Side Supply Voltage (3.3 V, min)

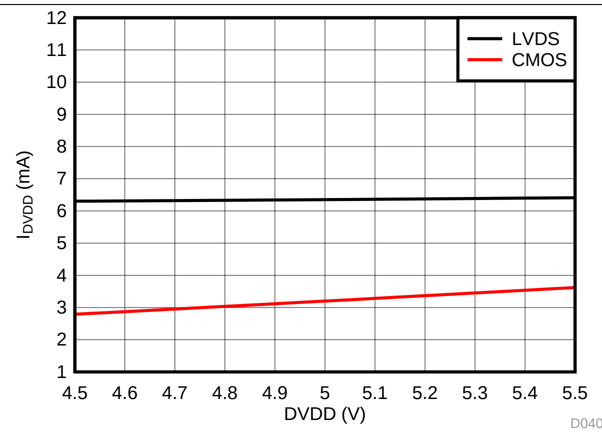


Figure 45. Controller-Side Supply Current vs Controller-Side Supply Voltage (5 V, min)

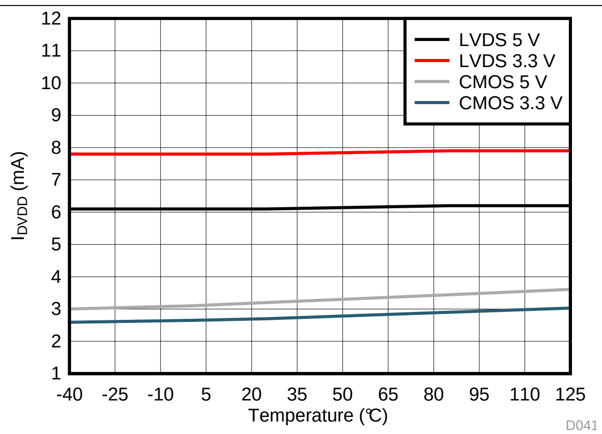


Figure 46. Controller-Side Supply Current vs Temperature

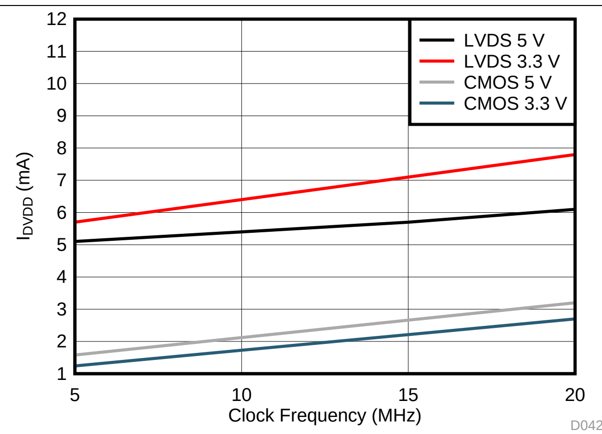


Figure 47. Controller-Side Supply Current vs Clock Frequency

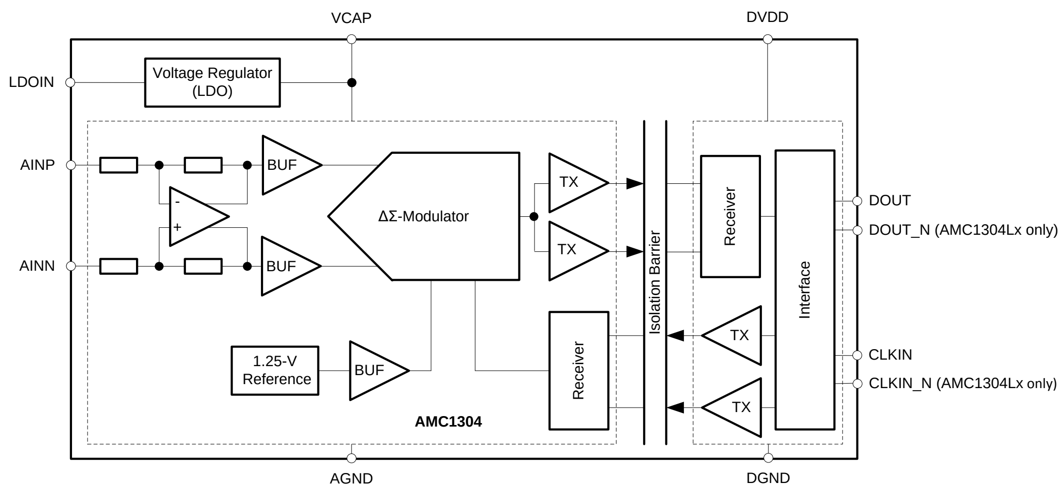
8 Detailed Description

8.1 Overview

The differential analog input (AINP and AINN) of the AMC1304 is a fully-differential amplifier feeding the switched-capacitor input of a second-order, delta-sigma (ΔΣ) modulator stage that digitizes the input signal into a 1-bit output stream. The isolated data output (DOUT and DOUT_N) of the converter provides a stream of digital ones and zeros that is synchronous to the externally-provided clock source at the CLKIN pin with a frequency in the range of 5 MHz to 20.1 MHz. The time average of this serial bit-stream output is proportional to the analog input voltage.

The *Functional Block Diagram* section shows a detailed block diagram of the AMC1304. The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. The SiO_2-based capacitive isolation barrier supports a high level of magnetic field immunity as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report (SLLA181A), available for download at www.ti.com. The external clock input simplifies the synchronization of multiple current-sensing channels on the system level. The extended frequency range of up to 20 MHz supports higher performance levels compared to the other solutions available on the market.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The AMC1304 incorporates a front-end circuitry that contains a differential amplifier and sampling stage, followed by a ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 for devices with a specified input voltage range of ±250 mV (this value is for the AMC1304x25), or to a factor of 20 in devices with a ±50-mV input voltage range (for the AMC1304x05), resulting in a differential input impedance of 5 kΩ (for the AMC1304x05) or 25 kΩ (for the AMC1304x25).

Consider the input impedance of the AMC1304 in designs with high-impedance signal sources that can cause degradation of gain and offset specifications. The importance of this effect, however, depends on the desired system performance. Additionally, the input bias current caused by the internal common-mode voltage at the output of the differential amplifier causes an offset that is dependent on the actual amplitude of the input signal. See the *Isolated Voltage Sensing* section for more details on reducing these effects.

There are two restrictions on the analog input signals (AINP and AINN). First, if the input voltage exceeds the range AGND – 6 V to 3.7 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range (FSR), that is ±250 mV (for the AMC1304x25) or ±50 mV (for the AMC1304x05), and within the specified input common-mode range.

Feature Description (continued)

8.3.2 Modulator

The modulator implemented in the AMC1304 is a second-order, switched-capacitor, feed-forward ΔΣ modulator, such as the one conceptualized in Figure 48. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is differentiated with the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage V_5, causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.

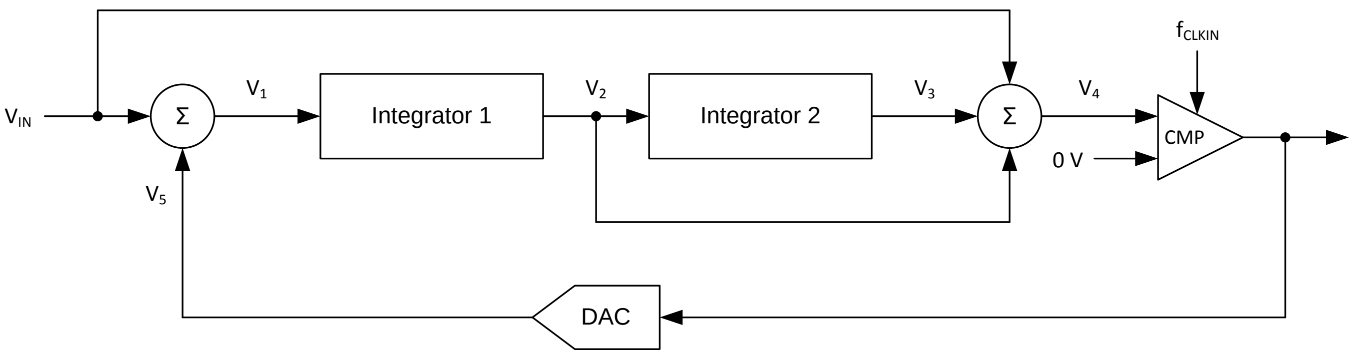


Figure 48. Block Diagram of a Second-Order Modulator

The modulator shifts the quantization noise to high frequencies, as shown in Figure 49. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's microcontroller families TMS320F2807x and TMS320F2837x offer a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1304 family. Also, SD24_B converters on the MSP430F677x microcontrollers offer a path to directly access the integrated sinc-filters, thus offering a system-level solution for multichannel, isolated current sensing. An additional option is to use a suitable application-specific device, such as the AMC1210 (a four-channel digital sinc-filter). Alternatively, a field-programmable gate array (FPGA) can be used to implement the filter.

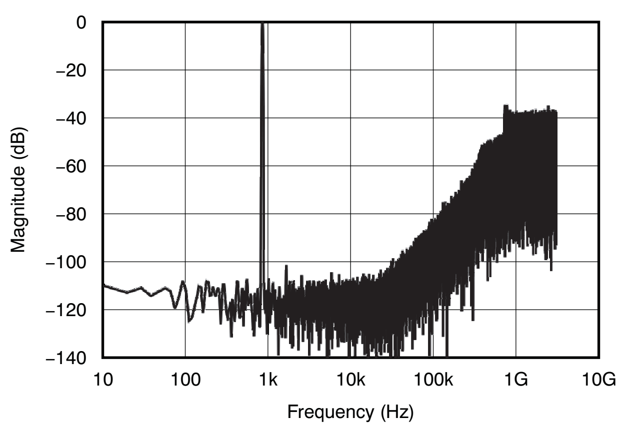


Figure 49. Quantization Noise Shaping

Feature Description (continued)

8.3.3 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 250 mV (for the AMC1304x25) or 50 mV (for the AMC1304x05) produces a stream of ones and zeros that are high 90% of the time. A differential input of –250 mV (–50 mV for the AMC1304x05) produces a stream of ones and zeros that are high 10% of the time. These input voltages are also the specified linear ranges of the different AMC1304 versions with performance as specified in this data sheet. If the input voltage value exceeds these ranges, the output of the modulator shows non-linear behavior when the quantization noise increases. The output of the modulator clips with a stream of only zeros with an input less than or equal to –312.5 mV (–62.5 mV for the AMC1304x05) or with a stream of only ones with an input greater than or equal to 312.5 mV (62.5 mV for the AMC1304x05). In this case, however, the AMC1304 generates a single 1 (if the input is at negative full-scale) or 0 every 128 clock cycles to indicate proper device function (see the *Fail-Safe Output* section for more details). The input voltage versus the output modulator signal is shown in Figure 50.

The density of ones in the output bit-stream for any input voltage value (with the exception of a full-scale input signal, as described in the *Output Behavior in Case of a Full-Scale Input* section) can be calculated using Equation 1:

$$\frac{V_{IN} + V_{Clipping}}{2 * V_{Clipping}} \quad (1)$$

The AMC1304 system clock is typically 20 MHz and is provided externally at the CLKIN pin. Data are synchronously provided at 20 MHz at the DOUT pin. Data change at the CLKIN falling edge. For more details, see the *Switching Characteristics* table.

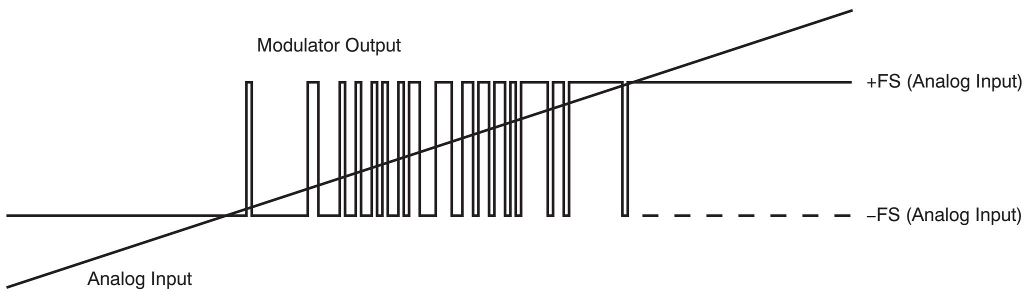


Figure 50. Analog Input versus AMC1304 Modulator Output

8.4 Device Functional Modes

8.4.1 Fail-Safe Output

In the case of a missing high-side supply voltage (LDOIN), the output of a ΔΣ modulator is not defined and can cause a system malfunction. In systems with high safety requirements, this behavior is not acceptable. Therefore, the AMC1304 implements a fail-safe output function that ensures the device maintains its output level in case of a missing LDOIN, as shown in Figure 51.

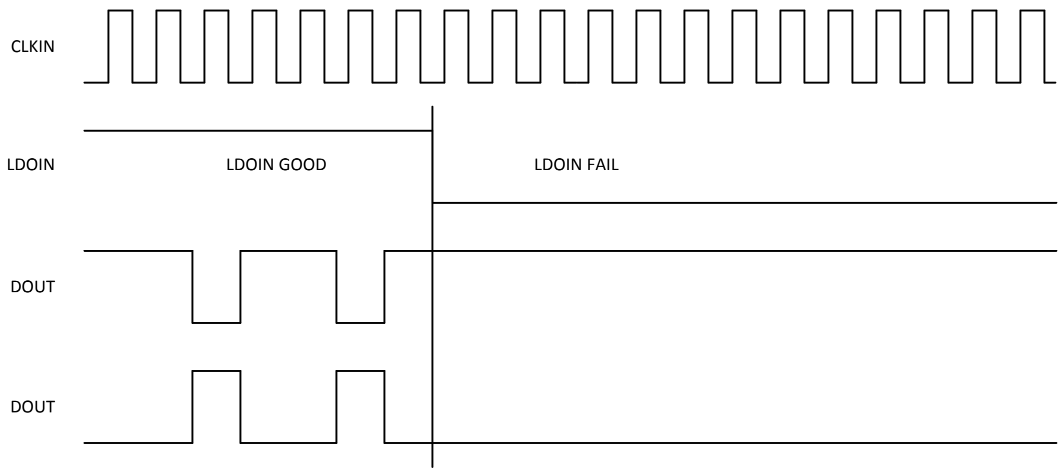


Figure 51. Fail-Safe Output of the AMC1304

8.4.2 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC1304 (that is, $V_{IN} \geq V_{Clipping}$), the device generates a single one or zero every 128 bits at DOUT, depending on the actual polarity of the signal being sensed, as shown in Figure 52. In this way, differentiating between a missing LDOIN and a full-scale input signal is possible on the system level.

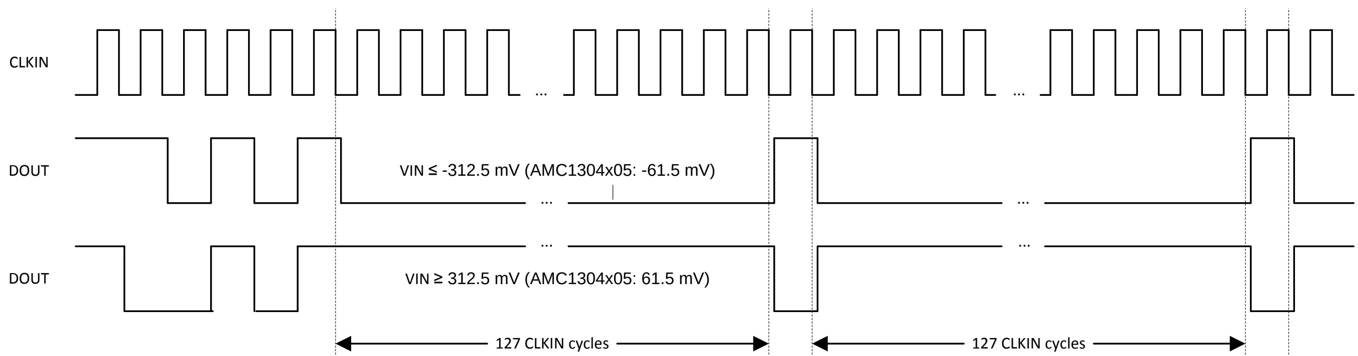


Figure 52. Overrange Output of the AMC1304

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Digital Filter Usage

The modulator generates a bit stream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, built with minimal effort and hardware, is a sinc^3-type filter, as shown in Equation 2:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \quad (2)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All the characterization in this document is also done with a sinc^3 filter with an oversampling ratio (OSR) of 256 and an output word duration of 16 bits.

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 53 shows the ENOB of the AMC1304 with different oversampling ratios. In this document, this number is calculated from the SNR by using Equation 3:

$$SNR = 1.76dB + 6.02dB * ENOB \quad (3)$$

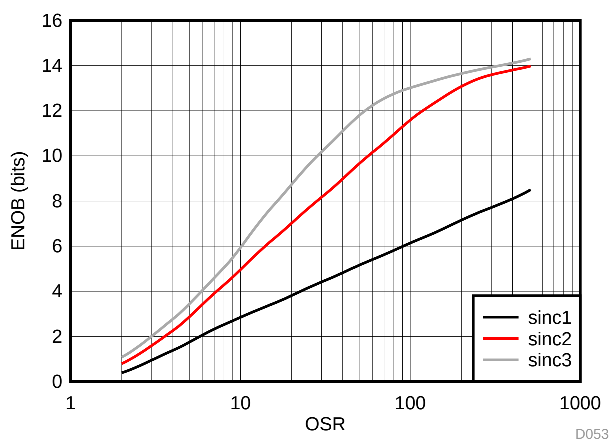


Figure 53. Measured Effective Number of Bits versus Oversampling Ratio

An example code for implementing a sinc^3 filter in an FPGA is discussed in the *Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications* application note (SBAA094), available for download at www.ti.com.

9.2 Typical Applications

9.2.1 Frequency Inverter Application

Isolated ΔΣ modulators are being widely used in new-generation frequency inverter designs because to their high ac and dc performance. Frequency inverters are critical parts of industrial motor drives, photovoltaic inverters (string and central inverters), uninterruptible power supplies (UPS), electrical and hybrid electrical vehicles, and other industrial applications. The input structure of the AMC1304 is optimized for use with low-impedance shunt resistors and is therefore tailored for isolated current sensing using shunts.

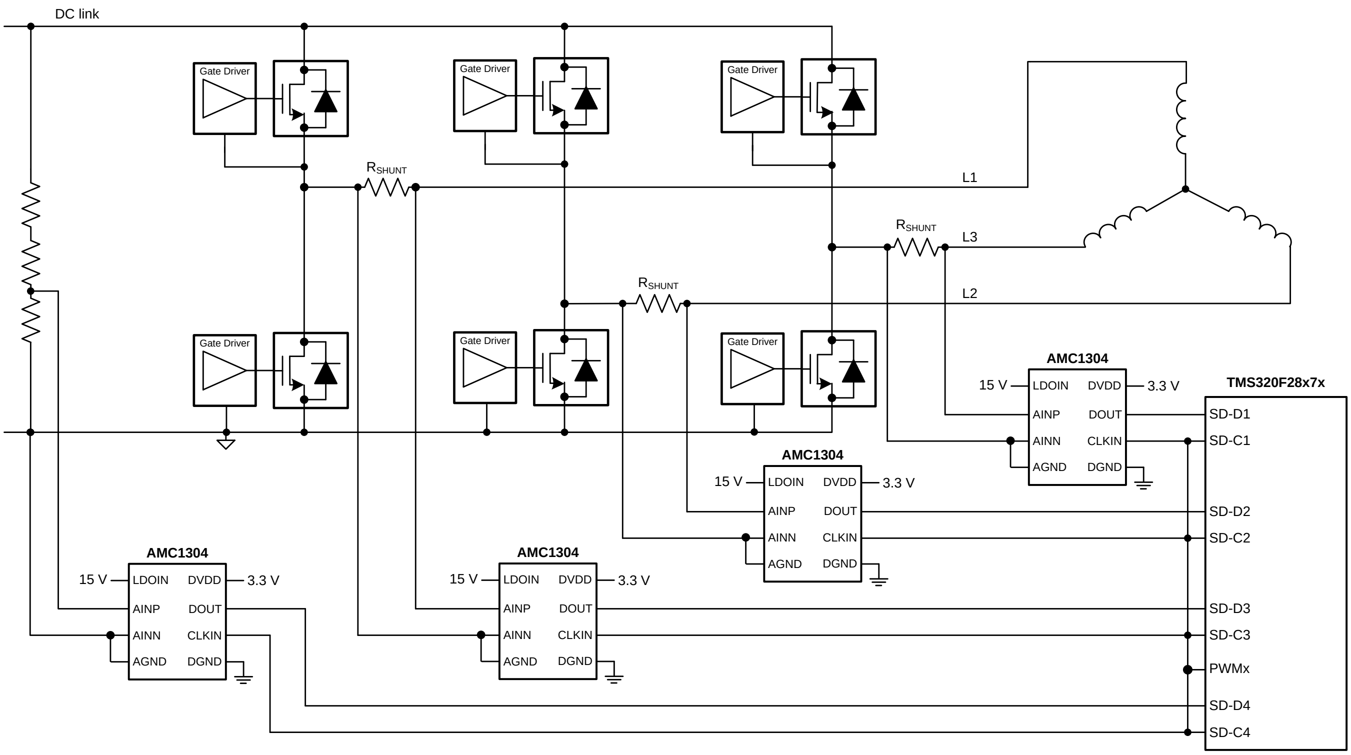


Figure 54. The AMC1304 in a Frequency Inverter Application

9.2.1.1 Design Requirements

A typical operation of the device in a frequency inverter application is shown in Figure 54. When the inverter stage is part of a motor drive system, measurement of the motor phase current is done via the shunt resistors (R_{SHUNT}). Depending on the system design, either all three or only two phase currents are sensed.

In this example, an additional fourth AMC1304 is used to support isolated voltage sensing of the dc link. This high voltage is reduced using a high-impedance resistive divider before being sensed by the device across a smaller resistor. The value of this resistor can degrade the performance of the measurement, as described in the *Isolated Voltage Sensing* section.

9.2.1.2 Detailed Design Procedure

The typically recommended RC filter in front of a ΔΣ modulator to improve signal-to-noise performance of the signal path is not required for the AMC1304. By design, the input bandwidth of the analog front-end of the device is limited to 1 MHz.

For modulator output bit-stream filtering, a device from TI's TMS320F2807x family of low-cost microcontrollers (MCUs) or TMS320F2837x family of dual-core MCUs is recommended. These families support up to eight channels of dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one fast response path for overcurrent detection.

Typical Applications (continued)

9.2.1.3 Application Curve

In motor control applications, a very fast response time for overcurrent detection is required. The time for fully settling the filter in case of a step-signal at the input of the modulator depends on its order; that is, a $sinc^3$ filter requires three data updates for full settling (with $f_{DATA} = f_{CLK}$ / OSR). Therefore, for overcurrent protection, filter types other than $sinc^3$ can be a better choice; an alternative is the $sinc^2$ filter. Figure 55 compares the settling times of different filter orders.

The delay time of the sinc filter with a continuous signal is half of its settling time.

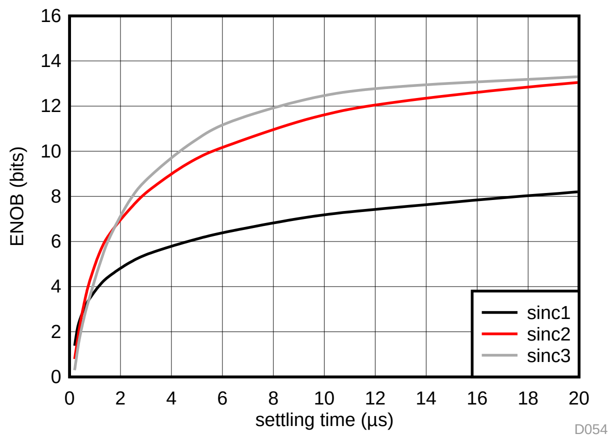


Figure 55. Measured Effective Number of Bits versus Settling Time

Typical Applications (continued)

9.2.2 Isolated Voltage Sensing

The AMC1304 is optimized for usage in current-sensing applications using low-impedance shunts. However, the device can also be used in isolated voltage-sensing applications if the affect of the (usually higher) impedance of the resistor used in this case is considered.

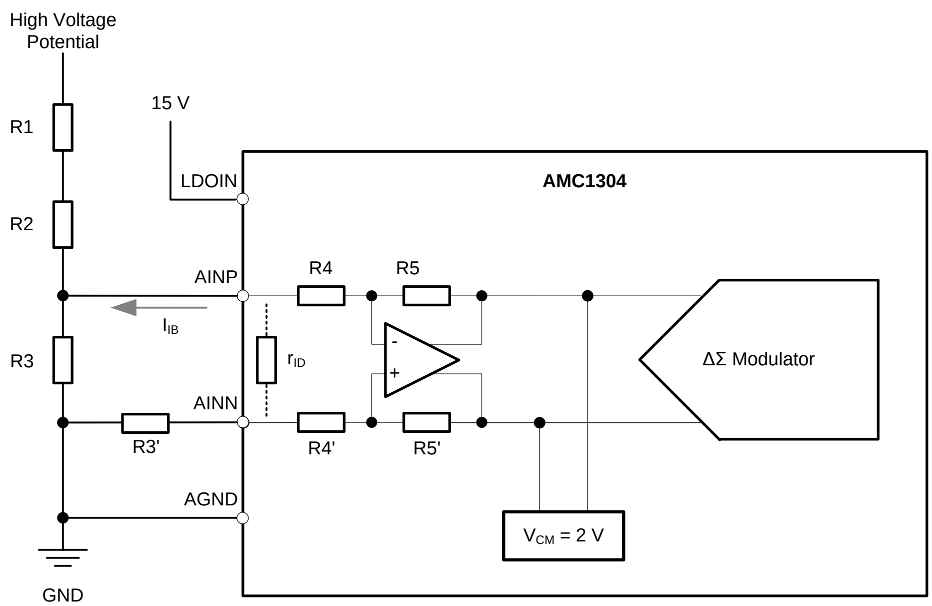


Figure 56. Using the AMC1304 for Isolated Voltage Sensing

9.2.2.1 Design Requirements

Figure 56 shows a simplified circuit typically used in high-voltage-sensing applications. The high impedance resistors (R1 and R2) are used as voltage dividers and dominate the current value definition. The resistance of the sensing resistor R3 is chosen to meet the input voltage range of the AMC1304. This resistor and the differential input impedance of the device (the AMC1304x25 is 25 kΩ, the AMC1304x05 is 5 kΩ) also create a voltage divider that results in an additional gain error. With the assumption of R1, R2, and R_{IN} having a considerably higher value than R3, the resulting total gain error can be estimated using Equation 4, with E_G being the gain error of the AMC1304.

$$\left|E_{Gtot}\right| = \left|E_G\right| + \frac{R3}{R_{IN}} \tag{4}$$

This gain error can be easily minimized during the initial system-level gain calibration procedure.

9.2.2.2 Detailed Design Procedure

As indicated in Figure 56, the output of the integrated differential amplifier is internally biased to a common-mode voltage of 2 V. This voltage results in a bias current I_{IB} through the resistive network R4 and R5 (or R4' and R5') used for setting the gain of the amplifier. The value range of this current is specified in the *Electrical Characteristics* table. This bias current generates additional offset error that depends on the value of the resistor R3. Because the value of this bias current depends on the actual common-mode amplitude of the input signal (as illustrated in Figure 57), the initial system offset calibration does not minimize its effect. Therefore, in systems with high accuracy requirements, TI recommends using a series resistor at the negative input (AINN) of the AMC1304 with a value equal to the shunt resistor R3 (that is, R3' = R3 in Figure 56) to eliminate the affect of the bias current.

Typical Applications (continued)

This additional series resistor (R3') influences the gain error of the circuit. The effect can be calculated using Equation 5 with R5 = R5' = 50 kΩ and R4 = R4' = 2.5 kΩ (for the AMC1304x05) or 12.5 kΩ (for the AMC1304x25).

$$E_G(\%) = \left(1 - \frac{R4}{R4' + R3'}\right) * 100\% \quad (5)$$

9.2.2.3 Application Curve

Figure 57 shows the dependency of the input bias current on the common-mode voltage at the input of the AMC1304.

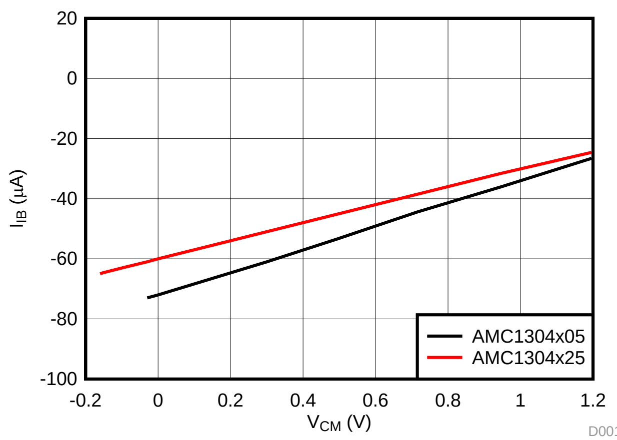


Figure 57. Input Current vs Input Common-Mode Voltage

9.2.3 Do's and Don'ts

Do not leave the inputs of the AMC1304 unconnected (floating) when the device is powered up. If both modulator inputs are left floating, the input bias current drives them to the output common-mode of the analog front end of approximately 2 V that is above the specified input common-mode range. As a result, the front gain diminishes and the modulator outputs a bitstream resembling a zero input differential voltage.

10 Power-Supply Recommendations

In a typical frequency-inverter application, the high-side power supply (LDOIN) for the device is directly derived from the floating power supply of the upper gate driver. A low-ESR decoupling capacitor of 0.1 µF is recommended for filtering this power-supply path. Place this capacitor (C2 in Figure 58) as close as possible to the LDOIN pin of the AMC1304 for best performance. If better filtering is required, an additional 10-µF capacitor can be used. The output of the internal LDO requires a decoupling capacitor of 0.1 µF to be connected between the VCAP pin and AGND as close as possible to the device.

The floating ground reference (AGND) is derived from the end of the shunt resistor, which is connected to the negative input (AINN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads and AGND is connected to one of the outer leads of the shunt.

For decoupling of the digital power supply on the controller side, TI recommends using a 0.1-µF capacitor assembled as close to the DVDD pin of the AMC1304 as possible, followed by an additional capacitor in the range of 1 µF to 10 µF.

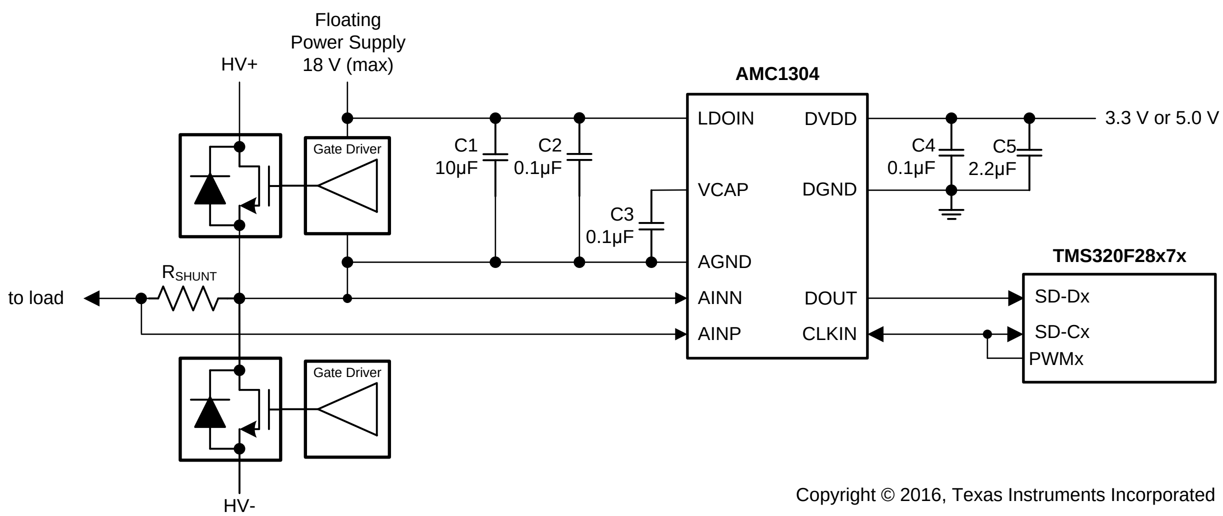


Figure 58. Decoupling the AMC1304

11 Layout

11.1 Layout Guidelines

A layout recommendation showing the critical placement of the decoupling capacitors (as close as possible to the AMC1304) and placement of the other components required by the device is shown in Figure 59. For best performance, place the shunt resistor close to the VINP and VINN inputs of the AMC1304 and keep the layout of both connections symmetrical.

For the AMC1304Lx version, place the 100-Ω termination resistor as close as possible to the CLKIN, CLKIN_N inputs of the device to achieve highest signal integrity. If not integrated, an additional termination resistor is required as close as possible to the LVDS data inputs of the MCU or filter device; see Figure 60.

11.2 Layout Examples

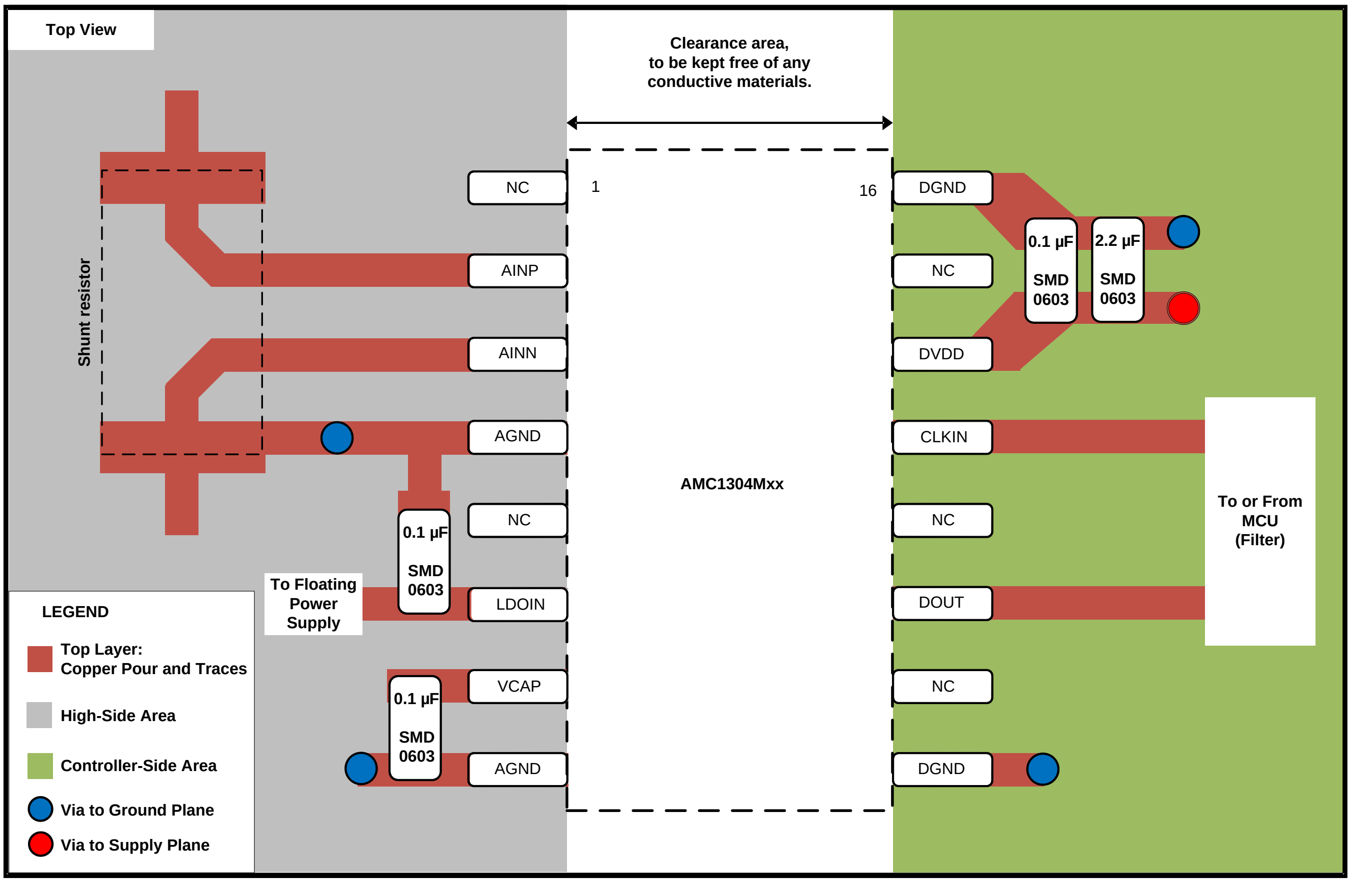


Figure 59. Recommended Layout of the AMC1304Mx

Layout Examples (continued)

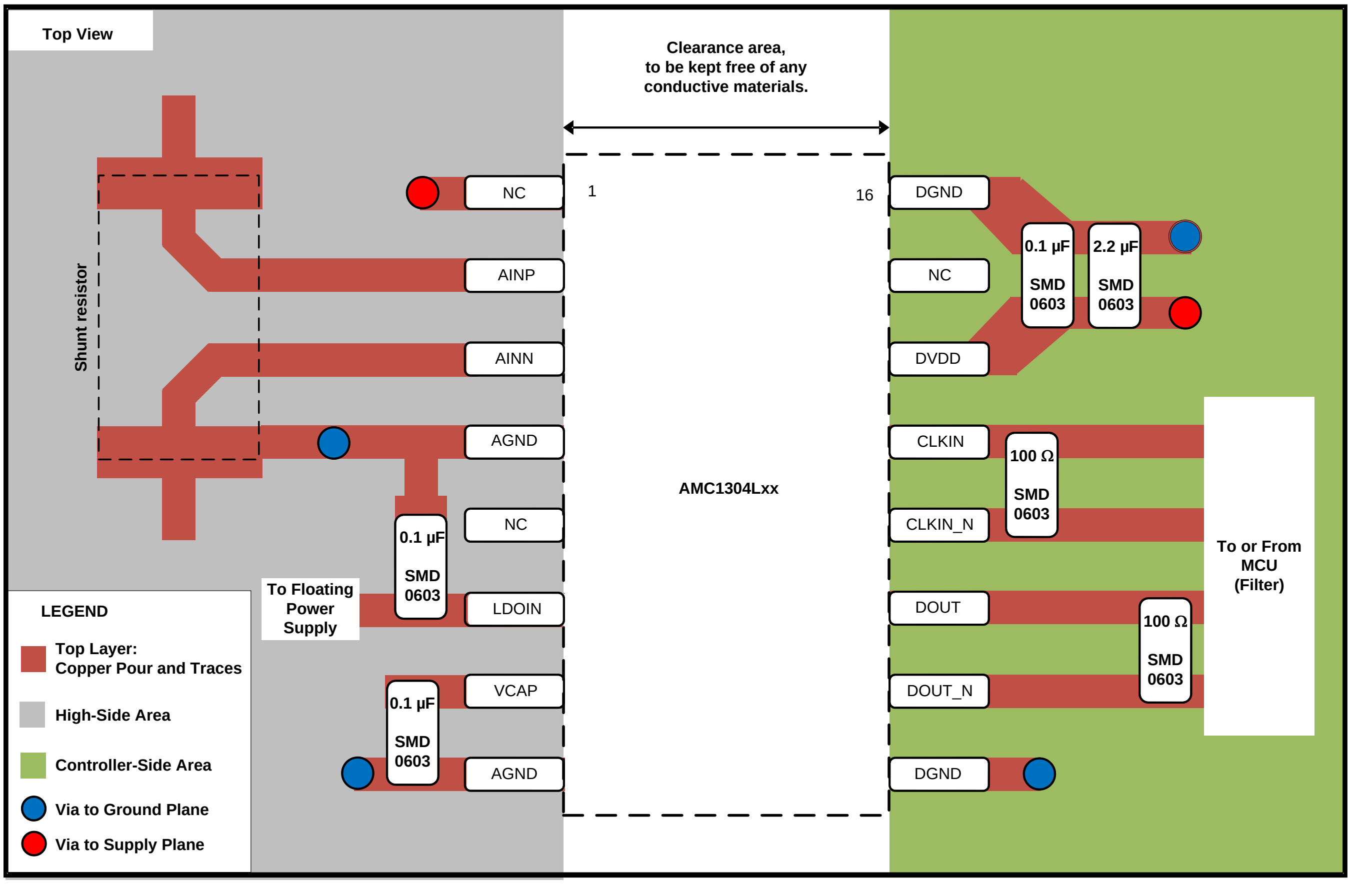


Figure 60. Recommended Layout of the AMC1304Lx

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *AMC1210 Quad Digital Filter for 2nd-Order Delta-Sigma Modulator* (SBAS372)
- *MSP430F677x Polyphase Metering SoCs* (SLAS768)
- *TMS320F2807x Piccolo™ Microcontrollers* (SPRS902)
- *TMS320F2837xD Dual-Core Delfino™ Microcontrollers* (SPRS880)
- *Isolation Glossary* (SLLA353)
- *ISO72x Digital Isolator Magnetic-Field Immunity* (SLLA181)
- *Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications* (SBAA094)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
AMC1304L05	Click here	Click here	Click here	Click here	Click here
AMC1304L25	Click here	Click here	Click here	Click here	Click here
AMC1304M05	Click here	Click here	Click here	Click here	Click here
AMC1304M25	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1304L05DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1304L05	Samples
AMC1304L05DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1304L05	Samples
AMC1304L25DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1304L25	Samples
AMC1304L25DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1304L25	Samples
AMC1304M05DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1304M05	Samples
AMC1304M05DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1304M05	Samples
AMC1304M25DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1304M25	Samples
AMC1304M25DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1304M25	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

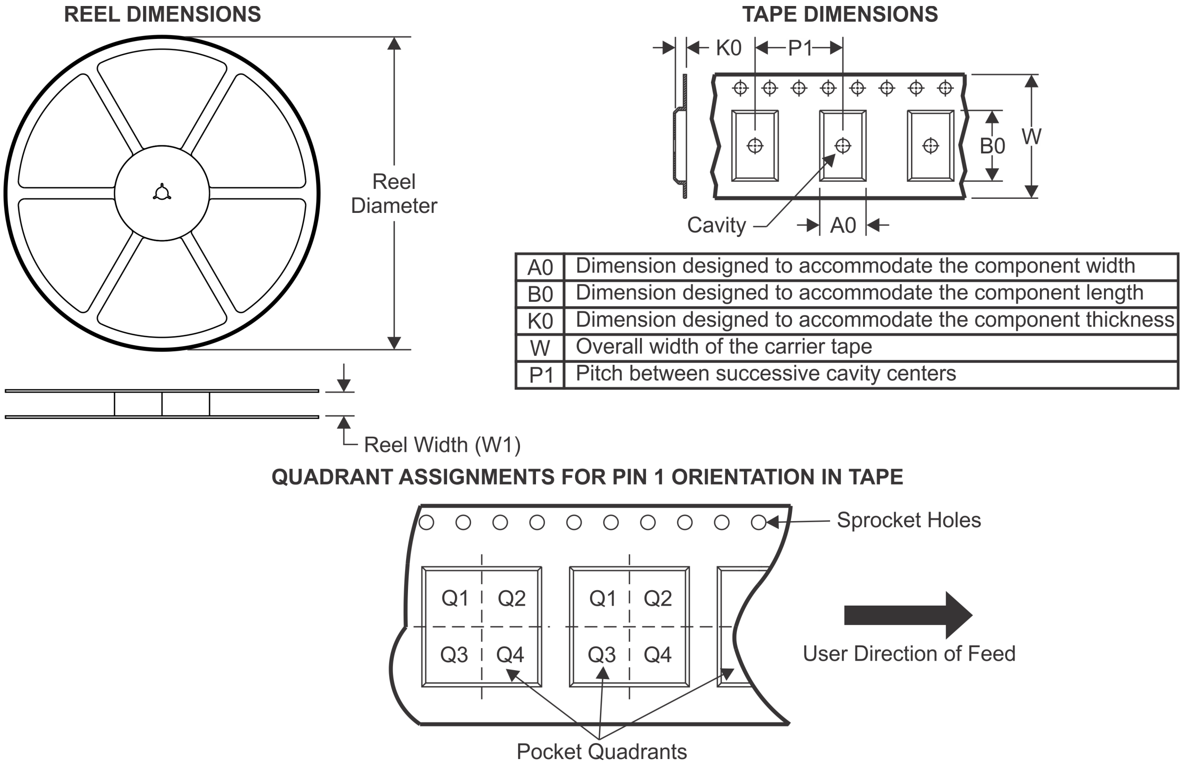
[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

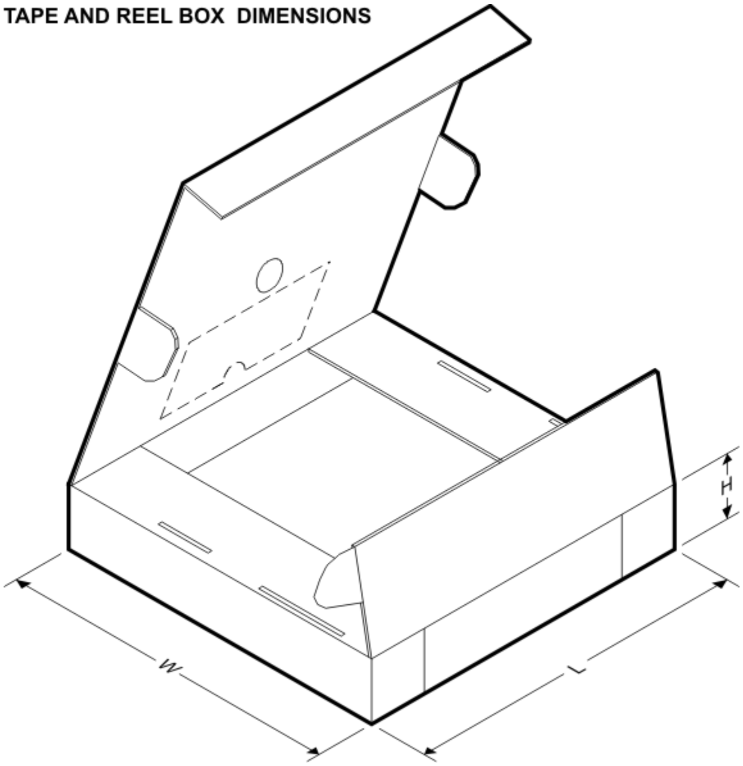
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1304L05DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
AMC1304M05DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

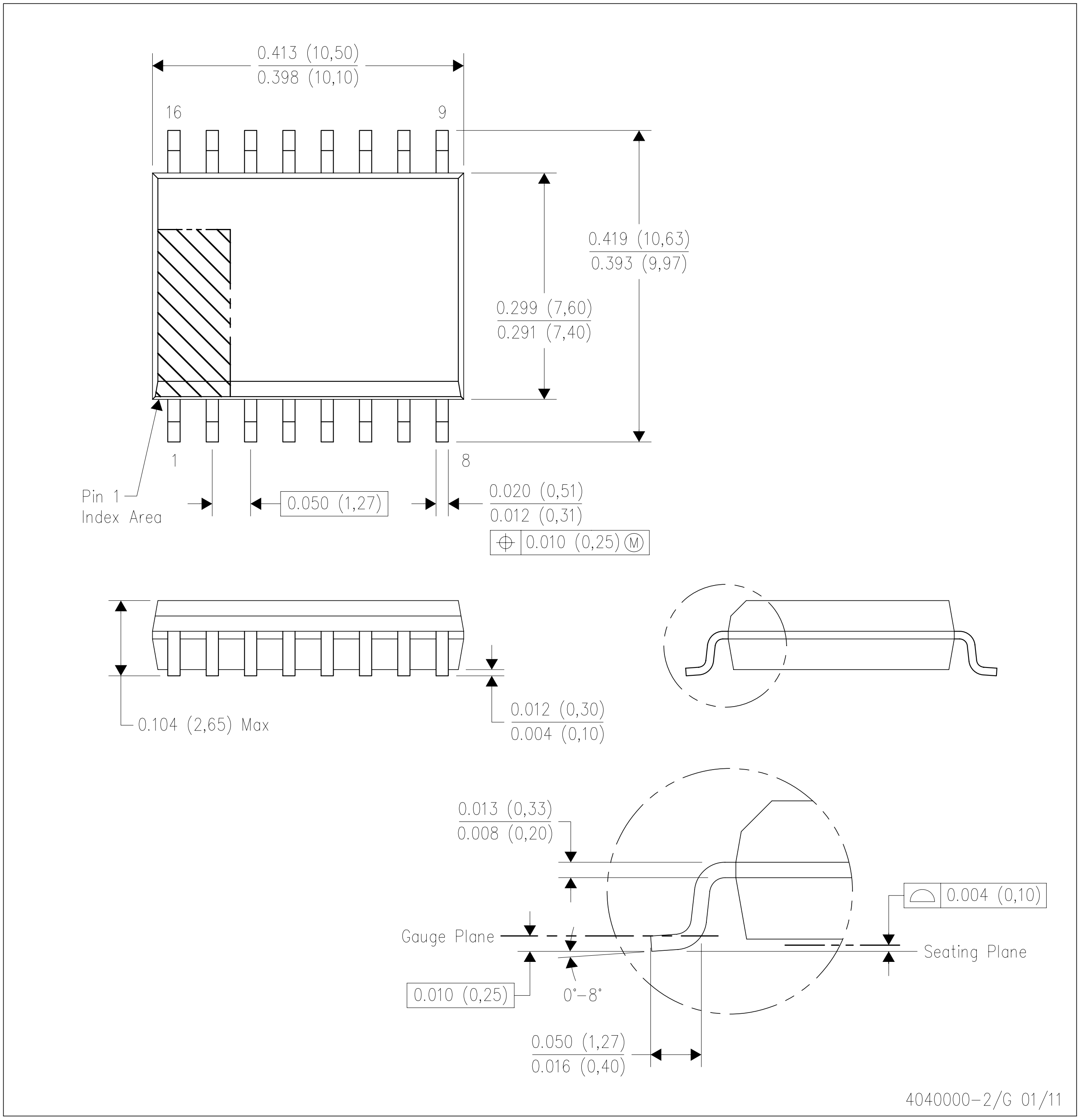
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

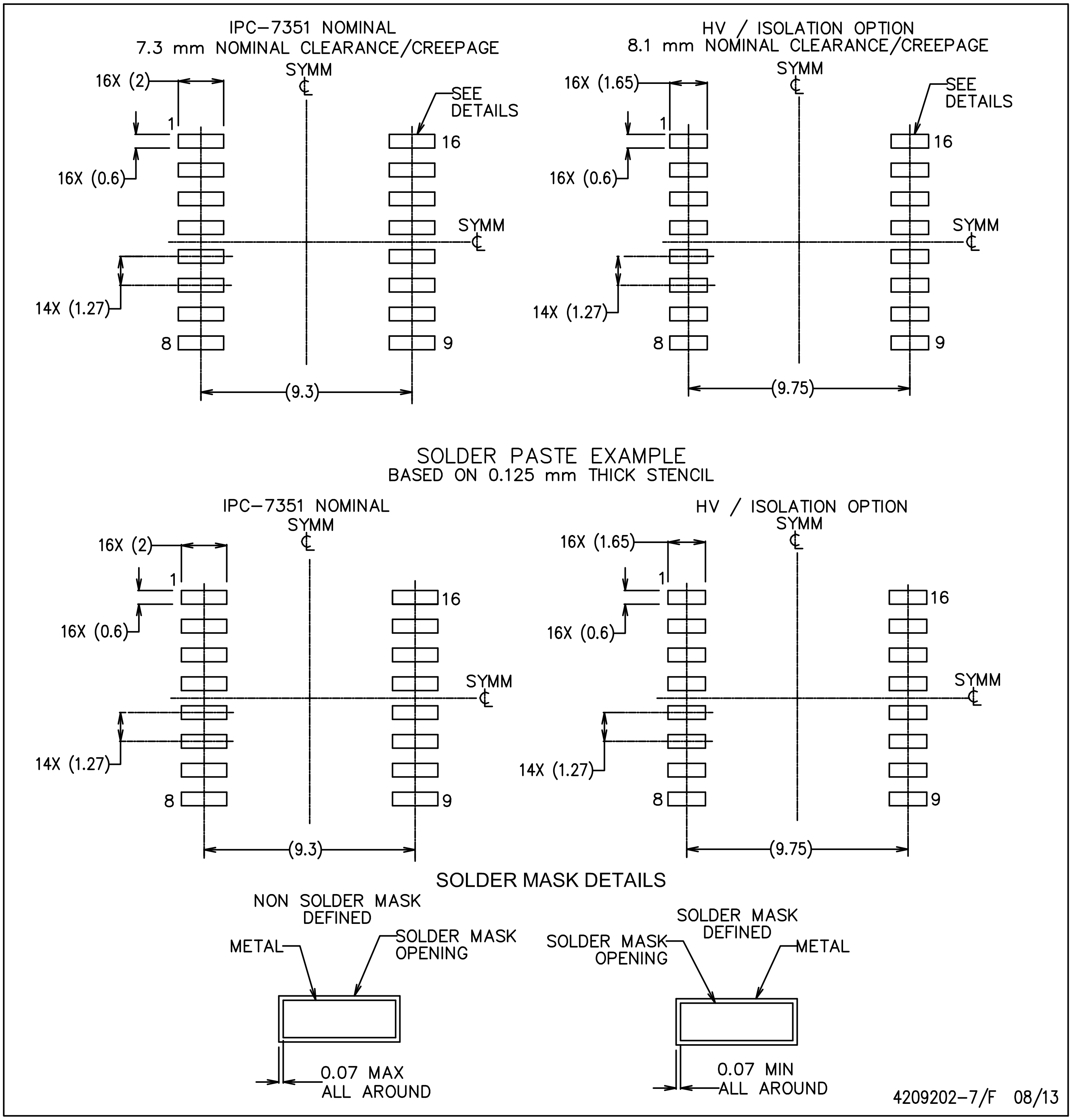
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1304L05DWR	SOIC	DW	16	2000	367.0	367.0	38.0
AMC1304M05DWR	SOIC	DW	16	2000	367.0	367.0	38.0

DW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- E. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC–7525 may have alternate design recommendations.
- F. Board assembly site may have different recommendations for stencil design.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265