bq24308 Overvoltage and Overcurrent Protection IC and Li+ Charger Front-End Protection IC

1 Features

- Provides Protection for Three Variables:
  - Input Overvoltage
  - Input Overcurrent with Current Limiting
  - Battery Overvoltage
- Maximum Input Voltage of 30 V
- Supports Up to 1.5-A Input Current
- Robust Against False Triggering Due to Current Transients
- Thermal Shutdown
- LDO Mode Voltage Regulation of 5 V
- Available in Space-Saving Small 2 mm × 2 mm 8-Pin WSON Package

2 Applications

- Mobile and Smart Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices
- Bluetooth™ Headsets

3 Description

The bq24308 device is a highly integrated circuit (IC) designed to provide protection to Li-ion batteries from failures of the charging circuit. The device continuously monitors the input voltage, the input current, and the battery voltage. In case of an input overvoltage condition, the device immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current to a safe value for a blanking duration before turning the switch off. Battery voltage may also be monitored and if the battery voltage exceeds the specified value the internal switch is turned off. Additionally, the device also monitors its own die temperature and switches off if it becomes too hot.

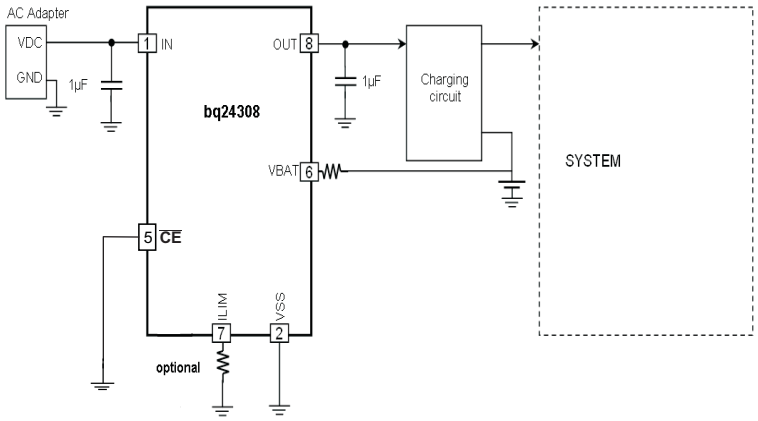
The input overcurrent threshold can be increased using an external resistor. The device also offers optional protection against reverse voltage at the input using an external P-channel FET.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24308	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2009) to Revision B **Page**

- Changed SON to WSON throughout the document ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed the location of the ESD information from the ABS MAX table to the news ESD Ratings table ... 4
- Moved Figures 1 through 10 from *Typical Characteristics* to *Application Curves* section ... 14

Changes from Original (September 2009) to Revision A **Page**

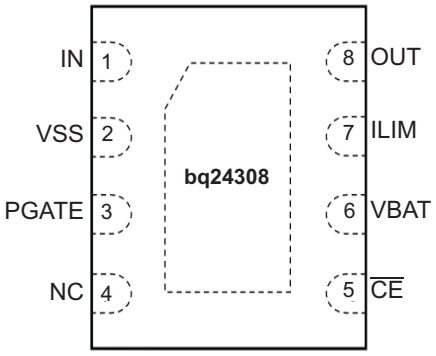
- Changed Units from V to A for Input and Output Current spec in Absolute Maximum Ratings table. ... 4
- Changed $V_{O(REG)}$ test condition, I_{OUT} value from 50 mA to 250 mA ... 5
- Added T_J = 0°C to 125°C to test conditions for I_{OCP} spec. ... 5
- Changed Q_{EXT} device symbol in the Input Reverse-Polarity Protection schematic. ... 14

5 Device Comparison Table

PART NUMBER	MARKING	MEDIUM	QUANTITY	PACKAGE
bq24308DSGR	DAS	Tape and Reel	3000	2.00 mm × 2.00 mm WSON
bq24308DSGT	DAS	Tape and Reel	250	2.00 mm × 2.00 mm WSON

6 Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{CE}$	5	I	Chip enable input. Active low. When $\overline{CE}$ = High, the input FET is off. Internally pulled down.
ILIM	7	I	Input overcurrent threshold programming. An optional external resistor can be used to increase input overcurrent threshold. Connect a resistor to VSS to increase the OCP threshold.
IN	1	I	Input power, connect to external DC supply. Connect external 0.1µF (minimum) ceramic capacitor to VSS.
NC	4	—	Do not connect to any external circuit. This pin may have internal connections used for test purposes.
OUT	8	O	Output terminal to the charging system. Connect external 1-µF capacitor (minimum) ceramic capacitor to VSS.
PGATE	3	O	Gate drive for optional external P-FET
VBAT	6	I	Battery voltage sense input. Connect to pack positive terminal through a resistor.
VSS	2	—	Ground terminal
Thermal Pad			There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed-circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN, PGATE (with respect to VSS)	–0.3	30	V
	OUT (with respect to VSS)	–0.3	12	
	ILIM, $\overline{CE}$, VBAT (with respect to VSS)	–0.3	7	
Input current	IN		2	A
Output current	OUT		2	A
	PGATE		5	mA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±500	
		IN (IEC 61000-4-2)(3)	Air Discharge	±15000	
			Contact	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) With IN bypassed to the VSS with a 1-µF low-ESR ceramic capacitor

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	3.3		26	V
I_{IN}	Input current, IN pin			1.5	A
I_{OUT}	Output current, OUT pin			1.5	A
R_{ILIM}	OCP programming resistor	31			kΩ
T_J	Junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		bq24308 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over junction temperature range –40°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN						
V_{UVLO}	Undervoltage lock-out, input power detected threshold	$\overline{CE}$= Low, V_{IN}: 0 V → 3 V	2.5	2.7	2.8	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	$\overline{CE}$= Low, V_{IN}: 3 V → 0 V	200	260	300	mV
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	$\overline{CE}$ = Low. Time measured from V_{IN} 0V → 4 V 1 µs rise-time, to output turning ON		8		ms
I_{DD}	Operating current	$\overline{CE}$= Low, V_{IN} = 5 V, no load on OUT pin		410	500	µA
I_{STDBY}	Standby current	$\overline{CE}$= High, V_{IN} = 5 V		65	95	µA
INPUT TO OUTPUT CHARACTERISTICS						
V_{DO}	Drop-out voltage IN to OUT	$\overline{CE}$ = Low, V_{IN} = 4 V, I_{OUT} = 250 mA		45	75	mV
INPUT OVERVOLTAGE PROTECTION						
V_{OVP}	Input overvoltage protection threshold	$\overline{CE}$= Low, V_{IN}: 4 V to 10 V	6.1	6.3	6.5	V
$V_{HYS-OVP}$	Hysteresis on OVP	$\overline{CE}$= Low, V_{IN}: 10 V to 4 V	20	60	110	mV
$t_{PD(OVP)}$	Input OVP propagation delay(1)	$\overline{CE}$= Low, Time measured from V_{IN} 4 V → 10 V, 1µs rising time, to output turning OFF		0.2	1	µs
$t_{ON(OVP)}$	Recovery time from input overvoltage condition	$\overline{CE}$ = Low, Time measured from V_{IN} 10 V → 4V, 1 µs fall-time, to output turning ON		8		ms
OUTPUT VOLTAGE REGULATION						
$V_{O(REG)}$	Output voltage	$\overline{CE}$ = Low, V_{IN}= 6 V, I_{OUT} = 250 mA	4.85	5	5.15	V
INPUT OVERCURRENT PROTECTION						
I_{OCP}	Internal input overcurrent protection threshold	$\overline{CE}$= Low, V_{IN} = 5V, ILIM floating; T_J = 0°C to 125°C	630	700	770	mA
	Input overcurrent protection range	$\overline{CE}$ = Low, V_{IN} = 5V; T_J = 0°C to 125°C	630		1500	mA
ΔI_{OCP}	OCP threshold accuracy	T_J = 0°C to 125°C		±10%		
		T_J = –40°C to 125°C		±13%		
K_{ILIM}	Current limit programming: IOCP(program) = I_{OCP} + K_{ILIM} ÷ R_{ILIM}			25000		AΩ
$t_{BLANK(OCP)}$	Blanking time, input overcurrent detected	$\overline{CE}$= Low		5		ms
$t_{REC(OCP)}$	Recovery time from input overcurrent condition	$\overline{CE}$ = Low		64		ms
BATTERY OVERVOLTAGE PROTECTION						
BV_{OVP}	Battery overvoltage protection threshold	$\overline{CE}$ = Low, V_{IN} > 4.4 V, V_{VBAT}: 4.2 V → 4.5 V	4.3	4.35	4.40	V
$V_{HYS-BOVP}$	Hysteresis on BV_{OVP}	$\overline{CE}$= Low, V_{IN} > 4.4 V, V_{VBAT}: 4.5 V → 3.9 V	200	275	320	mV
I_{VBAT}	Input bias current on VBAT pin	V_{VBAT} = 4.4 V, T_J = 25°C			10	nA
$t_{DGL(BOVP)}$	Deglitch time, battery overvoltage detected	$\overline{CE}$= Low, V_{IN} > 4.4 V, time measured from V_{VBAT} 4.2 V → 4.5 V, 1 µs rising time, to output turning OFF		176		µs
THERMAL PROTECTION						
$T_{J(OFF)}$	Thermal shutdown temperature			140	150	°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
P-FET GATE DRIVER						
V_{GCLMP}	Gate driver clamp voltage	V_{IN} > 17 V	13	15	17	V

(1) Not tested in production. Specified by design.

Electrical Characteristics (continued)

over junction temperature range –40°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC LEVELS ON $\overline{CE}$						
V_{IL}	Low-level input voltage		0		0.4	V
V_{IH}	High-level input voltage		1.4			V
I_{IL}	Low-level input current				1	µA
I_{IH}	High-level input current	V_{CE} = 1.8 V			15	µA

7.6 Typical Characteristics

Test conditions (unless otherwise noted) for typical operating performance are: V_{IN} = 5 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, R_{BAT} = 100 kΩ, R_{OUT} = 16 Ω, T_A = 25°C (see *Figure 12*)

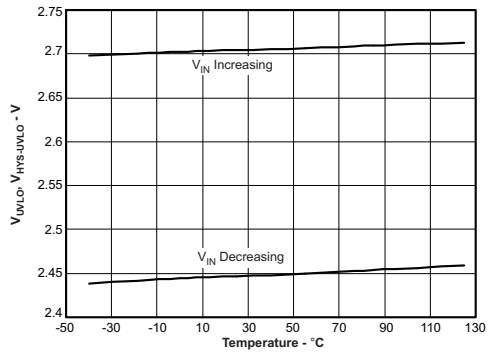


Figure 1. Undervoltage Lockout vs Free-Air Temperature

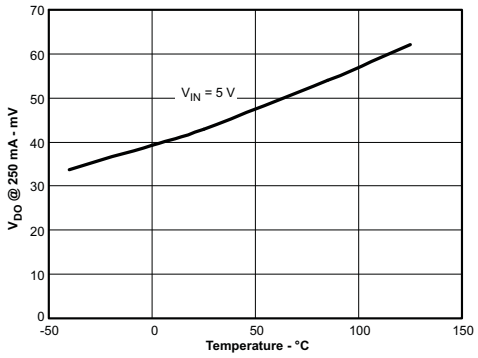


Figure 2. Dropout Voltage (IN to OUT) vs Free-Air Temperature

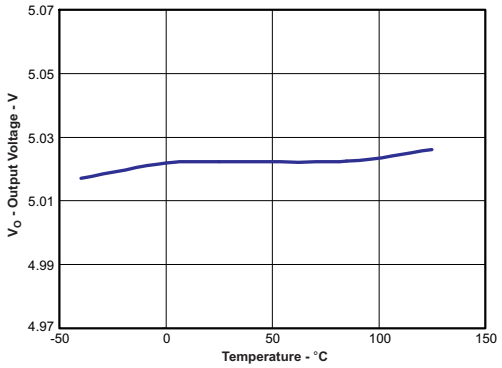


Figure 3. Regulation Voltage (OUT Pin) vs Free-Air Temperature

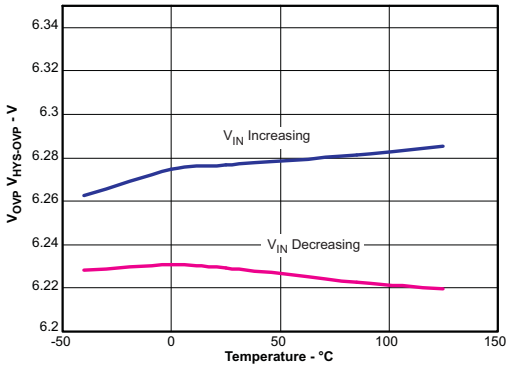


Figure 4. OVP Threshold vs Free-Air Temperature

Typical Characteristics (continued)

Test conditions (unless otherwise noted) for typical operating performance are: V_{IN} = 5 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, R_{BAT} = 100 kΩ, R_{OUT} = 16 Ω, T_A = 25°C (see *Figure 12*)

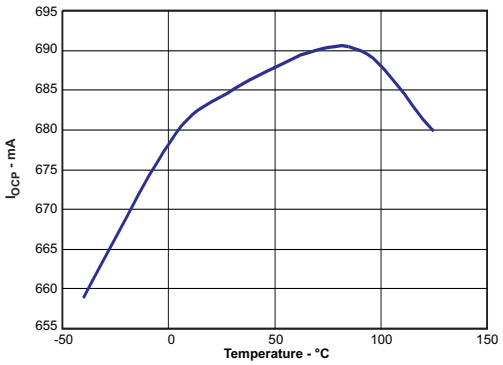


Figure 5. OCP Threshold vs Free-Air Temperature

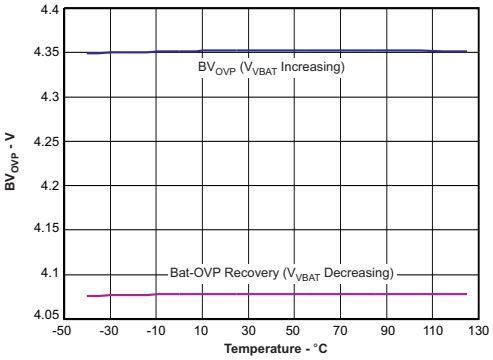


Figure 6. Battery OVP Thresholds vs Free-Air Temperature

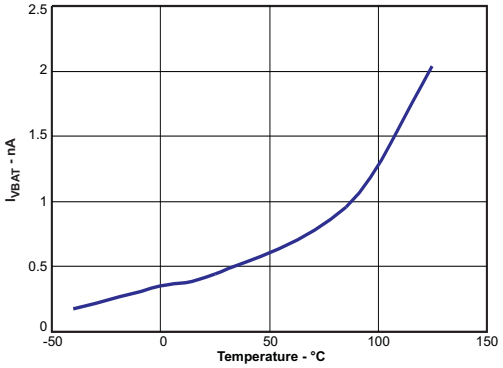


Figure 7. Leakage Current (BAT pin) vs Free-Air Temperature

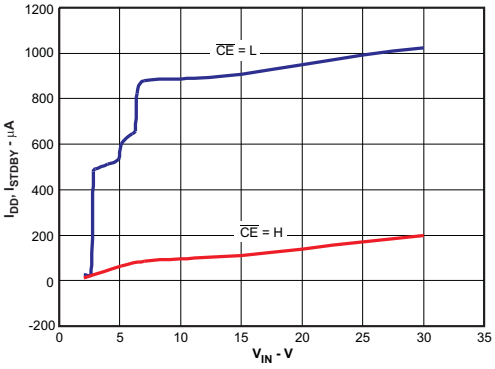


Figure 8. Supply Current vs Input Voltage

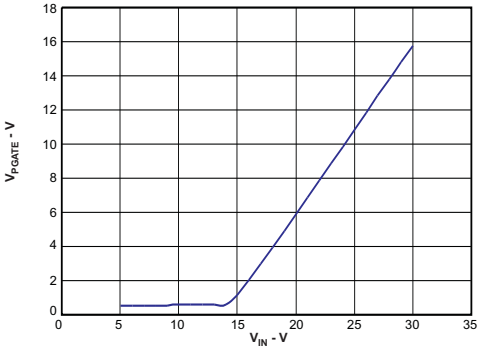


Figure 9. PGATE Voltage vs Input Voltage

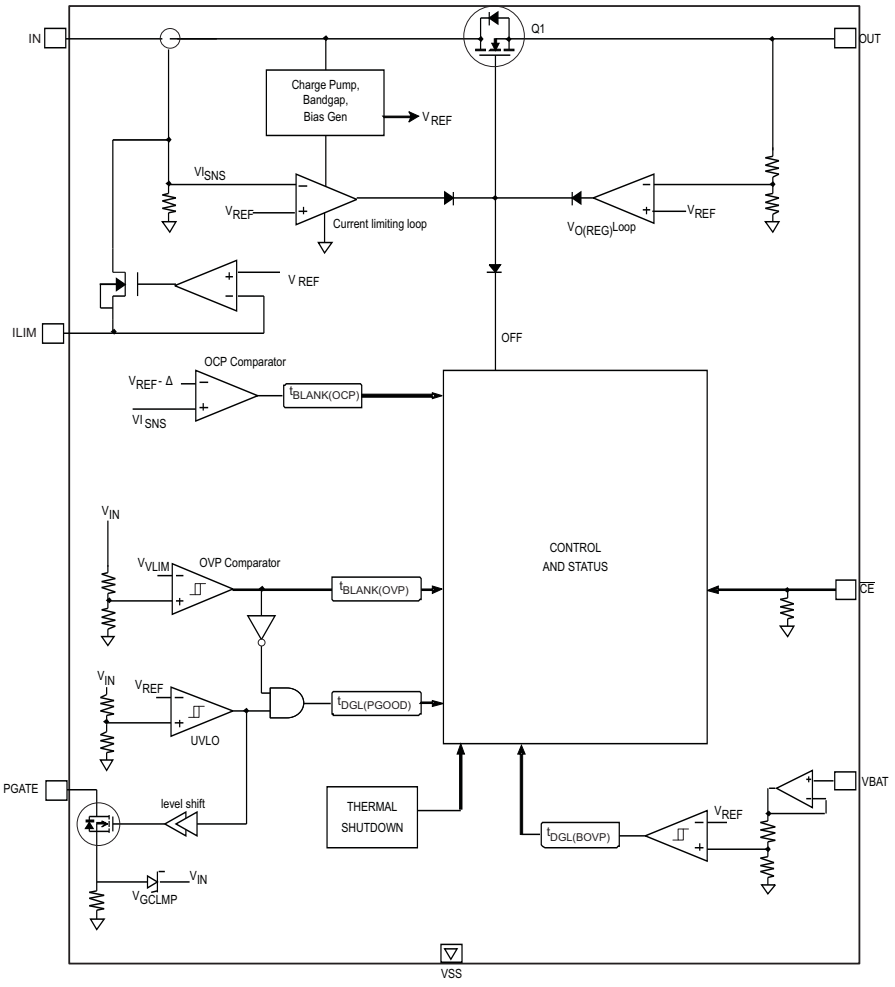
8 Detailed Description

8.1 Overview

The bq24308 device is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The device continuously monitors the input voltage, the input current, and the battery voltage. In case of an input overvoltage condition, the device immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the current to a safe value for a blanking duration before turning the switch off. Additionally, the device also monitors its own die temperature and switches off if it becomes too hot.

The input and overcurrent threshold is user-programmable. The device can be controlled by a processor using the CE pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Overvoltage Protection

The bq24308 device integrates an input overvoltage protection feature to protect downstream devices from faulty input sources. If the input voltage rises above V_{OVP}, the internal FET Q1 is turned off, removing power from the circuit. As shown in Figure 16 to Figure 17, the response is very rapid, with the FET turning off in less than a microsecond. When the input voltage returns below $V_{OVP} – V_{hys(OVP)}$ (but is still above UVLO), the FET Q1 is turned on again after a deglitch time of $t_{ON(OVP)}$ to ensure that the input supply has stabilized. Figure 18 shows the recovery from input OVP.

8.3.2 Input Overcurrent Protection

The device can supply load current up to I_{OCP} continuously. If the load current tries to exceed this threshold, the current limits I_{OCP} for a maximum duration of $t_{BLANK(OCP)}$. If the load current returns to less than I_{OCP} before $t_{BLANK(OCP)}$ times out, the device continues to operate (see Figure 19). However, if the overcurrent situation persists for $t_{BLANK(OCP)}$, the FET Q1 is turned off for a duration of $t_{REC(OCP)}$. The FET is then turned on again and the current is monitored all over again (see Figure 20 and Figure 21).

To prevent the input voltage from spiking up due to the inductance of the input cable, Q1 is turned off slowly in an overcurrent fault condition, resulting in a "soft-stop", as shown in Figure 22. The overcurrent threshold is programmed to a level greater than I_{OCP} by connecting a resistor R_{ILIM} from the ILIM pin to VSS. The programmed overcurrent threshold is given by the following equation:

$$I_{OCP(program)} = I_{OCP} + K_{ILIM} \div R_{ILIM}. \quad (1)$$

8.3.3 Battery Overvoltage Protection

The battery overvoltage threshold B_{VOVP} is internally set to 4.35 V. If the battery voltage exceeds the BV_{OVP} threshold for longer than $t_{DGL(BOVP)}$, the FET Q1 is turned off (see Figure 23). This switch-off is also a soft-stop. The FET Q1 is turned ON (soft-start) once the battery voltage drops to $BV_{OVP} – V_{HYS-BOVP}$.

8.3.4 Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, FET Q1 is turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} – T_{J(OFF-HYS)}$.

8.3.5 Enable Function

The device has an enable pin, which can be used to enable or disable the device. When the $\overline{CE}$ pin is driven high, the internal FET is turned off. When the $\overline{CE}$ pin is low, the FET is turned on if other conditions are safe. The $\overline{CE}$ pin has an internal pulldown resistor of 200 kΩ (typical) and can be left floating.

8.3.6 PGATE Output

The bq24308 contains an external PFET driver (PGATE) for reverse polarity protection. When used with an external P-Channel MOSFET, in addition to OVP, OCP, and Battery-OVP, the device offers protection against input reverse polarity up to –30 V. When an input source with correct polarity is connected, the device first turns on due to current flow through the body-diode of the external FET. The PGATE pin then goes low, turning ON the external FET. For input voltages larger than V_{GCLMP}, the voltage on the PGATE pin is driven to $V_{IN} – V_{GCLMP}$. This ensures that the gate to source voltage seen by the external FET does not exceed $–V_{GCLMP}$.

8.4 Device Functional Modes

8.4.1 OPERATION Mode

The bq24308 device continuously monitors the input voltage, the input current, and the battery voltage. As long as the input voltage is less than V_{OVP}, the output voltage tracks the input voltage (less the drop caused by $R_{DS}ON$ of Q1). During fault conditions, the internal FET is turned off and the output is isolated from the input source.

8.4.2 POWER-DOWN Mode

The device remains in POWER-DOWN mode when the input voltage at the IN pin is below the undervoltage lock-out threshold, V_{UVLO}. The FET Q1 (see *Functional Block Diagram*) connected between IN and OUT pins is off. See Figure 10.

8.4.3 POWER-ON RESET Mode

The device resets all internal timers when the input voltage at the IN pin exceeds the UVLO threshold. The gate driver for the external P-FET is enabled. The device then waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are safe, FET Q1 is turned ON. The device has a soft-start feature to control the inrush current. This soft-start minimizes voltage ringing at the input (the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). Figure 14 shows the power-up behavior of the device. Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, as shown in Figure 15.

Device Functional Modes (continued)

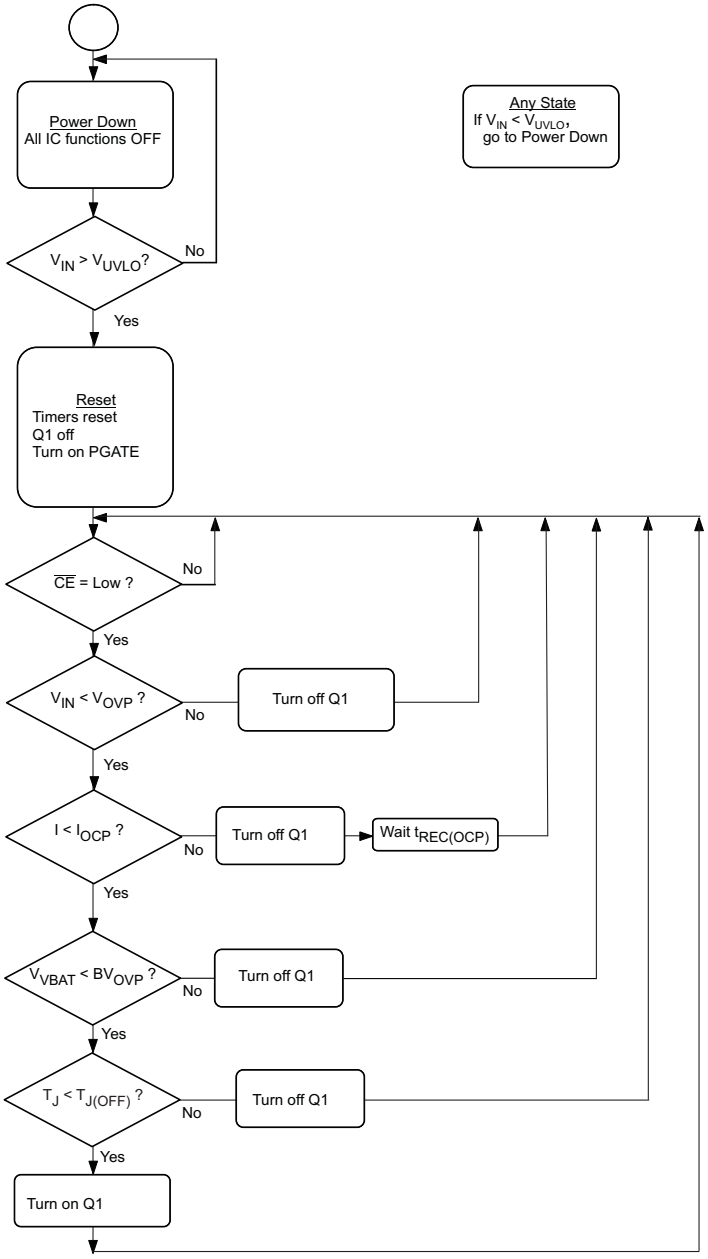


Figure 10. State Diagram

9 Application and Implementation

NOTE

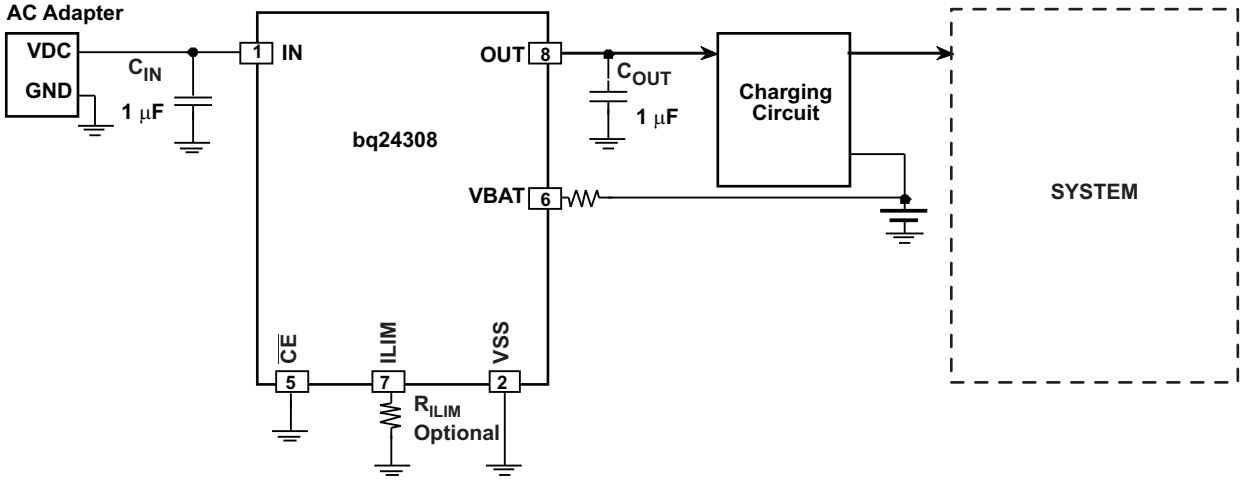
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq24308 device protects against overvoltage, overcurrent, and battery overvoltage events that occur due to faulty adapter or other input sources. If any of these faults occur, the bq24308 device isolates the downstream devices from the input source.

9.2 Typical Application

The typical values for an application are V_{OVP} = 6.3 V, I_{OCP} = 700 mA, and BV_{OVP} = 4.35 V.



Terminal numbers shown are for the 2 × 2 DSG package.

Figure 11. Typical Application Diagram

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply Voltage	5 V
INILIM	1 A

9.2.2 Detailed Design Procedure

9.2.2.1 Selection of R_{BAT}

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the device, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30 V, and applying 30 V to the battery in case of the failure of the device and can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in case of failure of the device. In the interests of safety, R_{BAT} should have a very high value. The problem with a large R_{BAT} is that the voltage drop across this resistor because of the VBAT bias current I_{VBAT} causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.35-V BV_{OVP} threshold.

Choosing R_{BAT} in the range from 100 KΩ to 470 kΩ is a good compromise. In the case of a device failure, with R_{BAT} equal to 100 kΩ, the maximum current flowing into the battery would be (30 V – 3 V) ÷ 100 kΩ = 270 µA, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 100 kΩ would result in a worst-case voltage drop of $R_{BAT} \times I_{VBAT}$ = 1 mV. This is negligible compared to the internal tolerance of 50 mV on the BV_{OVP} threshold.

If the Bat-OVP function is not required, the VBAT pin should be connected to VSS.

9.2.2.2 Selection of R_{CE}

The $\overline{CE}$ pin can be used to enable and disable the device. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left unconnected, permanently enabling the device.

In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As in the case of the VBAT pin (see previous discussion), the $\overline{CE}$ pin should be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum V_{OH} of the host GPIO pin less the drop across the resistor should be greater than V_{IH} of the bq24308 device's $\overline{CE}$ pin. The drop across the resistor is given by $R_{CE} \times I_{IH}$.

9.2.2.3 Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} in Figure 12 and Figure 13 is for decoupling and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from overshooting to dangerous levels. It is strongly recommended that a ceramic capacitor of at least 1 µF be used at the input of the device. It should be located in close proximity to the IN pin.

C_{OUT} in Figure 12 and Figure 13 is also important: If a very fast (< 1 µs rise-time) overvoltage transient occurs at the input, the current that charges C_{OUT} causes the device's current-limiting loop to kick in, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection. C_{OUT} should also be a ceramic capacitor of at least 1 µF, located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection device.

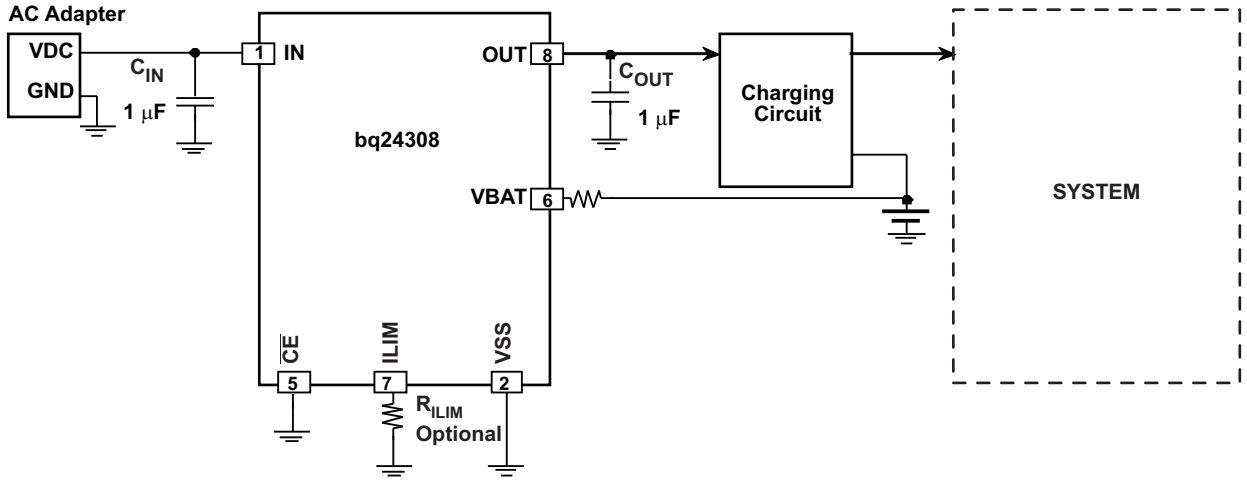


Figure 12. Overvoltage, Overcurrent, and Battery Overvoltage Protection

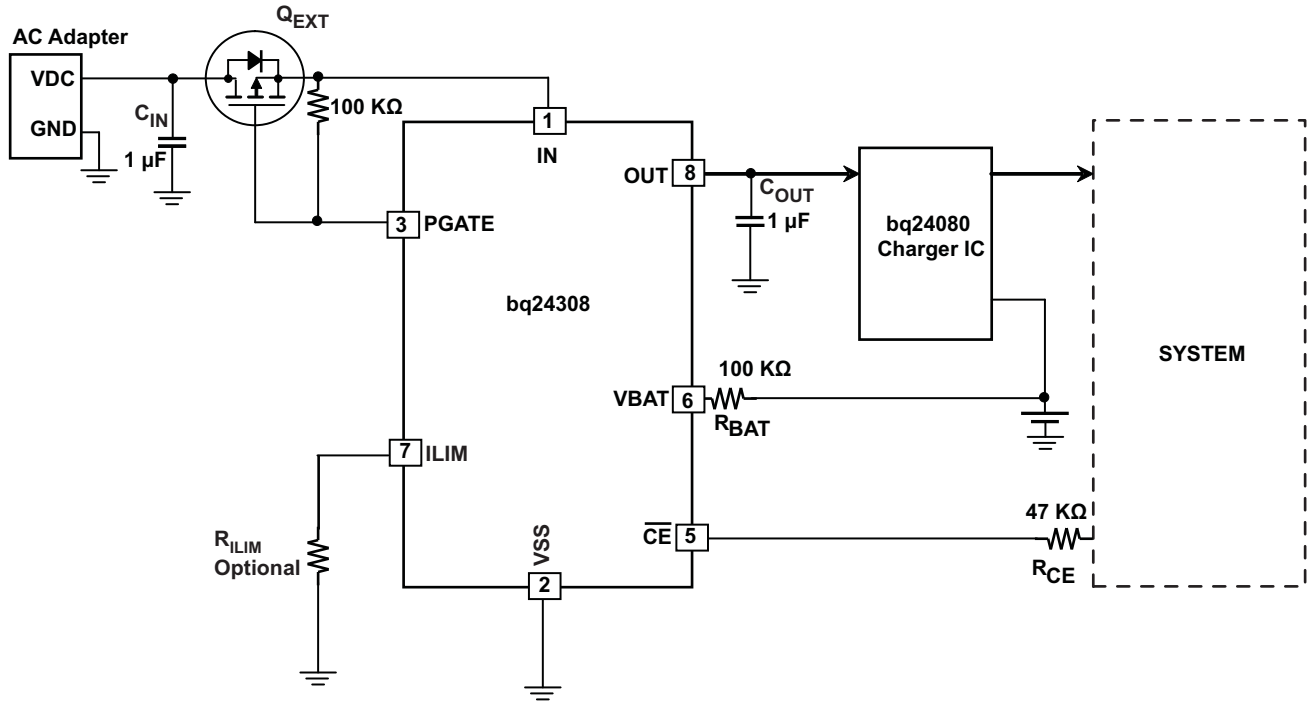
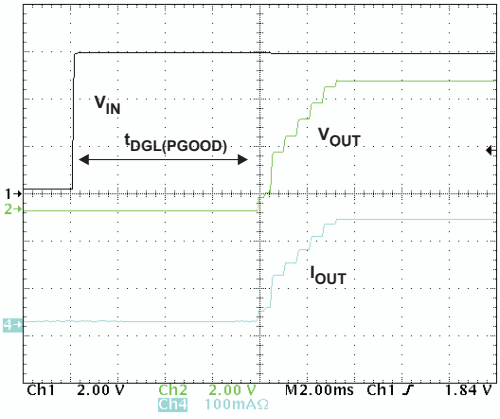


Figure 13. OVP, OCP, BATOVP With Input Reverse-Polarity Protection

9.2.2.4 Selection of the PGATE External MOSFET

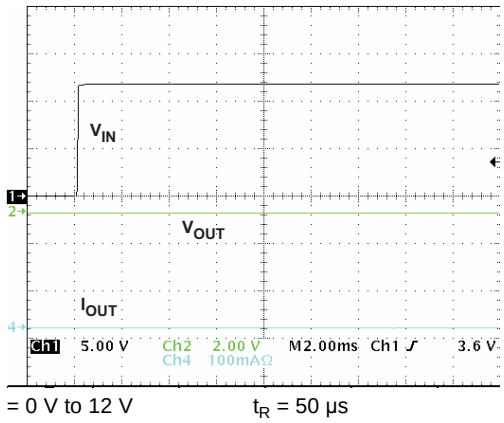
The PGATE output drives the gate of an external MOSFET to protect the device from reverse polarity input voltages. The MOSFET must be sized to handle the expected current in the application. Additionally, the impedance of the MOSFET is in series with the internal FET of the bq24308, so that the overall acceptable system resistance must be taken into account. Ensure the MOSFET VDS maximum rating exceeds the worst-case expected reverse voltage in the application. The bq24308 withstands up to –30 V, so a 30 V rating on the MOSFET is a good target. The maximum VGS of the MOSFET must be greater than –17 V to ensure operation up to 30 V inputs.

9.2.3 Application Curves



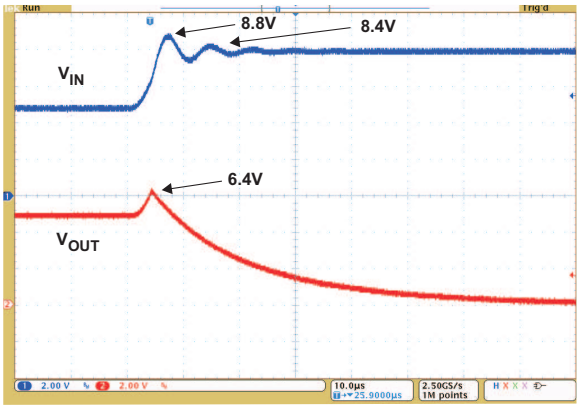
V_{IN} = 0 V to 6 V t_R = 20 µs

Figure 14. Normal Power-On Showing Soft-Start



V_{IN} = 0 V to 12 V t_R = 50 µs

Figure 15. Power-On with Input Overvoltage



V_{IN} = 5 V to 8 V t_R = 3 µs

Figure 16. OVP Response for Input Step

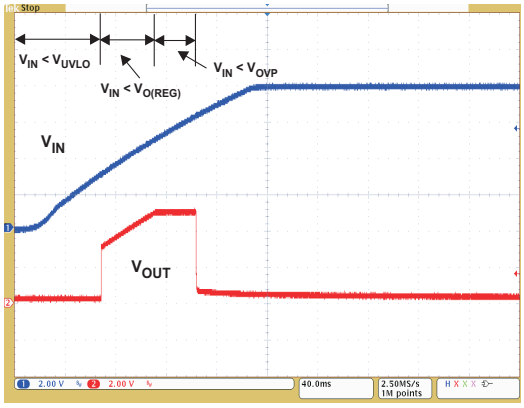
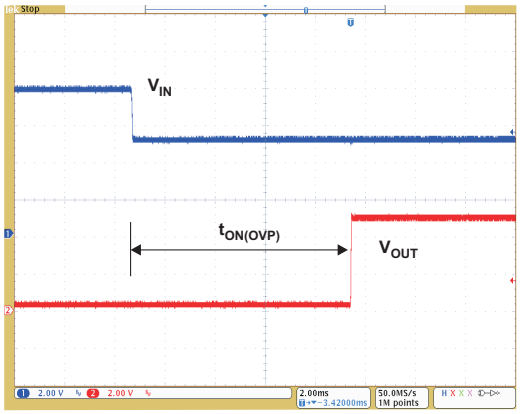


Figure 17. OUT Pin Response to Slow Input Ramp



V_{IN} = 8 V to 5 V t_F = 100 µs

Figure 18. Recovery from Input OVP

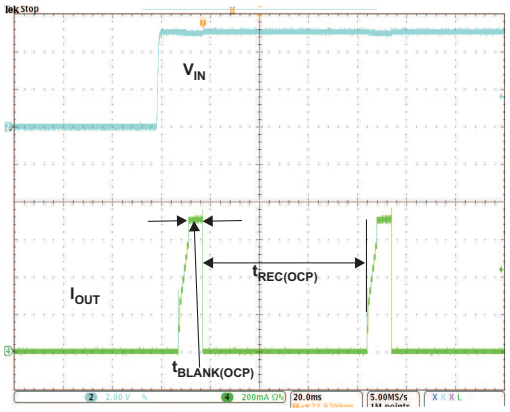
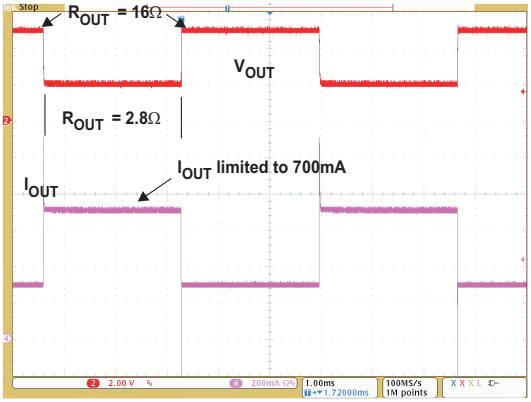
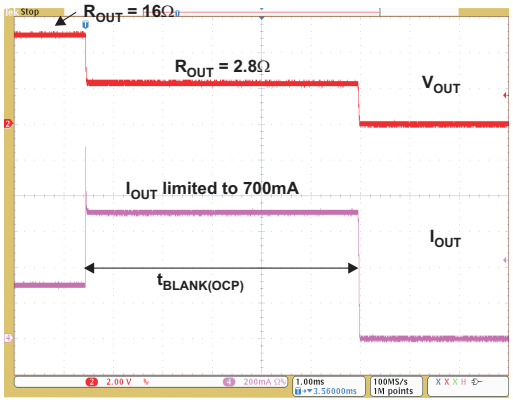


Figure 19. OCP, Powering up with OUT Pin Shorted to VSS



R_{OUT} Switches from 16 Ω to 2.8 Ω

Figure 20. OCP, Showing Current Limiting



R_{OUT} Switches from 16 Ω to 2.8 Ω

Figure 21. OCP, Showing Current Limiting and OCP Blanking

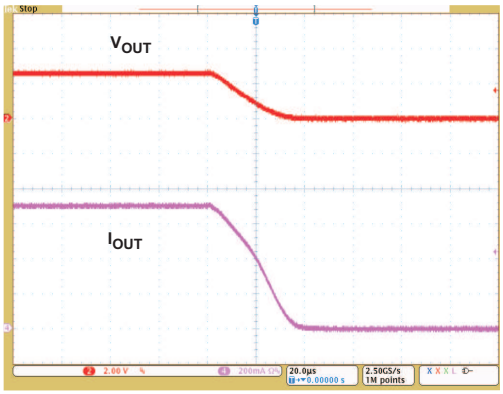
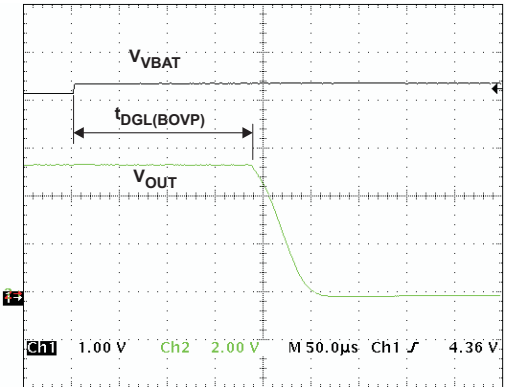


Figure 22. Zoom-in on Turnoff Region of Figure 21, Showing Soft-Stop



V_{VBAT} Steps from 4.3 V to 4.5 V.

Figure 23. Battery OVP, $t_{DGL(BOVP)}$ and Soft-Stop

10 Power Supply Recommendations

The intention is for the bq24308 device to operate with 5-V adapters with a maximum current rating of 1.5 A. The device operates from sources from 3 V to 5.7 V. Outside of this range, the output is disconnected due to either UVLO or the OVP function.

11 Layout

11.1 Layout Guidelines

- This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this device. It must be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for the high voltages. See Figure 24.
- The device uses WSON packages with a thermal pad. For good thermal performance, the thermal pad must be thermally coupled with the PCB ground plane (GND). This requires a copper pad directly under the device. This copper pad must be connected to the ground plane with an array of thermal vias.
- C_{IN} and C_{OUT} should be located close to the device. Other components like R_{ILIM} (optional) and R_{BAT} must also be located close to the device.

11.2 Layout Example

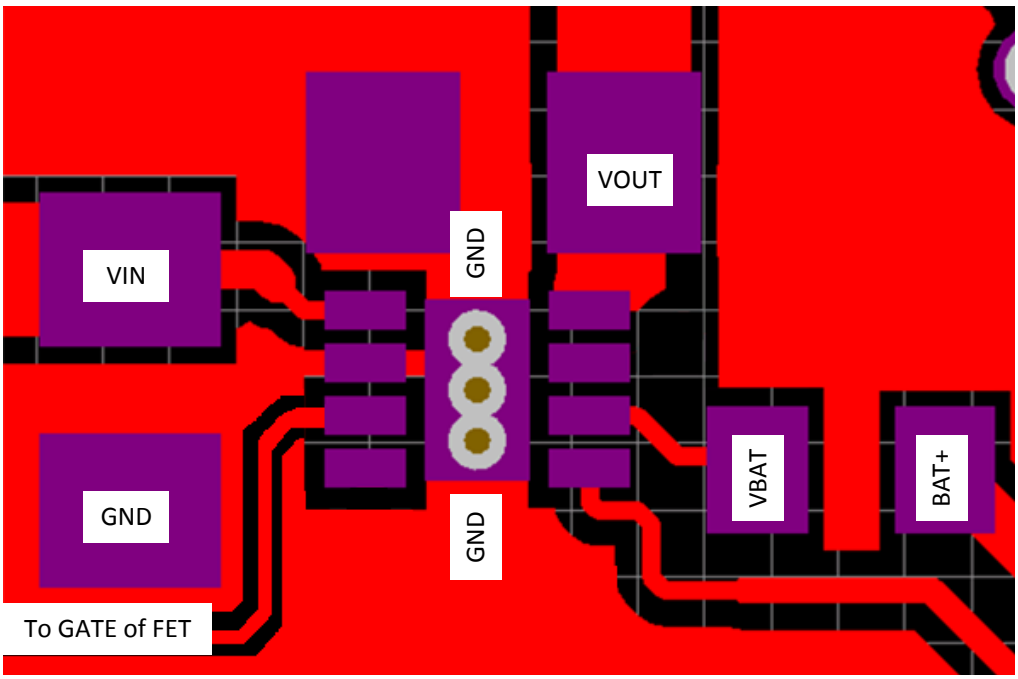


Figure 24. Layout Example Recommendation

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a trademark of Bluetooth SIG, Inc..
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24308DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	DAS	Samples
BQ24308DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	DAS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

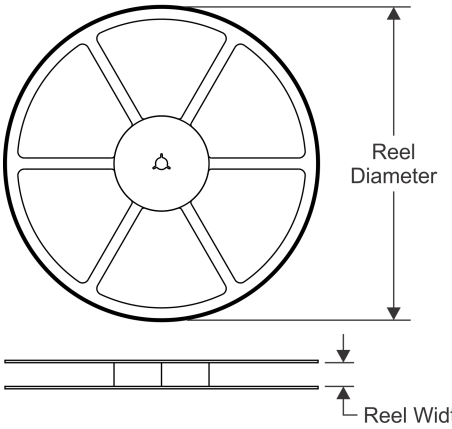
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

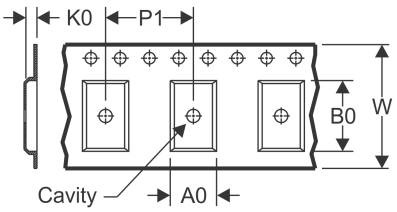
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

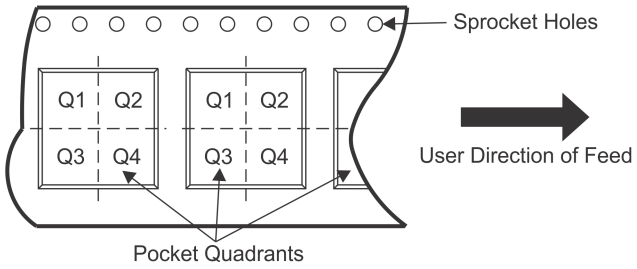


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

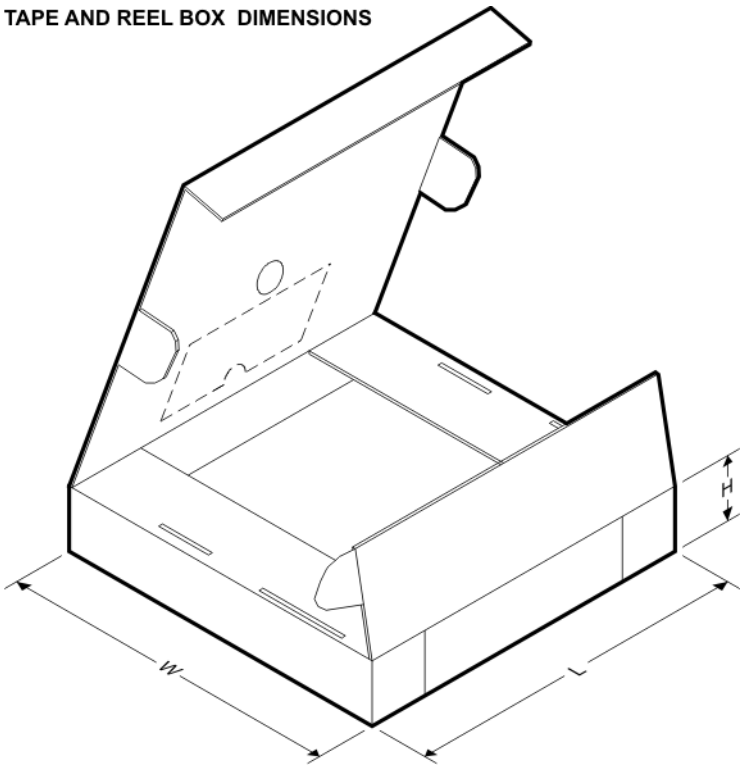
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24308DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24308DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

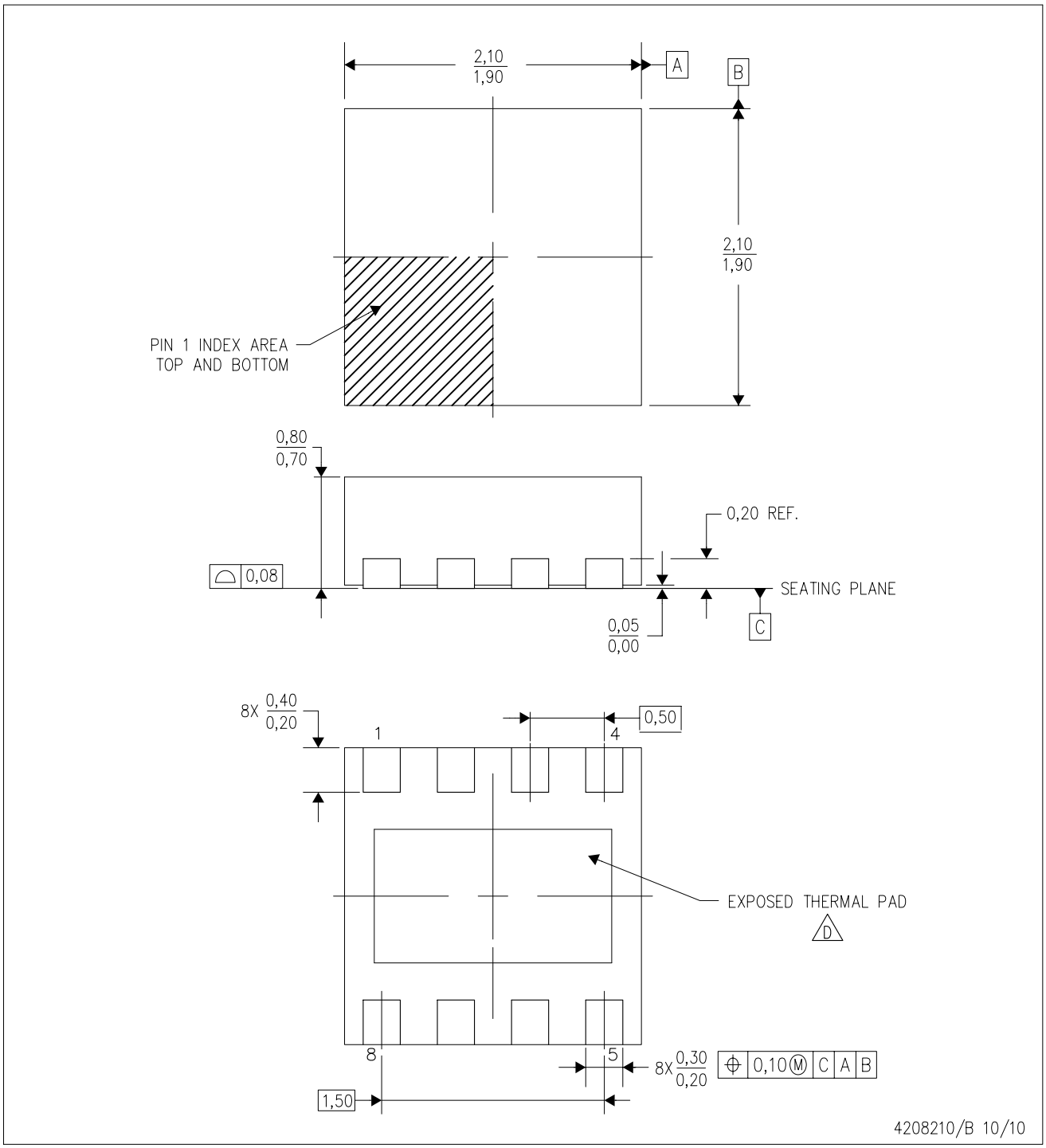
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24308DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
BQ24308DSGT	WSON	DSG	8	250	195.0	200.0	45.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

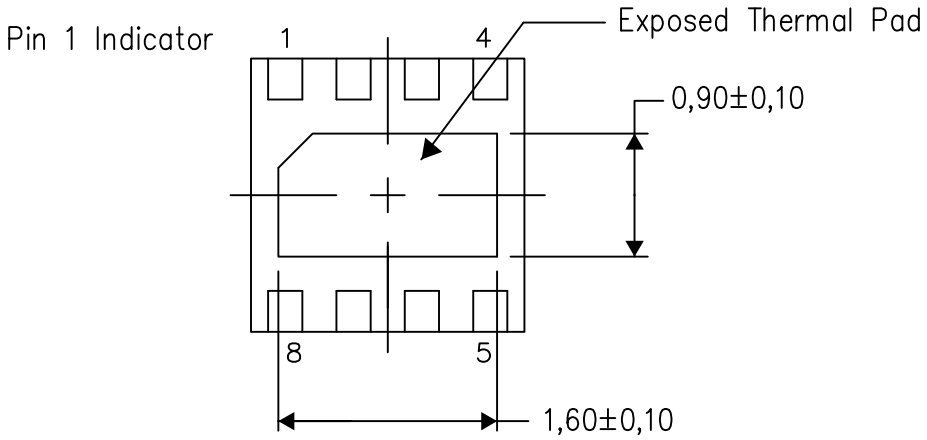
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



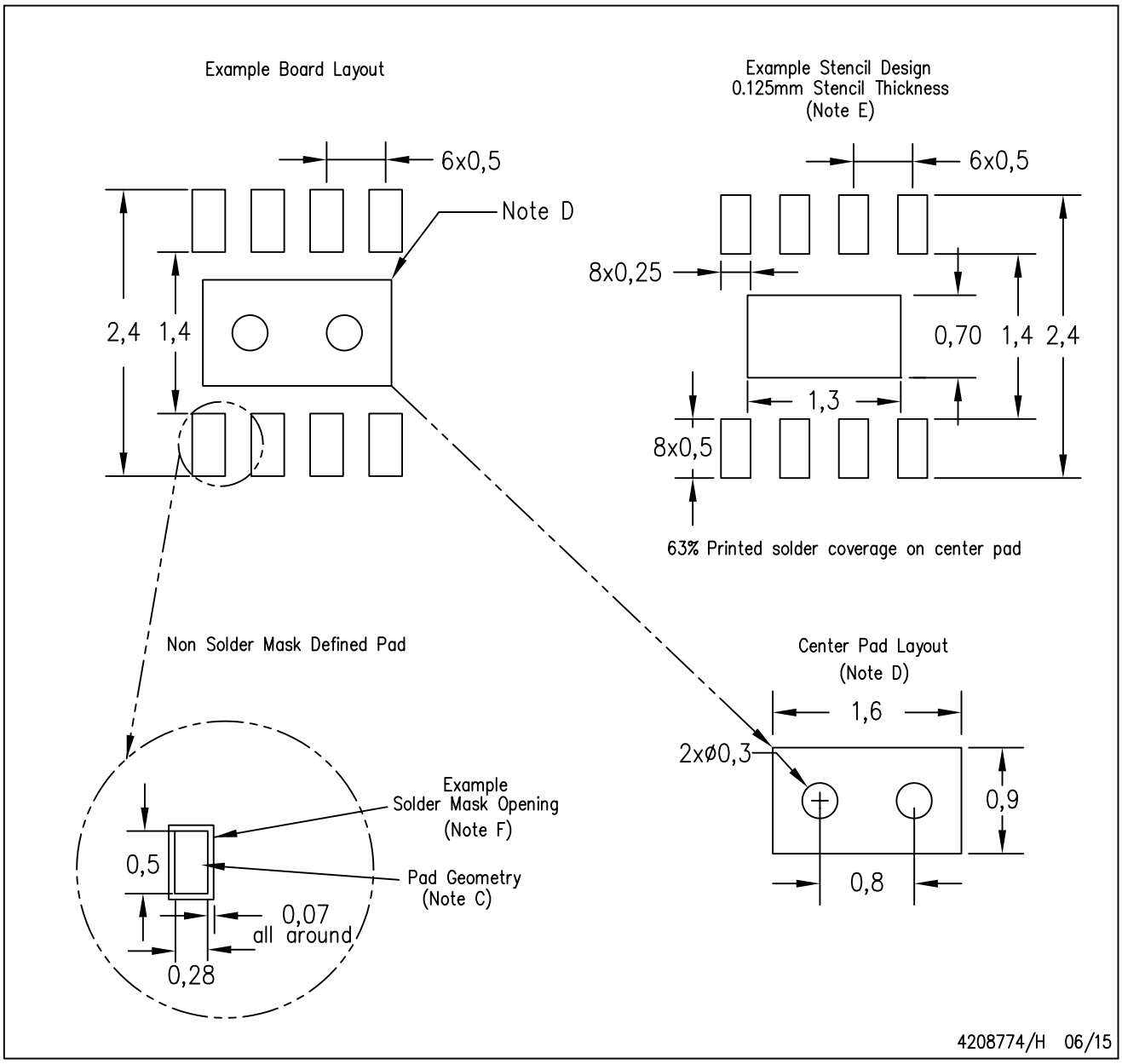
Bottom View

Exposed Thermal Pad Dimensions

4208347/I 06/15

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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