

Sample &

Buv



ADC12J1600, ADC12J2700

SLAS969C - JANUARY 2014 - REVISED JULY 2015

Support &

Community

ADC12Jxx00 12-Bit 1.6 or 2.7 GSPS ADCs With Integrated DDC

Technical

Documents

1 Features

- Excellent Noise and Linearity up to and beyond $F_{INI} = 3 \text{ GHz}$
- Configurable DDC
- Decimation Factors from 4 to 32 (Complex Baseband Out)
- Bypass Mode for Full Nyquist Output Bandwidth
- Usable Output Bandwidth of 540 MHz at 4x Decimation and 2700 MSPS
- Usable Output Bandwidth of 320 MHz at • 4x Decimation and 1600 MSPS
- Usable Output Bandwidth of 67.5 MHz at 32x Decimation and 2700 MSPS
- Usable Output Bandwidth of 40 MHz at 32x Decimation and 1600 MSPS
- Low Pin-Count JESD204B Subclass 1 Interface
- Automatically Optimized Output Lane Count
- Embedded Low Latency Signal Range Indication
- Low Power Consumption

Key Specifications

- Max Sampling Rate: 1600 or 2700 MSPS
- Min Sampling Rate: 1000 MSPS
- DDC Output Word Size: 15-Bit Complex (30) bits total)
- Bypass Output Word Size: 12-Bit Offset Binary
- Noise Floor: -147.3 dBFS/Hz (ADC12J2700)
- Noise Floor: –145 dBFS/Hz (ADC12J1600)
- IMD3: -64 dBc (F_{IN} = 2140 MHz ± 30 MHz at -13 dBFS)
- FPBW (–3 dB): 3.2 GHz
- Peak NPR: 46 dB
- Supply Voltages: 1.9 V and 1.2 V
- Power Consumption
 - Bypass (2700 MSPS): 1.8 W
 - Bypass (1600 MSPS): 1.6 W
 - Power Down Mode: <50 mW

2 Applications

Wireless Infrastructure

Tools &

Software

- **RF-Sampling Software Defined Radio**
- Wideband Microwave Backhaul •
- Military Communications
- SIGINT
- RADAR and LIDAR
- DOCSIS / Cable Infrastructure
- Test and Measurement

3 Description

The ADC12J1600 and ADC12J2700 devices are wideband sampling and digital tuning devices. Texas Instruments' giga-sample analog-to-digital converter (ADC) technology enables a large block of frequency spectrum to be sampled directly at RF. An integrated DDC (Digital Down Converter) provides digital filtering and down-conversion. The selected frequency block is made available on a JESD204B serial interface. Data is output as baseband 15-bit complex information for ease of downstream processing. Based on the digital down-converter (DDC) decimation and link output rate settings, this data is output on 1 to 5 lanes of the serial interface.

A DDC bypass mode allows the full rate 12-bit raw ADC data to also be output. This mode of operation requires 8 lanes of serial output.

The ADC12J1600 and ADC12J2700 devices are available in a 68-pin VQFN package. The device operates over the Industrial (-40°C \leq T_A \leq 85°C) ambient temperature range.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC12J1600	VQFN (68)	10.00 mm × 10.00 mm
ADC12J2700	VQFN (68)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Bypass — Spectral Response f_S = 2.7 GHz, F_{IN} = 1897 MHz at –1 dBFS





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4 Revision History

Cł	nanges from Revision B (September 2014) to Revision C	Page
•	Added additional voltage difference parameters to the Absolute Maximum Ratings table	8
•	Added junction temperature to the Absolute Maximum Ratings table	8
•	Added common mode voltage parameter to the <i>Recommended Operating Conditions</i> table. Changed CLK to SYSREF, and ~SYNC	9
•	Changed some of the maximum interleaving offset values for both devices to tighten the levels	10
•	Deleted the Differential Analog Input Connection image in The Analog Inputs section	31
•	Added note about offset adjust in Background Calibration Mode to the Offset Adjust section and I/O offset register tables	35
•	Added the Calibration Cycle Timing for Different Calibration Modes and Options table in the Timing Calibration Mode section	50
•	Changed 0x004-0x005 to RESERVED in the Standard SPI-3.0 Registers summary table	60

CI	hanges from Revision A (February 2014) to Revision B	Page
•	Changed the device status from Product Preview to Production Data	1

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5 Pin Configuration and Functions



DNC = Make no external connection

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	Pin Functions					
PIN			TYPE	DESCRIPTION		
NAME	NO.	EQUIVALENT CIRCOTT				
ANALOG						
RBIAS+	1	VA19				
RBIAS-	2	GND	I/O	External Bias Resistor Connections External bias resistor terminals. A 3.3 k Ω (±0.1%) resistor should be connected between RBIAS+ and RBIAS–. The RBIAS resistor is used as a reference for internal circuits which affect the linearity of the converter. The value and precision of this resistor should not be compromised. These pins must be isolated from all other signals and grounds.		
TDIODE-	63	Tdiode+				
TDIODE+	64	Tdiode-	Passive	Temperature Diode These pins are the positive (anode) and negative (cathode) diode connections for die temperature measurements. Leave these pins unconnected if they are not used. See the <i>Built-In Temperature Monitor Diode</i> section for more details.		
VBG	68	VA19	0	Bandgap Output Voltage This pin is capable of sourcing or sinking 100 μA and can drive a load up to 80 pF. Leave this pin unconnected if it is not used in the application. See the <i>The</i> <i>Reference Voltage</i> section for more details.		
VCMO	3	GND VCM	0	Common Mode Voltage The voltage output at this pin must be the common-mode input voltage at the VIN+ and VIN– pins when DC coupling is used. This pin is capable of sourcing or sinking 100 μ A and can drive a load up to 80 pF. Leave this pin unconnected if it is not used in the application.		
VIN+	8	VA19				
VIN-	9	VIN+ To T&H+ GND CONC	I	Signal Input The differential full-scale input range is determined by the full-scale voltage adjust register. An internal peaking inductor (L _{PEAK}) of 5 nH is included for parasitic compensation.		

NSTRUMENTS

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Pin Functions (continued)

PIN				
NAME	NO.		TYPE	DESCRIPTION
DATA	1	L		·
DS0-	32			
DS0+	33	VD12 VA19		
DS1-	35			
DS1+	36			
DS2-	38		-	Data CML These pins are the high-speed serialized-data outputs with user-configurable
DS2+	39	50 Ω –	0	pre-emphasis. These outputs must always be terminated with a $100-\Omega$ differential
DS3-	41			resistor at the receiver.
DS3+	42			
DS4-	44	GND		
DS4+	45			
DS5-/NCO 0	47			
DS5+/NCO 0	48	VA19		Data
DS6-/NCO 1	50			DS5-/NCO 0. DS5+/NCO 0. DS6-/NCO 1. DS6+/NCO 1.
DS6+/NCO 1	51			DS7-/NCO_2 and DS7+/NCO_2: When decimation is enabled, these
DS7-/NCO 2	53		0/1	pins become LVCMOS inputs and allow the host device to select the
DS7+/NCO_2	54		0,1	the positive (+) and negative (-) pins should be connected together and both driven. An acceptable alternative is to let one of the pair float while the other pin is driven. Connect these inputs to GND if they are not used in the application.
GROUND, RESER	RVED, D	NC		
DNC	67			Do Not Connect Do not connect DNC to any circuitry, power, or ground signals.
RSV	66	VA19	_	Reserved Connect to Ground or Leave Unconnected: This reserved pin is a logic input for possible future device versions. It is recommended to connect this pin to ground. Floating this pin is also permissible.
RSV2	61	GND	_	Reserved Connect to Ground Connect this reserved input pin to ground for proper operation.
Thermal Pad			_	Ground (GND) The exposed pad on the bottom of the package is the ground return for all supplies. This pad must be connected with multiple vias to the printed circuit board (PCB) ground planes to ensure proper electrical and thermal performance. The exposed center pad on the bottom of the package must be thermally and electrically connected (soldered) to a ground plane to ensure rated performance.
LVCMOS				
OR_T0	25	VA19 • • •		
OR_T1	26		Ο	Over-Range Over-range detection status for T0 and T1 thresholds. Leave these pins unconnected if they are not used in the application.

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Pin Functions (continued)

PIN				DECODIDITION	
NAME	NO.		TTPE	DESCRIPTION	
SCLK	58	VA19 Q	I	Serial Interface Clock This pin functions as the serial-interface clock input which clocks the serial data in and out. The Using the Serial Interface section describes the serial interface in more detail.	
SDI	57		I	Serial Data In This pin functions as the serial-interface data input. The Using the Serial Interface section describes the serial interface in more detail.	
SYNC~	30		I	SYNC- This pin provides the JESD204B-required synchronizing request input. A logic-low applied to this input initiates a lane alignment sequence. The choice of LVCMOS or differential SYNC- is selected through bit 6 of the configuration register 0x202h. Connect this input to GND or VA19 if differential SYNC- input is used.	
SCS	59	GND	I	Serial Chip Select (active low) This pin functions as the serial-interface chip select. The Using the Serial Interface section describes the serial interface in more detail.	
SDO	56	VA19 VA19 GND	0	Serial Data Out This pin functions as the serial-interface data output. The <i>Using the Serial Interface</i> section describes the serial interface in more detail.	
DIFFERENTIAL II	NPUT				
DEVCLK+ DEVCLK-	15 16		I	Device Clock Input The differential device clock signal must be AC coupled to these pins. The input signal is sampled on the rising edge of CLK.	
SYSREF+	19	νΑ19 Υ		SYSREF	
SYSREF-	20		I	The differential periodic waveform on these pins synchronizes the device per JESD204B. If JESD204B subclass 1 synchronization is not required and these inputs are not utilized they may be left unconnected. In that case ensure SysRef_Rcvr_En=0 and SysRef_Pr_En=0.	
SYNC~+/TMST+	22	AGND $\int 1 k\Omega$		SYNC~/TMST	
SYNC/TMST-	23	VA19 50 Ω AGND	I	This differential input provides the JESD204B-required synchronizing request input. A differential logic-low applied to these inputs initiates a lane alignment sequence. For differential SYNC~ usage, ensure that SYNC_DIFF_PD = 0 and SYNC_DIFFSEL = 1. When the LVCMOS SYNC~ is selected these inputs can be used as the differential TIMESTAMP input. For TMST usage, ensure that SYNC_DIFF_PD = 0, SYNC_DIFFSEL = 0, and TIME_STAMP_EN = 1. For additional information see the <i>Time Stamp</i> section. These inputs may be left unconnected if they are not used for either the SYNC~ or TIMESTAMP functions.	



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Pin Functions (continued)

PIN			TVDE	DESCRIPTION	
NAME	NO.	EQUIVALENT CIRCUIT	TTPE	DESCRIPTION	
POWER					
	6				
	11				
	14			Analog 1.2 V nower supply nins	
VA12	17		—	Bypass these pins to ground using one $10-\mu$ F capacitor and two $1-\mu$ F capacitors for	
	18			bulk decoupling plus one 0.1-µF capacitor per pin for individual decoupling.	
	21				
	65				
	4				
	7				
	10				
	13			Analog 1.9 V power supply pins	
VA19	24		_	Bypass these pins to ground using one $10-\mu$ F capacitor and two $1-\mu$ F capacitors for bulk decoupling plus one $0.1-\mu$ F capacitor per pin for individual decoupling	
	27				
	60				
	62				
	28				
	31		_		
	34				
	37				
	40			Digital 1.2 V power supply pins	
VD12	43			Bypass these pins to ground using one 10-µF capacitor and two 1-µF capacitors for bulk decoupling plus one 0.1-µF capacitor per pin for individual decoupling	
	46				
	49				
	52				
	55				
	5			VNEG	
VNEG	12		I	These pins must be decoupled to ground with a $0.1-\mu$ F ceramic capacitor near each pin. These power input pins must be connected to the VNEG_OUT pin with a low resistance path. The connections must be isolated from any noisy digital signals and must also be isolated from the analog input and clock input pins.	
VNEG_OUT	29		0	VNEG_OUT The voltage on this output can range from –1V to +1V. This pin must be decoupled to ground with a 4.7-µF, low ESL, low ESR multi-layer ceramic chip capacitor and connected to the VNEG input pins. This voltage must be isolated from any noisy digital signals, clocks, and the analog input.	

6 Specifications

6.1 Absolute Maximum Ratings

The soldering process must comply with TI's Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.⁽¹⁾⁽²⁾⁽³⁾

			MIN	MAX	UNIT
	1.2-V supply	VA12, VD12		1.4	V
Supply voltage	1.9-V supply	VA19		2.2	V
Supply voltage Voltage Voltage difference RF input power, P ₁ Input current Junction	1.2-V supply difference between VA1	2 and VD12	-200	200	mV
Voltage	On any input pin (except VIN+ or VIN	I–)	-0.15	V _(VA19) + 0.15	V
	On VIN+ or VIN-		0	2	V
	(VIN+) - (VIN-) ⁽⁴⁾			2	
	(DEVCLK+) – (DEVCLK–)			2	
voltage difference	(SYSREF+) – (SYSREF–)			2	V
	(~SYNC+) – (~SYNC–)			1	
	On VIN+, VIN–, with proper input common mode maintained. $F_{IN} \ge 3 \text{ GHz}$, $Z_{(SOURCE)} = 100 \Omega$, Input_Clamp_EN = 0 or 1			11.07	
RF input power, P _I	On VIN+, VIN–, with proper input common mode maintained. $F_{IN} = 1$ GHz, $Z_{(SOURCE)} = 100 \Omega$, Input_Clamp_EN = 1			14.95	dBm
	On VIN+, VIN–, with proper input common mode maintained. $F_{IN} \le 100 \text{ MHz}$, $Z_{(SOURCE)} = 100 \Omega$, Input_Clamp_EN = 1			20.97	
	At any pin other than VIN+ or VIN- ⁽⁵⁾)	-25	25	mA
Input current	VIN+ or VIN-		-50	50	mA DC
input current	Package ⁽⁵⁾ (sum of absolute value of all currents forced in or out, not including power supply current)			100	mA
Junction temperature, T _J	Power applied. Verified by High Tem hours.	perature Operation Life testing to 1000	-40	150	°C
Storage temperature	e, T _{sta}		-65	150	°C

(1) Reflow temperature profiles are different for lead-free and non-lead-free packages.

(2) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(4) The analog inputs are protected as in the following circuit. Input-voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



(5) When the input voltage at any pin (other than VIN+ or VIN–) exceeds the power supply limits (that is, less than GND or greater than VA19), the current at that pin must be limited to 25 mA. The 100-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies. This limit is not placed upon the power pins or thermal pad (GND).

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6.2 ESD Ratings

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			VALUE	UNIT
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000		
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all $\ensuremath{\text{pins}}^{(2)}$	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

All voltages are measured with respect to GND = 0 V, unless otherwise specified.

			MIN	MAX	UNIT
V	Supply voltage	1.2-V supply: VA12, VD12	1.14	1.26	V
VDD	Supply voltage	1.9-V supply: VA19	1.8	2	V
	Supply sequence (power-up and	d power-down)		1.9 supply ≥ 1.2 supply	V
V _{CMI}	Analog input common mode vol	tage	V _(VCMO) – 0.15	V _(VCMO) + 0.15	V
	VIN+, VIN- voltage (maintaining	g common mode)	0	V _(VA19)	V
	DEVCLK±, SYSREF±, ~SYNC±	pin voltage range	0	V _(VA19)	V
V _{ID(CLK)}	Differential DEVCLK±, SYSREF	±, ~SYNC± amplitude	0.4	2	V _{PP}
V _{CM(CLK)}	SYSREF±, ~SYNC± Common M	Node	0.64	1.1	V
T _A	Ambient temperature		-40	85	°C
TJ	Junction temperature			135	°C

6.4 Thermal Information

		ADC12J1x00	
	THERMAL METRIC ⁽¹⁾	NKE (VQFN)	UNIT
		68 PINS	
$R_{\theta J A}$	Thermal resistance, junction-to-ambient	19.8	°C/W
R _{0JCbot}	Thermal resistance, junction-to-case (bottom)	2.7	°C/W
Ψ_{JB}	Characterization parameter, junction-to-board	9.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN full scale range at default setting (725 mV_{PP}), VIN = -1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A = 25^{\circ}\text{C}$.⁽¹⁾⁽²⁾

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT			
DYNAMIC PERFORMANCE CHARACTERISTICS									
RES	ADC core resolution	Resolution with no missing codes		12		bits			
INL	Integral non-linearity	$T_A = 25^{\circ}C$		±2					
		$T_A = T_{MIN}$ to T_{MAX}		±3		LOD			
	Differential new linearity	$T_A = 25^{\circ}C$		±0.25					
DINE	Differential non-intearity	$T_A = T_{MIN}$ to T_{MAX}		±0.3		LOD			
Peak NPR	Peak noise power ratio	500-kHz tone spacing from 1 MHz to $f_{\rm S}$ / 2–1 MHz, DDC bypass mode 25-MHz wide notch at 320 MHz		46		dB			
IMD ₃	Third-order intermodulation distortion	F1 = 2110 MHz at -13 dBFS F2 = 2170 MHz at -13 dBFS		-64		dBc			

(1) To ensure accuracy, the VA19, VA12, and VD12 pins are required to be well bypassed. Each supply pin must be decoupled with one or more bypass capacitors.

(2) Interleave related fixed frequency spurs at f_S / 4 and f_S / 2 are excluded from all SNR, SINAD, ENOB and SFDR specifications. The magnitude of these spurs is provided separately.

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Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN full scale range at default setting (725 mV_{PP}), VIN = -1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A = 25^{\circ}\text{C}^{.(1)(2)}$

	PARAMETER	TEST CONDI	TIONS	MIN	TYP	MAX	UNIT			
DDC BYPASS Mode, ADC12J2700, f _(DEVCLK) = 2.7 GHz										
		$F_{IN} = 350 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	mode		55.1					
			$T_A = 25^{\circ}C$		54.9					
	Signal-to-noise ratio,	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	$T_A = T_{MIN}$ to T_{MAX}	52.5						
SNR	Nyquist bandwidth	mode	$T_A = 25^{\circ}C$, calibration = BG		54.8		dBFS			
	Input frequency-dependent		$T_A = T_{MIN}$ to T_{MAX} , calibration = BG	52.4						
	interiouving spure included	F _{IN} = 1500 MHz, -1 dBFS, 12-bit DDC bypass	s mode		52.5					
		F _{IN} = 2400 MHz, -1 dBFS, 12-bit DDC bypass	s mode		50					
		F _{IN} = 350 MHz, -1 dBFS, 12-bit DDC bypass mode			55					
			T _A = 25°C		54.8					
	Signal-to-noise and distortion	En = 600 MHz =1 dBES 12-bit DDC bypass	$T_A = T_{MIN}$ to T_{MAX}	52.3						
SINAD	ratio, integrated across entire Nyquist bandwidth	mode	$T_A = 25^{\circ}C$, calibration = BG		54.7		dBFS			
	Input frequency-dependent		$T_A = T_{MIN}$ to T_{MAX} , calibration = BG	52.2						
	interleaving spurs included	$F_{IN} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12 \text{-bit DDC bypass}$	s mode		52.4					
		$F_{\rm IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode}$			50					
		$F_{\rm IN} = 350$ MHz, -1 dBFS, 12-bit DDC bypass	mode		8.8					
		· · · · · · · · · · · · · · · · · · ·	$T_{A} = 25^{\circ}C$		8.8					
	Effective number of bits,		$T_A = 2000$	84	0.0		Bits			
ENOB	integrated across entire Nyquist bandwidth Input frequency-dependent	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode$	$T_{A} = 25^{\circ}C_{A}$ calibration = BG	0.1	8.8					
2.100			$T_A = 20^{\circ}$ C, calibration = 20	8.4	0.0					
	interleaving spurs included	E 1500 MHz -1 dBES 12-bit DDC bypass		0.4	8.4					
		$F_{\rm IN} = 2400 \text{ MHz} = 1 \text{ dBFS} = 12 \text{-bit DDC bypass}$	mode		8					
		$F_{\rm IN} = 250$ MHz 1 dBES 12 bit DDC bypass	mode		66.7					
		$T_{\rm IN} = 350$ WHz, $= 1$ dBi 3, 12-bit DDC bypass	T - 25%	71.6						
		F _{IN} = 600 MHz, −1 dBFS, 12-bit DDC bypass mode	$T_A = 25 \text{ C}$	64	71.0		dBFS			
	Spurious-free dynamic range Input frequency-dependent interleaving spurs included		$T_A = T_{MIN}$ to T_{MAX}	01	70					
SFDR			$T_A = 25^{\circ}$ C, calibration = BG		70		UBF5			
			$T_A = T_{MIN}$ to T_{MAX} , calibration = BG	29	05.0					
		FIN = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode			65.2					
		$F_{IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$			58.6		l			
			$I_A = 25^{\circ}C$		-//	50.5				
f _S /2	Interleaving offset spur at 1/2 sampling rate	F _{IN} = 600 MHz, -1 dBFS, 12-bit DDC bypass	$I_A = I_{MIN}$ to I_{MAX}			-59.5	dBFS			
	Samping rate	houe	$I_A = 25^{\circ}$ C, calibration = BG		-74					
			$I_A = I_{MIN}$ to I_{MAX} , calibration = BG			-57.5				
			$I_{A} = 25^{\circ}C$		-70					
f _s /4	Interleaving offset spur at 1/4	F _{IN} = 600 MHz, -1 dBFS, 12-bit DDC bypass	$T_A = T_{MIN}$ to T_{MAX}			-54.5	dBFS			
	sampling rate	mode	$T_A = 25^{\circ}C$, calibration = BG		-68					
			$T_A = T_{MIN}$ to T_{MAX} , calibration = BG			-53				
			$T_A = 25^{\circ}C$		-78					
fs/2 - FIN	Interleaving offset spur at 1/2 sampling rate – input	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	$T_A = T_{MIN}$ to T_{MAX}			-62	dBFS			
50 114	frequency	mode	$T_A = 25^{\circ}C$, calibration = BG		-76					
			$T_A = T_{MIN}$ to T_{MAX} , calibration = BG			-61				
			$T_A = 25^{\circ}C$		-76					
fs/4 + Fin	Interleaving offset spur at 1/4 sampling rate + input	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	$T_A = T_{MIN}$ to T_{MAX}			-61	dBFS			
J 5/ IN	frequency	mode	$T_A = 25^{\circ}C$, calibration = BG		-71		00.0			
			T_{A} = T_{MIN} to $T_{MAX},$ calibration = BG			-59	1			
			T _A = 25°C		-77		dRES			
f-/4 - F	Interleaving offset spur at 1/4	terleaving offset spur at $\frac{1}{4}$ mpling rate – input equency $F_{IN} = 600 \text{ MHz}$, -1 dBFS, 12-bit DDC bypass $T_A = \frac{1}{T_A}$	$T_A = T_{MIN}$ to T_{MAX}			-61.4				
JS/→ = ΓIN	frequency		$T_A = 25^{\circ}C$, calibration = BG		-76		udro			
			$T_A = T_{MIN}$ to T_{MAX} , calibration = BG			-61				



Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN full scale range at default setting (725 mV_{PP}), VIN = -1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A = 25^{\circ}\text{C}^{.(1)(2)}$

$ \begin{tabular}{ c c c } \hline F_{n} = 30 \ MHz, -1 \ def{e}{r}, 12-bit DC byses mode & -73$		PARAMETER	TEST COND	ITIONS	MIN	TYP	MAX	UNIT
$ \begin{tabular}{ c c c } T_{1} = 200 \ MHz = 1 \ dBFS, 12 \ bD DC byses mode $$ $$ $$ $$ $$ $$ $$$ $$$ $$$ $$$$$$$$$			F _{IN} = 350 MHz, -1 dBFS, 12-bit DDC bypass	mode		-73		
THD Total harmonic distrition $F_{n} = 500$ MHz, -1 dBFS, 12-bit DC bypase mode $T_{n} = T_{max}$ to T_{max}				$T_A = 25^{\circ}C$		-70		
$ \begin{tabular}{ c c c c } \hline True harmonic diatorial $$ $$ $$ $$$$$$$$$$$$$$$$$$$$$$$$$$$$			$F_{\rm IN} = 600 \text{ MHz}$ 1 dBFS, 12-bit DDC bypass	$T_A = T_{MIN}$ to T_{MAX}			-61	
	THD	Total harmonic distortion	mode	$T_A = 25^{\circ}C$, calibration = BG		-72		dBFS
$ \frac{1}{F_{h}} = 1500 \text{ MHz} - 1 49FS, 12-bit DOC bypass mode -68 F_{h} = 2400 \text{ MHz} - 1 49FS, 12-bit DOC bypass mode -72 F_{h} = 200 \text{ MHz} - 1 49FS, 12-bit DOC bypass mode -72 F_{h} = 200 \text{ MHz} - 1 49FS, 12-bit DOC bypass -76 F_{h} = 200 \text{ MHz} - 1 49FS, 12-bit DOC bypass -76 F_{h} = 200 \text{ MHz} - 1 49FS, 12-bit DOC bypass -76 F_{h} = 200 \text{ MHz} - 1 49FS, 12-bit DOC bypass -76 F_{h} = 200 \text{ MHz} - 1 49FS, 12-bit DOC bypass -76 F_{h} = 200 \text{ MHz} - 1 49FS, 12-bit DOC bypass -76 F_{h} = 200 \text{ MHz} - 1 49FS, 12-bit DOC bypass -76 F_{h} = 200 \text{ MHz} - 1 49FS, 12-bit DOC bypass -76 F_{h} = 200 \text{ MHz} - 1 49FS, 12-bit DOC bypass -76 F_{h} = 200 \text{ MHz} - 1 49FS, 12-bit DOC bypass -76 F_{h} = 200 \text{ MHz} - 1 49FS, 12-bit DOC bypass -70 F_{h} $				$T_A = T_{MIN}$ to T_{MAX} , calibration = BG			-62	
$ \begin{array}{ c c c c } \hline F_{\mu} = 2400 Mtz, -1 dBFS, 12-bit DDC bypass mode & -68 \\ \hline F_{\mu} = 300 Mtz, -1 dBFS, 12-bit DDC bypass mode & -72 \\ \hline F_{\mu} = 500 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypass mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 dBFS, 12-bit DDC bypas mode & -76 \\ \hline F_{\mu} = 200 Mtz, -1 $			F _{IN} = 1500 MHz, -1 dBFS, 12-bit DDC bypass	s mode		-68		
$ HO2 \qquad \text{Second harmonic distortion} \\ HO2 \qquad \text{Second harmonic distortion} \\ HO3 \qquad \text{Third harmonic distortion} \\ HD3 \qquad \text{Third harmonic distortion} \\ HD4 $			$F_{IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	s mode		-68		
$ HD2 \\ Second harmonic distortion \\ F_m = 600 MHz, -1 dBFS, 12-bit DDC bypass mode \\ F_m = 200 MHz, -1 dBFS, 12-bit DDC bypass mode \\$			F _{IN} = 350 MHz. –1 dBFS. 12-bit DDC bypass	mode		-72		
$ \begin{array}{ c c c c } HD2 & Second harmonic distortion \\ F_{Ni} = 600 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 1500 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 1500 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 1500 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 600 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 600 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 600 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-bit DDC byses mode \\ \hline F_{in} = 200 MH2, -1 dBFS, 12-b$				$T_{A} = 25^{\circ}C$		-79		
$ \begin{array}{c c c c c c } HD2 & Second harmonic distortion & $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$				$T_A = T_{ABA}$ to T_{ABA}			-62	
$ \frac{1}{F_{ni} = 100 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -76 \\ \hline \frac{1}{F_{ni} = 300 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -72 \\ \hline \frac{1}{F_{ni} = 300 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -72 \\ \hline \frac{1}{F_{ni} = 300 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -72 \\ \hline \frac{1}{F_{ni} = 400 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -72 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} - 86 \\ -72 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} - 86 \\ -72 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} - 86 \\ -72 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} - 86 \\ -74 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} - 86 \\ -76 \\ \hline \frac{1}{F_{ni} = 2400 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -76 \\ \hline \frac{1}{F_{ni} = 2400 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -76 \\ \hline \frac{1}{F_{ni} = 2400 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -76 \\ \hline \frac{1}{F_{ni} = 2400 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -76 \\ \hline \frac{1}{F_{ni} = 2400 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -76 \\ \hline \frac{1}{F_{ni} = 2400 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -76 \\ \hline \frac{1}{F_{ni} = 800 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -76 \\ \hline \frac{1}{F_{ni} = 800 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -76 \\ \hline \frac{1}{F_{ni} = 800 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -76 \\ \hline \frac{1}{F_{ni} = 800 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } -76 \\ \hline \frac{1}{F_{ni} = 800 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } \\ \hline \frac{1}{F_{ni} = 800 \text{ MHz}_{i} - 1 \text{ dBFS}_{i} 12 \text{ bit DOC bypass mode} } \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} = 80 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} = 80 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} = 80 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} = 80 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} = 80 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} = 80 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} = 80 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} = 80 \\ \hline \frac{1}{F_{ni} = 270 \text{ contraints} = 80 \\ \hline$	HD2	Second harmonic distortion	mode	$T_{A} = 25^{\circ}C_{A}$ calibration = BG		81		dBFS
$ \frac{1}{F_{n} = 1600 \text{ MHz} - 1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 2400 \text{ MHz} - 1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 2400 \text{ MHz} - 1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 350 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 600 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 00 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 00 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 00 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 00 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 00 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 00 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 00 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 00 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 00 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 00 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 00 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 00 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 200 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = 200 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = -70 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = -70 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = -70 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = -70 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = -76 \\ F_{n} = -70 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass mode} = $				$T_A = 2000$, calibration = 20			-64	
$ \begin{array}{ c } \hline F_{n} = 2400 \text{MHz}_{-1} \text{dBFS}_{-1} 12-bit \text{DDC bypass mode} & -70 \\ \hline F_{n} = 2400 \text{MHz}_{-1} \text{dBFS}_{-1} 12-bit \text{DDC bypass mode} & -72 \\ \hline F_{n} = 300 \text{MHz}_{-1} \text{dBFS}_{-1} 12-bit \text{DDC bypass mode} & -72 \\ \hline F_{n} = 500 \text{MHz}_{-1} \text{dBFS}_{-1} 12-bit \text{DDC bypass mode} & -76 \\ \hline F_{n} = 1500 \text{MHz}_{-1} \text{dBFS}_{-1} 12-bit \text{DDC bypass mode} & -76 \\ \hline F_{n} = 1500 \text{MHz}_{-1} \text{dBFS}_{-1} 12-bit \text{DDC bypass mode} & -76 \\ \hline F_{n} = 1500 \text{MHz}_{-1} \text{dBFS}_{-1} 12-bit \text{DDC bypass mode} & -76 \\ \hline F_{n} = 2400 \text{MHz}_{-1} \text{dBFS}_{-1} 12-bit \text{DDC bypass mode} & -76 \\ \hline F_{n} = 2400 \text{MHz}_{-1} \text{dBFS}_{-1} 12-bit \text{DDC bypass mode} & -76 \\ \hline F_{n} = 2400 \text{MHz}_{-1} \text{dBFS}_{-1} 12-bit \text{DDC bypass mode} & -76 \\ \hline F_{n} = 600 \text{MHz}_{-1} \text{dBFS}_{-1} 12-bit \text{DDC bypass mode} & -147.3 & \text{dBFS}_{-140.0} & \text{dBFS}_{-$			En = 1500 MHz =1 dBES_12-bit DDC bypass	s mode		-76		
$ \begin{array}{ c = 350 \ \text{MHz}_{-1} \ \text{dBFS}_{-1} \ \text{Tabulk}_{-1} \ Tabulk$			F = 2400 MHz 1 dBES 12 bit DDC bypass mode			_70		I
$ \begin{array}{c c c c c c } \mbox{HD3} & Third harmonic distortion \\ \hline F_{ig} = 600 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 500 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 500 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 500 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 2400 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 2400 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 500 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 500 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 500 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 500 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 500 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 500 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 500 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 2400 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 200 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 200 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 200 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 200 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 200 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} = 300 MHz, -1 dBFS, 12-bit DDC bypass mode \\ \hline F_{ig} =$			$F_{\rm IN} = 250$ MHz 1 dBES 12 bit DDC bypass	modo		72		
$ \begin{array}{ c c c c c } & & & & & & & & & & & & & & & & & & &$			$r_{\rm IN} = 350$ MHz, -1 dBr3, 12-bit DDC bypass			-72		
$ \begin{array}{ c c c c c } \mbox{Hz} & -1 \mbox{dist} \mbox{dist} \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 600 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 1500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 1500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 1500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 1500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 200 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline F_{N} & = 1500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline \hline F_{N} & = 1500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline \hline F_{N} & = 1500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline \hline F_{N} & = 1500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline \hline F_{N} & = 1500 \ MHz, -1 \ dBFS, 12-bit \ DC \ bypass \ mode \\ \hline \hline F_{N} & = 2400 \ MHz, -1 \ dBFS, 12-bit \ DC \$				$T_A = 25^{\circ}C$		-/5		dBES
$\frac{1}{16} = 20$, characterized = BG10 F _H = 20 C, characterized = BG10 F _H = 20 C, characterized = BG10 F _H = 20 C, characterized = BG10 F _H = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode - 70 F _H = 2400 MHz, -1 dBFS, 12-bit DDC bypass mode - 76 F _H = 2400 MHz, -1 dBFS, 12-bit DDC bypass mode - 76 BO Ω AC-coupled terminated input -140, 1 dBFS/Hz dBFS/Hz - 148FS - 148, 0 dBF/Hz - 148FS - 148, 0 dBF/Hz - 148FS - 148, 0 dBF/Hz - 148, 0 dBF/H		Third hormonic distortion	F _{IN} = 600 MHz, -1 dBFS, 12-bit DDC bypass	$I_A = I_{MIN}$ to I_{MAX}		01	-63	
$ \begin{array}{ c c c } \hline I_{Ac} = I_{AB} \mbox{ In } I_{Ac} \mbox{ In } I_{Ac} \mbox{ In } I_{Ac} = I_{AB} \mbox{ In } I_{Ac} \mbox{ In } I$	HD3	I hird harmonic distortion	houe	$I_A = 25^{\circ}C$, calibration = BG		-81		OBE2
$ \begin{array}{ c $				$I_A = I_{MIN}$ to I_{MAX} , calibration = BG			-64	
$ \begin{array}{ c $			$F_{IN} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12 \text{-bit DDC bypass}$	s mode		-70		
$ \begin{array}{ c c c c c } & NSD & arcses hypering is spectral density, arrange NSD across hypering is and width interfeating purport included in the frame of this, integrated across entire interfeating purports included inter$			$F_{IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12 \text{ bit DDC bypass}$	s mode		-76		
NSD Note spectral density, average ND bacross Nyquits bandwidth 12-bit DDC bypass mode, ADC12J2700, forevcun, = 2.7 GHz 12-bit DDC bypass mode, ADC12J2700, forevcun, = 2.7 GHz 148.0 4BFS/Hz F _N = 600 MHz, -1 dBFS, 12-bit DDC bypass mode 55.3 5 F _N = 500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 600 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 55.2 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 52.4 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 52.4 5 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 65.2 4 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.8 1 F _N = 1500 MHz, -1 dBF				50-Ω AC-coupled terminated input		-147.3		dBFS/Hz
$ \begin{array}{ c c c c c c } \hline bandwidth & \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ $	NSD	Noise spectral density, average NSD across Nyquist	12-bit DDC bypass mode, ADC12J2700,			-149.1		dBm/Hz
		bandwidth	$J_{(\text{DEVCLK})} = 2.7 \text{ GHz}$	F _{IN} = 600 MHz. –1 dBFS		-146.2		dBFS/Hz
$ \begin{array}{ c c c c c } \hline DDC BYPASS MODE, ADC12,11600, $f_{(DEVCLN)$ = 1.6 GHz \\ \hline \\ \hline \\ SIRA \\ N_{n} = Signal-to-noise ratio, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included \\ \hline \\ \mathsf{F_{ni} = 600 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \\ \hline \\ F_{ni} = 2400 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \\ \hline \\ F_{ni} = 2400 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \\ \hline \\ F_{ni} = 2300 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \\ \hline \\ F_{ni} = 2400 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \\ \hline \\ F_{ni} = 350 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \hline \\ \hline \\ F_{ni} = 2300 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \hline \\ \hline \\ F_{ni} = 350 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \hline \\ \hline \\ \\ F_{ni} = 500 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \hline \\ \hline \\ F_{ni} = 1500 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \hline \\ \hline \\ \\ F_{ni} = 1500 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \hline \\ \hline \\ \\ \hline \\ F_{ni} = 1500 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \hline \\ \hline \\ \hline \\ \\ F_{ni} = 1500 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \hline \\ \hline \\ \hline \\ \hline \\ \hline \\ \\ F_{ni} = 1500 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \hline \\ \hline \\ \hline \\ \hline \\ \hline \\ \hline \\ \\ F_{ni} = 1500 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \hline \\ \hline \\ \hline \\ \hline \\ \hline \\ \\ F_{ni} = 2400 \text{ MHz}, -1 dBFS, 12-bit DDC bypass mode \\ \hline \hline \\ \hline $						-148.0		dBm/Hz
$ SINAD \begin{tabular}{ c c c c c } \hline F_{NI} = 350 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 55.3 \\ \hline F_{NI} = 600 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 52.3 \\ \hline T_{A} = 25^{\circ}\mbox{ C} & 54.9 \\ \hline T_{A} = T_{MIN} \mbox{ to } T_{MAX} & 52.3 \\ \hline T_{A} = 25^{\circ}\mbox{ C} & calibration = BG & 54.8 \\ \hline T_{A} = 25^{\circ}\mbox{ C} & calibration = BG & 52.2 \\ \hline F_{NI} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 55.2 \\ \hline F_{NI} = 2400 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 55.2 \\ \hline F_{NI} = 2400 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 55.2 \\ \hline F_{NI} = 350 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 55.2 \\ \hline F_{NI} = 600 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 55.2 \\ \hline F_{NI} = 600 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 55.2 \\ \hline F_{NI} = 600 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 55.2 \\ \hline F_{NI} = 600 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 52.1 \\ \hline T_{A} = 25^{\circ}\mbox{ C} \mbox{ calibration = BG} & 52.1 \\ \hline T_{A} = 25^{\circ}\mbox{ C} \mbox{ calibration = BG} & 52.1 \\ \hline T_{A} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 52.1 \\ \hline T_{A} = 25^{\circ}\mbox{ calibration = BG} & 52.1 \\ \hline T_{A} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 52.1 \\ \hline T_{A} = 25^{\circ}\mbox{ calibration = BG} & 52.1 \\ \hline T_{A} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 52.4 \\ \hline F_{NI} = 500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 52.4 \\ \hline T_{A} = 25^{\circ}\mbox{ calibration = BG} & 52.4 \\ \hline T_{A} = 25^{\circ}\mbox{ calibration = BG} & 52.4 \\ \hline T_{A} = 25^{\circ}\mbox{ calibration = BG} & 52.4 \\ \hline T_{A} = 25^{\circ}\mbox{ calibration = BG} & 52.4 \\ \hline T_{A} = 25^{\circ}\mbox{ calibration = BG} & 52.4 \\ \hline T_{A} = 25^{\circ}\mbox{ calibration = BG} & 52.4 \\ \hline T_{A} = 25^{\circ}\mbox{ calibration = BG} & 52.4 \\ \hline T_{A} = 25^{\circ}\mbox{ calibration = BG} & 52.4 \\ \hline T_{$	DDC BYPAS	S MODE, ADC12J1600, $f_{(DEVCLK)}$ =	1.6 GHz		1			1
SNRSignal-to-noise ratio, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included $F_{IN} = 600$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 1200$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 1200$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 1200$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 350$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°C$ $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass $F_{IN} = 25°$			$F_{IN} = 350 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	mode		55.3		-
Signal-to-noise ratio, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included $F_N = 600 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass}F_N = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypass modeT_A = T_{MN} to T_{MAX}52.3T_A = 25^\circ C, calibration = BG52.3T_A = T_{MN} to T_{MAX}dBFSSignal-to-noise and distortionratio, integrated across entireNUmber of bits,integrated across entireNyquist bandwidthInput frequency-dependentinterleaving spurs includedF_{N} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypassF_{N} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC bypassmodeT_A = 25^\circ C54.8T_A = 25^\circ C52.476.8T_A = 25^\circ C76.8T_A = 25^\circ C76.8$				$T_A = 25^{\circ}C$		54.9		dBFS
$ \begin{array}{ c c c c c } SNR & \begin{tabular}{ c c c c } Night the purphy frequency-dependent in the frequency-dependent interfeaving spurs included & \end{tabular} \\ \hline mode & \end{tabular} \\ \hline T_{A} = 25^{\circ}C, calibration = BG & 54.8 & \end{tabular} \\ \hline T_{A} = T_{MN} \mbox{ to } T_{MAX}, calibration = BG & 52.2 & \end{tabular} \\ \hline T_{A} = T_{MN} \mbox{ to } T_{MAX}, calibration = BG & 52.2 & \end{tabular} \\ \hline T_{N} = 2400 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & \end{tabular} \\ \hline F_{N} = 2400 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & \end{tabular} \\ \hline F_{N} = 350 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & \end{tabular} \\ \hline F_{N} = 500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & \end{tabular} \\ \hline T_{A} = 25^{\circ}C, calibration = BG & \end{tabular} \\ \hline T_{A} = 25^{\circ}C, calibration = BG & \end{tabular} \\ \hline T_{A} = 25^{\circ}C, calibration = BG & \end{tabular} \\ \hline T_{A} = 25^{\circ}C, calibration = BG & \end{tabular} \\ \hline T_{A} = 25^{\circ}C, calibration = BG & \end{tabular} \\ \hline T_{A} = 25^{\circ}C, calibration = BG & \end{tabular} \\ \hline T_{A} = 2400 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & \end{tabular} \\ \hline F_{N} = 350 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & \end{tabular} \\ \hline F_{N} = 2400 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & \end{tabular} \\ \hline F_{N} = 2400 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & \end{tabular} \\ \hline F_{N} = 350 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & \end{tabular} \\ \hline T_{A} = 25^{\circ}C, calibration = BG & \end{tabular} \\ \hline T_{A} = 25^{\circ}C, calibration = BG & \end{tabular} \\ \hline T_{A} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & \end{tabular} \\ \hline T_{A} = 25^{\circ}C, calibration = BG & \end{tabular} \\ \hline T_{A} = 25^{\circ}C, calibration = BG & \end{tabular} \\ \hline T_{A} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & \end{tabular} \\ \hline T_{A} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit DDC bypass$		Signal-to-noise ratio, integrated across entire	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	$T_A = T_{MIN}$ to T_{MAX}	52.3			
$ \begin{array}{ c c c } \hline P_{N} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC \text{ bypass mode} & 52.2 \\ \hline F_{N} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC \text{ bypass mode} & 52.5 \\ \hline F_{N} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC \text{ bypass mode} & 55.2 \\ \hline F_{N} = 350 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC \text{ bypass mode} & 55.2 \\ \hline F_{N} = 600 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC \text{ bypass mode} & 55.2 \\ \hline P_{N} = 600 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC \text{ bypass mode} & 52.1 \\ \hline T_{A} = 25^{\circ}\text{C} & 54.8 \\ \hline P_{N} = 600 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC \text{ bypass} mode & 52.1 \\ \hline T_{A} = 25^{\circ}\text{C} & calibration = BG & 52.1 \\ \hline T_{A} = 25^{\circ}\text{C} & calibration = BG & 52.1 \\ \hline T_{A} = 25^{\circ}\text{C} & calibration = BG & 52.1 \\ \hline T_{A} = 25^{\circ}\text{C} & calibration = BG & 52.1 \\ \hline T_{A} = 25^{\circ}\text{C} & calibration = BG & 52.1 \\ \hline T_{A} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC \text{ bypass} mode & 62.4 \\ \hline F_{N} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC \text{ bypass mode} & 63.9 \\ \hline F_{N} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC \text{ bypass} mode & 8.9 \\ \hline F_{N} = 350 \text{ MHz}, -1 \text{ dBFS}, 12-bit DDC \text{ bypass} mode & 8.4 \\ \hline T_{A} = 25^{\circ}\text{C} & 8.8 $	SNR	Nyquist bandwidth	mode	$T_A = 25^{\circ}C$, calibration = BG		54.8		
$ \begin{tabular}{ c c c c c } \hline F_{IN} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 52.5 \\ \hline F_{IN} = 2400 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 49.8 \\ \hline F_{IN} = 350 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 55.2 \\ \hline F_{IN} = 500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 52.1 \\ \hline T_A = 25^{\circ}C, \mbox{ calibration = BG} & 52.1 \\ \hline T_A = 25^{\circ}C, \mbox{ calibration = BG} & 52.1 \\ \hline T_A = 25^{\circ}C, \mbox{ calibration = BG} & 52.1 \\ \hline T_A = 25^{\circ}C, \mbox{ calibration = BG} & 52.1 \\ \hline T_A = 1 \mbox{ mode} & 52.4 \\ \hline F_{IN} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 52.4 \\ \hline F_{IN} = 2400 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 52.4 \\ \hline F_{IN} = 2400 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 69.9 \\ \hline F_{IN} = 350 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 8.9 \\ \hline F_{IN} = 600 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 6.9 \\ \hline F_{IN} = 350 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 6.9 \\ \hline F_{IN} = 600 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 6.9 \\ \hline F_{IN} = 600 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 6.9 \\ \hline F_{IN} = 600 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 6.9 \\ \hline F_{IN} = 600 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 6.8 \\ \hline T_A = T_{MIN} \mbox{ to } T_{MAX}, \mbox{ calibration = BG} & 8.8 \\ \hline T_A = 25^{\circ}C, \mbox{ calibration = BG} & 8.8 \\ \hline T_A = T_{MIN} \mbox{ to } T_{MAX}, \mbox{ calibration = BG} & 8.4 \\ \hline T_A = 25^{\circ}C, \mbox{ calibration = BG} & 8.4 \\ \hline F_{IN} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 6.8 \\ \hline F_{IN} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 8.4 \\ \hline F_{IN} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 8.4 \\ \hline F_{IN} = 1500 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 8.4 \\ \hline F_{IN} =$		interleaving spurs included		$T_A = T_{MIN}$ to T_{MAX} , calibration = BG	52.2			
$ \begin{array}{ c c c c c c } \hline F_{IN} = 2400 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 49.8 \\ \hline F_{IN} = 350 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass mode} & 55.2 \\ \hline F_{IN} = 600 \mbox{ MHz}, -1 \mbox{ dBFS}, 12-bit \mbox{ DDC bypass} & $$ $$ $$ $$ $$ $$ $$ $$ $$ $$ $$ $$ $$			F_{IN} = 1500 MHz, -1 dBFS, 12-bit DDC bypase	s mode		52.5		
$ SINAD \qquad \qquad$			F_{IN} = 2400 MHz, -1 dBFS, 12-bit DDC bypase	s mode		49.8		
$ SINAD \qquad \qquad Signal-to-noise and distortion ratio, integrated across entire interleaving spurs included \\ SINAD \qquad \qquad$			F_{IN} = 350 MHz, -1 dBFS, 12-bit DDC bypass	mode		55.2		
$ \begin{array}{ c c c c c c } \hline Signal-to-noise and distortion ratio, integrated across entire interleaving spurs included \\ \hline SINAD \\ \hline$				$T_A = 25^{\circ}C$		54.8		
SINADNyduist bandwidth Input frequency-dependent interleaving spurs includedmodeT_A = 25°C, calibration = BG54.7dBFS $T_A = T_{MIN}$ to T_{MAX} , calibration = BG52 $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass mode52.4 $F_{IN} = 2400$ MHz, -1 dBFS, 12-bit DDC bypass mode49.7 $F_{IN} = 350$ MHz, -1 dBFS, 12-bit DDC bypass mode8.9 $F_{IN} = 350$ MHz, -1 dBFS, 12-bit DDC bypass mode8.9 $F_{IN} = 600$ MHz, -1 dBFS, 12-bit DDC bypass mode8.8 $F_{IN} = 600$ MHz, -1 dBFS, 12-bit DDC bypass mode8.8 $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass mode8.8 $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass mode8.4 $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass mode8.4 $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass mode8.4 $F_{IN} = 1500$ MHz, -1 dBFS, 12-bit DDC bypass mode8.4		Signal-to-noise and distortion	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	$T_A = T_{MIN}$ to T_{MAX}	52.1			
$\begin{tabular}{ c c c c c c c } \hline T_A = T_{MIN} \ to \ T_{MAX}, \ calibration = BG & 52 \\ \hline T_A = T_{MIN} \ to \ T_{MAX}, \ calibration = BG & 52 \\ \hline F_{IN} = 1500 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 49.7 \\ \hline F_{IN} = 2400 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.9 \\ \hline F_{IN} = 350 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.9 \\ \hline F_{IN} = 600 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 1500 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 1500 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 1500 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 1500 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 1500 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 1500 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ dBFS, 12-bit \ DDC \ bypass \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz, -1 \ MHz \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz \ mode & 8.4 \\ \hline F_{IN} = 100 \ MHz \ mode & 8.4 \\ \hline F_{IN} = 100 \$	SINAD	Nyquist bandwidth	mode	$T_A = 25^{\circ}C$, calibration = BG		54.7		dBFS
$\frac{F_{IN} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-bit \text{ DDC bypass mode}}{F_{IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-bit \text{ DDC bypass mode}} = \frac{52.4}{49.7}$ $F_{IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-bit \text{ DDC bypass mode}} = \frac{8.9}{8.9}$ $F_{IN} = 350 \text{ MHz}, -1 \text{ dBFS}, 12-bit \text{ DDC bypass mode}} = \frac{8.9}{14}$ $F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12-bit \text{ DDC bypass mode}} = \frac{7}{4} = 25^{\circ}\text{C} + 38.8}$ $\frac{T_A = 25^{\circ}\text{C}, \text{ calibration = BG}}{T_A = 25^{\circ}\text{C}, \text{ calibration = BG}} = \frac{8.4}{14}$ $F_{IN} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-bit \text{ DDC bypass mode}} = \frac{8.4}{14}$ $F_{IN} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-bit \text{ DDC bypass mode}} = \frac{8.4}{14}$		Input frequency-dependent interleaving spurs included		$T_A = T_{MIN}$ to T_{MAX} , calibration = BG	52			
$ \begin{array}{ c c c c c c c c } \hline F_{IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 49.7 \\ \hline F_{IN} = 350 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.9 \\ \hline F_{IN} = 500 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass} & \hline T_A = 25^\circ \text{C} & 8.8 \\ \hline T_A = T_{MIN} \text{ to } T_{MAX} & 8.4 \\ \hline T_A = 25^\circ \text{C}, \text{ calibration = BG} & 8.8 \\ \hline T_A = T_{MIN} \text{ to } T_{MAX}, \text{ calibration = BG} & 8.8 \\ \hline T_A = T_{MIN} \text{ to } T_{MAX}, \text{ calibration = BG} & 8.4 \\ \hline F_{IN} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.4 \\ \hline F_{IN} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.4 \\ \hline F_{IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.4 \\ \hline F_{IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.4 \\ \hline F_{IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.4 \\ \hline F_{IN} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.4 \\ \hline F_{IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{ bit DC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{ bit DC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{ bit DC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{ bit DC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{ bit DC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{ bit DC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{ bit DC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MHz}, -1 \text{ dBFS}, 12-\text{ bit DC bypass mode} & 8.4 \\ \hline F_{IN} = 100 \text{ MES}, -100 \text{ MES}, -10$		interfecting option included	F _{IN} = 1500 MHz, -1 dBFS, 12-bit DDC bypass	s mode		52.4		
$ENOB \qquad \begin{array}{ c c c c } \hline F_{IN} = 350 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass mode} & & & & & & & & & & & & & & & & & & &$			F _{IN} = 2400 MHz, -1 dBFS, 12-bit DDC bypass	$F_{IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12-\text{bit DDC bypass mode}$		49.7		
ENOB Effective number of bits, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included $F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass} = \frac{T_A = 25^\circ\text{C}}{T_A = T_{MIN} \text{ to } T_{MAX}} = \frac{8.8}{T_A = 25^\circ\text{C}} = \frac{8.8}{T_A = T_{MIN} \text{ to } T_{MAX}} = \frac{8.4}{T_A = 25^\circ\text{C}} = \frac{8.8}{T_A = 10^\circ\text{C}} = \frac{8.8}{T_A = 10^\circ\text{C}} = \frac{8.8}{T_A = 25^\circ\text{C}} = \frac{8.8}{T_A = 10^\circ\text{C}} = \frac{8.8}{T_A = 10^\circ$			F _{IN} = 350 MHz, -1 dBFS, 12-bit DDC bypass	mode		8.9		
ENOB Effective number of bits, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included $F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass} \qquad T_A = T_{MIN} \text{ to } T_{MAX} \qquad 8.4$ $T_A = 25^{\circ}\text{C}, \text{ calibration} = BG \qquad 8.8$ $T_A = T_{MIN} \text{ to } T_{MAX}, \text{ calibration} = BG \qquad 8.4$ $F_{IN} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass mode} \qquad 8.4$				$T_A = 25^{\circ}C$		8.8		
ENOB Nyquist bandwidth Input frequency-dependent interleaving spurs included TN = 000 MHz, -1 dBFS, 12-bit DDC bypass TA = 25°C, calibration = BG 8.8 Bits Fin = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode Fin = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.4 8.4		Effective number of bits,	E 600 MHz -1 dBES 12-bit DDC bypass	$T_A = T_{MIN}$ to T_{MAX}	8.4			Bits
Input frequency-dependent interleaving spurs included $T_A = T_{MIN}$ to T_{MAX} , calibration = BG 8.4 F _{IN} = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode 8.4 F _{IN} = 2400 MHz, -1 dBFS, 12-bit DDC bypass mode 8.4	ENOB	Integrated across entire Nyquist bandwidth	mode	$T_A = 25^{\circ}C$, calibration = BG		8.8		
$F_{\rm IN} = 1500 \text{ MHz}, -1 \text{ dBFS}, 12 \text{-bit DDC bypass mode}$ $\frac{1}{10000000000000000000000000000000000$		Input frequency-dependent	-	$T_{A} = T_{MIN}$ to T_{MAX} , calibration = BG	8.4			
$F_{\rm m} = 2400 \text{ MHz} = 1 \text{ dBES} 12 \text{ bit DDC bypass mode}$		meneaving spurs included	F _{IN} = 1500 MHz, -1 dBFS, 12-bit DDC bypass mode		-	8.4		-
		$F_{\rm IN}$ = 2400 MHz, -1 dBFS, 12-bit DDC bypass mode			8			

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Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN full scale range at default setting (725 mV_{PP}), VIN = -1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A = 25^{\circ}\text{C}^{.(1)(2)}$

	PARAMETER	TEST CONDI	TIONS	MIN	TYP	MAX	UNIT
		$F_{IN} = 350 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	mode		72.9		
			$T_A = 25^{\circ}C$		74.8		
	Sourious-free dynamic range	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12 \text{-bit DDC bypass}$	$T_A = T_{MIN}$ to T_{MAX}			61.8	
SFDR	Input frequency-dependent	mode	$T_A = 25^{\circ}C$, calibration = BG		71		dBFS
	interleaving spurs included		T_{A} = T_{MIN} to T_{MAX} , calibration = BG			60.7	
		F_{IN} = 1500 MHz, -1 dBFS, 12-bit DDC bypass	s mode		66.7		
		F_{IN} = 2400 MHz, -1 dBFS, 12-bit DDC bypass	mode		59.8		
			T _A = 25°C		-77		
f_/2	Interleaving offset spur at 1/2	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	$T_A = T_{MIN}$ to T_{MAX}			-59.8	dBES
192	sampling rate	mode	$T_A = 25^{\circ}C$, calibration = BG		-73		
			$T_A = T_{MIN}$ to T_{MAX} , calibration = BG			-57.3	
		_	$T_A = 25^{\circ}C$		-72		
f_/4	Interleaving offset spur at 1/4	F _{IN} = 600 MHz, -1 dBFS, 12-bit DDC bypass	$T_A = T_{MIN}$ to T_{MAX}			-54.3	dBFS
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	sampling rate	mode	$T_A = 25^{\circ}C$, calibration = BG		-69		
			$T_A = T_{MIN}$ to T_{MAX} , calibration = BG			-54	
		-	$T_A = 25^{\circ}C$		-77		
f _s /2 – F _{IN}	Interleaving offset spur at ½ sampling rate – input frequency	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	$T_A = T_{MIN}$ to T_{MAX}			-62	dBFS
,		mode	$T_A = 25^{\circ}C$, calibration = BG		-79		
			$T_A = T_{MIN}$ to T_{MAX} , calibration = BG			-62	
	latada a da a desta a como at 17		$T_A = 25^{\circ}C$		-76		
$f_{\rm S}/4 + F_{\rm IN}$	sampling rate + input	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	$T_A = T_{MIN}$ to T_{MAX}			-61.8	dBFS
	frequency	mode	$T_A = 25^{\circ}C$, calibration = BG		-74		
			$T_A = T_{MIN}$ to T_{MAX} , calibration = BG			-61	
	latada a da a desta a como et 17	F_{IN} = 600 MHz, -1 dBFS, 12-bit DDC bypass mode	T _A = 25°C		-76		dBFS
$f_{\rm S}/4 - F_{\rm IN}$	sampling rate – input frequency		$T_A = T_{MIN}$ to T_{MAX}			-62	
			$I_A = 25^{\circ}$ C, calibration = BG		-77		
			$I_A = I_{MIN}$ to I_{MAX} , calibration = BG			-61	
		$F_{IN} = 350 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$			-72		dBFS
			$I_A = 25^{\circ}C$		-12	60.0	
TUD	Total harmonic distantian	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$ mode	$I_A = I_{MIN}$ to I_{MAX}		74	-60.9	
IND	Total narmonic distortion		$T_A = 25^{\circ}$ C, calibration = BG		-/	61	
		E = 1500 MHz 1 dBES 12 bit DDC bypass	$T_A = T_{MIN}$ to T_{MAX} , calibration = BG		60	-01	
		$F_{\rm IN} = 2400 \text{ MHz} = 1 \text{ dBFS} + 12 \text{-bit DDC bypass}$	mode		_69		
		$F_{IN} = 350 \text{ MHz} = 1 \text{ dBFS} + 12 \text{ bit DDC bypass}$	mode		_79		
			$T_{\rm A} = 25^{\circ} C$		-78		
			$T_A = 2000$ $T_a = T_{ABA}$ to T_{ABA}		10	-62	
HD2	Second harmonic distortion	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$ mode	$T_A = 25^{\circ}$ C calibration = BG		-79	02	dBES
			$T_A = T_{AB}$ to T_{AAX} calibration = BG			-63	02.0
		E _{IN} = 1500 MHz. –1 dBFS, 12-bit DDC bypass	s mode		-73		
		$F_{\rm IN} = 2400 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	s mode		-70		
		$F_{IN} = 350 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$	mode		-76		
			T _A = 25°C		81		
		Fui = 600 MHz =1 dBES 12-bit DDC bypass	$T_A = T_{MIN}$ to T_{MAX}			-65	
HD3	Third harmonic distortion	$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}, 12\text{-bit DDC bypass}$ In harmonic distortion	$T_A = 25^{\circ}C$, calibration = BG		-76		dBFS
500			$T_A = T_{MIN}$ to T_{MAX} , calibration = BG			-61	
F		F _{IN} = 1500 MHz, -1 dBFS, 12-bit DDC bypass	mode		-72		
	F	F _{IN} = 2400 MHz, -1 dBFS, 12-bit DDC bypass	s mode		-76		



Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN full scale range at default setting (725 mV_{PP}), VIN = -1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A = 25^{\circ}\text{C.}^{(1)(2)}$

	PARAMETER	TEST COND	ITIONS	MIN	TYP	MAX	UNIT	
					-145		dBFS/Hz	
	Noise spectral density,	12-bit DDC bypass mode, ADC12J1600,	50-Ω AC-coupled terminated input		-146.8		dBm/Hz	
NSD	average NSD across Nyquist bandwidth	$f_{(\text{DEVCLK})} = 1.6 \text{ GHz}$			-143.9		dBFS/Hz	
			$F_{IN} = 600 \text{ MHz}, -1 \text{ dBFS}$		-145.7		dBm/Hz	
DECIMATE-BY-8	8 MODE, ADC12J2700, <i>f</i> (DEVCLK)	= 2.7 GHz						
	Signal-to-noise ratio,	FIN = 600 MHz1 dBFS, decimate-by-8			62.8			
SNR	integrated across DDC output bandwidth	mode	Calibration = BG		62.7		dBFS	
	Interleaving spurs included	F _{IN} = 2400 MHz, -1 dBFS, Decimate-by-8 m	ode		53.3			
	Signal-to-noise and distortion	FIN = 600 MHz1 dBFS, decimate-by-8			62.8			
SINAD	ratio, integrated across DDC	mode	Calibration = BG		62.7		dBFS	
	Interleaving spurs included	F _{IN} = 2400 MHz, -1 dBFS, decimate-by-8 mc	ode		53.3			
	Effective number of bits,	FIN = 600 MHz1 dBFS, decimate-by-8			10.1			
ENOB	integrated across DDC output bandwidth	mode	Calibration = BG		10.1		Bits	
	Interleaving spurs included	F _{IN} = 2400 MHz, -1 dBFS, decimate-by-8 mc	ode		8.6			
	Spurious-free dynamic range	$F_{m} = 600 \text{ MHz}$ 1 dBFS, decimate-by-8			75.9			
SFDR	Interleaving spurs included	mode	Calibration = BG		74.7		dBFS	
	Interleaving offset spur at 1/2	F _{IN} = 600 MHz. –1 dBFS, decimate-by-8			-73		dBFS	
f _{\$} /2	sampling rate ⁽³⁾	mode	Calibration = BG		-72			
	Interleaving offset spur at 1/4	$E_{\rm W} = 600 \text{ MHz} -1 \text{ dBES}$ decimate-by-8			-70			
f _S /4	sampling rate ⁽³⁾	mode	Calibration = BG		-70		dBFS	
	Interleaving spur at 1/2	E = 600 MHz 1 dBES docimate by 8			-80			
$f_{\rm S}/2 - {\rm F_{\rm IN}}$	sampling rate – input frequency ⁽³⁾	mode	Calibration = BG		-79		dBFS	
	Interleaving spur at 1/4	E = 600 MHz 1 dBES docimate by 8			-73			
$f_{\rm S}/4 + F_{\rm IN}$	sampling rate + input frequency ⁽³⁾	mode	Calibration = BG		-70		dBFS	
	Interleaving spur at 1/4	E 600 MHz -1 dBES decimate-by-8			-77			
$f_{\rm S}/4 - {\rm F_{\rm IN}}$	sampling rate – input frequency ⁽³⁾	mode	Calibration = BG		-77		dBFS	
		F _{IN} = 600 MHz, -1 dBFS, decimate-by-8			-70		dBFS	
THD	Total harmonic distortion ⁽³⁾	mode	calibration = BG		-71			
		F _{IN} = 2400 MHz, -1 dBFS, decimate-by-8 mode			-65		1	
		F _{IN} = 600 MHz, -1 dBFS, decimate-by-8			-78			
HD2	Second harmonic distortion ⁽³⁾	mode	Calibration = BG		-76		dBFS	
		F _{IN} = 2400 MHz, -1 dBFS, decimate-by-8 mc	ode		-67			
		F _{IN} = 600 MHz, -1 dBFS, decimate-by-8			-74			
HD3	Third harmonic distortion ⁽³⁾	mode	Calibration = BG		81		dBFS	
		F _{IN} = 2400 MHz, -1 dBFS, decimate-by-8 mc	ode		-73			
DECIMATE-BY-8	8 MODE, ADC12J1600, f _(DEVCLK)	= 1.6 GHz						
	Signal-to-noise ratio,	F _{IN} = 600 MHz, -1 dBFS, decimate-bv-8			63.5			
SNR	integrated across DDC output bandwidth	mode	Calibration = BG		63.4		dBFS	
	Interleaving spurs included	F _{IN} = 2400 MHz, -1 dBFS, decimate-by-8 mc	ode		55.8			
	Signal-to-noise and distortion	$F_{IN} = 600 \text{ MHz}$ 1 dBFS, decimate-by-8			63.5			
SINAD	ratio, integrated across DDC	mode	Calibration = BG		63.4		dBFS	
	Interleaving spurs included	F _{IN} = 2400 MHz, -1 dBFS, decimate-by-8 mc	ode		55.8			
	Effective number of bits,	F _{IN} = 600 MHz, -1 dBFS. decimate-bv-8			10.3			
ENOB	integrated across DDC output	mode	Calibration = BG		10.2		Bits	
	Interleaving spurs included	F _{IN} = 2400 MHz, -1 dBFS, decimate-by-8 mc	ode		9.0			
	Spurious-free dynamic range	$F_{IN} = 600 \text{ MHz}$ -1 dBFS_decimate-by-8			76.2			
SFDR	Interleaving Spurs Included	Inge r _{IN} = 600 MHZ, -1 GBFS, decimate-by-8 ad mode	Calibration = BG		76.7		dBFS	
	Interleaving offset spur at 1/4 F	4 E = 600 MHz =1 dBES_docimato-by-8			-73			
∫ _{\$} /2	sampling rate ⁽³⁾	mode	Calibration = BG		-72		dBFS	

(3) Magnitude of reported tones in output spectrum of ADC core. This tone will only be present in the DDC output for specific Decimation and NCO settings. Careful frequency planning can be used to intentionally place unwanted tones outside the DDC output spectrum.

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STRUMENTS

EXAS

Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN full scale range at default setting (725 mV_{PP}), VIN = -1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A = 25^{\circ}C$.⁽¹⁾⁽²⁾

	PARAMETER	TEST CONI	DITIONS	MIN	TYP	MAX	UNIT
f /A	Interleaving offset spur at 1/4	F _{IN} = 600 MHz, -1 dBFS, decimate-by-8			-70		dBES
J s/4	sampling rate ⁽³⁾	mode	Calibration = BG		-69		UDF 3
f /2 E	Interleaving spur at 1/2	F _{IN} = 600 MHz, -1 dBFS, decimate-by-8			-78		
J _S /2 - F _{IN}	frequency ⁽³⁾	mode	Calibration = BG		-79		UBF5
	Interleaving spur at 1/4	E _w = 600 MHz =1 dBES_decimate-by-8			-76		
$f_{\rm S}/4 + F_{\rm IN}$	sampling rate + input frequency ⁽³⁾	mode	Calibration = BG		-77		dBFS
	Interleaving spur at 1/4				-77		
$f_{\rm S}/4-{\rm F_{\rm IN}}$	sampling rate - input	$F_{IN} = 600$ MHz, -1 dBFS, decimate-by-8 mode	Calibration = BG		-72		dBFS
	liequency				71		
тно	Total harmonic distortion ⁽³⁾	F _{IN} = 600 MHz, -1 dBFS, decimate-by-8 mode	Calibration - BG		_71		dBES
THE		E., = 2400 MHz =1 dBES_decimate-by-8 mode			-63		ubi 5
		$\Gamma_{\rm IN} = 2400$ MHz, -1 dbi 0, decimate by 0 m			_77		
	Second harmonic distortion ⁽³⁾	$F_{IN} = 600$ MHz, -1 dBFS, decimate-by-8 mode	Calibration - BG		_78		dBES
1102	Second harmonic distortion	E., = 2400 MHz = 1 dBES_decimate-by-8 m	ode		-65		ubi 5
		$\Gamma_{\rm IN} = 2400$ MHz, -1 dbl C, decimate by C m			_80		
нрз	Third harmonic distortion ⁽³⁾	F _{IN} = 600 MHz, -1 dBFS, decimate-by-8 mode	Calibration - BG		_77		dBES
1123		E 2400 MHz -1 dBES decimate-by-8 m	ode		_74		ubi o
DDC CHARACT	FRISTICS	$\Gamma_{\rm IN} = 2400$ MHz, Γ dbi C, dcoimate by C m			14		
DDO ONANAON	Alias protection ⁽⁴⁾			80			dB
				00			% of
	Alias protected bandwidth ⁽⁴⁾			80			output BW
SFDR-DDC	Spurious-free dynamic range of digital down-converter ⁽⁴⁾			100			dB
	Implementation loss ⁽⁴⁾					0.5	dB
ANALOG INPUT	CHARACTERISTICS			1			
	Full-scale analog differential	Minimum FSR setting ⁽⁵⁾			500		
V _{ID(VIN)}	Full-scale analog-differential input range	Default FSR setting, $T_A = T_{MIN}$ to T_{MAX}		650	725	800	mV _{PP}
		Maximum FSR setting ⁽⁵⁾			950		
CIOVIN	Analog input capacitance ⁽⁴⁾	Differential			0.05		pF
		Each input pin to ground			1.5		pF
R _{ID(VIN)}	Differential input resistance			80	95	110	Ω
FPBW	Full power bandwidth	-3 dB — calibration = BG			2.8		GHz
	•	-3 dB — calibration = FG			3.2		
		DC to 2 GHz			1.2		
	Gain flatness	2 GHz to 4 GHz			3.8		dB
		DC to 2 GHz — calibration = BG			1.5		
		2 GHz to 4 GHz — calibration = BG			4.5		
ANALOG OUTP	UT CHARACTERISTICS (VCMC	D, VBG)		1			
V _(VCMO)	Common-mode output	I _(VCMO) = ±100 μA, T _A = 25°C			1.225		V
,	vollage	$I_{(VCMO)} = \pm 100 \ \mu A$, $T_A = T_{MIN}$ to T_{MAX}		1.185		1.265	
TCV _{O(VCMO)}	Common-mode output- voltage temperature coefficient	$T_A = T_{MIN}$ to T_{MAX}			-21		ppm/°C
C _(LOAD_VCMO)	Maximum VCMO output load capacitance					80	pF
Veree	Bandgap reference output	$I_{(BG)} = \pm 100 \ \mu A, \ T_A = 25^{\circ}C$			1.248		V
• O(BG)	voltage	$I_{(BG)}=\pm 100~\mu A,~T_A=T_{MIN}$ to T_{MAX}		1.195		1.3	v
TCV _{ref(BG)}	Bandgap reference voltage temperature coefficient				0		ppm/°C
C _(LOAD_BG)	Maximum bandgap reference output load capacitance					80	pF
L	· · ·			1			

(4) This parameter is specified by design and is not tested in production.

(5) This parameter is specified by design, characterization, or both and is not tested in production.



Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN full scale range at default setting (725 mV_{PP}), VIN = -1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A = 25^{\circ}C$.⁽¹⁾⁽²⁾

	PARAMETER	TEST COND	ITIONS	MIN	TYP	MAX	UNIT
TEMPERATU	IRE DIODE CHARACTERISTICS						
V	Temperature diode voltage	Offset voltage (approx. 0.77 V) varies with process and must be measured for each part. Offset measurement should be done	100-µA forward current Device active		-1.6		mV/°C
V (TDIODE)	slope	with PowerDown=1 to minimize device self- heating.	100-μA forward current Device in power-down		-1.6		mV/°C
CLOCK INPU	IT CHARACTERISTICS (DEVCLK±	, SYSREF±, SYNC~/TMST±)					
V	Differential clock input level	Sine wave clock, $T_A = T_{MIN}$ to T_{MAX}		0.4	0.6	2	V _{PP}
V ID(CLK)	Differential clock input level	Square wave clock, T_{A} = T_{MIN} to T_{MAX}		0.4	0.6	2	V _{PP}
I _{I(CLK)}	Input current	$V_I = 0 \text{ or } V_I = V_A$			±1		μΑ
<u> </u>	Input conscitonce (4)	Differential			0.02		pF
CI(CLK)		Each input to ground			1		pF
Р	Differential input registeres	T _A = 25°C			95		Ω
RID(CLK)	Differential input resistance	$T_A = T_{MIN}$ to T_{MAX}		80		110	Ω
CML OUTPUT	T CHARACTERISTICS (DS0-DS7±	-)					
V _{OD}	Differential output voltage	Assumes ideal 100-Ω load Measured differentially Default pre-emphasis setting		280	305	330	mV peak
V _{O(ofs)}	Output offset voltage				0.6		V
	Output about airquit aurrant	Output+ and output- shorted together			±6		
IOS	Output short-circuit current	Output+ or output- shorted to 0 V			12		mA
Z _{OD}	Differential output impedance				100		Ω
LVCMOS INP	PUT CHARACTERISTICS (SDI, SCI	LK, SCS, SYNC~)					
V _{IH}	Logic high input voltage	See ⁽⁵⁾		0.83			V
V _{IL}	Logic low input voltage	See ⁽⁵⁾				0.4	V
CI	Input capacitance ⁽⁴⁾⁽⁶⁾	Each input to ground			1		pF
LVCMOS OU	TPUT CHARACTERISTICS (SDO,	OR_T0, OR_T1)					
V _{OH}	CMOS H level output	$I_{OH} = -400 \ \mu A^{(5)}$		1.65	1.9		V
V _{OL}	CMOS L level output	$I_{OH} = 400 \ \mu A^{(5)}$			0.01	0.15	V
POWER SUP	PLY CHARACTERISTICS						
ADC12J2700	, $f_{(\text{DEVCLK})}$ = 2.7 GHz						
		PD = 0, calibration = FG, bypass DDC			457	495	
I _(VA19)	Analog 1.9-V supply current	PD = 0, calibration = BG, bypass DDC			557	594	mA
		PD = 0, calibration = BG, decimate by 8, DDF	R = 0, P54 = 1		557	598	
		PD = 0, calibration = FG, bypass DDC			245	296	
I _(VA12)	Analog 1.2-V supply current	PD = 0, calibration = BG, bypass DDC			261	312	mA
		PD = 0, calibration = BG, decimate by 8, DDF	R = 0, P54 = 1		270	322	
		PD = 0, calibration = FG, bypass DDC			330	541	
I _(VD12)	Digital 1.2-V supply current	PD = 0, calibration = BG, bypass DDC			341	588	mA
		PD = 0, calibration = BG, decimate by 8, DDF	R = 0, P54 = 1		366	610	
		PD = 0, calibration = FG, bypass DDC			1.56	1.94	
P _C	Device economican	PD = 0, calibration = BG, bypass DDC			1.78	2.21	W
	Power consumption	PD = 0, calibration = BG, decimate by 8, DDF	R = 0, P54 = 1		1.82	2.25	
		PD = 1			< 50		mW

(6) The digital control pin capacitances are die capacitances only and is in addition to package and bond-wire capacitance of approximately 0.4 pF.

Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN full scale range at default setting (725 mV_{PP}), VIN = -1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A = 25^{\circ}C$.⁽¹⁾⁽²⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC12J1600	, $f_{(\text{DEVCLK})} = 1.6 \text{ GHz}$					
		PD = 0, calibration = FG, bypass DDC		454	493	
I _(VA19)	Analog 1.9-V supply current	PD = 0, calibration = BG, bypass DDC		553	591	mA
		PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1		553	598	
I _(VA12)		PD = 0, calibration = FG, bypass DDC		180	222	
	Analog 1.2-V supply current	PD = 0, calibration = BG, bypass DDC		190	233	mA
		PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1		196	243	
		PD = 0, calibration = FG, bypass DDC		225	460	
I _(VD12)	Digital 1.2-V supply current	PD = 0, calibration = BG, bypass DDC		237	529	mA
		PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1		255	568	
		PD = 0, calibration = FG, bypass DDC		1.35	1.75	
P _C	Device consumption	PD = 0, calibration = BG, bypass DDC		1.56	2.04	W
	Power consumption	PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1		1.59	2.11	
		PD = 1		< 50		mW

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
DEVICE (SAMPLING) CLOCK					
		Sampling rate is equal to clock input, ADC12J2700	1		2.7	011
J (DEVCLK)	Input DEVCLK frequency	Sampling rate is equal to clock input, ADC12J1600	1		1.6	GHZ
t _{d(A)}	Sampling (aperture) delay	Input CLK transition to sampling instant		0.64		ns
t _(AJ)	Aperture jitter			0.1		ps RMS
t _(LAT)	ADC core latency ⁽¹⁾	Decimation = 1, DDR = 1, P54 = 0		64		t _(DEVCLK)
		Decimation = 4, DDR = 1, P54 = 0		292		
		Decimation = 4, DDR = 1, P54 = 1		284		
		Decimation = 8, DDR = 0, P54 = 0		384		
		Decimation = 8, DDR = 0, P54 = 1		368		
		Decimation = 8, DDR = 1, P54 = 0		392		
		Decimation = 8, DDR = 1, P54 = 1		368		
		Decimation = 10, DDR = 0, P54 = 0		386		
		Decimation = 10, DDR = 1, P54 = 0		386		
t _(LAT_DDC)	ADC core and DDC latency ⁽¹⁾	Decimation = 16, DDR = 0, $P54 = 0$		608		t _(DEVCLK)
		Decimation = 16, DDR = 0, P54 = 1		560		
		Decimation = 16, DDR = 1, P54 = 0		608		
		Decimation = 16, DDR = 1, P54 = 1		560		
		Decimation = 20, DDR = 0, P54 = 0		568		
		Decimation = 20, DDR = 1, P54 = 0		568		
		Decimation = 32, DDR = 0, $P54 = 0$		1044		
		Decimation = 32, DDR = 0, P54 = 1		948		
		Decimation = 32, DDR = 1, P54 = 0		1044		

(1) Unless otherwise specified, delays quoted are exact un-rounded functional delays (assuming zero propagation delay).



Timing Requirements (continued)

			MIN NOM MAX	UNIT	
JESD204	B INTERFACE LINK TIMING CHARACTERIS	FICS (REFER TO Figure 1)			
t _{d(LMFC)}	SYSREF to LMFC delay Functional delay between SYSREF assertion latched and LMFC frame boundary ⁽¹⁾	All decimation modes	40	t _(DEVCLK)	
t _{d(TX)}	LMFC to frame boundary delay - DDC bypass mode Functional delay from LMFC frame boundary to beginning of next multi-frame in transmitted data. ⁽²⁾	Decimation = 1, DDR = 1, P54 = 0	52.7	t _(DEVCLK)	
		Decimation = 4, DDR = 1, P54 = 0	52.7		
		Decimation = 4, DDR = 1, P54 = 1	43.9		
		Decimation = 8, DDR = 0, P54 = 0	60.7		
		Decimation = 8, DDR = 0, P54 = 1	51.5		
		Decimation = 8, DDR = 1, P54 = 0	52.7		
		Decimation = 8, DDR = 1, P54 = 1	43.9		
		Decimation = 10, DDR = 0, P54 = 0	60.7		
	LMFC to frame boundary delay - decimation modes	Decimation = 10, DDR = 1, P54 = 0	52.7		
t _{d(TX)}	Functional delay from LMFC frame boundary	Decimation = 16, DDR = 0, P54 = 0	60.7	t _(DEVCLK)	
	to beginning of next multi-frame in transmitted data ⁽²⁾	Decimation = 16, DDR = 0, P54 = 1	51.5		
		Decimation = 16, DDR = 1, P54 = 0	52.7		
		Decimation = 16, DDR = 1, P54 = 1	43.9		
		Decimation = 20, DDR = 0, P54 = 0	60.7		
		Decimation = 20, DDR = 1, P54 = 0	52.7		
		Decimation = 32, DDR = 0, P54 = 0	60.7		
		Decimation = 32, DDR = 0, P54 = 1	51.5		
		Decimation = 32, DDR = 1, P54 = 0	52.7		
t _{su(SYNC~-} F)	SYNC~ to LMFC setup time ⁽³⁾ Required SYNC~ setup time relative to the in-	ernal LMFC boundary.	40		
t _{h(SYNC~-} F)	SYNC~ to LMFC hold time ⁽³⁾ Required SYNC~ hold time relative to the inter-	rnal LMFC boundary.	-8	^I (DEVCLK)	
t _(SYNC~)	SYNC~ assertion time Required SYNC~ assertion time before dease	ertion to initiate a link resynchronization.	4	Frame clock cycles	
t _{d(LMFC)}	Delay from SYSREF sampled high by DEVCL	K to internal LMFC boundary	40	t _(DEVCLK)	
t _(ILA)	Duration of initial lane alignment sequence		4	Multi-frame clock cycles	
SYSREF					
t _{su(SYS)}	Setup time SYSREF relative to DEVCLK risin	g edge ⁽⁴⁾	40	ps	
t _{h(SYS)}	Hold time SYSREF relative to DEVCLK rising	edge ⁽⁴⁾	40	ps	
t _(PH_SYS)	SYSREF assertion duration after rising edge	event.	8	t _(DEVCLK)	
t _(PL_SYS)	SYSREF deassertion duration after falling edge	ge event.	8	t _(DEVCLK)	
		DDR = 0, P54 = 0	K × F × 10	t _(DEVCLK)	
	Deried SVSPEE	DDR = 0, P54 = 1	K×F× 8		
'(SYS)		DDR = 1, P54 = 0	K×F× 5		
		DDR = 1, P54 = 1	K×F× 4		

(2) The values given are functional delays only. Additional propagation delay of 0 to 3 clock cycles will be present.

This parameter must be met to achieve deterministic alignment of the data frame and NCO phase to other similar devices. If this (3)

parameter is not met the device will still function correctly but will not be aligned to other devices. This parameter is specified by design, characterization, or both and is not tested in production.

(4)

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Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
SERIAL	INTERFACE (REFER TO Figure 2)				
$f_{({\rm SCK})}$	Serial clock frequency ⁽⁵⁾			20	MHz
t _(PH)	Serial clock high time	20			ns
t _(PL)	Serial clock low time	20			ns
t _{su}	Serial-data to serial-clock rising setup time ⁽⁵⁾	10			ns
t _h	Serial-data to serial clock rising hold time ⁽⁵⁾	10			ns
t _(CSS)	SCS-to-serial clock rising setup time	10			ns
t _(CSH)	SCS-to-serial clock falling hold time	10			ns
t _(IAG)	Inter-access gap	10			ns

(5) This parameter is specified by design and is not tested in production.

6.7 Internal Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DEVICE	(SAMPLING) CLOCK					
t _{d(A)}	Sampling (aperture) delay Input CLK transition to sampling instant			0.64		ns
t _(AJ)	Aperture jitter			0.1		ps RMS
t _(LAT)	ADC core latency. See (1)	Decimation = 1, DDR = 1, P54 = 0		64		t _(DEVCLK)
CALIBRATION TIMING CHARACTERISTICS (REFER TO THE CALIBRATION SECTION)						
t	Calibration cyclo timo	Calibration = FG, T_AUTO=1			227 × 10 ⁶	t
(CAL)		Calibration = FG, T_AUTO=0			102 × 10 ⁶	(DEVCLK)
JESD204	B INTERFACE LINK TIMING CHARACTERISTI	CS (REFER TO Figure 1)				
t _{d(LMFC)}	SYSREF to LMFC delay Functional delay between SYSREF assertion latched and LMFC frame boundary ⁽¹⁾	All decimation modes		40		t _(DEVCLK)
t _{d(TX)}	LMFC to Frame Boundary delay - DDC Bypass Mode Functional delay from LMFC frame boundary to beginning of next multi-frame in transmitted data ⁽²⁾	Decimation = 1, DDR = 1, P54 = 0		52.7		t _(DEVCLK)
	LMFC to frame boundary delay - decimation	Decimation = 4, DDR = 1, P54 = 0		52.7		
		Decimation = 4, DDR = 1, P54 = 1		43.9		
		Decimation = 8, DDR = 0, P54 = 0		60.7		-
		Decimation = 8, DDR = 0, P54 = 1		51.5		
		Decimation = 8, DDR = 1, P54 = 0		52.7		
		Decimation = 8, DDR = 1, P54 = 1		43.9		
		Decimation = 10, DDR = 0, P54 = 0		60.7		
		Decimation = 10, DDR = 1, P54 = 0		52.7		
t _{d(TX)}	Functional delay from LMFC frame boundary	Decimation = 16, DDR = 0, P54 = 0		60.7		t _(DEVCLK)
	to beginning of next multi-frame in transmitted data ⁽²⁾	Decimation = 16, DDR = 0, P54 = 1		51.5		
		Decimation = 16, DDR = 1, P54 = 0		52.7		
		Decimation = 16, DDR = 1, P54 = 1		43.9		
		Decimation = 20, DDR = 0, P54 = 0		60.7		
		Decimation = 20, DDR = 1, P54 = 0		52.7		
		Decimation = 32, DDR = 0, P54 = 0		60.7		_
		Decimation = 32, DDR = 0, P54 = 1		51.5		
		Decimation = 32, DDR = 1, P54 = 0		52.7		
$t_{d(LMFC)}$	Delay from SYSREF sampled high by DEVCLK	to internal LMFC boundary		40		t _(DEVCLK)
t _(ILA)	A) Duration of initial lane alignment sequence			4		Multi-frame clock cycles

Unless otherwise specified, delays quoted are exact un-rounded functional delays (assuming zero propagation delay). The values given are functional delays only. Additional propagation delay of 0 to 3 clock cycles will be present. (1)

(2)



6.8 Switching Characteristics

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a foreground mode calibration with timing calibration enabled. Typical values are at $T_A = 25^{\circ}\text{C}$.

(1.00)		•			<i>'</i> · ·	
	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT	
SERIAL I	DATA OUTPUTS					
	Serialized output bit rate		1	10		
		DDR = 0, P54 = 0	fs			
	Carialized autout bit rate	DDR = 0, P54 = 1	1.25 × fs		Gbps	
	Serialized output bit rate	DDR = 1, P54 = 0	2 × f _S			
		DDR = 1, P54 = 1	2.5 × fs			
t _{TLH}	LH transition time — differential	10% to 90%, 8 Gbps	35		ps	
t _{THL}	HL transition time — differential	10% to 90%, 8 Gbps	35		ps	
UI	Unit interval	8 Gbps serial rate	125		ps	
DDJ	Data dependent jitter	8 Gbps serial rate	11.3		ps	
RJ	Random Jitter	8 Gbps serial rate	1.4		ps	
SERIAL I	NTERFACE					
t _(OZD)	SDO tri-state to driven			5	ns	
t _(ODZ)	SDO driven to tri-state	See Figure 2 2.5		5	ns	
t _(OD)	SDO output delay			20	ns	



Figure 1. JESD204 Synchronization







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6.9 Typical Characteristics

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a Foreground mode calibration with Timing Calibration enabled. $T_A = 25^{\circ}\text{C}$. $V_I = -1 \text{ dBFS}$.





Typical Characteristics (continued)



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Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a Foreground mode calibration with Timing Calibration enabled. $T_A = 25^{\circ}\text{C}$. $V_I = -1 \text{ dBFS}$.





Typical Characteristics (continued)



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Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a Foreground mode calibration with Timing Calibration enabled. $T_A = 25^{\circ}\text{C}$. $V_I = -1 \text{ dBFS}$.





Typical Characteristics (continued)



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Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)} = V_{(VD12)} = 1.2 \text{ V}$, $V_{(VA19)} = 1.9 \text{ V}$, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)} = 2.7 \text{ or } 1.6 \text{ GHz}$ at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)} = 3.3 \text{ k}\Omega \pm 0.1\%$, after a Foreground mode calibration with Timing Calibration enabled. $T_A = 25^{\circ}\text{C}$. $V_I = -1 \text{ dBFS}$.





Typical Characteristics (continued)





Typical Characteristics (continued)





Typical Characteristics (continued)



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7 Detailed Description

7.1 Overview

The ADC12J1600 and ADC12J2700 devices are an ultra-wideband sampling and digital tuning subsystem. The devices combine a very-wideband and high sampling-rate ADC front-end with a configurable digital-down conversion block. This combination provides the necessary features to facilitate the development of flexible software-defined radio products for a wide range of communications applications.

The ADC12J1600 and ADC12J2700 devices are based on an ultra high-speed ADC core. The core uses an interleaved calibrated folding and interpolating architecture that results in very high sampling rate, very good dynamic performance, and relatively low-power consumption. This ADC core is followed by a configurable DDC block which is implemented on a small geometry CMOS. The DDC block provides a range of decimation settings that allow the product to work in ultra-wideband, wideband, and more-narrow-band receive systems. The output data from the DDC block is transmitted through a JESD204B-compatible multi-lane serial-output system. This system minimizes the number of data pairs required to convey the output data to the downstream processing circuitry.



7.2 Functional Block Diagram



Functional Block Diagram (continued)



Figure 63. DDC Details Block Diagram

7.3 Feature Description

7.3.1 Signal Acquisition

The analog input is sampled on the rising edge of CLK and the digital equivalent of that data is available in the serialized datastream $t_{(LAT)}$ or $t_{(LAT)}$ input clock cycles later.

The ADC12J1600 and ADC12J2700 devices convert as long as the input clock signal is present. The fullydifferential comparator design and the innovative design of the sample-and-hold amplifier, together with calibration, enables very good performance at input frequencies beyond 3 GHz. The ADC12J1600 and ADC12J2700 data is output on a high-speed serial JESD204B interface.

7.3.2 The Analog Inputs

A differential input signal must be used to drive the ADC12J1600 and ADC12J2700 devices. Operation with a single-ended signal is not recommended as performance suffers. The input signals can be either be AC coupled or DC coupled. The analog inputs are internally connected to the V_{CMO} bias voltage. When DC-coupled input signals are used, the common mode voltage of the applied signal must meet the device Input common mode requirements. See V_{CMI} in the *Recommended Operating Conditions* table.

The full-scale input range for each converter can be adjusted through the serial interface. See the *Full Scale Range Adjust* section.

The buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If an amplifier circuit before the ADC is desired, use care when selecting an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application. If gain is not required, a balun (balanced-to-unbalanced transformer) is generally used to provide single ended (SE) to differential conversion.

The input impedance of VIN± consists of two 50- Ω resistors in series between the inputs and a capacitance from each of these inputs to ground. A resistance of approximately 20 k Ω exists from the center point of the 50- Ω resistors to the on-chip V_{CMO} providing self-biasing for AC-coupled applications.

Performance is good in both DC-coupled mode and AC coupled mode, provided the common-mode voltage at the analog input is within specifications.

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Feature Description (continued)

7.3.2.1 Input Clamp

The ADC12J1600 and ADC12J2700 maximum DC input voltage is limited to the range 0 to 2 V to prevent damage to the device. To help maintain these limits, an active input clamping circuit is incorporated which sources or sinks input currents up to \pm 50 mA. The clamping circuit is enabled by default and is controlled via the Input_Clamp_EN bit (register 0x034, bit 5). The protection provided by this circuit is limited as follows:

- Shunt current-clamping is only effective for non-zero source impedances.
- At frequencies above 3 GHz the clamping is ineffective because of the finite turn-on and turn-off time of the switch.

With these limitations in mind, analysis has been done to determine the allowable input signal levels as a function of input frequency when the Input Clamp is enabled, assuming the source impedance matches the input impedance of the device (100- Ω differential). This information is incorporated in the *Absolute Maximum Ratings* table.

7.3.2.2 AC Coupled Input Usage

The easiest way to accomplish SE-to-differential conversion for AC-coupled signals is with an appropriate balun.



Figure 64. Single-Ended-to-Differential Signal Conversion With a Balun

Figure 64 shows a generic depiction of a SE-to-differential signal conversion using a balun. The circuitry specific to the balun depends on the type of balun selected and the overall board layout. TI recommends that the system designer contact the manufacturer of the selected balun to aid in designing the best performing single-ended to differential conversion circuit using that particular balun.

When selecting a balun, understanding the input architecture of the ADC is important. Specific balun parameters must be considered. The balun must match the impedance of the analog source to the on-chip 100- Ω differential input termination of the ADC12J1600 and ADC12J2700 devices. The range of this input termination resistor is described in the *Electrical Characteristics* table as the specification R_{ID}.

Also, as a result of the ADC architecture, the phase and amplitude balance are important. The lowest possible phase and amplitude imbalance is desired when selecting a balun. The phase imbalance must be no more than $\pm 2.5^{\circ}$ and the amplitude imbalance must be limited to less than 1 dB at the desired input frequency range.

Finally, when selecting a balun, the voltage standing-wave ratio (VSWR), bandwidth, and insertion loss of the balun must also be considered. The VSWR aids in determining the overall transmission line termination capability of the balun when interfacing to the ADC input. The insertion loss must be considered so that the signal at the balun output is within the specified input range of the ADC as described in the *Electrical Characteristics* table as the specification V_{ID} .

Table 1 lists the recommended baluns for specific signal frequency ranges.

MINIMUM FREQUENCY (MHz)	MAXIMUM FREQUENCY (MHz)	IMPEDANCE RATIO	PART NUMBER	MANUFACTURER
4.5	3000	1:1	TC1-1-13MA+	Mini-Circuits
400	3000	1:2	B0430J50100AHF	Anaren
30	1800	1:2	ADTL2-18+	Mini-Circuits
10	4000	1:2	TCM2-43X+	Mini-Circuits

Table 1. Balun Recommendations

7.3.2.3 DC Coupled Input Usage

When a DC-coupled signal source is used, the common mode voltage of the applied signal must be within a specified range (V_{CMI}). To achieve this range, the common mode of the driver should be based on the VCMO output provided for this purpose.

Full-scale distortion performance degrades as the input common-mode voltage deviates from VCMO. Therefore, maintaining the input common-mode voltage within the V_{CMI} range is important.

Table 2 lists the recommended amplifiers for DC-coupled usage or if AC-coupling with gain is required.

-3-dB BANDWIDTH (MHz)	MIN GAIN (dB)	MAX GAIN (dB)	GAIN TYPE	PART NUMBER
7000	16	16	Fixed	LMH3401
2800	0	17	Resistor set	LMH6554
2400	6	26	Digital programmable	LMH6881
900	-1.16	38.8	Digital programmable	LMH6518

Table 2. Amplifier Recommendations

7.3.2.4 Handling Single-Ended Input Signals

The ADC12J1600 and ADC12J2700 devices have no provision to adequately process single-ended input signals. The best way to handle single-ended signals is to convert these signals to balanced differential signals before presenting the signals to the ADC.

7.3.3 Clocking

The ADC12J1600 and ADC12J2700 devices have a differential clock input, DEVCLK+ and DEVCLK–, that must be driven with an AC-coupled differential clock-signal. The clock inputs are internally terminated and biased. The input clock signal must be capacitively coupled to the clock pins as shown in Figure 65.



Figure 65. Differential Sample-Clock Connection

The differential sample-clock line pair must have a characteristic impedance of 100 Ω and must be terminated at the clock source of that 100- Ω characteristic impedance. The input clock line must be as short and direct as possible. The ADC12J1600 and ADC12J2700 clock input is internally terminated with an untrimmed 100- Ω resistance.

Insufficient input clock levels results in poor dynamic performance. Excessively-high input-clock levels can cause a change in the analog-input offset voltage. To avoid these issues, maintain the input clock level within the range specified in the *Electrical Characteristics* table.

The low times and high times of the input clock signal can affect the performance of any ADC. The ADC12J1600 and ADC12J2700 devices feature a duty-cycle clock-correction circuit which maintains performance over temperature. The ADC meets the performance specification when the input clock high times and low times are maintained as specified in the *Electrical Characteristics* table.

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High-speed high-performance ADCs such as the ADC12J1600 and ADC12J2700 devices require a very-stable input clock-signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution or ENOB (effective number of bits), maximum ADC input frequency, and the input signal amplitude relative to the ADC input full-scale range. Use Equation 1 to calculate the maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR.

$$RMS_{tot(J)} = \frac{V_{FSR}}{V_{I(PP)}} \times \frac{1}{\left(2^{(n+1)} \times \pi \times F_{IN}\right)}$$

where

- RMS_{tot(J)} is the RMS total of all jitter sources in seconds
- V_{I(PP)} is the peak-to-peak analog input signal
- V_{FSR} is the full-scale range of the ADC
- n is the ADC resolution in bits
- F_{IN} is the maximum input frequency, in Hertz, at the ADC analog input

(1)

Note that the maximum jitter previously described is the root sum square (RSS) of the jitter from all sources, including that from the clock source, the jitter added by noise coupling at board level and that added internally by the ADC clock circuitry, in addition to any jitter added to the input signal. Because the effective jitter added by the ADC is beyond user control, the best option is to minimize the jitter from the clock source, the sum of the externally-added input clock jitter and the jitter added by any circuitry to the analog signal.

Input clock amplitudes above those specified in the *Recommended Operating Conditions* table can result in increased input-offset voltage. Increased input-offset voltage causes the converter to produce an output code other than the expected 2048 when both input pins are at the same potential.

7.3.4 Over-Range Function

To ensure that system-gain management has the quickest-possible response time, a low-latency configurable over-range function is included. The over-range function works by monitoring the raw 12-bit samples exiting the ADC module. The upper 8 bits of the magnitude of the ADC data are checked against two programmable thresholds, OVR_T0 and OVR_T1. The following table lists how a raw ADC value is converted to an absolute value for a comparison of the thresholds.

ADC SAMPLE (OFFSET BINARY)	ADC SAMPLE (2's COMPLEMENT)	ABSOLUTE VALUE	UPPER 8 BITS USED FOR COMPARISON
1111 1111 1111 (4095)	0111 1111 1111 (+2047)	111 1111 1111 (2047)	1111 1111 (255)
1111 1111 0000 (4080)	0111 1111 0000 (+2032)	111 1111 0000 (2032)	1111 1110 (254)
1000 0000 0000 (2048)	0000 0000 0000 (0)	000 0000 0000 (0)	0000 0000 (0)
0000 0001 0000 (16)	1000 0001 0000 (-2032)	111 1111 0000 (2032)	1111 1110 (254)
0000 0000 0000 (0)	1000 0000 0000 (-2048)	111 1111 1111 (2047)	1111 1111 (255)

If the upper 8 bits of the absolute value equal or exceed the OVR_T0 or OVR_T1 threshold during the monitoring period, then the over-range bit associated with the threshold is set to 1, otherwise the over-range bit is 0. The resulting over-range bits are embedded into the complex output data samples and output on OR_T0 and OR_T1. Table 3 lists the outputs, related data samples, threshold settings and the monitoring period equation.

Table 3.	Threshold	and Monitor	Period for	Embedded OR Bits	
----------	-----------	-------------	------------	-------------------------	--

EMBEDDED OVER-RANGE OUTPUTS	ASSOCIATED THRESHOLD	ASSOCIATED SAMPLES	MONITORING PERIOD (ADC SAMPLES)
OR_T0	OVR_T0 In-Phase (I) samples		20VR N(1)
OR_T1	OVR_T1	Quadrature (Q) samples	2 - ()

(1) OVR_N is the monitoring period register setting.



	5
OVR_N	MONITORING PERIOD
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

Table 4. Over-Range Monitoring Period

Typically, the OVR_T0 threshold can be set near the full-scale value (228 for example). When the threshold is triggered, a typical system can turn down the system gain to avoid clipping. The OVR_T1 threshold can be set much lower. For example, the OVR_T1 threshold can be set to 64 (-12 dBFS). If the input signal is strong, the OVR_T1 threshold is tripped occasionally. If the input is quite weak, the threshold is never tripped. The downstream logic device monitors the OVR_T1 bit. If OVR_T1 stays low for an extended period of time, then the system gain can be increased until the threshold is occasionally tripped (meaning the peak level of the signal is above -12 dBFS).

The OR_T0 threshold is embedded as the LSB along with the upper 15 bits of every complex I sample. The OR_T1 threshold is embedded as the LSB along with the upper 15 bits of every complex Q sample.

7.3.5 ADC Core Features

7.3.5.1 The Reference Voltage

The reference voltage for the ADC12J1600 and ADC12J2700 devices is derived from an internal bandgap reference. A buffered version of the reference voltage is available at the VBG pin for user convenience. This output has an output-current capability of $\pm 100 \ \mu$ A. The VBG output must be buffered if more current is required. No provision exists for the use of an external reference voltage, but the full-scale input voltage can be adjusted through the full-scale-range register settings.

7.3.5.2 Common-Mode Voltage Generation

The internal reference voltage is used to generate a stable common-mode voltage reference for the analog Inputs and the DEVCLK and SYSREF differential-clock inputs.

7.3.5.3 Bias Current Generation

An external bias resistor, in combination with the on-chip voltage reference is used to provide an accurate and stable source of bias currents for internal circuitry. Using an external accurate resistor minimizes variation in device power consumption and performance.

7.3.5.4 Full Scale Range Adjust

The ADC input full-scale range can be adjusted through the GAIN_FS register setting (registers 0x022 and 0x023). The adjustment range is approximately 500 mV_{PP} to 950 mV_{PP}. The full-scale range adjustment is useful for matching the input-signal amplitude to the ADC full scale, or to match the full-scale range of multiple ADCs when developing a multi-converter system.

7.3.5.5 Offset Adjust

The ADC-input offset voltage can be adjusted through the OFFSET_FS register setting (registers 0x025 and 0x026). The adjustment range is approximately 28 mV to –28 mV differential.

NOTE

Offset adjust has no effect when background calibration mode is enabled.

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7.3.5.6 Power-Down

The power-down bit (PD) allows the ADC12J1600 and ADC12J2700 devices to be entirely powered down. The serial data output drivers are disabled when PD is high. When the device returns to normal operation, the JESD204 link must be re-established, and the ADC pipeline and decimation filters contain meaningless information and must be flushed.

7.3.5.7 Built-In Temperature Monitor Diode

A built-in thermal monitoring diode junction is made available on the TDIODE+ and TDIODE– pins. This diode facilitates temperature monitoring and characterization of the device in higher ambient temperature environments. While the on-chip diode is not highly characterized, the diode can be used effectively by performing a baseline measurement at a known ambient or board temperature with the device in power-down (PD) mode. Recommended monitoring ICs include the LM95233 device and similar remote-diode temperature monitoring products from Texas Instruments.

7.3.6 Digital Down Converter (DDC)

The digitized data is the input to the digital down-converter block. This block provides frequency conversion and decimation filtering to allow a specific range of frequencies to be selected and output in the digital data stream.

7.3.6.1 NCO/Mixer

The DDC contains a complex numerically-controlled oscillator and a complex mixer. The oscillator generates a complex exponential sequence shown in Equation 2.

 $x[n] = e^{j\omega n}$

(2)

The frequency (ω) is specified by the a 32-bit register setting. The complex exponential sequence is multiplied by the real input from the ADC to mix the desired carrier down to 0 Hz.

7.3.6.2 NCO Settings

7.3.6.2.1 NCO Frequency Phase Selection

Within the DDC, eight different frequency and phase settings are always available for use. Each of the eight settings uses a different phase accumulator within the NCO. Because all eight phase accumulators are continuously running independently, rapid switching between different NCO frequencies is possible allowing rapid tuning of different signals.

The specific frequency-phase pair in use is selected through either the NCO_x input pins, or the NCO_SEL configuration bits (register 0x20D, bits 2:0). The CFG_MODE bit (register 0x20C, bit 0) is used to choose whether the input pins or selection bits are used. When the CFG_MODE bit is set to 0, the NCO_x input pins select the active NCO frequency and phase setting. When the CFG_MODE bit is set to 1, the NCO_SEL register settings select the active NCO frequency and phase setting.

The frequency for each phase accumulator is programmed independently through the NCO_FREQn (and optionally NCO_RDIV) settings. The phase offset for each accumulator is programmed independently through the NCO_PHASEn register settings.

7.3.6.2.2 NCO_0, NCO_1, and NCO_2 (NCO_x)

When the CFG_MODE bit is set to 0, the state of these three inputs determines the active NCO frequency and phase accumulator settings.

7.3.6.2.3 NCO_SEL Bits (2:0)

When the CFG_MODE bit is set to 1, the state of these register bits determines the active NCO frequency and phase accumulator settings.


7.3.6.2.4 NCO Frequency Setting (Eight Total)

7.3.6.2.4.1 Basic NCO Frequency-Setting Mode

In basic NCO frequency-setting mode, the NCO frequency setting is set by the 32-bit register value, NCO_FREQn (n = preset 0 trough 7, see the NCO Frequency (Preset x) Register section).

(n = 0 - 7) $f_{(NCO)}$ = NCO_FREQn × 2⁻³² × $f_{(DEVCLK)}$

(3)

NOTE

Changing the register setting after the JESD204B interface is running results in nondeterministic NCO phase. If deterministic phase is required, the JESD204B link must be re-initialized after changing the register setting. See the *Multiple ADC Synchronization* section.

7.3.6.2.4.2 Rational NCO Frequency Setting Mode

In basic NCO frequency mode, the frequency step size is very small and many frequencies can be synthesized, but sometimes an application requires very specific frequencies that fall between two frequency steps. For example with $f_{\rm S}$ equal to 2457.6 MHz and a desired $f_{\rm (NCO)}$ equal to 5.02 MHz the value for NCO_FREQ is 8773085.867. Truncating the fractional portion results in an $f_{\rm (NCO)}$ equal to 5.0199995 MHz, which is not the desired frequency.

To produce the desired frequency, the NCO_RDIV parameter is used to force the phase accumulator to arrive at specific frequencies without error. First, select a frequency step size ($f_{(STEP)}$) that is appropriate for the NCO frequency steps required. The typical value of $f_{(STEP)}$ is 10 kHz. Next, program the NCO_RDIV value according to Equation 4.

NCO_RDIV =
$$\frac{\left(\frac{f_{(\text{DEVCLK})}}{f_{(\text{STEP})}}\right)}{128}$$

(4)

(5)

The result of Equation 4 must be an integer value. If the value is not an integer, adjust either of the parameters until the result in an integer value.

For example, select a value of 1920 for NCO_RDIV.

NOTE

NCO_RDIV values larger than 8192 can degrade the NCO SFDR performance and are not recommended.

Now use Equation 5 to calculate the NCO_FREQ register value.

NCO_FREQ = round ×
$$\left(\frac{2^{25} \times N}{NCO_RDIV}\right)$$

Alternatively, the following equations can be used:

$$N = \frac{f_{(NCO)}}{f_{(STEP)}}$$
(6)
$$NCO_FREQ = round \times \left(\frac{2^{25} \times N}{NCO_RDIV}\right)$$
(7)

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f _(DEVCLK) (MHz)	NCO_RDIV
2457.6	1920
1966.08	1536
1474.56	1152
1228.8	960

Table 5. Common NCO_RDIV Values (For 10-kHz Frequency Steps)

7.3.6.2.5 NCO Phase-Offset Setting (Eight Total)

The NCO phase-offset setting is set by the 16-bit register value NCO_PHASEn (n = preset 0 trough 7, see the NCO Phase (Preset x) Register section). The value is left-justified into a 32-bit field and then added to the phase accumulator.

Use Equation 8 to calculate the phase offset in radians.

NCO_PHASEn × 2^{-16} × 2 × π

(8)

NOTE

Changing the register setting after the JESD204B interface is running results in nondeterministic NCO phase. If deterministic phase is required, the JESD204B link must be re-initialized after changing the register setting. See *Multiple ADC Synchronization*.

7.3.6.2.6 Programmable DDC Delay

The DDC Filter elements incorporate a programmable sample delay. The delay can be programmed from 0 to (decimation setting -0.5) ADC sample periods. The delay step-size is 0.5 ADC sample periods. The delay settings are programmed through the DDC_DLYn parameter.

Table 6. Programmable DDC Delay Range

D (Decimation Setting)	Min Delay (t _(DEVCLK))	Max Delay (t _(DEVCLK))
4	0	3.5
8	0	7.5
10	0	9.5
16	0	15.5
20	0	19.5
32	0	31.5



7.3.6.3 Decimation Filters

The decimation filters are arranged to provide a programmable overall decimation of 4, 8, 10, 16, 20, or 32. The input and output of each filter is complex. The output data consists of 15-bit complex baseband information. Table 7 lists the effective output sample rates.

		COMPLEX S (OUT	AMPLE OUTPUT RA PUT SAMPLE = 15-B	TE AND RESULTIN IT I + 15-BIT Q + 2	IG BANDWIDTH -BIT OR)			
DECIMATION		$f_{(DEVCLK)}$		$f_{(\text{DEVCLK})} = 4000 \text{ MHz}$				
SETTING	OUTPUT RATE (MSPS)	RAW OUTPUT BANDWIDTH (MHz)	ALIAS PROTECTED BANDWIDTH (MHz)	OUTPUT RATE (MSPS)	RAW OUTPUT BANDWIDTH (MHz)	ALIAS PROTECTED BANDWIDTH (MHz)		
4	f _(DEVCLK) / 4	$f_{(DEVCLK)}$ / 4	0.8 × f _(DEVCLK) / 4	1000	1000	800		
8	f _(DEVCLK) / 8	$f_{(DEVCLK)}N$ / 8	0.8 × f _(DEVCLK) / 8	500	500	400		
10	f _(DEVCLK) / 10	f _(DEVCLK) / 10	$0.8 \times f_{(\text{DEVCLK})} / 10$	400	400	320		
16	f _(DEVCLK) / 16	$f_{(DEVCLK)}$ / 16	0.8 × f _(DEVCLK) / 16	250	250	200		
20	f _(DEVCLK) / 20	f _(DEVCLK) / 20	$0.8 \times f_{(\text{DEVCLK})} / 20$	200	200	160		
32	f _(DEVCLK) / 32	f _(DEVCLK) / 32	$0.8 \times f_{(\text{DEVCLK})} / 32$	125	125	100		

Table 7. Output Sample Rates

For maximum efficiency a group of high speed filter blocks are implemented with specific blocks used for each decimation setting. The first table below describes the combination of filter blocks used for each decimation setting. The next table lists the coefficient details and decimation factor of each filter block.

Table 8. Decimation Mode Filter Usage

Decimation Setting	Filter Blocks Used
4	CS19, CS55
8	CS11, CS15, CS55
10	CS11, CS139
16	CS7, CS11, CS15, CS55
20	CS7, CS11, CS139
32	CS7, CS7, CS11, CS15, CS55

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Table 9. Filter Coefficient Details

	Filter Coefficient Set (Decimation Factor of Filter)												
CS	7 (2)	CS1	1 (2)	CS1	5 (2)	CS1	19 (2)	CS5	5 (2)	CS13	39 (5)		
-65	-65	109	109	-327	-327	22	22	-37	-37	-5	-5		
0	0	0	0	0	0	0	0	0	0	-9	-9		
577	577	-837	-837	2231	2231	-174	-174	118	118	-9	-9		
1024		0	0	0	0	0	0	0	0	-5	-5		
-		4824	4824	-8881	-8881	744	744	-291	-291	0	0		
		8192		0	0	0	0	0	0	20	20		
		0.01		39742	39742	-2429	-2429	612	612	33	33		
				65536	007.12	0	0	0	0	33	33		
				00000		10029	10029	_1159	_1159	21	21		
						16384	10023	-1100	-1100	0	0		
						10304		2021	2021	54	54		
								2031	2031	-34	-04		
								2256	2256	-00	-00		
								-3330	-3330	-03	-03		
								5200	5200	-30	-00		
								5308	5308	0	0		
								0	0	119	119		
								-8140	-8140	196	196		
								0	0	199	199		
								12284	12284	125	125		
								0	0	0	0		
								-18628	-18628	-234	-234		
								0	0	-385	-385		
								29455	29455	-393	-393		
								0	0	-248	-248		
								-53191	-53191	0	0		
								0	0	422	422		
								166059	166059	696	696		
								262144		711	711		
										450	450		
										0	0		
										-711	-711		
										-1176	-1176		
										-1206	-1206		
										-766	-766		
										0	0		
										1139	1139		
										1893	1893		
										1949	1949		
										1244	1244		
										0	0		
										-1760	-1760		
										-2940	-2940		
										-3044	-3044		
										-1955	-1955		
										0	0		
										2656	2656		
										4472	4472		
										4671	4671		
										3026	3026		
										0	0		
										-3993	-3993		
										-6802	-6802		
										_7196	_7196		
										_4730	_4730		
										-130			
	1	1					1			U	U		

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Table 9. Filter Coefficient Details (continued)

	Filter Coefficient Set (Decimation Factor of Filter)													
CS	7 (2)	CS1	1 (2)	CS1	5 (2)	CS1	9 (2)	CS5	5 (2)	CS139 (5)				
										6159	6159			
										10707	10707			
										11593	11593			
										7825	7825			
										0	0			
										-10423	-10423			
										-18932	-18932			
										-21629	-21629			
										-15618	-15618			
										0	0			
										24448	24448			
										52645	52645			
										78958	78958			
										97758	97758			
										104858				

7.3.6.4 DDC Output Data

The DDC output data consist of 15-bit complex data plus the two over-range threshold-detection control bits. The following table lists the data format:

	16-BIT OUTPUT WORD												
CHANNEL	15	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1											0
I		DDC Output In-Phase (I) 15 bit										OR_T0	
Q	DDC Output Quadrature (Q) 15 bit										OR_T1		

7.3.6.5 Decimation Settings

7.3.6.5.1 Decimation Factor

The decimation setting is adjustable over the following settings:

- Bypass no decimation
- Decimate-by-4
- Decimate-by-8
- Decimate-by-10
- Decimate-by-16
- Decimate-by-20
- Decimate-by-32

NOTE

Because the output format is complex I+Q, the effective output bandwidth is approximately two-times the value for a *real* output with the same decimation factor.

7.3.6.5.2 DDC Gain Boost

The DDC gain boost (register 0x200, bit 4) provides additional gain through the DDC block. With a setting of 1 the final filter has 6.02-dB gain. With a setting of 0, the final filter has a 0-dB gain. This setting is recommended when the NCO is set near DC.

7.3.7 Data Outputs

The data outputs (DSx±) are very high-speed differential outputs and conform to the JESD204B JEDEC standard. A CML (current-mode logic)-type output driver is used for each output pair. Output pre-emphasis is adjustable to compensate for longer PCB-trace lengths.

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7.3.7.1 The Digital Outputs

The ADC12J1600 and ADC12J2700 output data is transmitted on up to eight high-speed serial-data lanes. The output data from the ADC or DDC is formatted to the eight lanes, 8b10b encoded, and serialized. Up to four different serial output rates are possible depending on the decimation mode setting: 1x, 1.25x, 2x, and 2.5x. In 1x mode, the output serializers run at the same bit rate as the frequency of the applied DEVCLK. In 1.25x mode, the output serializers run at a bit rate that is 1.25-times that of the applied DEVCLK, and so on. For example, for a 1.6-GHz input DEVCLK, the output rates are 1.6 Gbps in 1x mode, 2 Gbps in 1.25x mode, 3.2 Gbps in 2x mode and 4 Gbps in 2.5x mode.

7.3.7.2 JESD204B Interface Features and Settings

7.3.7.2.1 Scrambler Enable

Scrambling randomizes the 8b10b encoded data, spreading the frequency content of the data interface. This reduces the peak EMI energy at any given frequency reducing the possibility of feedback to the device inputs impacting performance. The scrambler is disabled by default and is enabled via SCR (register 0x201, bit 7).

7.3.7.2.2 Frames Per Multi-Frame (K-1)

The frames per multi-frame (K) setting can be adjusted within constraints that are dependent on the selected decimation (D) and serial rate (DDR) settings. The K-minus-1 (KM1) register setting (register 0x201, bits 6:2) must be one less than the desired K setting.

7.3.7.2.3 DDR

The serial rate can be either $1f_{(CLK)}$ (DDR = 0) or $2f_{(CLK)}$ (DDR = 1).

7.3.7.2.4 JESD Enable

The JESD interface must be disabled (JESD_EN is set to 0) while any of the other JESD parameters are changed. While JESD_EN is set 0 the block is held in reset and the serializers are powered down. The clocks for this section are also gated off to further save power. When the parameters have been set as desired the JESD block can be enabled (JESD_EN is set to 1).

7.3.7.2.5 JESD Test Modes

Several different JESD204B test modes are available to assist in link verification and debugging. The list of modes follows.

NOTE

PRBS test signals are output directly, without 8b10b encoding.

- Normal operation
- PRBS7 test mode
- PRBS15 test mode
- PRBS23 test mode
- Ramp test mode
- Short or long transport-layer test mode
- D21.5 test mode
- K28.5 test mode
- Repeated ILA test mode
- Modified RPAT test mode
- Serial-outputs differential 0 test mode
- Serial-outputs differential 1 test mode



7.3.7.2.6 Configurable Pre-Emphasis

The high-speed serial-output drivers incorporate a configurable pre-emphasis feature. This feature allows the output drive waveform to be optimized for different PCB materials and signal transmission distances. The pre-emphasis setting is adjusted through the serializer pre-emphasis setting in register 0x040, bits 3 to 0. The default setting is 4d. Higher values will increase the pre-emphasis to compensate for more lossy PCB materials. This adjustment is best used in conjunction with an eye-diagram analysis capability in the receiver. The pre-emphasis setting should be adjusted to optimize the eye-opening for the hardware configuration and line rates needed.

7.3.7.2.7 Serial Output-Data Formatting

Output data is generated by the DDC then formatted according to the selected decimation and output rate settings. When less than the maximum of eight lanes are active, lanes are disabled beginning with the highest numerical lanes. For example when only two lanes are active, lanes 0 and 1 are active, while all higher lanes are inactive.

PARAMETER	DESCRIPTION	USER CONFIGURED OR DERIVED	STANDARD JESD204B LINK PARAMETER
D	Decimation factor, determined by DMODE register	User	No
DDR	Serial line rate: $1 = DDR$ rate (2x), $0 = SDR$ rate (1x)	User	No
P54	Enable 5/4 PLL to increase line rate by 1.25x.	User	No
	0 = no PLL (1x), 1 = enable PLL (1.25x)		
К	Number of frames per multiframe	User	Yes
Ν	Bits per sample (before adding control bits and tails bits)	Derived	Yes
CS	Control bits per sample	Derived	Yes
N'	Bits per sample (after adding control bits and tail bits). Must be a multiple of 4.	Derived	Yes
L	Number of serial lanes	Derived	Yes
F	Number of octets (bytes) per frame (per lane)	Derived	Yes
М	Number of (logical) converters	Derived	Yes
S	Number of samples per converter per frame	Derived	Yes
CF	Number of control words per frame	Derived	Yes
HD	1=High density mode (samples may be broken across lanes), 0 = normal mode (samples may not be broken across lanes)	Derived	Yes
KS	Legal adjustment step for K, to ensure that the multi-frame clock is a sub- harmonic of other internal clocks	Derived	No

Table 10. Parameter Definitions

Table 11. Serial Link Parameters⁽¹⁾

USER SPECIFI	ED PARA	METERS				DERIVED PA	RAMETER	RS			OTHER II	NFORMATION
DECIMATION FACTOR (D)	DDR	P54	N	CS	N'	L	F	м	s	ĸs	LEGAL K RANGE	BIT RATE / ADC CLOCK ⁽²⁾
1	1	0	12	0	12	8	8	8	5	2	4-32	2x
4	1	0	15	1	16	5	4	2	5	4	8-32	2x
4	1	1	15	1	16	4	2	2	2	2	10-32	2.5x
8	0	0	15	1	16	5	4	2	5	2	6-32	1x
8	0	1	15	1	16	4	2	2	2	1	9-32	1.25x
8	1	0	15	1	16	3	8	2	5	2	4-32	2x
8	1	1	15	1	16	2	2	2	1	2	10-32	2.5x
10	0	0	15	1	16	4	2	2	2	4	12-32	1x
10	1	0	15	1	16	2	2	2	1	8	16-32	2x
16	0	0	15	1	16	3	8	2	5	1	3-32	1x
16	0	1	15	1	16	2	2	2	1	1	9-32	1.25x

(1) In all modes: HD = 0 and CF = 0

(2) x = times (for example, 2x = 2-times)

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USER SPECIFI	ED PARA	METERS	DERIVED PARAMETERS						DERIVED PARAMETERS				
DECIMATION FACTOR (D)	DDR	P54	N	CS	N'	L	F	м	S	KS	LEGAL K RANGE	BIT RATE / ADC CLOCK ⁽²⁾	
16	1	0	15	1	16	2	16	2	5	1	2-32	2x	
16	1	1	15	1	16	1	4	2	1	1	5-32	2.5x	
20	0	0	15	1	16	2	2	2	1	4	12-32	1x	
20	1	0	15	1	16	1	4	2	1	4	8-32	2x	
32	0	0	15	1	16	2	16	2	5	1	2-32	1x	
32	0	1	15	1	16	1	4	2	1	1	5-32	1.25x	
32	1	0	15	1	16	1	32	2	5	1	1-32	2x	

Table 11. Serial Link Parameters⁽¹⁾ (continued)

Output data is formatted in a specific optimized fashion for each decimation and DDR setting combination. For bypass mode (decimation = 1) the 12-bit offset binary values are mapped to the 8-bit characters. For the DDC mode the 16-bit values (15-bit complex data plus 1 bit OR_Tn) are mapped to the 8-bit characters. The following tables list the specific mapping formats. In all mappings the T or tail bits are 0 (zero).

Table 12. Bypass Mode, No Decimation, DDR = 1, P54 = 0, LMF = 8,8,8

				ТІМ	$E \rightarrow$				
CHAR NUMBER	0	1	2	3	4	5	6	7	
Lane 0	C0S0		C0S1	C0S2		C0S3	C0S4	Т	
Lane 1	C1S0		C1S1	C1S2		C1S3	C1S4	Т	
Lane 2	C2S0		C2S1	C2S2	C2S3		C2S4	Т	
Lane 3	C3S0		C3S1	C3S2		C3S3	C3S4	Т	
Lane 4	C4S0		C4S1	C4S2		C4S3	C4S4	Т	
Lane 5	C5S0		C5S1	C5S2		C5S3	C5S4	Т	
Lane 6	C6S0		C6S1	C6S2		C6S3	C6S4	Т	
Lane 7	C7S0		C7S1	C7S2		C7S3	C7S4	Т	
	Frame n								

Table 13. Bypass Mode, No Decimation, DDR = 1, P54 = 0, Composite View of Interleaved Converters

				ТІМ	E→			
CHAR NUMBER	0	1	2	3	4	5	6	7
Lane 0	S0		S8	S16		S24	S32	Т
Lane 1	S1		S9	S17		S25	S33	Т
Lane 2	S2		S10	S18		S26	S34	т
Lane 3	S3		S11	S19		S27	S35	Т
Lane 4	S4		S12	S20		S28	S36	Т
Lane 5	S5		S13	S21		S29	S37	Т
Lane 6	S6		S14	S22		S30	S38	Т
Lane 7	S7		S15	S23		S31	S39	Т
				Fran	ne n			



Table 14. Decimate-by-4, DDR = 1, P54 = 0, LMF = 5,2,4

		ТІМ	E→	
CHAR NUMBER	0	1	2	3
Lane 0		0		1
Lane 1	I	2	l	3
Lane 2	I	4	C	Q_0
Lane 3	C	Q ₁	C	Q_2
Lane 4	C	Q ₃	C	Q ₄
		Frar	ne n	

Table 15. Decimate-by-4, DDR = 1, P54 = 1, LMF = 4,2,2

		ТІМ	E →			
CHAR NUMBER	0	1	2	3	4	5
Lane 0	I	0	I	2	Ι	4
Lane 1	I	1	I	3	Ι	5
Lane 2	C	2 0	C	Q ₂	G	Q ₄
Lane 3	C	۱ ₁	C	Q 3	G	\mathfrak{d}_5
	Fra r	ime า	Fra n -	ime + 1	Fra n -	ime + 2

Table 16. Decimate-by-8, DDR = 0, P54 = 0, LMF = 5,2,4

		ТІМ	E→	
CHAR NUMBER	0	1	2	3
Lane 0	I	0	I	1
Lane 1	I	2	I	3
Lane 2	I	4	C	2 0
Lane 3	C	Q ₁	C	\mathfrak{d}_2
Lane 4	C	Q ₃	C	Ω_4
		Fran	ne n	

Table 17. Decimate-by-8, DDR = 0, P54 = 1, LMF = 4,2,2

		ТІМ	E →			
CHAR NUMBER	0	1	2	3	4	5
Lane 0	I	0	I	2	I	4
Lane 1	I	1	I	3	Ι	5
Lane 2	C	2 0	C	Q ₂	C	Q ₄
Lane 3	C	≬ 1	C	Q ₃	G	\mathfrak{d}_5
	Fra	ime n	Fra n	ame + 1	Fra n -	ime + 2

Table 18. Decimate-by-8, DDR = 1, P54 = 0, LMF = 3,2,8

		ТІМ	E →								
CHAR NUMBER	0	1	2	3	4	5	6	7			
Lane 0	I,	0	I	1	I	2	I	3			
Lane 1	I.	4	C	۵ ⁰	G	۵ ₁	C	Q_2			
Lane 2	C) ₃	G	Q ₄	-	Г	-	Г			
		Frame n									

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	Table 19.	Decimate-by-	8, DDR = 1, P	54=1, LMF = 2	,2,2	
		TIME	\rightarrow			
CHAR NUMBER	0	1	2	3	4	5
Lane 0	I ₀		I	1	I	2
Lane 1	Q)	C	Q ₁	C) ₂
	Fran	ne	Fra n ·	ame + 1	Fra n -	ime ⊦ 2

Table 20. Decimate-by-10, DDR = 0, P54 = 0, LMF = 4,2,2

		ТІМ	E→						
CHAR NUMBER	0	1	2	3	4	5	6 7		
Lane 0	I	0	I	2		4		6	
Lane 1	I	1	I	l ₃	I	5	I	7	
Lane 2	G	2 0	C	Q_2	C	Q ₄	C	2 ₆	
Lane 3	C	۱ ₁	C	λ_3	C	¢₅	C	۵ ₇	
	Fra	ime 1	Fra n	ame + 1	Fra n	ame + 2	Fra	ame + 3	

Table 21. Decimate-by-10, DDR = 1, P54 = 0, LMF = 2,2,2

		ТІМ	E→					
CHAR NUMBER	0	1	2	3	4	5	6 7	
Lane 0	l,	0	I	1	I	2	I	3
Lane 1	C	l ₀	Q ₁		Q ₂		Q ₃	
	Fra r	me າ	Fra n -	ame + 1	Fra n -	ime + 2	Fra n-	ame +3

Table 22. Decimate-by-16, DDR = 0, P54 = 0, LMF = 3,2,8

		ТІМ	E→								
CHAR NUMBER	0	1	2	3	4	5	6	7			
Lane 0	l,	0	I	1	I	2	I	3			
Lane 1	I,	4	G	2 0	C	Q ₁	C	Q ₂			
Lane 2	C) ₃	G	Q ₄	-	Г	-	Г			
		Frame n									

Table 23. Decimate-by-16, DDR = 0, P54 = 1, LMF = 2,2,2

		ТІМ	E →			
CHAR NUMBER	0	1	2	3	4	5
Lane 0	I	0	I	1	I	2
Lane 1	C	۵ ₀	C	Q ₁	C	Q_2
	Fra	ame n	Fra n -	ıme ⊦ 1	Fra n -	ame + 2

Table 24. Decimate-by-16, DDR = 1, P54 = 0, LMF = 2,2,16

				ТІМ	E →											
CHAR NUMBER	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Lane 0	I	0	I	1	I	2	l	3	I	4	G	l ₀	G	Q ₁	G	2
Lane 1	C) ₃	C) ₄	-	Г		Т	-	Г	-	Г	-	Г	٦	Г
	Frame n															



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Table 25. Decimate-by-16, DDR = 1, P54 = 1, LMF = 1,2,4

				$\text{TIME} \rightarrow$								
CHAR NUMBER	0	1	2	3	4	5	6	7	8	9	10	11
Lane 0	I	0	0	۵ ₀	I	1	C	۵ ₁	I	l ₂	Q ₂	
	Frame n				Frame n + 1				Frame n + 2			

Table 26. Decimate-by-20, DDR = 0, P54 = 0, LMF = 2,2,2

		ТІМ	E→							
CHAR NUMBER	0	1	2	3	4	5	6	7		
Lane 0	l.	0	I	1	I	2	l ₃			
Lane 1	C	l0	C	Q ₁	G	Q ₂	Q ₃			
	Fra r	me າ	Fra n -	ame + 1	Fra n -	ame + 2	Fra n ·	ame + 3		

Table 27. Decimate-by-20, DDR = 1, P54 = 0, LMF = 1,2,2

		TIM	E→								
CHAR NUMBER	0	1	2	3	4	5	6	7			
Lane 0	l,	0	C	¢0	I ₁ Q ₁						
		Fran	me n			Frame	e n + 1				

Table 28. Decimate-by-32, DDR = 0, P54 = 0, LMF = 2,2,16

				TIM	E →											
CHAR NUMBER	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Lane 0	I	I ₀ I ₁		I	2	Ι	I ₃		4	C	¢0	C) ₁	C	2	
Lane 1	C	$\overline{Q_3}$ $\overline{Q_4}$ \overline{T} \overline{T} \overline{T} \overline{T} \overline{T} \overline{T} \overline{T}														
							-	Frar	ne n		-					

Table 29. Decimate-by-32, DDR = 0, P54 = 1, LMF = 1,2,4

				$\text{TIME} \rightarrow$								
CHAR NUMBER	0	1	2	3	4	5	6	7	8	9	10	11
Lane 0	I ₀ Q ₀				I	1	0	Q ₁	I	2	G	ì ₂
		Frar	ne n			Frame	en + 1			Frame	en+2	

Table 30. Decimate-by-32, DDR = 1, P54 = 0, LMF = 1,2,32

		TIME	\rightarrow																													
CHAR NUMBE R	0	1	2	S	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Lane 0	I)		I1	I	2	I	3	I	4	G) 0	C) ₁	C) ₂	G) ₃	C	Q ₄	-	Г	-	Г	-	Г	-	T	T		ſ	Г
																Fra	ime n															

The formatted data is 8b10b encoded and output on the serial lanes. The 8b10b encoding provides a number of specific benefits, including:

- Standard encoding format. Therefore the IP is readily available in off-the-shelf FPGAs and ASIC building blocks.
- Inherent DC balance allows AC coupling of lanes with small on-chip capacitors
- Inherent error checking



7.3.7.2.8 JESD204B Synchronization Features

The JESD204B standard defines methods for synchronization and deterministic latency in a multi-converter system. These devices are a JESD204B Subclass 1 device and conforms to the various aspects of link operation as described in section 5.3.3 of the JESD204B standard. The specific signals used to achieve link operation are described briefly in the following sections.

7.3.7.2.9 SYSREF

The SYSREF is a periodic signal which is sampled by the device clock, and is used to align the boundary of the local multi-frame clock inside the data converter. SYSREF

is required to be a sub-harmonic of the LMFC internal timing. To meet this requirement, the timing of SYSREF is dependent on the device clock frequency and the LMFC frequency as determined by the selected DDC decimation and frames per multi-frame settings. This clock is typically in the range of 10 MHz to 300 MHz. See the *Multiple ADC Synchronization* section for more details on SYSREF timing requirements.

7.3.7.2.10 SYNC~

SYNC~ is asserted by the receiver to initiate a synchronization event.

Single ended and differential SYNC~ inputs are provided. The SYNC_DIFFSEL bit (register 0x202, bit 6) is used to select which input is used. Using the single ended SYNC~ input is recommended, as this frees the differential SYNC~/TMST input pair for use in the Time Stamp function. To assert SYNC~, a logic low is applied. To deassert SYNC~ a logic high is applied.

7.3.7.2.11 Time Stamp

When configured through the TIME_STAMP_EN register setting (register 0x050, bit 5), the SYNC~ differential input (pins 22 and 23) can be used as a time-stamp input. The time-stamp feature enables the user to capture the timing of an external trigger event relative to the sampled signal. When enabled, the LSB of the 12-bit ADC digital output captures the trigger information. In effect, the 12-bit converter becomes an 11-bit converter and the LSB acts as a 1-bit converter with the same latency as the 11-bit converter. The trigger must be applied to the differential SYNC~/TMST inputs. The trigger can be asynchronous to the ADC sampling clock and is sampled at approximately the same time as the analog input.

7.3.7.2.12 Code-Group Synchronization

Code-group synchronization is achieved using the following process:

- The receiver issues a synchronization request through the SYNC~ input
- The transmitter issues a stream of K28.5 symbols
- The receiver synchronizes and waits for correct reception of at least 4 consecutive K symbols
- The receiver deactivates the synchronization request
- Upon detecting that the receiver has deactivated the SYNC~ pin, the transmitter continues emitting K symbols
 until the next LMFC boundary (or optionally a later LMFC boundary)
- On the first frame following the selected LMFC boundary the transmitters emit an initial lane-alignment sequence

The initial-lane alignment sequence transmitted by the ADC device is defined in additional detail in JESD204B section 5.3.3.5.

7.3.7.2.13 Multiple ADC Synchronization

The second function for the SYSREF input is to facilitate the precise synchronization of multiple ADCs in a system.

One key challenge is to ensure that this synchronization works is to ensure that the SYSREF inputs are repeatedly captured by the input CLK. Two key elements must occur for the SYSREF inputs to be captured. First, the SYSREF input must be created so that it is synchronous to the input DEVCLK, be an integer sub-harmonic of the multi-frame (K × $t_{(FRAME)}$) and a repeatable and fixed-phase offset. When this constraint is achieved, repeatedly capturing SYSREF is easier. To further ease this task, the SYSREF signal is routed through a user-adjustable delay which eases the timing requirements with respect to the input DEVCLK signal. The SYSREF delay RDEL is adjusted through bits 3 through 0 in register 0x032.



As long as the SYSREF signal has a fixed timing relationship to DEVCLK, the internal delay can be used to maximize the setup and hold times between the internally delayed SYSREF and the internal DEVCLK signal. These timing relationships are listed in the *Timing Requirements* table. To find the proper delay setting, the RDEL value is adjusted from minimum to maximum while applying SYSREF and monitoring the SysRefDet and Dirty Capture detect bits. The SysRefDet bit is set whenever a rising edge of SYSREF is detected. The Dirty Capture bit is set whenever the setup or hold time between DEVCLK and the delayed SYSREF is insufficient. The SysRefDetClr bit is used to clear the SysRefDet bit. The Clear Dirty Capture bit is used to clear that bit.

This procedure should be followed to determine the range of delay settings where a clean SYSREF capture is achieved. The delay value at the center of the clean capture range must be loaded as the final RDEL setting. Table 31 lists a summary of the control bits that are used and the monitor bits that are read.

BIT NAME	REGISTER ADDRESS	REGISTER BIT	FUNCTION
RDEL	0x032	3:0	Adjust relative delay between DEVCLK and SYSREF
SysRefDet	0x031	7	Detect if a SYSREF rising edge has been captured (not self clearing)
Dirty Capture	0x031	6	Detect if SYSREF rising edge capture failed setup/hold (not self clearing)
SysRefDetClr	0x030	5	Clear SYSREF detection bit
Clear Dirty Capture	0x030	4	Clear Dirty Capture detection bit
SysRef_Rcvr_En	0x030	7	Enable SYSREF receiver. See the CLKGEN_0 descriptions in the <i>Clock Generator Control 0 Register</i> section for more information.
SysRef_Pr_En	0x030	6	Enable SYSREF processing. See the CLKGEN_0 descriptions in the <i>Clock Generator Control 0 Register</i> section for more information.

Table 31. SYSREF Capture Control and Status

One final aspect of multi-device synchronization relates to phase alignment of the NCO phase accumulators when DDC modes are enabled. The NCO phase accumulators are reset during the ILA phase of link startup which means that for multiple ADCs to have NCO phase alignment, all links must be enabled in the same LMFC period. Enabling all links in the same LMFC period requires synchronizing the SYNC~ de-assertion across all data receivers in the system, so that all of the SYNC~ signals are released during the same LMFC period. Using large K values and resulting longer LMFC periods will ease this task, at the expense of potentially higher latency in the receiving device.

7.4 Device Functional Modes

7.4.1 DDC Bypass Mode

In DDC bypass mode (decimation = 1) the raw 12 bit data from the ADC is output at the full sampling rate.

7.4.2 DDC Modes

In the DDC modes (decimation > 1) complex (I,Q) data is output at a lower sample rate as determined by the decimation factor (4, 8, 10, 16, 20, and 32).

7.4.3 Calibration

Calibration adjusts the ADC core to optimize the following device parameters:

- ADC core linearity
- ADC core-to-core offset matching
- ADC core-to-core full-scale range matching
- ADC core 4-way interleave timing

All calibration processes occur internally. Calibration does not require any external signals to be present and works properly as long as the device is maintained within the values listed in the *Recommended Operating Conditions* table.



Device Functional Modes (continued)

7.4.3.1 Foreground Calibration Mode

In foreground mode the calibration process interrupts normal ADC operation and no output data is available during this time (the output code is forced to a static value). The calibration process should be repeated if the device temperature changes by more than 20° C to ensure rated performance is maintained. Foreground calibration is initiated by setting the CAL_SFT bit (register 0x050, bit 3) which is self clearing. The foreground calibration process finishes within t_(CAL) number of DEVCLK cycles. The process occurs somewhat longer when the timing calibration mode is enabled.

NOTE

Initiating a foreground calibration asynchronously resets the calibration control logic and may glitch internal device clocks. Therefore after setting the CAL_SFT bit clearing and then setting JESD_EN is necessary. If resetting the JESD204B link is undesirable for system reasons, background calibration mode may be preferred.

7.4.3.2 Background Calibration Mode

In background mode an additional ADC core is powered-up for a total of 5 ADC cores. At any given time, one core is off-line and not used for data conversion. This core is calibrated in the background and then placed online simultaneous with another core going off-line for calibration. This process operates continuously without interrupting data flow in the application and ensures that all cores are optimized in performance regardless of any changes of temperature. The background calibration cycle rate is fixed and is not adjustable by the user.

Because of the additional circuitry active in background calibration mode, a slight degradation in performance occurs in comparison to foreground calibration mode at a fixed temperature. As a result of this degradation, using foreground calibration mode is recommended if the expected change in operating temperature is <30°C. Using background calibration mode is recommended if the expected change in operating temperature is >30°C. The exact difference in performance is dependent on the DEVCLK (sampling clock) frequency, and the analog input signal frequency and amplitude. For this reason, device and system performance should be evaluated using both calibration modes before finalizing the choice of calibration mode.

To enable the background calibration feature, set the CAL_BCK bit (register 0x057, bit 0) and the CAL_CONT bit (register 0x057, bit 1). The value written to the register 0x057 to enable background calibration is therefore 0x013h. After writing this value to register 0x057, set the CAL_SFT bit in register 0x050 to perform the one-time foreground calibration to begin the process.

NOTE

The ADC offset-adjust feature has no effect when background calibration mode is enabled.

7.4.4 Timing Calibration Mode

The timing calibration process optimizes the matching of sample timing for the 4 internally interleaved converters. This process minimize the presence of any timing related interleaving spurs in the captured spectrum. The timing calibration feature is disabled by default, but using this feature is highly recommended. To enable timing calibration, set the T_AUTO bit (register 0x066, bit 0). When this bit is set, the timing calibration performs each time the CAL_SFT bit is set.

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Device Functional Modes (continued)

CAL_CONT, CAL_BCK	T_AUTO	LOW_SIG_EN	$\begin{array}{l} \mbox{INITIAL ONE-TIME} \\ \mbox{CALIBRATION} \\ \mbox{CAL_SFT 0} \rightarrow 1 \\ \mbox{(}t_{\mbox{DevCLK}}) \end{array}$	BACKGROUND CALIBRATION CYCLE ⁽¹⁾ (ALL CORES) (t _{DEVCLK})
0	0	0	102 E+6	N/A
0	0	1	64 E+6	N/A
0	1	0	227 E+6	N/A
0	1	1	189 E+6	N/A
1	0	0	127.5 E+6	816 E+6
1	0	1	80 E+6	512 E+6
1	1	0	283.75 E+6	816 E+6
1	1	1	236.25 E+6	512 E+6

(1) N/A = not applicable

7.4.5 Test-Pattern Modes

A number of device test modes are available. These modes insert known patterns of information into the device data path for assistance with system debug, development, or characterization.

7.4.5.1 ADC Test-Pattern Mode

The 12-bit ADC core has a built-in test-pattern generator. This mode is helpful for verifying the full data link from the ADC to the data receiver when in DDC bypass mode. When the test-pattern mode is enabled, the ADC output data is replaced by a pattern that repeats every two frames. The data sequence is is shown in Table 33 (shown for default settings with foreground calibration mode).

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LANE (CONVERTER ID)		SAMPLE NUMBER (SID)												
	0	1	2	3	4	5	6	7	8	9				
0	0x000	0xFFF	0x000	0xFFF	0x000	0xFFF	0x000	0xFFF	0x000	0xFFF				
1	0x008	0xFF7	0x008	0xFF7	0x008	0xFF7	0x008	0xFF7	0x008	0xFF7				
2	0x010	0xFEF	0x010	0xFEF	0x010	0xFEF	0x010	0xFEF	0x010	0xFEF				
3	0x020	0xFDF	0x020	0xFDF	0x020	0xFDF	0x020	0xFDF	0x020	0xFDF				
4	0x040	0xFBF	0x040	0xFBF	0x040	0xFBF	0x040	0xFBF	0x040	0xFBF				
5	0x100	0xEFF	0x100	0xEFF	0x100	0xEFF	0x100	0xEFF	0x100	0xEFF				
6	0x200	0xDFF	0x200	0xDFF	0x200	0xDFF	0x200	0xDFF	0x200	0xDFF				
7	0x400	0xBFF	0x400	0xBFF	0x400	0xBFF	0x400	0xBFF	0x400	0xBFF				

Table 33. ADC Test Pattern⁽¹⁾

(1) When background-calibration mode is enabled, the pattern values are dynamic because the internal converter banks are output on different lanes during the calibration bank-switching process. Each converter bank has dedicated pattern values as listed in Table 34.

BANK	LOCATION	LOW VALUE	HIGH VALUE
0	Lane n	0x000	0xFFF
0	Lane n+4	0x040	0xFBF
4	Lane n	0x004	0xFFE
1	Lane n+4	0x080	0xF7F
0	Lane n	0x008	0xFF7
2	Lane n+4	0x100	0xEFF
2	Lane n	0x010	0xFEF
3	Lane n+4	0x200	0xDFF
4	Lane n	0x020	0xFDF
4	Lane n+4	0x400	0xBFF

Table 34. ADC Bank Pattern Values

7.4.5.2 Serializer Test-Mode Details

Test modes are enabled by setting the appropriate configuration of the JESD204B_TEST setting (Register 0x202, Bits 3:0). Each test mode is described in detail in the following sections. Regardless of the test mode, the serializer outputs are powered up based on the configuration decimation and DDR settings. The test modes should only be enabled while the JESD204B link is disabled.



Figure 66. Test-Mode Insertion Points



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7.4.5.3 PRBS Test Modes

The PRBS test modes bypass the 8B10B encoder. These test modes produce pseudo-random bit streams that comply with the ITU-T O.150 specification. These bit streams are used with lab test equipment that can self-synchronize to the bit pattern and therefore the initial phase of the pattern is not defined.

The sequences are defined by a recursive equation. For example, the PRBS7 sequence is defined as shown in Equation 9.

 $y[n] = y[n - 6]^{y[n - 7]}$

where

• Bit n is the XOR of bit [n - 6] and bit [n - 7] which are previously transmitted bits

(9)

PRBS TEST MODE	SEQUENCE	SEQUENCE LENGTH (bits)
PRBS7	$y[n] = y[n - 6]^{y[n - 7]}$	127
PRBS15	$y[n] = y[n - 14]^{y[n - 15]}$	32767
PRBS23	$y[n] = y[n - 18]^{y[n - 23]}$	8388607

Table 35. PBRS Mode Equations

The initial phase of the pattern is unique for each lane.

7.4.5.4 Ramp Test Mode

In the ramp test mode, the JESD204B link layer operates normally, but the transport layer is disabled and the input from the formatter is ignored. After the ILA sequence, each lane transmits an identical octet stream that increments from 0x00 to 0xFF and repeats.

7.4.5.5 Short and Long-Transport Test Mode

The short-transport test mode is available when the device is operated in DDC bypass mode (decimation = 1). The short transport pattern has a length of one frame. Table 36 lists the formula followed by each sample of the pattern.

Table 36. Short Transport Test Pattern Definition

					В	IT					
11	10	9	8	7	6	5	4	3	2	1	0
	~L	ID			L	ID			SIE	D+1	

LID is the lane ID (0 to 7) and SID is the sample number within the frame (0 to 4). The entire pattern has a length of one frame and is listed in Table 37.

		•								
LANE (CONVERTER ID)		SAMPLE NUMBER (SID)								
	0	1	2	3	4					
0	0xF01	0xF02	0xF03	0xF04	0xF05					
1	0xE11	0xE12	0xE13	0xE14	0xE15					
2	0xD21	0xD22	0xD23	0xD24	0xD25					
3	0xC31	0xC32	0xC33	0xC34	0xC35					
4	0xB41	0xB42	0xB43	0xB44	0xB45					
5	0xA51	0xA52	0xA53	0xA54	0xA55					
6	0x961	0x962	0x963	0x964	0x965					
7	0x871	0x872	0x873	0x874	0x875					

Table 37. Short Transport Test Pattern

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The long-transport test mode is available in all DDC modes (decimation > 1). Patterns are generated in accordance with the JESD204B standard and are different for each output format.

Table 38 lists one example of the long transport test pattern:

						-	TIME –	→														
CHAR NO.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
Lane 0	0x0	003	0x0	002	0x8	000	0x8	000	0x8	3000	0x8	000	0x8	8000	0x8	000	0x8	000	0x8	000	0x0	003
Lane 1	0x0	002	0x0	005	0x8	000	0x8	000	0x8	3000	0x8	000	0x8	8000	0x8	000	0x8	000	0x8	000	0x0	002
Lane 2	0x0	004	0x0	002	0x8	001	0x8	000	0x8	3000	0x8	000	0x8	8000	0x8	000	0x8	000	0x8	000	0x0	004
Lane 3	0x0	004	0x0	004	0x8	000	0x8	001	0x8	3000	0x8	000	0x8	8000	0x8	000	0x8	000	0x8	000	0x0	004
	Fra 1	ime 1	Fra n ·	ime + 1	Fra n -	ime ⊦ 2	Fra n ·	ame + 3	Fra n	ame + 4	Fra n +	ime ⊦5	Fra n ·	ame + 6	Fra n ·	ime ⊦ 7	Fra n -	ime + 8	Fra n -	ime ⊦9	Fra n +	me 10

Table 38. Long Transport Test Pattern - Decimate-by-4, DDR = 1, P54 = 1, K=10

If multiple devices are all programmed to the transport layer test mode (while JESD_EN = 0), then JESD_EN is set to 1, and then SYSREF is used to align the LMFC of the devices, the patterns will be aligned to the SYSREF event (within the skew budget of JESD204B). For more details see JESD204B, section 5.1.6.3.

7.4.5.6 D21.5 Test Mode

In this test mode, the controller transmits a continuous stream of D21.5 characters (alternating 0s and 1s).

7.4.5.7 K28.5 Test Mode

In this test mode, the controller transmits a continuous stream of K28.5 characters.

7.4.5.8 Repeated ILA Test Mode

In this test mode, the JESD204B link layer operates normally with one exception: when the ILA sequence completes, the sequence repeats indefinitely. Whenever the receiver issues a synchronization request, the transmitter will initiate code group synchronization. Upon completion of code group synchronization, the transmitter will repeatedly transmit the ILA sequence. If there is no active code group synchronization request at the moment the transmitter enters the test mode, the transmitter will behave as if it received one.

7.4.5.9 Modified RPAT Test Mode

A 12-octet repeating pattern is defined in INCITS TR-35-2004. The purpose of this pattern is to generate white spectral content for JESD204B compliance and jitter testing. Table 39 lists the pattern before and after 8b10b encoding.

OCTET NUMBER	Dx.y NOTATION	8-BIT INPUT TO 8b10b ENCODER	20b OUTPUT OF 8b10b ENCODER (2 CHARACTERS)
0	D30.5	0xBE	0.000
1	D23.6	0xD7	UXOODAO
2	D3.1	0x23	0.000475
3	D7.2	0x47	0xC6475
4	D11.3	0x6B	
5	D15.4	0x8F	0xD0E8D
6	D19.5	0xB3	
7	D20.0	0x14	UXCA8B4
8	D30.2	0x5E	0.70405
9	D27.7	0xFB	0x7949E
10	D21.1	0x35	0.44665
11	D25.2	0x59	COOMANU

Table 39. Modified RPAT Pattern Values



The serial interface is accessed using the following four pins: serial clock (SCLK), serial-data in (SDI), serial-data out (SDO), and serial-interface chip-select (SCS). Registers access is enabled through the SCS pin.

- **SCS** This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.
- **SCLK** Serial data input is accepted at the rising edge of this signal. SCLK has no minimum frequency requirement.
- **SDI** Each register access requires a specific 24-bit pattern at this input. This pattern consists of a readand-write (R/W) bit, register address, and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed (see Figure 2).
- **SDO** The SDO signal provides the output data requested by a read command. This output is high impedance during write bus cycles and during the read bit and register address portion of read bus cycles.

Each register access consists of 24 bits, as shown in Figure 2. The first bit is high for a read and low for a write.

The next 15 bits are the address of the register that is to be written to. During write operations, the last 8 bits are the data written to the addressed register. During read operations, the last 8 bits on SDI are ignored, and, during this time, the SDO outputs the data from the addressed register. The serial protocol details are illustrated in Figure 67.



Figure 67. Serial Interface Protocol - Single Read / Write

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Programming (continued)

7.5.1.1 Streaming Mode

The serial interface supports streaming reads and writes. In this mode, the initial 24 bits of the transaction specifics the access type, register address, and <u>data</u> value as normal. Additional clock cycles of write or read data are immediately transferred, as long as the SCS input is maintained in the asserted (logic low) state. The register address auto increments (default) or decrements for each subsequent 8 bit transfer of the streaming transaction. The ADDR_ASC bit (register 000h, bits 5 and 2) controls whether the address value ascends (increments) or descends (decrements). Streaming mode can be disabled by setting the ADDR_STATIC bit (register 010h, bit 0). The streaming mode transaction details are shown in Figure 68.



Figure 68. Serial Interface Protocol - Streaming Read / Write

See the Register Map section for detailed information regarding the registers.

NOTE

The serial interface must not be accessed during calibration of the ADC. Accessing the serial interface during this time impairs the performance of the device until the device is calibrated correctly. Writing or reading the serial registers also reduces dynamic performance of the ADC for the duration of the register access time.



7.6 Register Map

Several groups of registers provide control and configuration options for this device. Each following register description also shows the power-on reset (POR) state of each control bit.

NOTE All multi-byte registers are arranged in little-endian format (the least-significant byte is stored at the lowest address) unless explicitly stated otherwise.

	метогу мар						
Address	Reset	Туре	Register				
		Standar	rd SPI-3.0 (0x000 to 0x00F)				
0x000	0x3C	R/W	Configuration A Register				
0x001	0x00	R	Configuration B Register				
0x002	0x00	R/W	Device Configuration Register				
0x003	0x03	R	Chip Type Register				
0x004-0x005	Undefined	R	RESERVED				
0x006	0x03	R	Chip Version Register				
0x007-0x00B	Undefined	R	RESERVED				
0x00C-0x00D	0x0451	R	Vendor Identification Register				
0x00E-0x00F	Undefined	R	RESERVED				
		User SPI C	onfiguration (0x010 to 0x01F)				
0x010	0x00	R/W	User SPI Configuration Register				
0x011-0x01F	Undefined	R	RESERVED				
	General A	nalog, Bias, Bar	nd Gap, and Track and Hold (0x020 to 0x02F)				
0x020	0x9D	R/W	RESERVED				
0x021	0x00	R/W	Power-On Reset Register				
0x022	0x40	R/W	I/O Gain 0 Register				
0x023	0x00	R/W	I/O Gain 1 Register				
0x024	0x00	R/W	W RESERVED				
0x025	0x40	R/W	I/O Offset 0 Register				
0x026	0x00	R/W	I/O Offset 1 Register				
0x027	0x06	R/W	RESERVED				
0x028	0xBA	R/W	RESERVED				
0x029	0xD4	R/W	RESERVED				
0x02A	0xEA	R/W	RESERVED				
0x02B-0x02F	Undefined	R	RESERVED				
		CI	lock (0x030 to 0x03F)				
0x030	0xC0	R/W	Clock Generator Control 0 Register				
0x031	0x07	R	Clock Generator Status Register				
0x032	0x80	R/W	Clock Generator Control 2 Register				
0x033	0xC3	R/W	Analog Miscellaneous Register				
0x034	0x2F	R/W	Input Clamp Enable Register				
0x035	0xDF	R/W	RESERVED				
0x036	0x00	R/W	RESERVED				
0x037	0x45	R/W	RESERVED				
0x038-0x03F	Undefined	R/W	RESERVED				
		Seri	alizer (0x040 to 0x04F)				
0x040	0x04	R/W	Serializer Configuration Register				
0x041-0x04F	Undefined	R	RESERVED				

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Register Map (continued)

Memory Map (continued)

Address	Reset	Туре	Register
		ADC Ca	libration (0x050 to 0x1FF)
0x050	0x06	R/W	Calibration Configuration 0 Register
0x051	0xF4	R/W	Calibration Configuration 1 Register
0x052	0x00	R/W	RESERVED
0x053	0x5C	R/W	RESERVED
0x054	0x1C	R/W	RESERVED
0x055	0x92	R/W	RESERVED
0x056	0x20	R/W	RESERVED
0x057	0x10	R/W	Calibration Background Control Register
0x058	0x00	R/W	ADC Pattern and Over-Range Enable Register
0x059	0x00	R/W	RESERVED
0x05A	0x00	R/W	Calibration Vectors Register
0x05B	Undefined	R	Calibration Status Register
0x05C	0x00	R/W	RESERVED
0x05D-0x05E	Undefined	R/W	RESERVED
0x05F	0x00	R/W	RESERVED
0x060	Undefined	R	RESERVED
0x061	Undefined	R	RESERVED
0x062	Undefined	R	RESERVED
0x063	Undefined	R	RESERVED
0x064	Undefined	R	RESERVED
0x065	Undefined	R	RESERVED
0x066	0x02	R/W	Timing Calibration Register
0x067	0x01	R/W	RESERVED
0x068	Undefined	R	RESERVED
0x069	Undefined	R	RESERVED
0x06A	0x00	R/W	RESERVED
0x06B	0x20	R/W	RESERVED
0x06C-0x1FF	Undefined	R	RESERVED
	C	igital Down Conv	verter and JESD204B (0x200-0x27F)
0x200	0x10	R/W	Digital Down-Converter (DDC) Control
0x201	0x0F	R/W	JESD204B Control 1
0x202	0x00	R/W	JESD204B Control 2
0x203	0x00	R/W	JESD204B Device ID (DID)
0x204	0x00	R/W	JESD204B Control 3
0x205	Undefined	R/W	JESD204B and System Status Register
0x206	0xF2	R/W	Overrange Threshold 0
0x207	0xAB	R/W	Overrange Threshold 1
0x208	0x00	R/W	Overrange Period
0x209-0x20B	0x00	R/W	RESERVED
0x20C	0x00	R/W	DDC Configuration Preset Mode
0x20D	0x00	R/W	DDC Configuration Preset Select
0x20E-0x20F	0x0000	R/W	Rational NCO Reference Divisor
PRESET 0	1	1	T
0x210-0x213	0xC0000000	R/W	NCO Frequency (Preset 0)
0x214-0x215	0x0000	R/W	NCO Phase (Preset 0)

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Register Map (continued)

Memory Map (continued)

Address	Reset	Туре	Register				
0x216	0xFF	R/W	DDC Delay (Preset 0)				
0x217	0x00	R/W	RESERVED				
PRESET 1							
0x218-0x21B	0xC0000000	R/W	NCO Frequency (Preset 1)				
0x21C-0x21D	0x0000	R/W	NCO Phase (Preset 1)				
0x21E	0xFF	R/W	DDC Delay (Preset 1)				
0x21F	0x00	R/W	RESERVED				
PRESET 2							
0x220-0x223	0xC0000000	R/W	NCO Frequency (Preset 2)				
0x224-0x225	0x0000	R/W	NCO Phase (Preset 2)				
0x226	0xFF	R/W	DDC Delay (Preset 2)				
0x227	0x00	R/W	RESERVED				
PRESET 3							
0x228-0x22B	0xC0000000	R/W	NCO Frequency (Preset 3)				
0x22C-0x22D	0x0000	R/W	NCO Phase (Preset 3)				
0x22E	0xFF	R/W	DDC Delay (Preset 3)				
0x22F	0x00	R/W	RESERVED				
PRESET 4							
0x230-0x233	0xC0000000	R/W	NCO Frequency (Preset 4)				
0x234-0x235	0x0000	R/W	NCO Phase (Preset 4)				
0x236	0xFF	R/W	DDC Delay (Preset 4)				
0x237	0x00	R/W	RESERVED				
PRESET 5							
0x238-0x23B	0xC0000000	R/W	NCO Frequency (Preset 5)				
0x23C-0x23D	0x0000	R/W	NCO Phase (Preset 5)				
0x23E	0xFF	R/W	DDC Delay (Preset 5)				
0x23F	0x00	R/W	RESERVED				
PRESET 6							
0x240-0x243	0xC0000000	R/W	NCO Frequency (Preset 6)				
0x244-0x245	0x0000	R/W	NCO Phase (Preset 6)				
0x246	0xFF	R/W	DDC Delay (Preset 6)				
0x247	0x00	R/W	RESERVED				
PRESET 7							
0x248-0x24B	0xC0000000	R/W	NCO Frequency (Preset 7)				
0x24C-0x24D	0x0000	R/W	NCO Phase (Preset 7)				
0x24E	0xFF	R/W	DDC Delay (Preset 7)				
0x24F-0x251	0x00	R/W	RESERVED				
0x252-0x27F	Undefined	R	RESERVED				
			Reserved				
0x0280-0x7FFF	Undefined	R	RESERVED				

7.6.1 Register Descriptions

7.6.1.1 Standard SPI-3.0 (0x000 to 0x00F)

Table 40. Standard SPI-3.0 Registers

Address	Reset	Acronym	Register Name	Section
0x000	0x3C	CFGA	Configuration A Register	Go
0x001	0x00	CFGB	Configuration B Register	Go
0x002	0x00	DEVCFG	Device Configuration Register	Go
0x003	0x03	CHIP_TYPE	Chip Type Register	Go
0x004-0x005	0x0000	RESERVED	RESERVED	Go
0x006	0x03	CHIP_VERSION	Chip Version Register	Go
0x007-0x00B	Undefined	RESERVED	RESERVED	
0x00C-0x00D	0x0451	VENDOR_ID	Vendor Identification Register	Go
0x00E-0x00F	Undefined	RESERVED	RESERVED	

7.6.1.1.1 Configuration A Register (address = 0x000) [reset = 0x3C]

All writes to this register must be a palindrome (for example: bits [3:0] are a mirror image of bits [7:4]). If the data is not a palindrome, the entire write is ignored.

Figure 69. Configuration A Register (CFGA)

7	6	5	4	3	2	1	0
SWRST	RESERVED	ADDR_ASC	RESERVED	RESERVED	ADDR_ASC	RESERVED	SWRST
R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0

Table 41. CFGA Field Descriptions

Bit	Field	Туре	Reset	Description
7	SWRST	R/W	0	Setting this bit causes all registers to be reset to their default state. This bit is self-clearing.
6	RESERVED	R/W	0	
5	ADDR_ASC	R/W	1	This bit is NOT reset by a soft reset (SWRST) 0 : descend – decrement address while streaming (address wraps from 0x0000 to 0x7FFF) 1 : ascend – increment address while streaming (address wraps from 0x7FFF to 0x0000) (default)
4	RESERVED	R/W	1	Always returns 1
3	RESERVED	R/W		
2	ADDR_ASC	R/W	1100	Palindrome bits
1	RESERVED	R/W	1100	bit $3 = bit 4$, bit $2 = bit 5$, bit $1 = bit 6$, bit $0 = bit 7$
0	SWRST	R/W		

7.6.1.1.2 Configuration B Register (address = 0x001) [reset = 0x00]

Figure 70. Configuration B Register (CFGB)

7	6	5	4	3	2	1	0
			RESE	RVED			
			R - 0	x00h			

Table 42. CFGB Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	RESERVED	R	0000 0000	



7.6.1.1.3 Device Configuration Register (address = 0x002) [reset = 0x00]

7	6	5	4	3	2	1	0
		RESEI	RVED			MC	DDE
		R/W-0	00000			R/V	V-00

Table 43. DEVCFG Field Descriptions

Bit	Field	Туре	Reset	Description
7-2	RESERVED	R/W	0000 00	
1-0	MODE	R/W	00	 SPI 3.0 specification has 1 as low power functional mode and 2 as low power fast resume. This chip does not support these modes. O: Normal Operation – full power and full performance (default) 1: Normal Operation – full power and full performance (default) 2: Power Down – Everything powered down 3: Power Down – Everything powered down

7.6.1.1.4 Chip Type Register (address = 0x003) [reset = 0x03]

Figure 72. Chip Type Register (CHIP_TYPE)

7	6	5	4	3	2	1	0	
RESERVED				CHIP_TYPE				
R-0000					R-0	011		

Table 44. CHIP_TYPE Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	RESERVED	R	0000	
3-0	CHIP_TYPE	R	0011	Always returns 0x3, indicating that the part is a high speed ADC.

7.6.1.1.5 Chip Version Register (address = 0x006) [reset = 0x03]

Figure 73. Chip Version Register (CHIP_VERSION)

7	6	5	4	3	2	1	0
			CHIP_V	ERSION			
R-0000 0011							

Table 45. CHIP_VERSION Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	CHIP_VERSION	R	0000 0011	Chip version, returns 0x03

Field

VENDOR_ID

Bit

15-0

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7.6.1.1.6 Vendor Identification Register (address = 0x00C to 0x00D) [reset = 0x0451]

Туре

R

15	14	13	12	11	10	9	8
			VEND	OR_ID			
R-0x04h							
7	6	5	4	3	2	1	0
			VEND	OR_ID			
R-0x51h							
Table 46. VENDOR ID Field Descriptions							

Reset

0x0451h

Figure 74. Vendor Identification Register (VENDOR_ID)

7.6.1.2 User SPI Configuration (0x010 to 0x01F)

Table 47. User SPI Configuration Registers

Description

Always returns 0x0451 (TI Vendor ID)

Address	Reset	Acronym	Register Name	Section
0x010	0x00	USR0	User SPI Configuration Register	Go
0x011-0x01F	Undefined	RESERVED	RESERVED	

7.6.1.2.1 User SPI Configuration Register (address = 0x010) [reset = 0x00]

Figure 75. User SPI Configuration Register (USR0)

7	6	5	4	3	2	1	0
			RESERVED				ADDR_STATIC
	R/W-0000 000						R/W-0

Table 48. USR0 Field Descriptions

				-
Bit	Field	Туре	Reset	Description
7-1	RESERVED	R/W	0000 000	
0	ADDR_STATIC	R/W	0	 0 : Use ADDR_ASC bit to define what happens to address during streaming (default). 1 : Address stays static throughout streaming operation. Useful for reading/writing calibration vector information at CAL_VECTOR register.



7.6.1.3 General Analog, Bias, Band Gap, and Track and Hold (0x020 to 0x02F)

Address	Reset	Acronym	Register Name	Section
0x020	0x9D	RESERVED	RESERVED	
0x021	0x00	POR	Power-On Reset Register	Go
0x022	0x40	IO_GAIN_0	I/O Gain 0 Register	Go
0x023	0x00	IO_GAIN_1	I/O Gain 1 Register	Go
0x024	0x00	RESERVED	RESERVED	
0x025	0x40	IO_OFFSET_0	I/O Offset 0 Register	Go
0x026	0x00	IO_OFFSET_1	I/O Offset 1 Register	Go
0x027	0x06	RESERVED	RESERVED	
0x028	0xBA	RESERVED	RESERVED	
0x029	0xD4	RESERVED	RESERVED	
0x02A	0xAA	RESERVED	RESERVED	
0x02B-0x02F	Undefined	RESERVED	RESERVED	

Table 49. General Analog, Bias, Band Gap, and Track and Hold Registers

7.6.1.3.1 Power-On Reset Register (address = 0x021) [reset = 0x00]

Figure 76. Power-On Reset Register (POR)

7	6	5 4		3	2	1	0
		RESERVED					SPI_RES
	R/W-0000 000						

Table 50. POR Field Descriptions

Bit	Field	Туре	Reset	Description
7-1	RESERVED	R/W	0000 000	
0	SPI_RES	R/W	0	Reset all digital. Emulates a power on reset (not self-clearing). Write a 0 and then write a 1 to emulate a reset. Transition from 0 —>1 initiates reset. Default: 0

7.6.1.3.2 I/O Gain 0 Register (address = 0x022) [reset = 0x40]

Figure 77. I/O Gain 0 Register (IO_GAIN_0)

7	6	5	4	3	2	1	0
RESERVED	GAIN_FS[14]	GAIN_FS[13]	GAIN_FS[12]	GAIN_FS[11]	GAIN_FS[10]	GAIN_FS[9]	GAIN_FS[8]
R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 51. IO_GAIN_0 Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R/W	0	
6-0	GAIN_FS[14:8]	R/W	100 0000	MSB Bits for GAIN_FS[14:0]. (See the IO_GAIN_1 description in General Analog, Bias, Band Gap, and Track and Hold (0x020 to 0x02F))

7.6.1.3.3 IO_GAIN_1 Register (address = 0x023) [reset = 0x00]

7	6	5	4	Ļ.	3	2	1	0
GAIN_FS	[7] GAIN_FS[6]	GAIN_FS[5]	GAIN_	FS[4] (GAIN_FS[3]	GAIN_FS[2]	GAIN_FS[1]	GAIN_FS[0]
R/W-0	R/W-0	R/W-0	R/V	V-0	R/W-0	R/W-0	R/W-0	R/W-0
Table 52. IO_GAIN_1 Field Descriptions								
Bit	Field	٦	Туре	Reset	Description			
7-0	GAIN_FS[7:0]	F	R/W	0000 0000	LSB bits for GAIN_FS[14 0x0000 500 0x4000 725 0x7FFF 950	GAIN_FS[14:0] I:0] Value mVp-p mVp-p (default) mVp-p		

Figure 78. IO_GAIN_1 Register (IO_GAIN_1)

7.6.1.3.4 I/O Offset 0 Register (address = 0x025) [reset = 0x40]

Figure 79. I/O Offset 0 Register (IO_OFFSET_0)

7	6	5	4	3	2	1	0
RESERVED	OFFSET_FS[1	OFFSET_FS[1	OFFSET_FS[1	OFFSET_FS[1	OFFSET_FS[1	OFFSET_FS[9]	OFFSET_FS[8]
	4]	3]	2]	1]	0]		
R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 53. IO_OFFSET_0 Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R/W	0	
6-0	OFFSET_FS[14:8]	R/W	100 0000	MSB Bits for OFFSET_FS[14:0]. The ADC offset adjust feature has no effect when Background Calibration Mode is enabled. (See IO_OFFSET_1 description in the <i>General Analog, Bias, Band Gap, and Track and Hold</i> (0x020 to 0x02F) section).

7.6.1.3.5 I/O Offset 1 Register (address = 0x026) [reset = 0x00]

Figure 80. I/O Offset 1 Register (IO_OFFSET_1)

7	6	5	4	3	2	1	0
OFFSET_FS[7]	OFFSET_FS[6]	OFFSET_FS[5]	OFFSET_FS[4]	OFFSET_FS[3]	OFFSET_FS[2]	OFFSET_FS[1]	OFFSET_FS[0]
R/W-0							

Table 54. IO_OFFSET_1 Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	OFFSET_FS[7:0]	R/W	0000 0000	LSB bits for OFFSET_FS[14:0]. OFFSET_FS[14:0] adjusts the offset of the entire ADC (all banks are impacted). OFFSET_FS[14:0] Value 0x0000 –28-mV offset 0x4000 no offset (default) 0x7FFF 28-mV offset The ADC offset adjust feature has no effect when Background Calibration Mode is enabled.

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7.6.1.4 Clock (0x030 to 0x03F)

Address	Reset	Acronym	Register Name	Section
0x030	0xC0	CLKGEN_0	Clock Generator Control 0 Register	Go
0x031	0x07	CLKGEN_1	Clock Generator Status Register	Go
0x032	0x80	CLKGEN_2	Clock Generator Control 2 Register	Go
0x033	0xC3	ANA_MISC	Analog Miscellaneous Register	Go
0x034	0x2F	IN_CL_EN	Clamp Enable Register	Go
0x035	0xDF	RESERVED	RESERVED	
0x036	0x00	RESERVED	RESERVED	
0x037	0x45	RESERVED	RESERVED	
0x038-0x03F	Undefined	RESERVED	RESERVED	

Table 55. Clock Registers

7.6.1.4.1 Clock Generator Control 0 Register (address = 0x030) [reset = 0xC0]

Figure 81. Clock Generator Control 0 Register (CLKGEN_0)

7	6	5	4	3	2	1	0
SysRef_Rcvr_E n	SysRef_Pr_En	SysRefDetClr	Clear Dirty Capture	RESERVED	DC_LVPECL_C LK en	DC_LVPECL_S YSREF en	DC_LVPECL_T S en
R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 56. CLKGEN_0 Field Descriptions

Bit	Field	Туре	Reset	Description
7	SysRef_Rcvr_En	R/W	1	Default: 1 0 : SYSREF receiver is disabled. 1 : SYSREF receiver is enabled (default)
6	SysRef_Pr_En	R/W	1	To power down the SYSREF receiver, clear this bit first, then clear SysRef_Rcvr_En. To power up the SYSREF receiver, set SysRef_Rcvr_En first, then set this bit. Default: 1 0 : SYSREF Processor is disabled. 1 : SYSREF Processor is enabled (default)
5	SysRefDetClr	R/W	0	Default: 0 Write a <i>1</i> and then a <i>0</i> to clear the SysRefDet status bit.
4	Clear Dirty Capture	R/W	0	Default: 0 Write a <i>1</i> and then a <i>0</i> to clear the DC status bit.
3	RESERVED	R/W	0	Default: 0
2	DC_LVPECL_CLK_en	R/W	0	Default: 0 Set this bit if DEVCLK is a DC-coupled LVPECL signal through a 50 - Ω resistor.
1	DC_LVPECL_SYSREF_en	R/W	0	Default: 0 Set this bit if SYSREF is a DC-coupled LVPECL signal through a $50-\Omega$ resistor.
0	DC_LVPECL_TS_en	R/W	0	Default: 0 Set this bit if TimeStamp is a DC-coupled LVPECL signal through a $50-\Omega$ resistor.

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7.6.1.4.2 Clock Generator Status Register (address = 0x031) [reset = 0x07]

Figure 82. Clock Generator Status Register (CLKGEN_1)

7	6	5	4	3	2	1	0
SysRefDet	Dirty Capture			RESE	RVED		
R-0	R-0			R-00	0111		

Table 57. CLKGEN_1 Field Descriptions

Bit	Field	Туре	Reset	Description
7	SysRefDet	R	0	When high, indicates that a SYSREF rising edge was detected. To clear this bit, write SysRefDetClr to <i>1</i> and then back to <i>0</i> .
6	Dirty Capture	R	0	When high, indicates that a SYSREF rising edge occurred very close to the device clock edge, and setup or hold is not ensured (dirty capture). To clear this bit, write CDC to 1 and then back to 0. NOTE: When sweeping the timing on SYSREF, it may jump across the clock edge without triggering this bit. The REALIGNED status bit must be used to detect this (see the JESD_STATUS register description in Digital Down Converter and JESD204B (0x200-0x27F))
5-0	RESERVED	R	00 0111	Reserved register. Always returns 000111b

7.6.1.4.3 Clock Generator Control 2 Register (address = 0x032) [reset = 0x80]

Figure 83. Clock Generator Control 2 Register (CLKGEN_2)

7	6	5	4	3	2	1	0
RESERVED					RD	EL	
	R/W-	1000			R/W-	0000	

Table 58. CLKGEN_2 Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	RESERVED	R/W	1000	Default: 1000b
3-0	RDEL	R/W	0000	Adjusts the delay of the SYSREF input signal with respect to DEVCLK. Each step delays SYSREF by 20 ps (nominal) Default: 0 Range: 0 to 15 decimal



7.6.1.4.4 Analog Miscellaneous Register (address = 0x033) [reset = 0xC3]

Figure 84. Analog Miscellaneous Register (ANA_MISC)

7	6	5	4	3	2	1	0
		RESERVED			SYNC_DIFF_PD	RESE	RVED
		R/W-1100 0			R/W-0	R/W	/-11

Table 59. ANA_MISC Field Descriptions

Bit	Field	Туре	Reset	Description
7-3	RESERVED	R/W	1100 0	
2	SYNC_DIFF_PD	R/W	0	Set this bit to power down the differential SYNC-± inputs for the JESD204B interface. The SYNC-± inputs can also serve as the TimeStamp input receiver for the TimeStamp function. The receiver must be powered up to support the time stamp or differential SYNC Default: 0b
1-0	RESERVED	R/W	11	Default: 11b

7.6.1.4.5 Input Clamp Enable Register (address = 0x034) [reset = 0x2F]

Figure 85. Input Clamp Enable Register (IN_CL_EN)

7	6	5	4	3	2	1	0
RESER	RVED	INPUT_CLAMP_EN			RESERVED	I	
R/W-	·00	R/W-1			R/W-0 1111		

Table 60. IN_CL_EN Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	RESERVED	R/W	00	Default: 00b
5	INPUT_CLAMP_EN	R/W	1	Set this bit to enable the analog input active clamping circuit. Enabled by default. Default: 1b
4-0	RESERVED	R/W	0 1111	Default: 01111b

7.6.1.5 Serializer (0x040 to 0x04F)

Table 61. Serializer Registers

Address	Reset	Acronym	Register Name	Section
0x040	0x04	SER_CFG	Serializer Configuration Register	Go
0x041-0x04F	Undefined	RESERVED	RESERVED	

7.6.1.5.1 Serializer Configuration Register (address = 0x040) [reset = 0x04]

Figure 86. Serializer configuration Register (SER_CFG)

7	6	5	4	3	2	1	0
	RESE	RVED		SERIALIZER PRE-EMPHASIS			
	R/W-	0000			R/W-	0100	

Table 62. SER_CFG Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	RESERVED	R/W	0000	
3-0	SERIALIZER PRE-EMPHASIS	R/W	0100	Control bits for the pre-emphasis strength of the serializer output driver. Pre-emphasis is required to compensate the low pass behavior of the PCB trace. Default: 4d





7.6.1.6 ADC Calibration (0x050 to 0x1FF)

Address	Reset	Acronym	Register Name	Section
0x050	0x06	CAL_CFG0	Calibration Configuration 0 Register	Go
0x051	0xF4	CAL_CFG1	Calibration Configuration 1 Register	Go
0x052	0x00	RESERVED	RESERVED	
0x053	0x5C	RESERVED	RESERVED	
0x054	0x1C	RESERVED	RESERVED	
0x055	0x92	RESERVED	RESERVED	
0x056	0x20	RESERVED	RESERVED	
0x057	0x10	CAL_BACK	Calibration Background Control Register	Go
0x058	0x00	ADC_PAT_OVR_EN	ADC Pattern and Over-Range Enable Register	Go
0x059	0x00	RESERVED	RESERVED	
0x05A	0x00	CAL_VECTOR	Calibration Vectors Register	Go
0x05B	Undefined	CAL_STAT	Calibration Status Register	Go
0x05C	0x00	RESERVED	RESERVED	
0x05D-0x05E	Undefined	RESERVED	RESERVED	
0x05F	0x00	RESERVED	RESERVED	
0x060	Undefined	RESERVED	RESERVED	
0x061	Undefined	RESERVED	RESERVED	
0x062	Undefined	RESERVED	RESERVED	
0x063	Undefined	RESERVED	RESERVED	
0x064	Undefined	RESERVED	RESERVED	
0x065	Undefined	RESERVED	RESERVED	
0x066	0x02	T_CAL	Timing Calibration Register	Go
0x067	0x01	RESERVED	RESERVED	
0x068	Undefined	RESERVED	RESERVED	
0x069	Undefined	RESERVED	RESERVED	
0x06A	0x00	RESERVED	RESERVED	
0x06B	0x20	RESERVED	RESERVED	
0x06C-0x1FF	Undefined	RESERVED	RESERVED	

Table 63. ADC Calibration Registers

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7.6.1.6.1 Calibration Configuration 0 Register (address = 0x050) [reset = 0x06]

7	6	5	4	3	2	1	0
RESE	ESERVED TIME_STAMP_EN CALIBRATION_READ_WRITE_EN		CAL_SFT	RESERVED			
R/W	/-00	R/W-0	R/W-0	R/W-0		R/W-110	
			Table 64 CAL CEG0 Field	Descriptions			

Figure 87. Calibration Configuration 0 Register (CAL_CFG0)

Bit	Field	Туре	Reset	Description						
7-	RESERVED	R/W	00							
5	TIME_STAMP_EN	R/W	0	Enables the capture of the external time stamp signal to allow tracking of input signal. Default: 0						
4	CALIBRATION_READ_WRITE_EN	R/W	0	Enables the scan register to read or write calibration vectors at register 0x05A. Default: 0						
3	CAL_SFT ⁽¹⁾	R/W	0	Software calibration bit. Set bit to initiate foreground calibration. This bit is self-clearing. This bit resets the calibration state machine. Most calibration SPI registers are not synchronized to the calibration clock. Changing them may corrupt the calibration state machine. Always set CAL_SFT AFTER making any changes to the calibration registers.						
2-0	RESERVED	R/W	110	Default: 110						

(1) IMPORTANT NOTE: Setting CAL_SFT can glitch internal state machines. The JESD_EN bit must be cleared and then set after setting CAL_SFT.

7.6.1.6.2 Calibration Configuration 1 Register (address = 0x051) [reset = 0xF4]

Figure 88. Calibration Configuration 1 Register (CAL_CFG1)

7	6	6 5		3	2	1	0
RESERVED		LOW_SIG_EN			RESE	RVED	
R/W-1		R/W-111			R/W-	0100	

Table 65. CAL_CFG1 Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R/W	1	
6-4	LOW_SIG_EN	R/W	111	Controls signal range optimization for calibration processes. 111: Calibration is optimized for lower amplitude input signals (< -10dBFS). 000: Calibration is optimized for large (-1dBFS) input signals. Default: 111 but recommend 000 for large input signals.
3-0	RESERVED	R/W	0100	



7.6.1.6.3 Calibration Background Control Register (address = 0x057) [reset = 0x10]

- I iguie ob. Outbration Buokground Control Register (CAL_BAOK	Figure 89.	Calibration Background Co	ontrol Register (CAL_BACK
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7	6	5	4	3	2	1	0
		RESE	RVED			CAL_CONT	CAL_BCK
		R/W-00	001 00			R/W-0	R/W-0

Table 66. CAL_BACK Field Descriptions

Bit	Field	Туре	Reset	Description
7-2	RESERVED	R/W	0001 00	Set to 0001 00b
1	CAL_CONT	R/W	0	CAL_CONT is the only calibration register bit that can be modified while background calibration is ongoing. This bit must be set to 0 before modifying any of the other bits. 0 : Pause or stop background calibration sequence. 1 : Start background calibration sequence.
0	CAL_BCK	R/W	0	Background calibration mode enabled. When pausing background calibration leave this bit set, only change CAL_CONT to 0. If CAL_BCK is set to 0 after background calibration has been operation the calibration processes may stop in an incomplete condition. Set CAL_SFT to perform a foreground calibration

7.6.1.6.4 ADC Pattern and Over-Range Enable Register (address = 0x058) [reset = 0x00]

Figure 90. ADC Pattern and Over-Range Enable Register (ADC_PAT_OVR_EN)

7	6	5 4 3		3	2	1	0
		RESERVED			ADC_PAT_EN	OR_EN	RESERVED
		R/W-0000 0			R/W-0	R/W-0	R/W-0

Table 67. ADC_PAT_OVR_EN Field Descriptions

Bit	Field	Туре	Reset	Description
7-3	RESERVED	R/W	0000 0	Set to 00000b
2	ADC_PAT_EN	R/W	0	Enable ADC test pattern
1	OR_EN	R/W	0	Enable over-range output
0	RESERVED	R/W	0	Set to 0

7.6.1.6.5 Calibration Vectors Register (address = 0x05A) [reset = 0x00]

Figure 91. Calibration Vectors Register (CAL_VECTOR)

7	6	5	4	3	2	1	0
			CAL_	DATA			
			R/W-00	00 0000			

Table 68. CAL_VECTOR Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	CAL_DATA	R/W	0000 0000	Repeated reads of this register outputs all the calibration register values for analysis if the CALIBRATION_READ_WRITE_EN bit is set. Repeated writes of this register inputs all the calibration register values for configuration if the CAL_RD_EN bit is set.

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7.6.1.6.6 Calibration Status Register (address = 0x05B) [reset = undefined]

Figure 92.	Calibration	Status	Register	(CAL_	_STAT)
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7	6	5	4	3	2	1	0
		RE	SERVED			CAL_CONT_OFF	FIRST_CAL_DONE
		R-	0000 10			R-X	R-X

Table 69. CAL_STAT Field Descriptions

Bit	Field	Туре	Reset	Description
7-2	RESERVED	R	0000 10XX	
1	CAL_CONT_OFF	R	x	After clearing CAL_CONT, calibration does not stop immediately. Use this register to confirm it has stopped before changing calibration settings. 0: Indicates calibration is running (foreground or background) 1: Indicates that calibration is finished or stopped because CAL_CONT = 0
0	FIRST_CAL_DONE	R	Х	Indicates first calibration sequence has been done and ADC is operational.

7.6.1.6.7 Timing Calibration Register (address = 0x066) [reset = 0x02]

Figure 93. Timing Calibration Register (T_CAL)

7	6	5	4	3	2	1	0
RESERVED						T_AUTO	
R/W-0000 001							R/W-0

Table 70. CAL_STAT Field Descriptions

Bit	Field	Туре	Reset	Description
7-1	RESERVED	R/W	0000 001	Set to 0000001b
0	T_AUTO	R/W	0	Set to enable automatic timing optimization. Timing calibration will occur once CAL_SFT is set.
7.6.1.7 Digital Down Converter and JESD204B (0x200-0x27F)

		U	<u> </u>	
Address	Reset	Acronym	Register Name	Section
0x200	0x10	DDC_CTRL1	Digital Down-Converter (DDC) Control	Go
0x201	0x0F	JESD_CTRL1	JESD204B Control 1	Go
0x202	0x00	JESD_CTRL2	JESD204B Control 2	Go
0x203	0x00	JESD_DID	JESD204B Device ID (DID)	Go
0x204	0x00	JESD_CTRL3	JESD204B Control 3	Go
0x205	Undefined	JESD_STATUS	JESD204B and System Status Register	Go
0x206	0xF2	OVR_T0	Overrange Threshold 0	Go
0x207	0xAB	OVR_T1	Overrange Threshold 1	Go
0x208	0x00	OVR_N	Overrange Period	Go
0x209-0x20B	0x00	RESERVED	RESERVED	
0x20C	0x00	NCO_MODE	DDC Configuration Preset Mode	Go
0x20D	0x00	NCO_SEL	DDC Configuration Preset Select	Go
0x20E-0x20F	0x0000	NCO_RDIV	Rational NCO Reference Divisor	Go
0x210-0x213	0xC0000000	NCO_FREQ0	NCO Frequency (Preset 0)	Go
0x214-0x215	0x0000	NCO_PHASE0	NCO Phase (Preset 0)	Go
0x216	0xFF	DDC_DLY0	DDC Delay (Preset 0)	Go
0x217	0x00	RESERVED	RESERVED	
0x218-0x21B	0xC0000000	NCO_FREQ1	NCO Frequency (Preset 1)	Go
0x21C-0x21D	0x0000	NCO_PHASE1	NCO Phase (Preset 1)	Go
0x21E	0xFF	DDC_DLY1	DDC Delay (Preset 1)	Go
0x21F	0x00	RESERVED	RESERVED	
0x220-0x223	0xC0000000	NCO_FREQ2	NCO Frequency (Preset 2)	Go
0x224-0x225	0x0000	NCO_PHASE2	NCO Phase (Preset 2)	Go
0x226	0xFF	DDC_DLY2	DDC Delay (Preset 2)	Go
0x227	0x00	RESERVED	RESERVED	
0x228-0x22B	0xC0000000	NCO_FREQ3	NCO Frequency (Preset 3)	Go
0x22C-0x22D	0x0000	NCO_PHASE3	NCO Phase (Preset 3)	Go
0x22E	0xFF	DDC_DLY3	DDC Delay (Preset 3)	Go
0x22F	0x00	RESERVED	RESERVED	
0x230-0x233	0xC0000000	NCO_FREQ4	NCO Frequency (Preset 4)	Go
0x234-0x235	0x0000	NCO PHASE4	NCO Phase (Preset 4)	Go
0x236	0xFF	DDC DLY4	DDC Delay (Preset 4)	Go
0x237	0x00	RESERVED	RESERVED	
0x238-0x23B	0xC0000000	NCO FREQ5	NCO Frequency (Preset 5)	Go
0x23C-0x23D	0x0000	NCO PHASE5	NCO Phase (Preset 5)	Go
0x23E	0xFF	DDC DLY5	DDC Delay (Preset 5)	Go
0x23F	0x00	RESERVED	RESERVED	
0x240-0x243	0xC0000000	NCO FREQ6	NCO Frequency (Preset 6)	Go
0x244-0x245	0x0000	NCO_PHASE6	NCO Phase (Preset 6)	Go
0x246	OxFE		DDC Delay (Preset 6)	Go
0x247	0x00	BESERVED	RESERVED	
0x247	0x00			Go
	0x0000		NCO Phase (Preset 7)	60
0x240	0.000			60
				60
0x24F-0X251	UXUU			
0x252-0x27F	Undefined	RESERVED	RESERVED	

Table 71. Digital Down Converter and JESD204B Registers

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7.6.1.7.1 Digital Down-Converter (DDC) Control Register (address = 0x200) [reset = 0x10]

7	6	5	4	3	2	1	0
RESEF	RVED	SFORMAT	DDC GAIN BOOST		DM	ODE	
R/W-	·00	R/W-0	R/W-1		R/W-	0000	

Figure 94. Digital Down-Converter (DDC) Control Register (DDC_CTRL1)

Table 72. DDC_CTRL1 Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	RESERVED	R/W	00	
5	SFORMAT	R/W	0	Output sample format for bypass mode: 0 : Offset binary (default) 1 : Signed 2s complement ⁽¹⁾
4	DDC GAIN BOOST	R/W	1	0 : Final filter has 0-dB gain (recommended when NCO is set near DC). 1 : Final filter has 6.02-dB gain (default)
3-0	DMODE ⁽²⁾	R/W	0000	0 : Bypass mode (12-bit output, decimate-by-1, DDC off) (default) 1 : Reserved 2 : decimate-by-4 3 : decimate-by-8 4 : decimate-by-10 5 : decimate-by-16 6 : decimate-by-20 7 : decimate-by-32 815 : RESERVED

(1) Decimated modes always output in signed 2s complement.

(2) The DMODE setting must only be changed when JESD_EN is 0.

7.6.1.7.2 JESD204B Control 1 Register (address = 0x201) [reset = 0x0F]

Figure 95. JESD204B Control 1 Register (JESD_CTRL1)

7	6	5	4	3	2	1	0
SCR			DDR	JESD_EN			
R/W-0			R/W-1	R/W-1			

Table 73. JESD_CTRL1 Field Descriptions

Bit	Field	Туре	Reset	Description
7	SCR	R/W	0	0 : Scrambler disabled (default) 1 : Scrambler enabled
6-2	K_Minus_1	R/W	000 11	K is the number of frames per multiframe, and $K - 1$ is programmed here. Default: $K = 4$, K _Minus_1 = 3. Depending on the decimation (D) and serial rate (DDR), there are constraints on the legal values of K.
1	DDR	R/W	1	0 : SDR serial rate $(f_{(B T)} = f_S)$ 1 : DDR serial rate $(f_{(B T)} = 2f_S)$ (default)
0	JESD_EN ⁽¹⁾	R/W	1	0 : Block disabled 1 : Normal operation (default)

(1) Before altering any parameters in the JESD_CTRL1 register, you must set JESD_EN to 0. When JESD_EN is 0, the block is held in reset and the serializers are powered down. The clocks are gated off to save power.



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7.6.1.7.3 JESD204B Control 2 Register (address = 0x202) [reset = 0x00]

7	6	5	4	3 2 1 0				
P54	SYNC_DIFFSEL	RESER	/ED	JESD204B_TEST				
R/W-	-0 R/W-0 R/W-00			R/W-0000				
		Table 74. J	ESD_CTR	L2 Field Descriptions				
Bit	Field	Туре	Reset	Description				
7	P54		0	 0 : Disable 5/4 PLL. Serial bit rate is 1x or 2x based on DDF parameter. 1 : Enable 5/4 PLL. Serial bit rate is 1.25x or 2.5x based on DDR parameter. 	R			
6	SYNC_DIFFSEL		0	0 : Use SYNC_SE_N input for SYNC_N function 1 : Use SYNC_DIFF_N input for SYNC_N function				
5-4	RESERVED	R/W	00	Set to 00b				
3-0	JESD204B_TEST ⁽¹⁾	R/W	0000	See 0 : Test mode disabled. Normal operation (default) 1 : PRBS7 test mode 2 : PRBS15 test mode 3 : PRBS23 test mode 4 : Ramp test mode 5 : Short and long transport layer test mode 6 : D21.5 test mode 7 : K28.5 test mode 8 : Repeated ILA test mode 9 : Modified RPAT test mode 10: Serial outputs held low 11: Serial outputs held high 12 through 15 : RESERVED				

Figure 96. JESD204B Control 2 Register (JESD_CTRL2)

(1) The JESD_CTRL2 register must only be changed when JESD_EN is 0.

7.6.1.7.4 JESD204B Device ID (DID) Register (address = 0x203) [reset = 0x00]

Figure 97. JESD204B Device ID (DID) Register (JESD_DID)

7	6	5	4	3	2	1	0	
	JESD_DID							
 R/W-0000 0000								

Table 75. JESD_DID Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	JESD_DID ⁽¹⁾	R/W	0000 0000	Specifies the DID value that is transmitted during the second multiframe of the JESD204B ILA.

(1) The DID setting must only be changed when JESD_EN is 0.

7.6.1.7.5 JESD204B Control 3 Register (address = 0x204) [reset = 0x00]

Figure 98. JESD204B Control 3 Register (JESD_CTRL3)

7	6	5	4	3	2	1	0
RESERVED						FCI	HAR
	R/W-0000 00						V-00

Table 76. JESD_CTRL3 Field Descriptions

Bit	Field	Туре	Reset	Description
7-2	RESERVED	R/W	0000 00	
1-0	FCHAR ⁽¹⁾	R/W	00	Specify which comma character is used to denote end-of-frame. This character is transmitted opportunistically according to JESD204B Section 5.3.3.4. When using a JESD204B receiver, always use FCHAR=0. When using a general purpose 8-b or 10-b receiver, the K28.7 character can cause issues. When K28.7 is combined with certain data characters, a false, misaligned comma character can result, and some receivers realign to the false comma. To avoid this, program FCHAR to 1 or 2. 0 : Use K28.7 (default) (JESD204B compliant) 1 : Use K28.1 (not JESD204B compliant) 2 : Use K28.5 (not JESD204B compliant) 3 : Reserved

(1) The JESD_CTRL3 register must only be changed when JESD_EN is 0.

7.6.1.7.6 JESD204B and System Status Register (address = 0x205) [reset = Undefined]

See the JESD204B Synchronization Features section for more details.

Figure 99. JESD204B and System Status Register (JESD_STATUS)

7	6	5	4	3	2	1 0
RESERVED	LINK_UP	SYNC_STATUS	REALIGNED	ALIGNED	PLL_LOCKED	RESERVED
R/W-0	R/W-0	R/W-X	R/W-X	R/W-0	R/W-0	R/W-00

Table 77. JESD_STATUS Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R/W	0	Always returns 0
6	LINK_UP	R/W	0	When set, indicates that the JESD204B link is in the DATA_ENC state.
5	SYNC_STATUS	R/W	x	Returns the state of the JESD204B SYNC~ signal (SYNC_SE_N or SYNC_DIFF_N). 0 : SYNC~ asserted 1 : SYNC~ deasserted
4	REALIGNED	R/W	x	When high, indicates that the div8 clock, frame clock, or multiframe clock phase was realigned by SYSREF. Writing a 1 to this bit clears it.
3	ALIGNED	R/W	0	When high, indicates that the multiframe clock phase has been established by SYSREF. The first SYSREF event after enabling the JESD204B encoder will set this bit. Writing a 1 to this bit clears it.
2	PLL_LOCKED	R/W	0	When high, indicates that the PLL is locked.
1-0	RESERVED	R/W	0	Always returns 0



7.6.1.7.7 Overrange Threshold 0 Register (address = 0x206) [reset = 0xF2]

Figure 100. Overrange Threshold 0 Register (OVR_T0)

7	6	5	4	3	2	1	0		
OVR_T0									
R/W-1111 0010									
		Table	78. OVR T0	Field Descrip	otions				

BitFieldTypeResetDescription7-0 OVR_T0 R/W1111 0010Over-range threshold 0. This parameter defines the absolute
sample level that causes control bit 0 to be set. Control bit 0 is
attached to the DDC I output samples. The detection level in
dBFS (peak) is
 $20_{log10}(OVR_T0 / 256)$
Default: $0xF2 = 242 \rightarrow -0.5$ dBFS

7.6.1.7.8 Overrange Threshold 1 Register (address = 0x207) [reset = 0xAB]

Figure 101. Overrange Threshold 1 Register (OVR_T1)

7	6	5	4	3	2	1	0	
OVR_T1								
R/W-1010 1011								

Table 79. OVR_T1 Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	OVR_T1	R/W	1010 1011	Overrange threshold 1. This parameter defines the absolute sample level that causes control bit 1 to be set. Control bit 1 is attached to the DDC Q output samples. The detection level in dBFS (peak) is 20_{log10} (OVR_T1 / 256) Default: 0xAB = 171 \rightarrow -3.5 dBFS

7.6.1.7.9 Overrange Period Register (address = 0x208) [reset = 0x00]

Figure 102. Overrange Period Register (OVR_N)

7	6	5	4	3	2	1	0
		RESERVED				OVR_N	
	R/W-0000 0				R/W-000		

Table 80. OVR_N Field Descriptions

Bit	Field	Туре	Reset	Description
7-3	RESERVED	R/W	0000 0	
2-0	OVR_N ⁽¹⁾	R/W	000	This bit adjusts the monitoring period for the OVR[1:0] output bits. The period is scaled by 2^{OVR_N} . Incrementing this field doubles the monitoring period.

(1) Changing the OVR_N setting while JESD_EN=1 may cause the phase of the monitoring period to change.

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7.6.1.7.10 DDC Configuration Preset Mode Register (address = 0x20C) [reset = 0x00]

Figure 103. DDC Configuration Preset Mode Register (NCO_MODE)

7	6	5	4	3	2	1	0
RESERVED						CFG_MODE	
	R/W-0000 000						

Table 81. NCO_MODE Field Descriptions

Bit	Field	Туре	Reset	Description
7-1	RESERVED	R/W	0000 000	
0	CFG_MODE	R/W	0	The NCO frequency and phase are set by the NCO_FREQx and NCO_PHASEx registers, where <i>x</i> is the configuration preset (0 through 7). The DDC delay setting is defined by the DDC_DLYx register. 0 : Use NCO_[2:0] input pins to select the active DDC and NCO configuration preset. 1 : Use the NCO_SEL register to select the active DDC and NCO configuration preset.

7.6.1.7.11 DDC Configuration Preset Select Register (address = 0x20D) [reset = 0x00]

Figure 104. DDC Configuration Preset Select Register (NCO_SEL)

7	6	5	4	3	2	1	0		
RESERVED					NCO_SEL				
		R/W-0000 0			R/W-000				

Table 82. NCO_SEL Field Descriptions

Bit	Field	Туре	Reset	Description
7-3	RESERVED	R/W	0000 0	
2-0	NCO_SEL	R/W	000	When NCO_MODE = 1, this register is used to select the active configuration preset.



7.6.1.7.12 Rational NCO Reference Divisor Register (address = 0x20E to 0x20F) [reset = 0x0000]

15	14	13	12	11	10	9	8	
NCO_RDIV								
R/W-0x00h								
7	6	5	4	3	2	1	0	
NCO_RDIV								

Figure 105. Rational NCO Reference Divisor Register (NCO_RDIV)

Table 83. NCO_RDIV Field Descriptions

Bit	Field	Туре	Reset	Description		
15-0	NCO_RDIV	R/W	0x0000h	Sometimes the 32-bit NCO frequency word does not provide the desired frequency step size and can only approximate the desired frequency. This results in a frequency error. Use this register to eliminate the frequency error. Use this equation to compute the proper value to program:		
				NCO_RDIV = $f_S / f_{(STEP)} / 128$		
				where		
				 <i>f</i>_S is the ADC sample rate 		
				 f_(STEP) is the desired NCO frequency step size 		
				(10)		
				For example, if f_{S} = 3072 MHz, and $f_{(STEP)}$ = 10 KHz then:		
				NCO_RDIV = 3072 MHz / 10 KHz / 128 = 2400 (11)		
				Any combination of $f_{\rm S}$ and $f_{\rm (STEP)}$ that results in a fractional value for NCO_RDIV is not supported. Values of NCO_RDIV larger than 8192 can degrade the NCO's SFDR performance and are not recommended. This register is used for all configuration presets.		

7.6.1.7.13 NCO Frequency (Preset x) Register (address = see Table 71) [reset = see Table 71]

31	30	29	28	27	26	25	24			
NCO_FREQ_x										
R/W-0xC0h										
23	22	21	20	19	18	17	16			
	NCO_FREQ_x									
			R/W-0	0x00h						
15	14	13	12	11	10	9	8			
			NCO_F	REQ_x						
			R/W-0	0x00h						
7	6	5	4	3	2	1	0			
			NCO_F	REQ_x						
			R/W-0	Dx00h						

Figure 106. NCO Frequency (Preset x) Register (NCO_FREQ_x)

Table 84. NCO_FREQ_x Field Descriptions

Bit	Field	Туре	Reset	Description
31-0	NCO_FREQ_x	R/W	0xC00000 00h	Changing this register after the JESD204B interface is running results in non-deterministic NCO phase. If deterministic phase is required, the JESD204B interface must be re-initialized after changing this register. The NCO frequency ($f_{(NCO)}$) is: $f_{(NCO)} = NCO_FREQ_x \times 2^{-32} \times f_S$
				where
				• <i>f</i> _S is the sampling frequency of the ADC
				NCO_FREQ_x is the integer value of this register (12)
				This register can be interpreted as signed or unsigned. Use this equation to determine the value to program:
				$NCO_FREQ_x = 2^{32} \times f_{(NCO)} / f_{S} $ (13)
				If the equation does not result in an integer value, you must choose an alternate frequency step ($f_{(STEP)}$) and program the NCO_RDIV register. Then use one of the following equations to compute NCO_FREQ_x:
				NCO_FREQ_x = round($2^{32} \times f_{(NCO)} / f_S$) (14)
				NCO_FREQ_x = round($2^{25} \times f_{(NCO)} / f_{(STEP)} / NCO_RDIV$) (15)



7.6.1.7.14 NCO Phase (Preset x) Register (address = see Table 71) [reset = see Table 71]

15	14	13	12	11	10	9	8		
NCO_PHASE_x									
R/W-0x00h									
7	6	5	4	3	2	1	0		
NCO_PHASE_x									
	R/W-0x00h								

Figure 107. NCO Phase (Preset) Register (NCO_PHASE_x)

R/W-0x00h

Table 85. NCO_PHASE_x Field Descriptions	
--	--

Bit	Field	Туре	Reset	Description	
15-0	NCO_PHASE_x	R/W	0x0000h	This value is MSB-justified into a 32-bit field and then adde the phase accumulator. The phase (in radians) is NCO_PHASE_x × 2^{-16} × 2π This register can be interpreted as signed or unsigned.	ed to (16)

7.6.1.7.15 DDC Delay (Preset x) Register (address = see Table 71) [reset = see Table 71]

Figure 108. DDC Delay (Preset) Register (DDC_DLY_x)

7	6	5	4	3	2	1	0	
DDC_DLY_x								
R/W-0xFFh								

Table 86. DDC_DLY_x Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	DDC_DLY_x	R/W	0xFFh	DDC delay for configuration preset 0 This register provides fine adjustments to the DDC group delay. The step size is one half of an ADC sample period ($t_{(DEVCLK)}$ / 2). This is equivalent to Equation 17.
				t _o / (2 × D)
				where
				 t_o is the DDC output sample period
				• D is the decimation factor (17)
				The legal range for this register is 0 to 2D-1. Illegal values result in undefined behavior. Example: When D = 8, the legal register range is 0 to 15. The step size is $t_0 / 16$ and the maximum delay is $15 \times t_0 / 16$. Programming this register to 0xFF (the default value) powers down and bypasses the fractional delay filter which reduces the DDC latency by 34 ADC sample periods (as compared to the 0 setting).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ADC12J1600 and ADC12J2700 devices are a wideband sampling and digital tuning device. The ADC input captures input signals from DC to greater than 3 GHz. The DDC performs digital-down conversion and programmable decimation filtering, and outputs complex (15 bit I and 15 bit Q) data. In DDC Bypass Mode (Decimation = 1) the raw 12 bit ADC data is also available. The resulting output data is output on the JESD204B data interface for capture by the downstream capture or processing device. Most frequency-domain applications benefit from DDC capability to select the desired frequency band and provide only the necessary bandwidth of output data, minimizing the required number of data signals. Time domain applications generally require the raw 12-bit ADC output data provided by the DDC bypass feature.

8.2 Typical Application

8.2.1 RF Sampling Receiver

An RF Sampling Receiver is used to directly sample a signal in the RF frequency range and provide the data for the captured signal to downstream processing. The wide input bandwidth, high sampling rate, and DDC features of the ADC12J1600 and ADC12J2700 make them ideally suited for this application.



Figure 109. Simplified Schematic



Typical Application (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 87.

DESIGN PARAMETERS	EXAMPLE VALUES
Signal center frequency	2500 MHz
Signal bandwidth	100 MHz
Signal nominal amplitude	–7 dBm
Signal maximum amplitude	6 dBm
Minimum SINAD (in bandwidth of interest)	48 dBc
Minimum SFDR (in bandwidth of interest)	60 dBc

Table 87. Design Parameters

8.2.1.2 Detailed Design Procedure

Use the following steps to design the RF receiver:

- Use the signal-center frequency and signal bandwidth to select an appropriate sampling rate (DEVCLK frequency) and decimate factor (x / 4 to x / 32).
- Select the sampling rate so that the band of interest is completely within a Nyquist zone.
- Select the sampling rate so that the band of interest is away from any harmonics or interleaving tones.
- Use a frequency planning tool, such as the ADC harmonic calculator (see the *Development Support* section).
- Select the decimation factor that provides the highest factor possible with an adequate alias-protected output bandwidth to capture the frequency bandwidth of interest.
- Select other system components to provide the needed signal frequency range and DEVCLK rate.
- See Table 1 for recommended balun components.
- Select bandpass filters and limiter components based on the requirement to attenuate unwanted signals outside the band of interest (blockers) and to prevent large signals from damaging the ADC inputs. See the *Absolute Maximum Ratings* table.

The LMK048xx JESD204B clocking devices can provide the DEVCLK clock and other system clocks for $f_{(DEVCLK)}$ < 3101 MHz.

For DEVCLK frequencies up to 4 GHz the consider using the LMX2581 and TRF3765 devices as the DEVCLK source. Use the LMK048xx device to provide the JESD204B clocks. For additional device information, see the *Related Documentation* section.

8.2.1.3 Application Curves

The following curves show an RF signal at 2497.97 MHz captured at a sample rate of 1600 MSPS. Figure 110 shows the spectrum for the full Nyquist band. Figure 111 shows the spectrum for the output data in decimate-by-32 mode with $f_{(NCO)}$ equal to 700 MHz. Figure 111 shows the ability to provide only the spectrum of interest in the decimated output data. Figure 111 also shows how proper selection of the sampling rate can ensure interleaving tones are outside the band of interest and outside the decimated frequency range. Lastly, Figure 111 shows the reduction in the noise floor provided by the processing gain of decimation.

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8.2.2 Oscilloscope

The ADC12J1600 and ADC12J2700 devices are equally well-suited for high-speed time-domain applications such as oscilloscopes. The following typical application is for a generic high-speed oscilloscope. Adjustable gain is provided by the front-end resistor ladder and selection mux, and the gain adjustments of the LMH6518 device. Additional gain fine-tuning can be achieved using the full-scale range adjustment features of the ADC.







8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 88.

Table ou. Design Falameters	Tabl	e 88.	Design	Parameters
-----------------------------	------	-------	--------	-------------------

DESIGN PARAMETERS	EXAMPLE VALUES
Maximum sample rate	1600 MSPS
Maximum input frequency	1500 MHz
1-dB flat-frequency range	0 to 1000 MHz
Signal maximum amplitude	6 dBm
Signal minimum amplitude	48 dBc
Maximum capture depth	1 million points

8.2.2.2 Detailed Design Procedure

Use the following primary steps to design a 12-bit oscilloscope:

- Select the desired sampling rate based on the maximum sampling-rate requirement.
- Select the input path components (LNA, amplifier, and other components) based on the maximum input frequency and 1-dB flat-frequency range requirements.
- Set the attenuation range steps based on the required minimum and maximum values for the signal amplitude.
- Select the memory size based on the resolution of the ADC output (12 bits) and the required maximum number of sample points.

8.2.2.3 Application Curves

The following curves show the time-domain sample data for a 150-MHz input signal at -1 dBFS, sampled at 1600 MSPS using the ADC12J1600 device. Figure 113 shows the raw time-domain data. Figure 114 shows the spectrum of the captured signal which shows the additional capability of a 12-bit ADC oscilloscope to provide basic spectrum-analysis functions with reasonable performance.





8.3 Initialization Set-Up

8.3.1 JESD204B Startup Sequence

The JESD204B interface requires a specific startup and alignment sequence. The general order of that sequence is listed in the following steps.

- 1. Power up or reset the ADC12J1600 and ADC12J2700 devices.
- 2. Program JESD_EN = 0 to shut down the link and enable configuration changes.
- 3. Program DECIMATE, SCRAM_EN, KM1 and DDR to the desired settings.
- 4. Configure the device calibration settings as desired, and initiate a calibration (set CAL_SFT = 1).
- 5. Program JESD_EN = 1 to enable the link.
- 6. Apply at least one SYSREF rising edge to establish the LMFC phase.
- 7. Assert SYNC~ from the data receiver to initiate link communications.
- 8. After the JESD204B receiver has established code group synchronization, SYNC~ is de-asserted and the ILA process begins.
- 9. Immediately following the end of the ILA sequence normal data output begins.

NOTE

If deterministic latency is not required this step can be omitted.

8.4 Dos and Don'ts

8.4.1 Common Application Pitfalls

Driving the inputs (analog or digital) beyond the power supply rails. For device reliability, an input must not go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits even on a transient basis can cause faulty, or erratic, operation and can impair device reliability. High-speed digital circuits exhibiting undershoot that goes more than a volt below ground is common. To control overshoot, the impedance of high-speed lines must be controlled and these lines must be terminated in the characteristic impedance.

Care must be taken not to overdrive the inputs of the ADC12J1600 and ADC12J2700 devices. Such practice can lead to conversion inaccuracies and even to device damage.

Incorrect analog input common-mode voltage in the DC-coupled mode. As described in the *The Analog Inputs* and *DC Coupled Input Usage* sections, the input common-mode voltage (V_{CMI}) must remain the specified range as referenced to the VCMO pin, which has a variability with temperature that must also be tracked. Distortion performance is degraded if the input common mode voltage is outside the specified V_{CMI} range.

Using an inadequate amplifier to drive the analog input. Use care when choosing a high frequency amplifier to drive the ADC12J1600 and ADC12J2700 devices because many high-speed amplifiers have higher distortion than the ADC12J1600 and ADC12J2700 devices which results in overall system performance degradation.

Driving the clock input with an excessively high level signal. The ADC input clock level must not exceed the level described in the *Recommended Operating Conditions* table because the input offset can change if these levels are exceeded.

Inadequate input clock levels. As described in the *Using the Serial Interface* section, insufficient input clock levels can result in poor performance. Excessive input-clock levels can result in the introduction of an input offset.

Using a clock source with excessive jitter, using an excessively long input clock signal trace, or having other signals coupled to the input clock signal trace. These pitfalls cause the sampling interval to vary which causes excessive output noise and a reduction in SNR performance.

Failure to provide adequate heat removal. As described in the *Thermal Management* section, providing adequate heat removal is important to ensure device reliability. Adequate heat removal is primarily provided by properly connecting the thermal pad to the circuit board ground planes. Multiple vias should be arranged in a grid pattern in the area of the thermal pad. These vias will connect the topside pad to the internal ground planes and to a copper pour area on the opposite side of the printed circuit board.

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9 Power Supply Recommendations

Data-converter-based systems draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A $10-\mu$ F capacitor must be placed within one inch (2.5 cm) of the device power pins for each supply voltage. A $0.1-\mu$ F capacitor must be placed as close as possible to each supply pin, preferably within 0.5 cm. Leadless chip capacitors are preferred due to their low-lead inductance.

As is the case with all high-speed converters, the ADC12J1600 and ADC12J2700 devices must be assumed to have little power-supply noise-rejection. Any power supply used for digital circuitry in a system where a large amount of digital power is consumed must not be used to supply power to the ADC12J1600 and ADC12J2700 devices. If not a dedicated supply, the ADC supplies must be the same supply used for other analog circuitry.

9.1 Supply Voltage

The ADC12J1600 and ADC12J2700 devices are specified to operate with nominal supply voltages of 1.9 V (VA19) and 1.2 V (VA12, VD12). For detailed information regarding the operating voltage minimums and maximums see the *Recommended Operating Conditions* table.

During power-up the voltage on all 1.9-V supplies must always be equal to or greater than the voltage on the 1.2-V supplies. Similarly, during power-down, the voltage on the 1.2-V supplies must always be lower than or equal to that of the 1.9-V supplies. In general, supplying all 1.9-V buses from a single regulator, and all 1.2-V buses from a single regulator is the easiest method to ensure that the 1.9-V supplies are greater than the 1.2-V supplies. If the 1.2-V buses are generated from separate regulators, they must rise and fall together (within 200 mV).

The voltage on a pin, including a transient basis, must not have a voltage that is in excess of the supply voltage or below ground by more than 150 mV. A pin voltage that is higher than the supply or that is below ground can be a problem during startup and shutdown of power. Ensure that the supplies to circuits driving any of the input pins, analog or digital, do not rise faster than the voltage at the ADC12J1600 and ADC12J2700 power pins.

The values in the *Absolute Maximum Ratings* table must be strictly observed including during power up and power down. A power supply that produces a voltage spike at power turnon, turnoff, or both can destroy the ADC12J1600 and ADC12J2700 devices. Many linear regulators produce output spiking at power on unless there is a minimum load provided. Active devices draw very little current until the supply voltages reach a few hundred millivolts. The result can be a turn-on spike that destroys the ADC12J1600 and ADC12J2700 devices, unless a minimum load is provided for the supply. A 100- Ω resistor at the regulator output provides a minimum output current during power up to ensure that no turn-on spiking occurs. Whether a linear or switching regulator is used, TI recommends using a soft-start circuit to prevent overshoot of the supply.

10 Layout

10.1 Layout Guidelines

Proper grounding and proper routing of all signals is essential to ensure accurate conversion. Each ground layer should be a single unified ground plane, rather than splitting the ground planes into analog and digital areas.

Because digital switching transients are composed largely of high frequency components, the skin effect dictates that the total ground-plane copper weight has little effect upon the logic-generated noise. Total surface area is more important than the total ground-plane volume. Coupling between the typically-noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that can be impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High-power digital components must not be located on or near any linear component or power-supply trace or plane that services analog or mixed-signal components because the resulting common return current path could cause fluctuation in the analog input *ground* return of the ADC which causes excessive noise in the conversion result.

In general, assume that analog and digital lines must cross each other at 90° to avoid digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. The input clock lines must be isolated from **all** other lines, both analog and digital. The generally-accepted 90° crossing must be avoided because even a same amount of coupling causes problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

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Layout Guidelines (continued)

Coupling onto or between the clock and input signal paths must be avoided using any isolation techniques available including distance isolation, orientation planning to prevent field coupling of components like inductors and transformers, and providing well coupled reference planes. Via stitching around the clock signal path and the input analog signal path provides a quiet ground reference for the critical signal paths and reduces noise coupling onto these paths. Sensitive signal traces must not cross other signal traces or power routing on adjacent PCB layers, rather a ground plane must separate the traces. If necessary, the traces should cross at 90° angles to minimize crosstalk.

Isolation of the analog input is important because of the low-level drive required of the ADC12J1600 and ADC12J2700 devices. Quality analog input signal and clock signal path layout is required for full dynamic performance. Symmetry of the differential signal paths and discrete components in the path is mandatory and symmetrical shunt-oriented components should have a common grounding via. The high frequency requirements of the input and clock signal paths necessitate using differential routing with controlled impedances and minimizing signal path stubs (including vias) when possible.

Layout of the high-speed serial-data lines is of particular importance. These traces must be routed as tightly coupled 100- Ω differential pairs, with minimal vias. When vias must be used, care must be taken to implement control-impedance vias (that is, 50- Ω) with adjacent ground vias for image current control.

10.2 Layout Example

The following examples show layout-example plots (top and bottom layers only). Figure 117 shows a typical stackup for a 10 layer board.



Figure 115. ADC12J1600 and ADC12J2700 Layout Example 1 — Top Side



Layout Example (continued)



Figure 116. ADC12J1600 and ADC12J2700 Layout Example 2 — Bottom Side







10.3 Thermal Management

The ADC12J1600 and ADC12J2700 devices are capable of impressive speeds and performance at low power levels for speed. However, the power consumption is still high enough to require attention to thermal management. The VQFN package has a primary-heat transfer path through the center pad on the bottom of the package. The thermal resistance of this path is provided as $R_{\theta,JCbot}$.

For reliability reasons, the die temperature must be kept to a maximum of 135° C which is the ambient temperature (T_A) plus the ADC power consumption multiplied by the net junction-to-ambient thermal resistance (R_{0JA}). Maintaining this temperature is not a problem if the ambient temperature is kept to a maximum of 85° C as specified in the *Recommended Operating Conditions* table and the center ground pad on the bottom of the package is thermally connected to a large-enough copper area of the PC board.

The package of the ADC12J1600 and ADC12J2700 devices have a center pad that provides the primary heatremoval path as well as excellent electrical grounding to the PCB. Recommended land pattern and solder paste examples are provided in the *Mechanical, Packaging, and Orderable Information* section. The center-pad vias shown must be connected to internal ground planes to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

If needed to further reduce junction temperature, TI recommends to build a simple heat sink into the PCB which occurs by including a copper area of about 1 to 2 cm² on the opposite side of the PCB. This copper area can be plated or solder-coated to prevent corrosion, but should not have a conformal coating which would provide thermal insulation. Thermal vias will be used to connect these top and bottom copper areas and internal ground planes. These thermal vias act as *heat pipes* to carry the thermal energy from the device side of the board to the opposite side of the board where the heat can be more effectively dissipated.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

For the ADC Harmonic Calculator, got to http://www.ti.com/tool/adc-harmonic-calc.

11.1.3 Device Nomenclature

- Aperture (sampling) Delay is the amount of delay, measured from the sampling edge of the clock input, after which the signal present at the input pin is sampled inside the device.
- Aperture Jitter (t_(AJ)) is the variation in aperture delay from sample to sample. Aperture jitter appears as input noise.
- Clock Duty Cycle is the ratio of the time that the clock waveform is at a logic high to the total time of one clock period.
- **Full Power Bandwidth (FPBW)** is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below the low frequency value for a full scale input.
- **Interleaving Spurs** are frequency domain (FFT) artifacts resulting from non-idealities in the multi-bank interleaved architecture of the ADC. Offset errors between banks result in fixed spurs at f_S / 4 and f_S / 2. Gain and timing errors result

in input-signal-dependent spurs at $f_S/4 \pm F_{IN}$ and $f_S/2 \pm F_{IN}$.

Intermodulation Distortion (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. IMD is defined as the ratio of the power in the second-order and third-order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.



(19)

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Device Support (continued)

Least Significant Bit (LSB) is the bit that has the smallest value or weight of all bits. This value is calculated with Equation 18.

V_{FS(dif)} / 2ⁿ

where

- V_{FS(dif)} is the differential full-scale amplitude of V_I as set by the FSR input (pin 14)
- *n* is the ADC resolution in bits, which is 12 for the ADC12J1600 and ADC12J2700 devices (18)

CML Differential Output Voltage (V_{OD}) is the absolute value of the difference between the positive and negative outputs. Each output is measured with respect to Ground.



CML Output Signal Levels

CML Output Offset Voltage (V_{O(ofs)}) is the midpoint between the D+ and D- pins output voltage. Equation 19 is an example of V_{OS}.

 $[(V_{D}+) + (V_{D}-)]/2$

- Most Significant Bit (MSB) is the bit that has the largest value or weight. The value of the MSB is one half of full scale.
- **Overrange Recovery Time** is the time required after the differential input voltages goes from ±1.2 V to 0 V for the converter to recover and make a conversion with its rated accuracy.
- Other Spurs is the sum of all higher harmonics (fourth and above), interleaving spurs, and any other fixed or input-dependent spurs.
- Data Delay (Latency) is the number of input clock cycles between initiation of conversion and when related data is present at the serializer output.
- **Spurious-free Dynamic Range (SFDR)** is the difference, expressed in dB, between the RMS values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding DC.
- **Total Harmonic Distortion (THD)** is the ratio expressed in dB, of the RMS total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated with Equation 20.

THD = 20 x log
$$\sqrt{\frac{A_{f2}^2 + ... + A_{f10}^2}{A_{f1}^2}}$$

where

- A_(f1) is the RMS power of the fundamental (output) frequency
- A_(f2) through A_(f10) are the RMS power of the first nine harmonic frequencies in the output spectrum (20)
- Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency detected at the output and the power in the second harmonic level at the output.
- **Third Harmonic Distortion (3rd Harm)** is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in the third harmonic level at the output.
- **Word Error Rate** is the probability of error and is defined as the probable number of errors per unit of time divided by the number of words seen in that amount of time. A Word Error Rate of 10⁻¹⁸ corresponds to a statistical error in one conversion about every four years.

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- LMH3401 7-GHz, Ultra-Wideband, Fixed-Gain, Fully-Differential Amplifier, SBOS695
- LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs, SNAS605
- LMX2581 Wideband Frequency Synthesizer with Integrated VCO, SNAS601
- TRF3765 Integer-N/Fractional-N PLL with Integrated VCO, SLWS230

11.3 Related Links

Below are direct links to information available to accelerate design activity. Categories include technical information, community resources, design information, and quick access to sample or purchase once you have made a decision.

Parts	Product Folder	Sample & Buy	Technical Documents	Tools & Software	Support & Community
ADC12J1600	Click here	Click here	Click here	Click here	Click here
ADC12J2700	Click here	Click here	Click here	Click here	Click here

11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E[™] Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



26-Jun-2016

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
ADC12J1600NKE	ACTIVE	VQFN	NKE	68	168	Green (RoHS & no Sb/Br)	CU SN Call TI	Level-3-260C-168 HR	-40 to 85	ADC12J1600	Samples
ADC12J1600NKER	ACTIVE	VQFN	NKE	68	2000	Green (RoHS & no Sb/Br)	CU SN Call TI	Level-3-260C-168 HR	-40 to 85	ADC12J1600	Samples
ADC12J1600NKET	ACTIVE	VQFN	NKE	68	250	Green (RoHS & no Sb/Br)	CU SN Call TI	Level-3-260C-168 HR	-40 to 85	ADC12J1600	Samples
ADC12J2700NKE	ACTIVE	VQFN	NKE	68	168	Green (RoHS & no Sb/Br)	CU SN Call TI	Level-3-260C-168 HR	-40 to 85	ADC12J2700	Samples
ADC12J2700NKER	ACTIVE	VQFN	NKE	68	2000	Green (RoHS & no Sb/Br)	CU SN Call TI	Level-3-260C-168 HR	-40 to 85	ADC12J2700	Samples
ADC12J2700NKET	ACTIVE	VQFN	NKE	68	250	Green (RoHS & no Sb/Br)	CU SN Call TI	Level-3-260C-168 HR	-40 to 85	ADC12J2700	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



PACKAGE OPTION ADDENDUM

26-Jun-2016

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	
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Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC12J1600NKET	VQFN	NKE	68	250	178.0	24.4	10.3	10.3	1.1	16.0	24.0	Q1

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PACKAGE MATERIALS INFORMATION

25-Aug-2016



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC12J1600NKET	VQFN	NKE	68	250	213.0	191.0	55.0

NKE0068A



PACKAGE OUTLINE

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NKE0068A

EXAMPLE BOARD LAYOUT

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

 This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



NKE0068A

EXAMPLE STENCIL DESIGN

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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