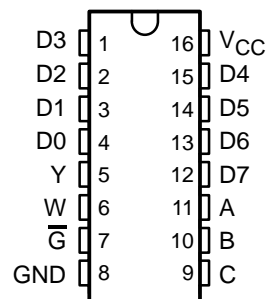


# CD54ACT151, CD74ACT151 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCHS338 – MARCH 2003

- Inputs Are TTL-Voltage Compatible
- 8-Line to 1-Line Multiplexers Can Perform as:
  - Boolean Function Generators
  - Parallel-to-Serial Converters
  - Data Source Selectors
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- $\pm 24$ -mA Output Drive Current
  - Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54ACT151 . . . F PACKAGE  
CD74ACT151 . . . M PACKAGE  
(TOP VIEW)



## description/ordering information

These data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe ( $\bar{G}$ ) input must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC – M	Tape and reel		
–55°C to 125°C	SOIC – M	Tape and reel	CD74ACT151M96	ACT151M
	CDIP – F	Tube	CD54ACT151F3A	CD54ACT151F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE $\bar{G}$	Y	W
C	B	A			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

D0, D1 . . . D7 = the level of the respective D input



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

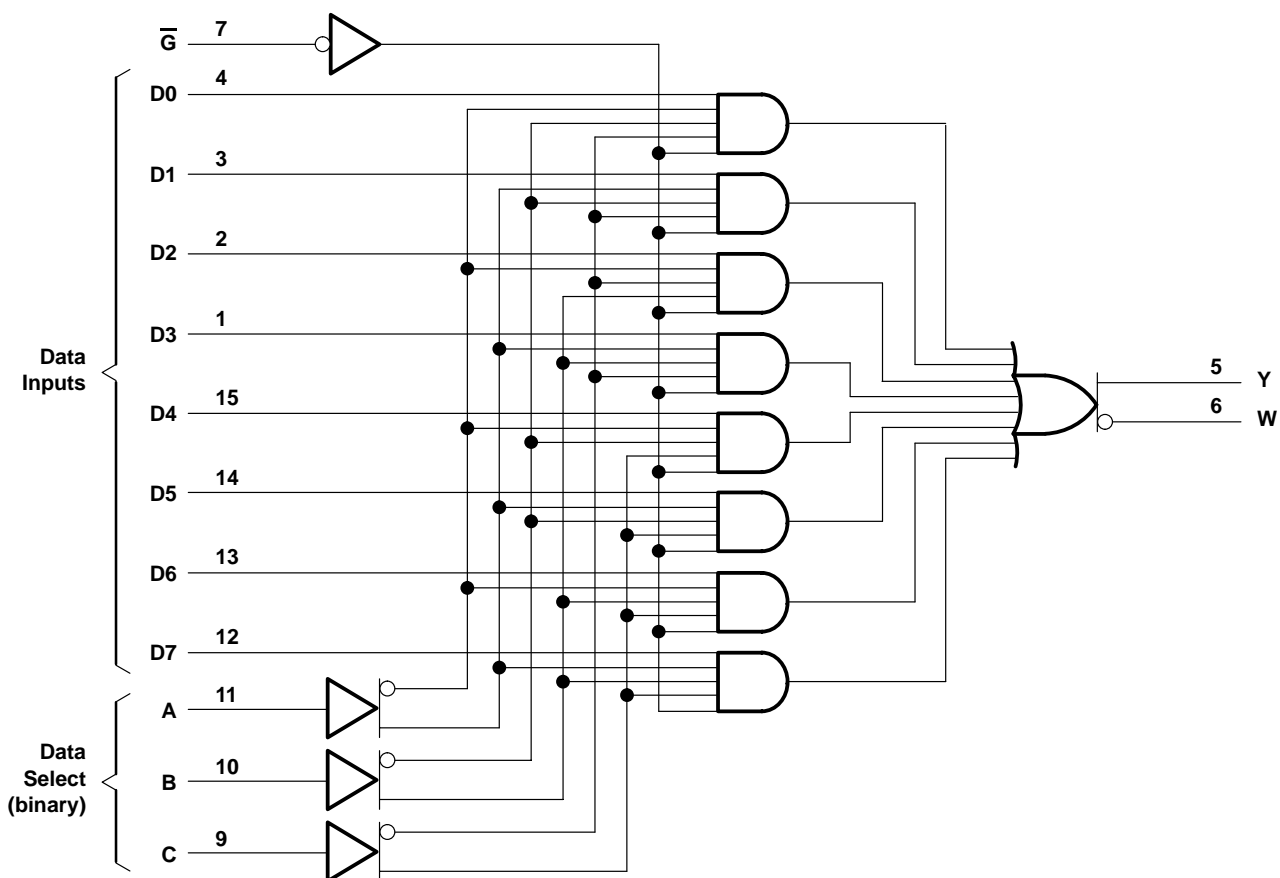
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# CD54ACT151, CD74ACT151 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCHS338 – MARCH 2003

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 6 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ V or $V_I > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ V or $V_O > V_{CC}$ ) (see Note 1)	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O > 0$ V or $V_O < V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2)	73°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# CD54ACT151, CD74ACT151

## 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCHS338 – MARCH 2003

### recommended operating conditions (see Note 3)

		T <sub>A</sub> = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		–24		–24		–24	mA
I <sub>OL</sub>	Low-level output current		24		24		24	mA
Δt/Δv	Input transition rise or fall rate		10		10		10	ns/V

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = –50 μA	4.5 V	4.4		4.4		4.4	V	
		I <sub>OH</sub> = –24 mA	4.5 V	3.94		3.7		3.8		
		I <sub>OH</sub> = –50 mA†	5.5 V			3.85				
		I <sub>OH</sub> = –75 mA†	5.5 V					3.85		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	4.5 V		0.1		0.1		V	
		I <sub>OL</sub> = 24 mA	4.5 V		0.36		0.5			0.44
		I <sub>OL</sub> = 50 mA†	5.5 V				1.65			
		I <sub>OL</sub> = 75 mA†	5.5 V					1.65		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		5.5 V		±0.1		±1		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		5.5 V		8		160		80	μA
ΔI <sub>CC</sub> ‡	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V		4.5 V to 5.5 V		2.4		3		2.8	mA
C <sub>i</sub>					10		10		10	pF

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

‡ Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

#### ACT INPUT LOAD TABLE

INPUT	UNIT LOAD
D	1
$\overline{G}$	1
A, B, or C	1

Unit Load is ΔI<sub>CC</sub> limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).



# CD54ACT151, CD74ACT151

## 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCHS338 – MARCH 2003

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

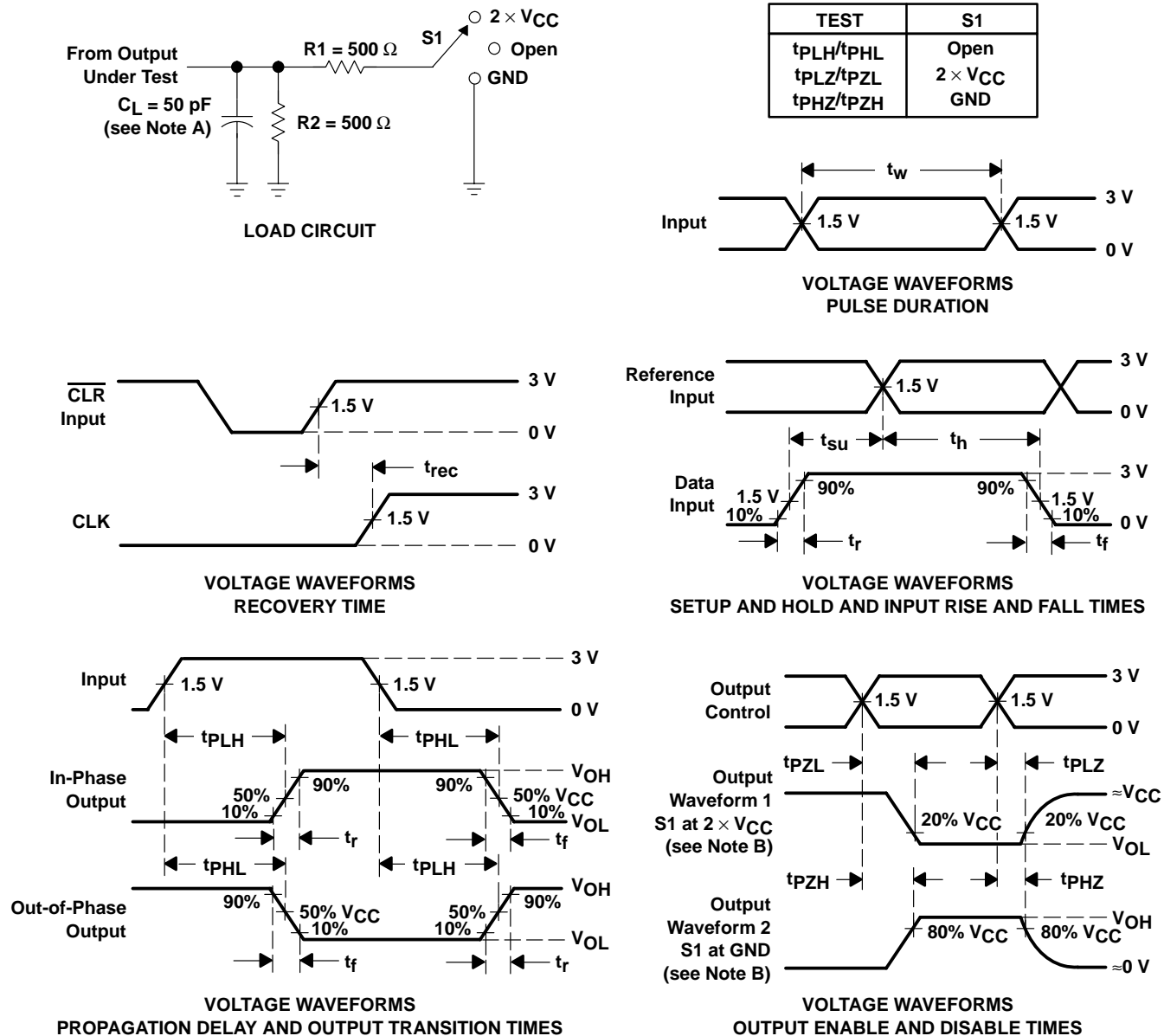
PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Y	3.9	15.5	4	14.1	ns
t <sub>PHL</sub>			3.9	15.5	4	14.1	
t <sub>PLH</sub>	D	W	4.2	16.9	4.4	15.4	ns
t <sub>PHL</sub>			4.2	16.9	4.4	15.4	
t <sub>PLH</sub>	A, B, or C	Y	5.1	20.2	5.2	18.4	ns
t <sub>PHL</sub>			5.1	20.2	5.2	18.4	
t <sub>PLH</sub>	A, B, or C	W	5.4	21.6	5.6	19.6	ns
t <sub>PHL</sub>			5.4	21.6	5.6	19.6	
t <sub>PLH</sub>	$\bar{G}$	Y	3	12.1	3.1	11	ns
t <sub>PHL</sub>			3	12.1	3.1	11	
t <sub>PLH</sub>	$\bar{G}$	W	3.4	13.5	3.5	12.3	ns
t <sub>PHL</sub>			3.4	13.5	3.5	12.3	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	120	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ . Phase relationships between waveforms are arbitrary.
  - For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
  - The outputs are measured one at a time with one input transition per measurement.
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54ACT151F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54ACT151F3A	<a href="#">Samples</a>
CD74ACT151M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT151M	<a href="#">Samples</a>
CD74ACT151M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT151M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54ACT151, CD74ACT151 :**

- Catalog: [CD74ACT151](#)
- Military: [CD54ACT151](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT151M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT151M96	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

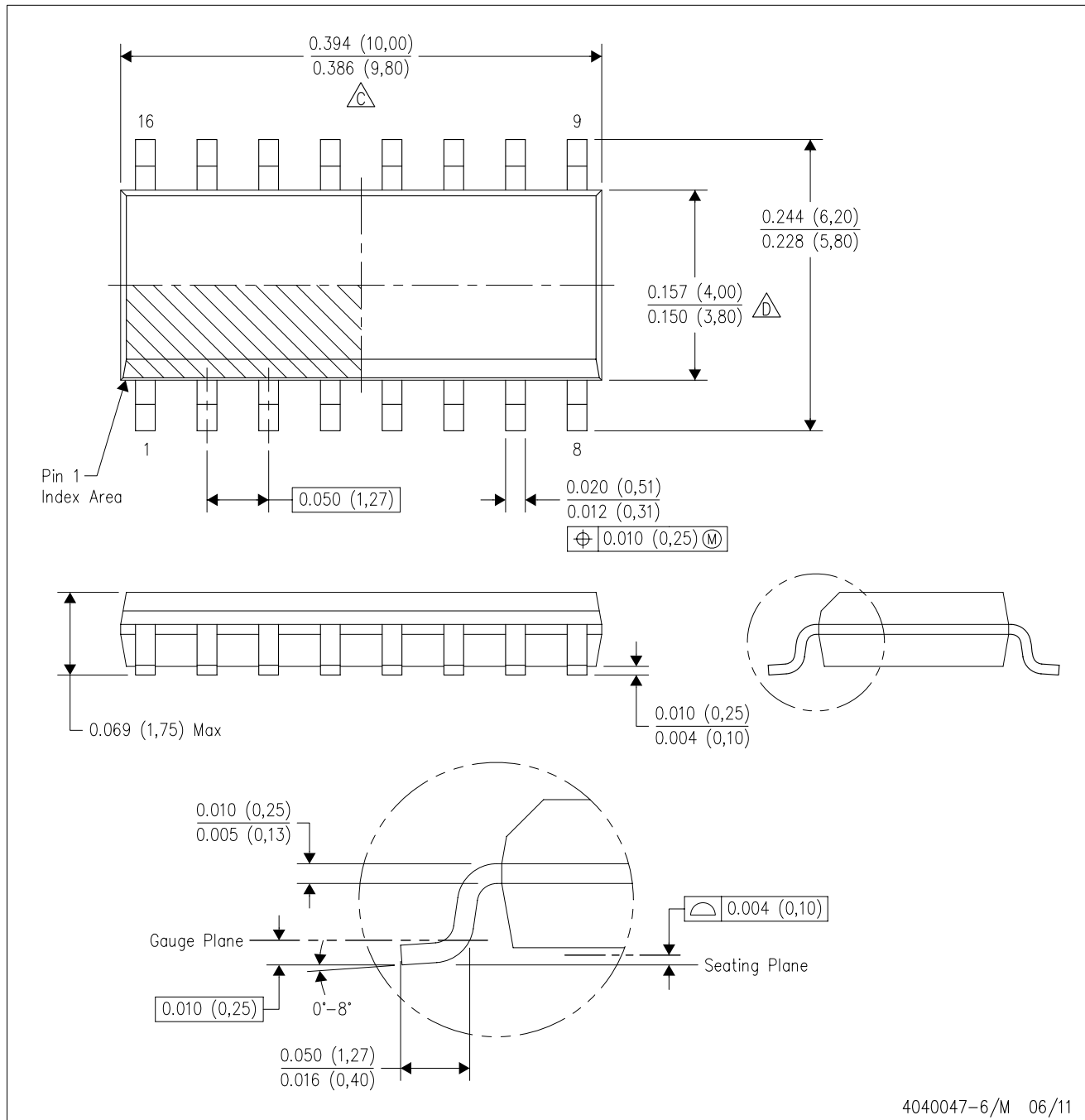




4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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