DACxx6x Dual 16-, 14-, 12-Bit, Low-Power, Buffered, Voltage-Output DACs With 2.5-V, 4-PPM/°C Internal Reference

1 Features

- Relative Accuracy:
  - DAC756x (12-Bit): 0.3 LSB INL
  - DAC816x (14-Bit): 1 LSB INL
  - DAC856x (16-Bit): 4 LSB INL
- Glitch Impulse: 0.1 nV-s
- Bidirectional Reference: Input or 2.5-V Output
  - Output Disabled by Default
  - ±5-mV Initial Accuracy (Max)
  - 4-ppm°C Temperature Drift (Typ)
  - 10-ppm/°C Temperature Drift (Max)
  - 20-mA Sink and Source Capability
- Power-On Reset to Zero Scale or Mid-Scale
- Low-Power: 4 mW (Typ, 5-V AV_{DD}, Including Internal Reference Current)
- Wide Power-Supply Range: 2.7 V to 5.5 V
- 50-MHz SPI With Schmitt-Triggered Inputs
- LDAC and CLR Functions
- Output Buffer With Rail-to-Rail Operation
- Packages: WSON-10 (3 mm × 3 mm), VSSOP-10
- Temperature Range: –40°C to 125°C

2 Applications

- Portable Instrumentation
- PLC Analog Output Module
- Closed-Loop Servo Control
- Voltage Controlled Oscillator Tuning
- Data Acquisition Systems
- Programmable Gain and Offset Adjustment

3 Description

The DAC756x, DAC816x, and DAC856x devices are low-power, voltage-output, dual-channel, 16-, 14-, and 12-bit digital-to-analog converters (DACs), respectively. These devices include a 2.5-V, 4-ppm/°C internal reference, giving a full-scale output voltage range of 2.5 V or 5 V. The internal reference has an initial accuracy of ±5 mV and can source or sink up to 20 mA at the V_{REFIN}/V_{REFOUT} pin.

These devices are monotonic, providing excellent linearity and minimizing undesired code-to-code transient voltages (glitch). They use a versatile three-wire serial interface that operates at clock rates up to 50 MHz. The interface is compatible with standard SPI™, QSPI™, Microwire, and digital signal processor (DSP) interfaces. The DACxx62 devices incorporate a power-on-reset circuit that ensures the DAC output powers up and remains at zero scale until a valid code is written to the device, whereas the DACxx63 devices similarly power up at mid-scale. These devices contain a power-down feature that reduces current consumption to typically 550 nA at 5 V. The low power consumption, internal reference, and small footprint make these devices ideal for portable, battery-operated equipment.

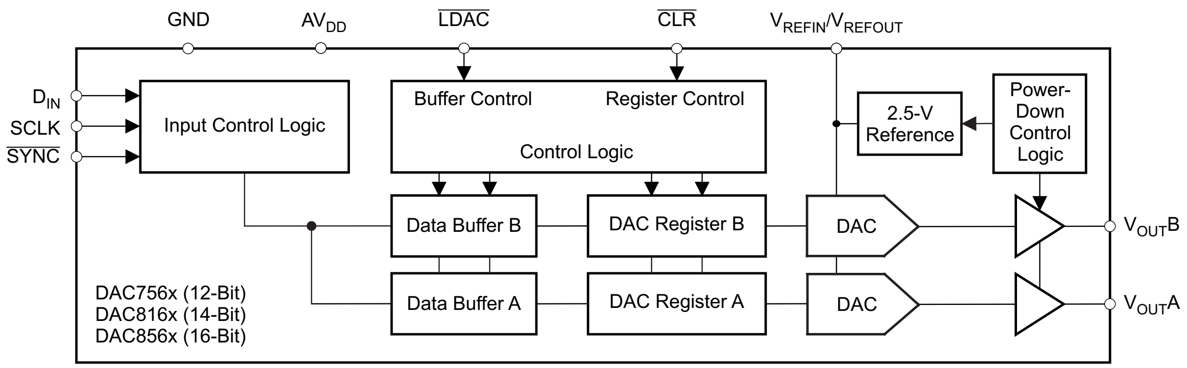
The DACxx62 devices are drop-in and function-compatible with each other, as are the DACxx63 devices. The entire family is available in MSOP-10 and SON-10 packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC8562	VSSOP (10), WSON (10)	3.00 mm × 3.00 mm
DAC8162		
DAC7562		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2012) to Revision E	Page
• Changed all instances of *glitch energy* in the data sheet to *glitch impulse*	1
• Changed *Applications* list	1
• Revised the Device Comparison Table	3
• Added an I/O column to the Pin Functions table	4
• Added storage temperature to the Absolute Maximum Ratings table	5
• Added ESD Ratings table to the data sheet	5
• Added Recommended Operating Conditions table to the data sheet	5
• Deleted several notes following the Thermal Information table	5
• Replaced the previous typical application	41

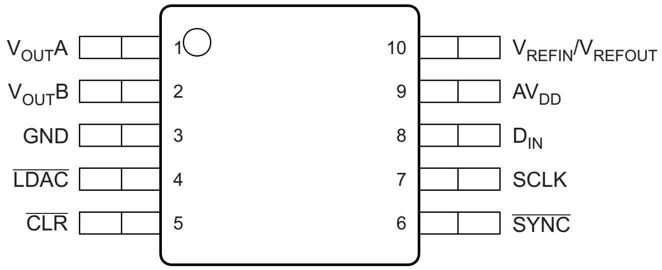
Changes from Revision C (June 2011, first official release) to Revision D	Page
• Replaced text "QFN" with "SON" (name change only, package and orderable did not change)	1
• Typical power-down current consumption changed from 10 nA to 550 nA.	1
• Changed power requirements specifications	8
• Power-down current vs Temperature typical characteristic plot updated, AV_{DD} = 5.5 V	16
• Power-down current vs Power-supply voltage typical characteristic plot updated	16
• Added Power-On Reset (POR) Levels section	31

5 Device Comparison Table

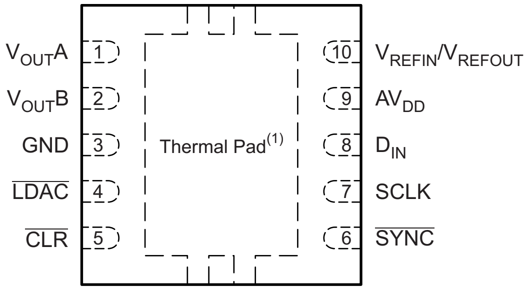
DEVICE	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	MAXIMUM REFERENCE DRIFT (ppm/°C)	RESET TO
DAC7562	±0.75	±0.25	10	Zero
DAC7563				Mid-scale
DAC8162	±3	±0.5	10	Zero
DAC8163				Mid-scale
DAC8562	±12	±1	10	Zero
DAC8563				Mid-scale

6 Pin Configuration and Functions

10-Pin VSSOP
DGS Package
(Top View)



10-Pin WSON With Thermal Pad
DSC Package
(Top View)



(1) TI recommends connecting the thermal pad to the ground plane for better thermal dissipation.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AV_{DD}	9	I	Power-supply input, 2.7 V to 5.5 V
$\overline{\text{CLR}}$	5	I	Asynchronous clear input. The $\overline{\text{CLR}}$ input is falling-edge sensitive. On activation of $\overline{\text{CLR}}$, zero scale (DACxx62) or mid-scale (DACxx63) is loaded to all input and DAC registers. This sets the DAC output voltages accordingly. The device exits clear code mode on the 24th falling edge of the next write to the device. Activating $\overline{\text{CLR}}$ during a write sequence aborts the write.
D_{IN}	8	I	Serial data input. Data are clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-trigger logic input
GND	3	—	Ground reference point for all circuitry on the device
$\overline{\text{LDAC}}$	4	I	In *synchronous* mode, data update occurs with the falling edge of the 24th SCLK cycle, which follows a falling edge of $\overline{\text{SYNC}}$. Such *synchronous* updates do not require the $\overline{\text{LDAC}}$, which must be connected to GND permanently or asserted and held low before sending commands to the device. In *asynchronous* mode, the $\overline{\text{LDAC}}$ pin is used as a negative edge-triggered timing signal for simultaneous DAC updates. Multiple single-channel commands can be written in order to set different channel buffers to desired values and then make a falling edge on the $\overline{\text{LDAC}}$ pin to update the DAC output registers simultaneously.
SCLK	7	I	Serial clock input. Data can be transferred at rates up to 50 MHz. Schmitt-trigger logic input
$\overline{\text{SYNC}}$	6	I	Level-triggered control input (active-low). This input is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register, and data are sampled on subsequent falling clock edges. The DAC output updates following the 24th clock falling edge. If $\overline{\text{SYNC}}$ is taken high before the 23rd clock edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC756x, DAC816x, and DAC856x devices. Schmitt-trigger logic input
$V_{OUT}A$	1	O	Analog output voltage from DAC-A
$V_{OUT}B$	2	O	Analog output voltage from DAC-B
V_{REFIN}/V_{REFOUT}	10	I/O	Bidirectional voltage reference pin. If internal reference is used, 2.5-V output.

7 Specifications

7.1 Absolute Maximum Ratings(1)

Over operating ambient temperature range (unless otherwise noted).

	MIN	MAX	UNIT
AV_{DD} to GND	–0.3	6	V
$\overline{\text{CLR}}$, D_{IN}, $\overline{\text{LDAC}}$, SCLK and $\overline{\text{SYNC}}$ input voltage to GND	–0.3	AV_{DD} + 0.3	V
V_{OUT}[A, B] to GND	–0.3	AV_{DD} + 0.3	V
V_{REFIN}/V_{REFOUT} to GND	–0.3	AV_{DD} + 0.3	V
Operating temperature range	–40	125	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Supply voltage	AV_{DD} to GND	2.7		5.5	V
DIGITAL INPUTS						
	Digital input voltage	$\overline{\text{CLR}}$, D_{IN}, $\overline{\text{LDAC}}$, SCLK and $\overline{\text{SYNC}}$	0		AV_{DD}	V
REFERENCE INPUT						
V_{REFIN}	Reference input voltage		0		AV_{DD}	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC		DAC756x, DAC816x, DAC856x		UNIT
		DSC (WSON)	DGS (VSSOP)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.8	173.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.3	48.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.5	79.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.5	68.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	46.2	N/A	°C/W

7.5 Electrical Characteristics

At AV_{DD} = 2.7 V to 5.5 V and T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
DAC856x	Resolution		16			Bits
	Relative accuracy	Using line passing through codes 512 and 65,024		±4	±12	LSB
	Differential nonlinearity	16-bit monotonic		±0.2	±1	LSB
DAC816x	Resolution		14			Bits
	Relative accuracy	Using line passing through codes 128 and 16,256		±1	±3	LSB
	Differential nonlinearity	14-bit monotonic		±0.1	±0.5	LSB
DAC756x	Resolution		12			Bits
	Relative accuracy	Using line passing through codes 32 and 4,064		±0.3	±0.75	LSB
	Differential nonlinearity	12-bit monotonic		±0.05	±0.25	LSB
Offset error		Extrapolated from two-point line(1), unloaded		±1	±4	mV
Offset error drift				±2		µV/°C
Full-scale error		DAC register loaded with all 1s		±0.03	±0.2	% FSR
Zero-code error		DAC register loaded with all 0s		1	4	mV
Zero-code error drift				±2		µV/°C
Gain error		Extrapolated from two-point line(1), unloaded		±0.01	±0.15	% FSR
Gain temperature coefficient				±1		ppm FSR/°C
OUTPUT CHARACTERISTICS(2)						
Output voltage range			0		AV_{DD}	V
Output voltage settling time(3)		DACs unloaded		7		µs
		R_L = 1 MΩ		10		
Slew rate		Measured between 20%–80% of a full-scale transition		0.75		V/µs
Capacitive load stability		$R_L = \infty$		1		nF
		R_L = 2 kΩ		3		
Code-change glitch impulse		1-LSB change around major carry		0.1		nV-s
Digital feedthrough		SCLK toggling, $\overline{\text{SYNC}}$ high		0.1		nV-s
Power-on glitch impulse		R_L = 2 kΩ, C_L = 470 pF, AV_{DD} = 5.5 V		40		mV
Channel-to-channel dc crosstalk		Full-scale swing on adjacent channel, External reference		5		µV
		Full-scale swing on adjacent channel, Internal reference		15		
DC output impedance		At mid-scale input		5		Ω
Short-circuit current		DAC outputs at full-scale, DAC outputs shorted to GND		40		mA
Power-up time, including settling time		Coming out of power-down mode		50		µs
AC PERFORMANCE(2)						
DAC output noise density		T_A = 25°C, at mid-scale input, f_{OUT} = 1 kHz		90		$nV/\sqrt{Hz}$
DAC output noise		T_A = 25°C, at mid-scale input, 0.1 Hz to 10 Hz		2.6		μV_{PP}

(1) 16-bit: codes 512 and 65,024; 14-bit: codes 128 and 16,256; 12-bit: codes 32 and 4,064
(2) Specification based on design or characterization. Not production tested
(3) Transition time between 1 / 4 scale and 3 / 4 scale, including settling to within ±0.024% FSR

Electrical Characteristics (continued)

At AV_{DD} = 2.7 V to 5.5 V and T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUTS[2]					
Input-pin leakage current		–1	±0.1	1	µA
Logic input LOW voltage V_{IL}		0		0.8	V
Logic input HIGH voltage V_{IH}		0.7 × AV_{DD}		AV_{DD}	V
Pin capacitance				3	pF
REFERENCE					
External reference current	External V_{REF} = 2.5 V (when internal reference is disabled), all channels active using gain = 1		15		µA
Reference input impedance	Internal reference disabled, gain = 1		170		kΩ
	Internal reference disabled, gain = 2		85		
REFERENCE OUTPUT					
Output voltage	T_A = 25°C	2.495	2.5	2.505	V
Initial accuracy	T_A = 25°C	–5	±0.1	5	mV
Output-voltage temperature drift			4	10	ppm/°C
Output-voltage noise	f = 0.1 Hz to 10 Hz		12		μV_{PP}
Output-voltage noise density (high-frequency noise)	T_A = 25°C, f = 1 kHz, C_L = 0 µF		250		nV/$\sqrt{Hz}$
	T_A = 25°C, f = 1 MHz, C_L = 0 µF		30		
	T_A = 25°C, f = 1 MHz, C_L = 4.7 µF		10		
Load regulation, sourcing[4]	T_A = 25°C		20		µV/mA
Load regulation, sinking[4]	T_A = 25°C		185		µV/mA
Output-current load capability[2]			±20		mA
Line regulation	T_A = 25°C		50		µV/V
Long-term stability or drift (aging)[4]	T_A = 25°C, time = 0 to 1900 hours		100		ppm
Thermal hysteresis[4]	First cycle		200		ppm
	Additional cycles		50		

(4) See the *Application Information* section of this data sheet.

Electrical Characteristics (continued)

At AV_{DD} = 2.7 V to 5.5 V and T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER REQUIREMENTS(5)					
Power supply current (I_{DD})	AV_{DD} = 3.6 V to 5.5 V, normal mode, internal reference off		0.25	0.5	mA
	AV_{DD} = 3.6 V to 5.5 V, normal mode, internal reference on		0.9	1.6	
	AV_{DD} = 3.6 V to 5.5 V, power-down modes(6)		0.55	2	µA
	AV_{DD} = 3.6 V to 5.5 V, power-down modes		0.55	4	
	AV_{DD} = 2.7 V to 3.6 V, normal mode, internal reference off		0.2	0.4	mA
	AV_{DD} = 2.7 V to 3.6 V, normal mode, internal reference on		0.73	1.4	
	AV_{DD} = 2.7 V to 3.6 V, power-down modes(6)		0.35	2	µA
	AV_{DD} = 2.7 V to 3.6 V, power-down modes		0.35	3	
Power dissipation	AV_{DD} = 3.6 V to 5.5 V, normal mode, internal reference off		0.9	2.75	mW
	AV_{DD} = 3.6 V to 5.5 V, normal mode, internal reference on		3.2	8.8	
	AV_{DD} = 3.6 V to 5.5 V, power-down modes(6)		2	11	µW
	AV_{DD} = 3.6 V to 5.5 V, power-down modes		2	22	
	AV_{DD} = 2.7 V to 3.6 V, normal mode, internal reference off		0.54	1.44	mW
	AV_{DD} = 2.7 V to 3.6 V, normal mode, internal reference on		1.97	5	
	AV_{DD} = 2.7 V to 3.6 V, power-down modes(6)		0.95	7.2	µW
	AV_{DD} = 2.7 V to 3.6 V, power-down modes		0.95	10.8	

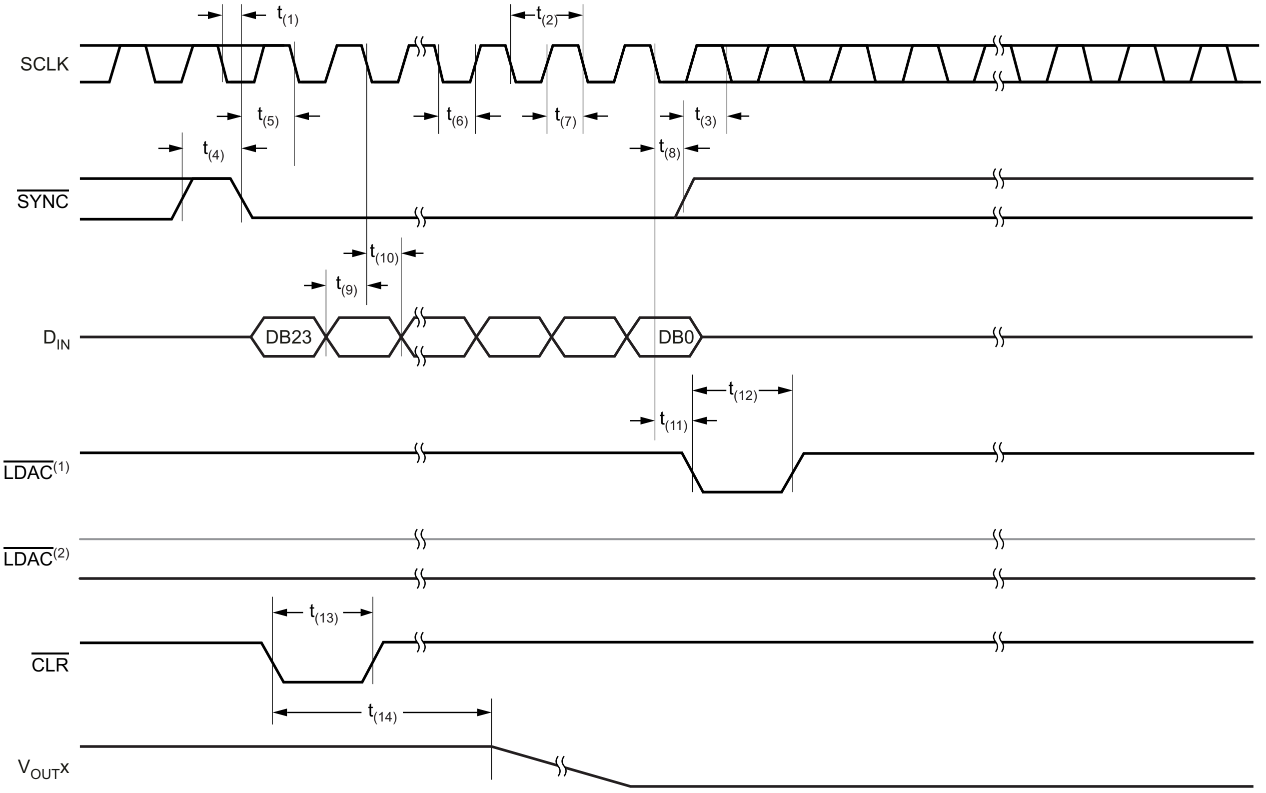
(5) Input code = mid-scale, no load, $V_{IN}H$ = AV_{DD}, and $V_{IN}L$ = GND
(6) T_A = –40°C to 105°C

7.6 Timing Requirements(1)(2)

At AV_{DD} = 2.7 V to 5.5 V and over –40°C to 125°C (unless otherwise noted).

		DAC756x, DAC816x, DAC856x			UNIT
		MIN	TYP	MAX	
$f_{(SCLK)}$	Serial clock frequency			50	MHz
$t_{(1)}$	SCLK falling edge to $\overline{\text{SYNC}}$ falling edge (for successful write operation)	10			ns
$t_{(2)}$	SCLK cycle time	20			ns
$t_{(3)}$	$\overline{\text{SYNC}}$ rising edge to 23rd SCLK falling edge (for successful $\overline{\text{SYNC}}$ interrupt)	13			ns
$t_{(4)}$	Minimum $\overline{\text{SYNC}}$ HIGH time	80			ns
$t_{(5)}$	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	13			ns
$t_{(6)}$	SCLK LOW time	8			ns
$t_{(7)}$	SCLK HIGH time	8			ns
$t_{(8)}$	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	10			ns
$t_{(9)}$	Data setup time	6			ns
$t_{(10)}$	Data hold time	5			ns
$t_{(11)}$	SCLK falling edge to $\overline{\text{LDAC}}$ falling edge for asynchronous LDAC update mode	5			ns
$t_{(12)}$	$\overline{\text{LDAC}}$ pulse duration, LOW time	10			ns
$t_{(13)}$	$\overline{\text{CLR}}$ pulse duration, LOW time	80			ns
$t_{(14)}$	$\overline{\text{CLR}}$ falling edge to start of V_{OUT} transition			100	ns

(1) All input signals are specified with $t_r = t_f$ = 3 ns (10% to 90% of AV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$.
(2) See the *Serial Write Operation* timing diagram (Figure 1).



(1) Asynchronous $\overline{\text{LDAC}}$ update mode. For more information, see the *LDAC Functionality* section.

(2) Synchronous $\overline{\text{LDAC}}$ update mode; $\overline{\text{LDAC}}$ remains low. For more information, see the *LDAC Functionality* section.

Figure 1. Serial Write Operation

7.7 Typical Characteristics

Table 1. Typical Characteristics: Internal Reference Performance

MEASUREMENT	POWER-SUPPLY VOLTAGE	FIGURE NUMBER
Internal Reference Voltage vs Temperature	5.5 V	Figure 2
Internal Reference Voltage Temperature Drift Histogram		Figure 3
Internal Reference Voltage vs Load Current		Figure 4
Internal Reference Voltage vs Time		Figure 5
Internal Reference Noise Density vs Frequency		Figure 6
Internal Reference Voltage vs Supply Voltage	2.7 V–5.5 V	Figure 7

Table 2. Typical Characteristics: DAC Static Performance

MEASUREMENT		POWER-SUPPLY VOLTAGE	FIGURE NUMBER
FULL-SCALE, GAIN, OFFSET AND ZERO-CODE ERRORS			
Full-Scale Error vs Temperature		5.5 V	Figure 16
Gain Error vs Temperature			Figure 17
Offset Error vs Temperature			Figure 18
Zero-Code Error vs Temperature			Figure 19
Full-Scale Error vs Temperature		2.7 V	Figure 63
Gain Error vs Temperature			Figure 64
Offset Error vs Temperature			Figure 65
Zero-Code Error vs Temperature			Figure 66
LOAD REGULATION			
DAC Output Voltage vs Load Current		5.5 V	Figure 30
		2.7 V	Figure 74
DIFFERENTIAL NONLINEARITY ERROR			
Differential Linearity Error vs Digital Input Code	T = –40°C	5.5 V	Figure 9
	T = 25°C		Figure 11
	T = 125°C		Figure 13
Differential Linearity Error vs Temperature			Figure 15
Differential Linearity Error vs Digital Input Code	T = –40°C	2.7 V	Figure 56
	T = 25°C		Figure 58
	T = 125°C		Figure 60
Differential Linearity Error vs Temperature			Figure 62
INTEGRAL NONLINEARITY ERROR (RELATIVE ACCURACY)			
Linearity Error vs Digital Input Code	T = –40°C	5.5 V	Figure 8
	T = 25°C		Figure 10
	T = 125°C		Figure 12
Linearity Error vs Temperature			Figure 14
Linearity Error vs Digital Input Code	T = –40°C	2.7 V	Figure 55
	T = 25°C		Figure 57
	T = 125°C		Figure 59
Linearity Error vs Temperature			Figure 61

Table 2. Typical Characteristics: DAC Static Performance (continued)

MEASUREMENT		POWER-SUPPLY VOLTAGE	FIGURE NUMBER
POWER-DOWN CURRENT			
Power-Down Current vs Temperature		5.5 V	Figure 28
Power-Down Current vs Power-Supply Voltage		2.7 V – 5.5 V	Figure 29
Power-Down Current vs Temperature		2.7 V	Figure 73
POWER-SUPPLY CURRENT			
Power-Supply Current vs Temperature	External V_{REF}	5.5 V	Figure 20
	Internal V_{REF}		Figure 21
Power-Supply Current vs Digital Input Code	External V_{REF}		Figure 22
	Internal V_{REF}		Figure 23
Power-Supply Current Histogram	External V_{REF}		Figure 24
	Internal V_{REF}		Figure 25
Power-Supply Current vs Power-Supply Voltage	External V_{REF}	2.7 V – 5.5 V	Figure 26
	Internal V_{REF}		Figure 27
Power-Supply Current vs Temperature	External V_{REF}	3.6 V	Figure 49
	Internal V_{REF}		Figure 50
Power-Supply Current vs Digital Input Code	External V_{REF}		Figure 51
	Internal V_{REF}		Figure 52
Power-Supply Current Histogram	External V_{REF}		Figure 53
	Internal V_{REF}		Figure 54
Power-Supply Current vs Temperature	External V_{REF}	2.7 V	Figure 67
	Internal V_{REF}		Figure 68
Power-Supply Current vs Digital Input Code	External V_{REF}		Figure 69
	Internal V_{REF}		Figure 70
Power-Supply Current Histogram	External V_{REF}		Figure 71
	Internal V_{REF}		Figure 72

Table 3. Typical Characteristics: DAC Dynamic Performance

MEASUREMENT		POWER-SUPPLY VOLTAGE	FIGURE NUMBER
CHANNEL-TO-CHANNEL CROSSTALK			
Channel-to-Channel Crosstalk	5-V Rising Edge	5.5 V	Figure 43
	5-V Falling Edge		Figure 44
CLOCK FEEDTHROUGH			
Clock Feedthrough	500 kHz, Midscale	5.5 V	Figure 48
		2.7 V	Figure 87
GLITCH IMPULSE			
Glitch Impulse, 1-LSB Step	Rising Edge, Code 7FFFh to 8000h	5.5 V	Figure 37
	Falling Edge, Code 8000h to 7FFFh		Figure 38
Glitch Impulse, 4-LSB Step	Rising Edge, Code 7FFCh to 8000h		Figure 39
	Falling Edge, Code 8000h to 7FFCh		Figure 40
Glitch Impulse, 16-LSB Step	Rising Edge, Code 7FF0h to 8000h		Figure 41
	Falling Edge, Code 8000h to 7FF0h		Figure 42

Table 3. Typical Characteristics: DAC Dynamic Performance (continued)

MEASUREMENT		POWER-SUPPLY VOLTAGE	FIGURE NUMBER
Glitch Impulse, 1-LSB Step	Rising Edge, Code 7FFFh to 8000h	2.7 V	Figure 79
	Falling Edge, Code 8000h to 7FFFh		Figure 80
Glitch Impulse, 4-LSB Step	Rising Edge, Code 7FFCh to 8000h		Figure 81
	Falling Edge, Code 8000h to 7FFCh		Figure 82
Glitch Impulse, 16-LSB Step	Rising Edge, Code 7FF0h to 8000h		Figure 83
	Falling Edge, Code 8000h to 7FF0h		Figure 84
NOISE			
DAC Output Noise Density vs Frequency	External V_{REF}	5.5 V	Figure 45
	Internal V_{REF}		Figure 46
DAC Output Noise 0.1 Hz to 10 Hz	External V_{REF}		Figure 47
POWER-ON GLITCH			
Power-On Glitch	Reset to Zero Scale	5.5 V	Figure 35
	Reset to Midscale		Figure 36
	Reset to Zero Scale	2.7 V	Figure 85
	Reset to Midscale		Figure 86
SETTLING TIME			
Full-Scale Settling Time	Rising Edge, Code 0h to FFFFh	5.5 V	Figure 31
	Falling Edge, Code FFFFh to 0h		Figure 32
Half-Scale Settling Time	Rising Edge, Code 4000h to C000h		Figure 33
	Falling Edge, Code C000h to 4000h		Figure 34
Full-Scale Settling Time	Rising Edge, Code 0h to FFFFh	2.7 V	Figure 75
	Falling Edge, Code FFFFh to 0h		Figure 76
Half-Scale Settling Time	Rising Edge, Code 4000h to C000h		Figure 77
	Falling Edge, Code C000h to 4000h		Figure 78

7.7.1 Typical Characteristics: Internal Reference

At T_A = 25°C, AV_{DD} = 5.5 V, gain = 2, and V_{REFOUT} unloaded, unless otherwise noted.

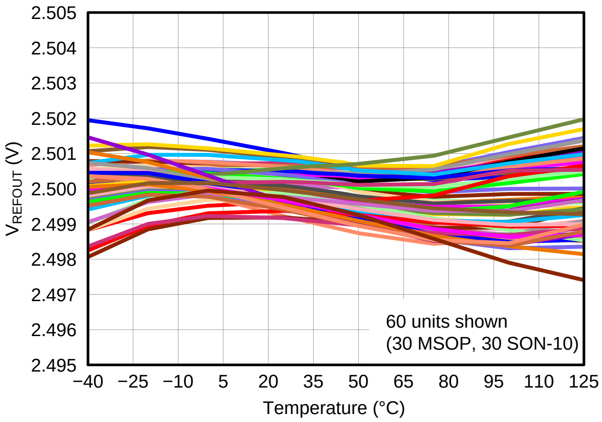


Figure 2. Internal Reference Voltage vs Temperature

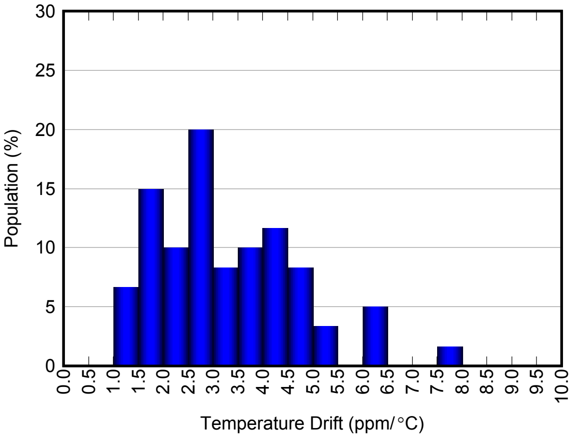


Figure 3. Internal Reference Voltage, Temperature Drift Histogram

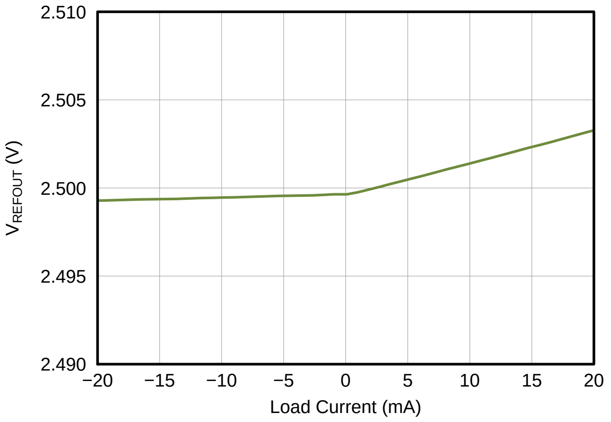


Figure 4. Internal Reference Voltage vs Load Current

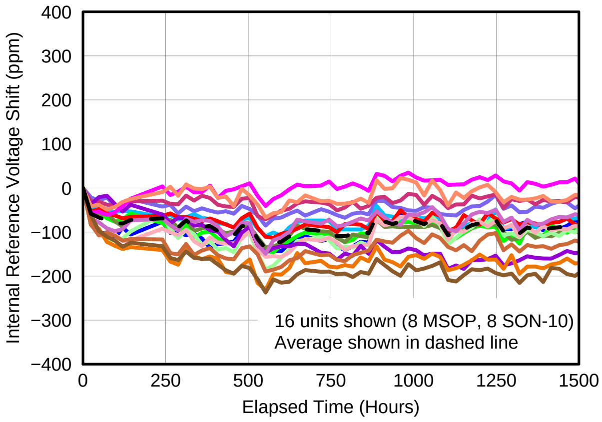


Figure 5. Internal Reference Voltage vs Time

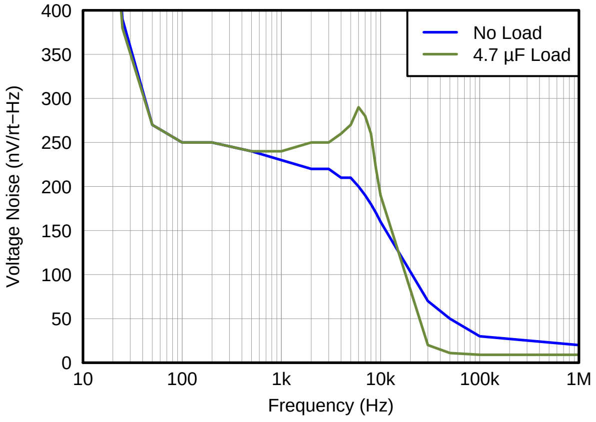


Figure 6. Internal Reference Noise Density vs Frequency

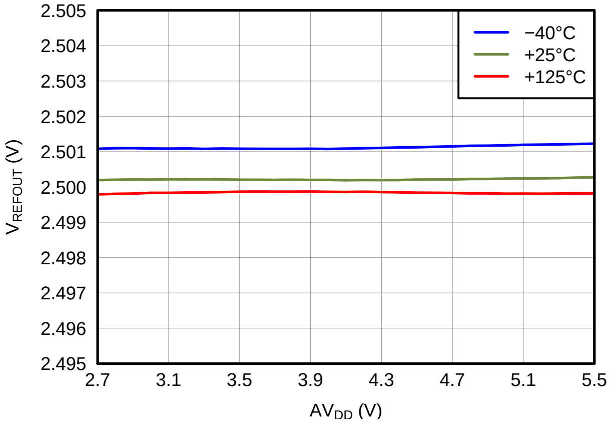


Figure 7. Internal Reference Voltage vs Supply Voltage

7.7.2 Typical Characteristics: DAC at AV_{DD} = 5.5 V

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

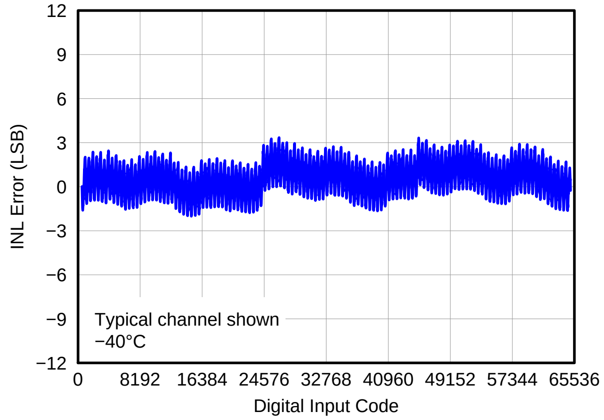


Figure 8. Linearity Error vs Digital Input Code (–40°C)

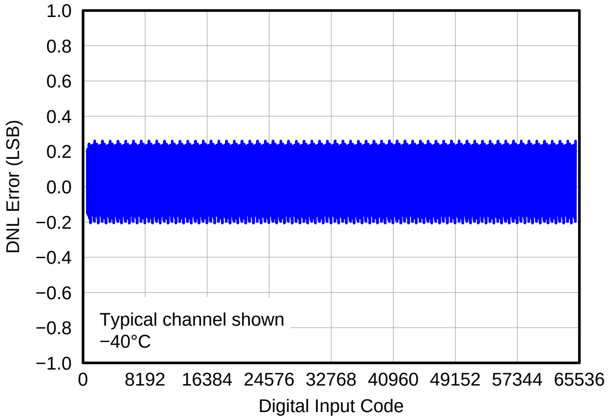


Figure 9. Differential Linearity Error vs Digital Input Code (–40°C)

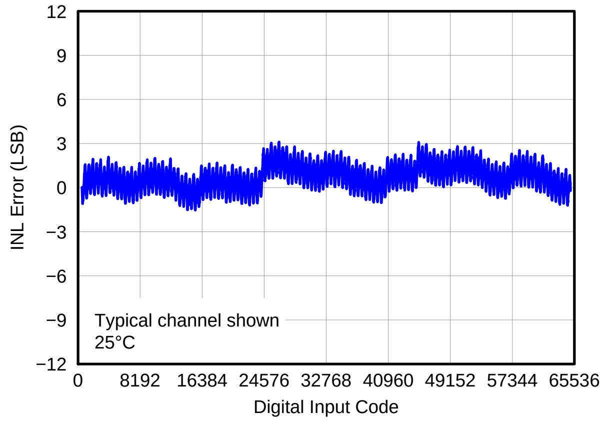


Figure 10. Linearity Error vs Digital Input Code (25°C)

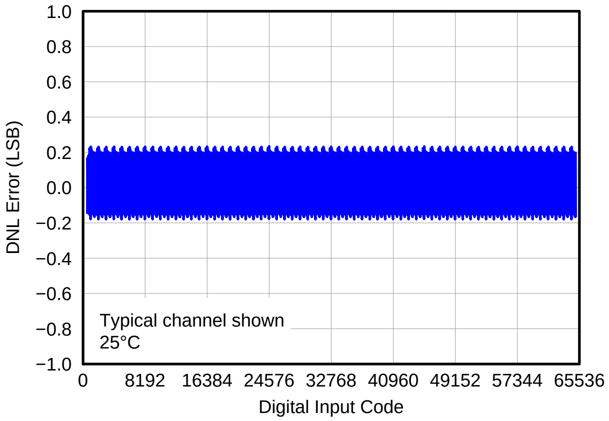


Figure 11. Differential Linearity Error vs Digital Input Code (25°C)

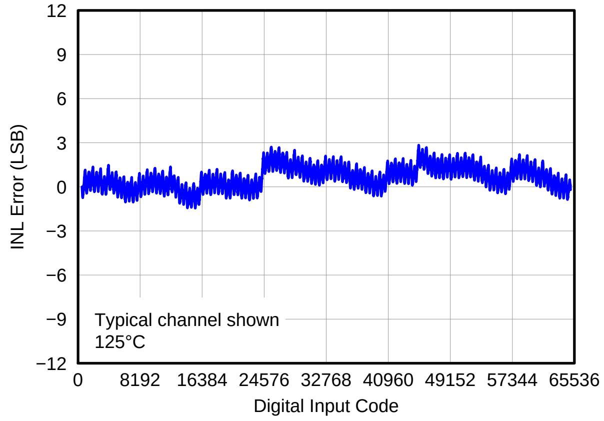


Figure 12. Linearity Error vs Digital Input Code (125°C)

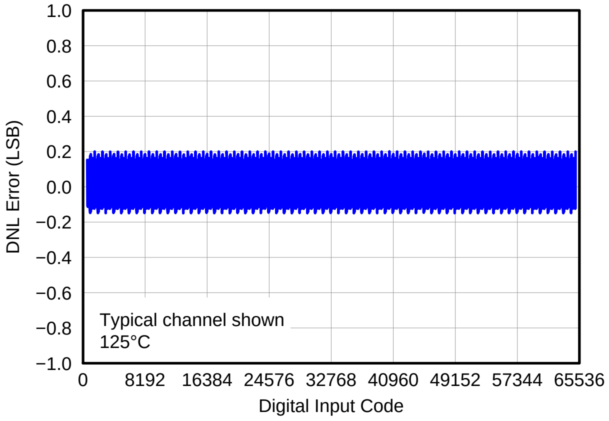


Figure 13. Differential Linearity Error vs Digital Input Code (125°C)

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

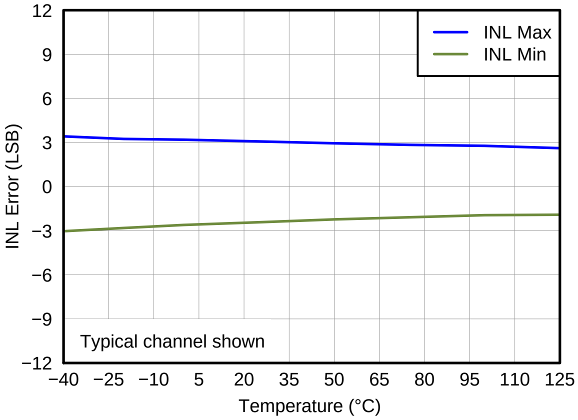


Figure 14. Linearity Error vs Temperature

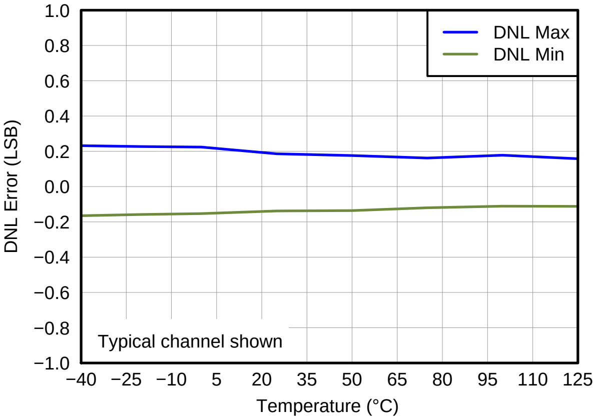


Figure 15. Differential Linearity Error vs Temperature

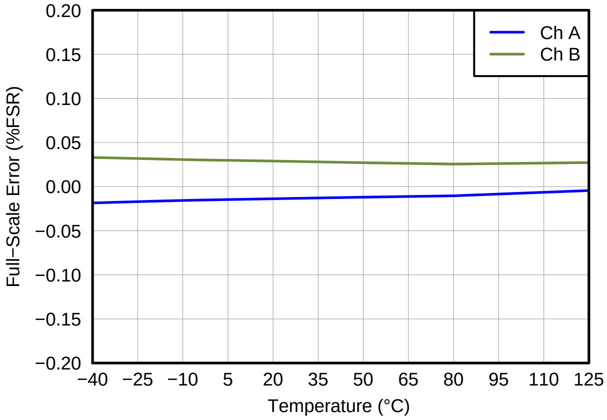


Figure 16. Full-Scale Error vs Temperature

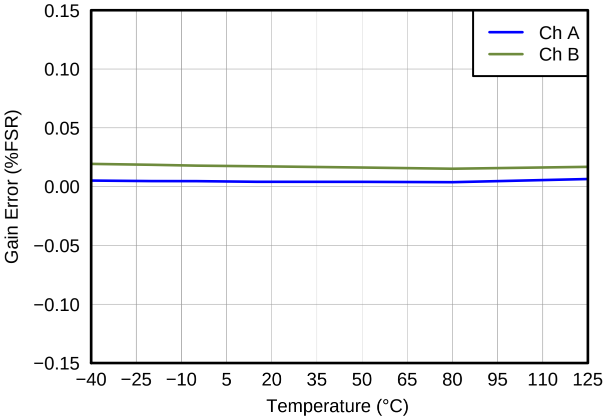


Figure 17. Gain Error vs Temperature

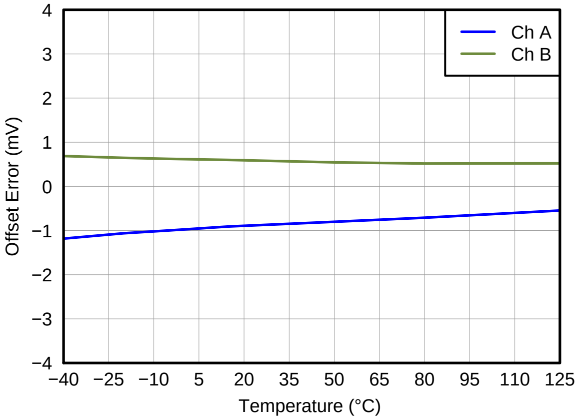


Figure 18. Offset Error vs Temperature

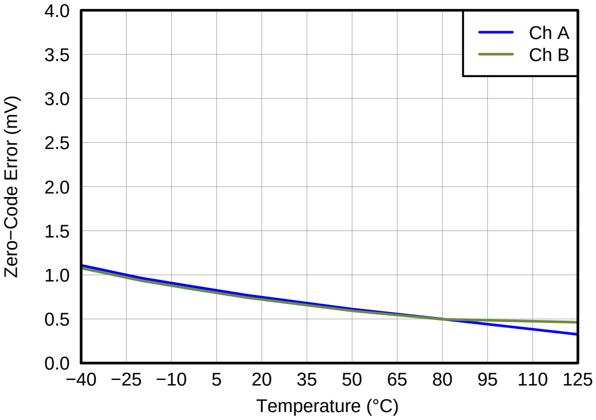


Figure 19. Zero-Code Error vs Temperature

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

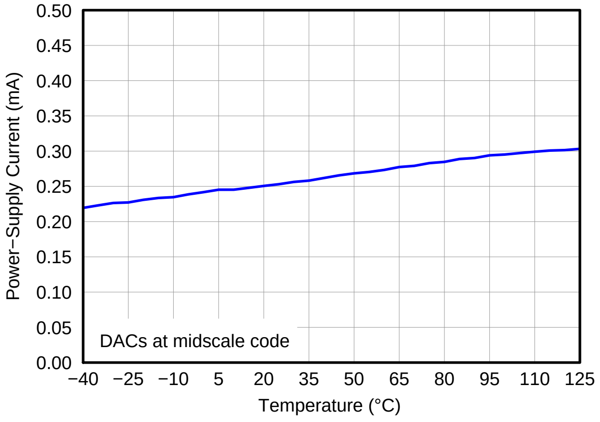


Figure 20. Power-Supply Current vs Temperature

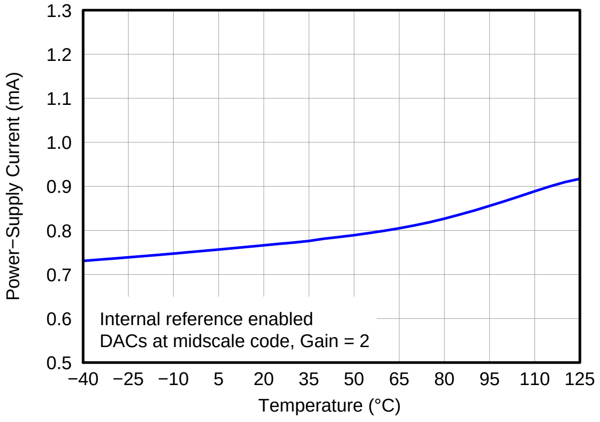


Figure 21. Power-Supply Current vs Temperature

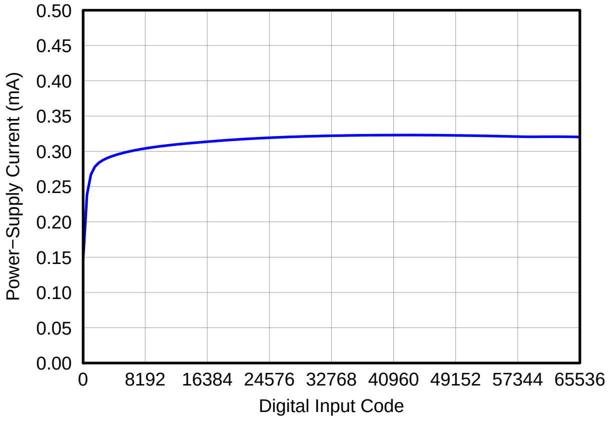


Figure 22. Power-Supply Current vs Digital Input Code

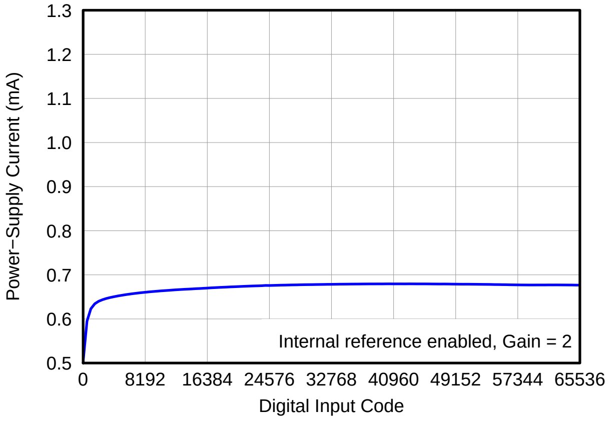


Figure 23. Power-Supply Current vs Digital Input Code

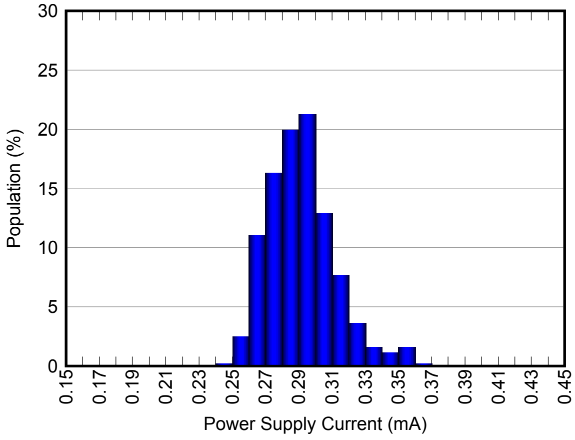


Figure 24. Power-Supply Current Histogram

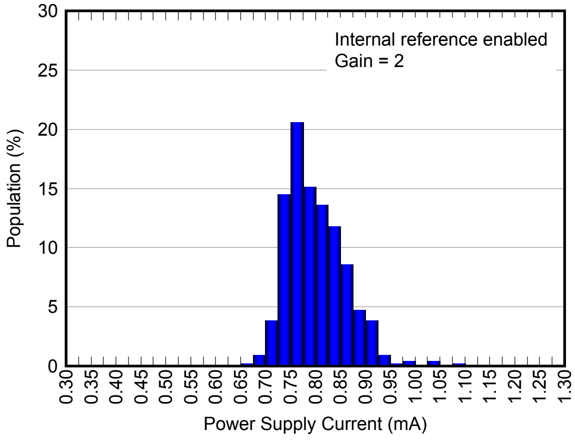


Figure 25. Power-Supply Current Histogram

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

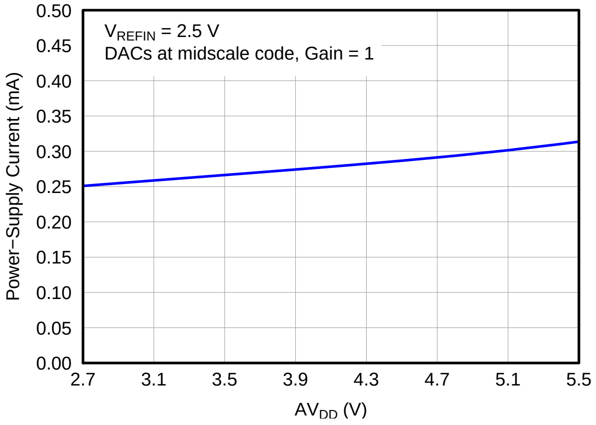


Figure 26. Power-Supply Current vs Power-Supply Voltage

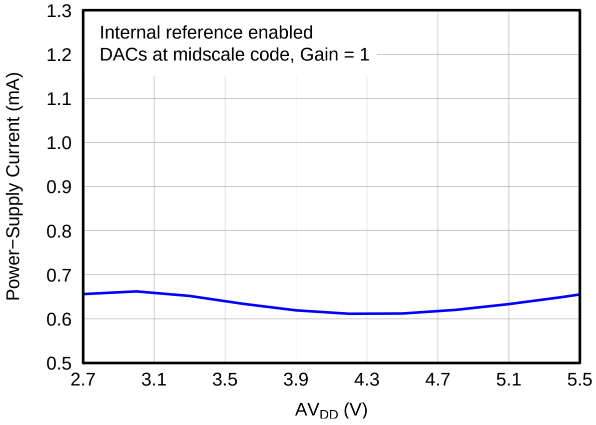


Figure 27. Power-Supply Current vs Power-Supply Voltage

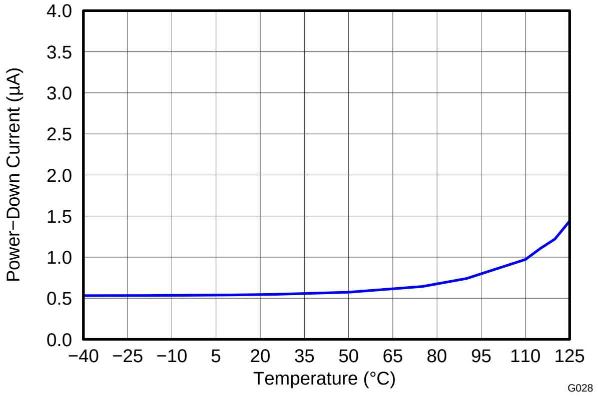


Figure 28. Power-Down Current vs Temperature

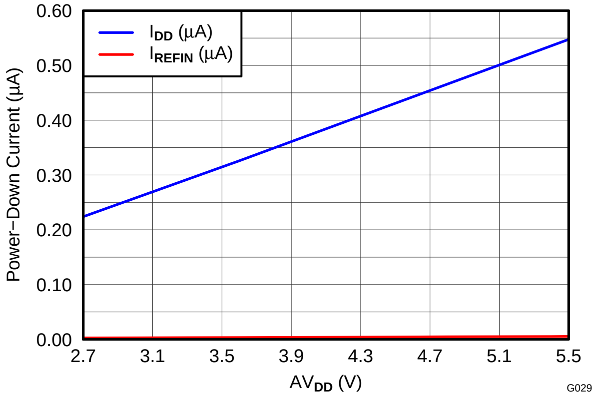


Figure 29. Power-Down Current vs Power-Supply Voltage

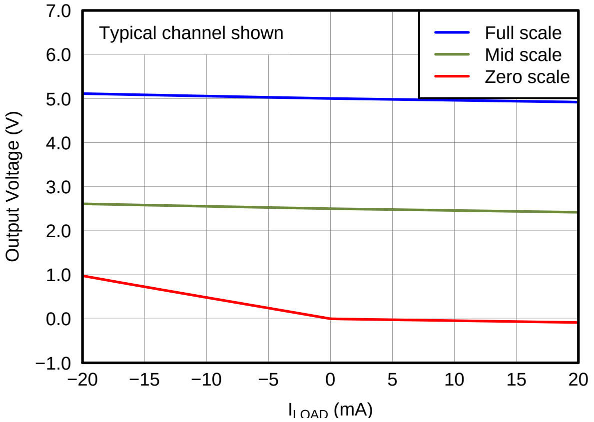


Figure 30. DAC Output Voltage vs Load Current

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

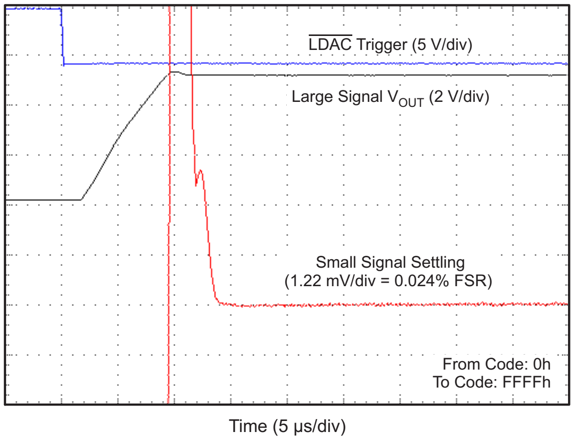


Figure 31. Full-Scale Settling Time, Rising Edge

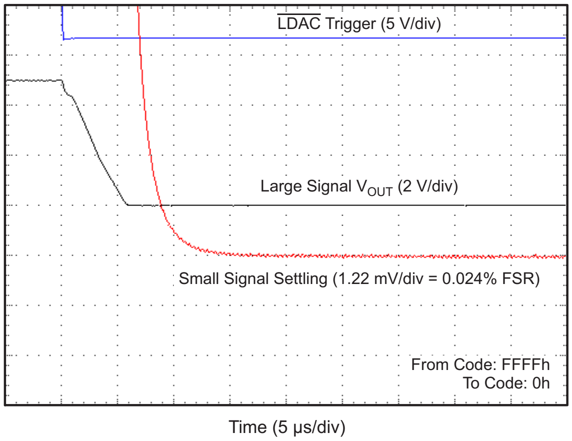


Figure 32. Full-Scale Settling Time, Falling Edge

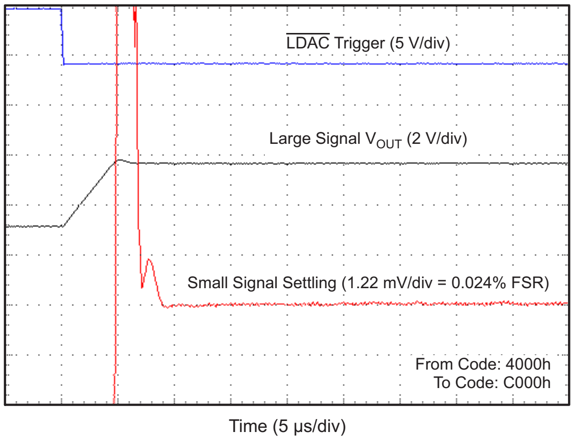


Figure 33. Half-Scale Settling Time, Rising Edge

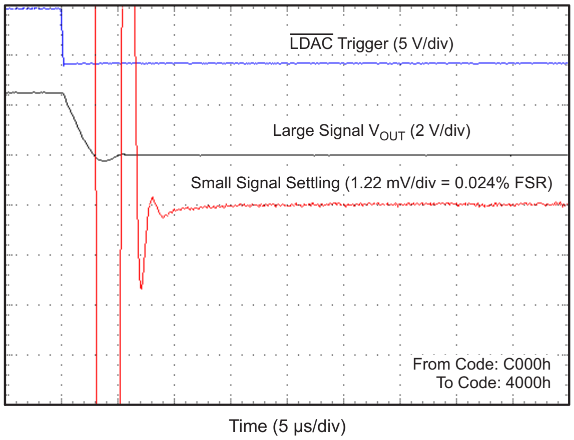


Figure 34. Half-Scale Settling Time, Falling Edge

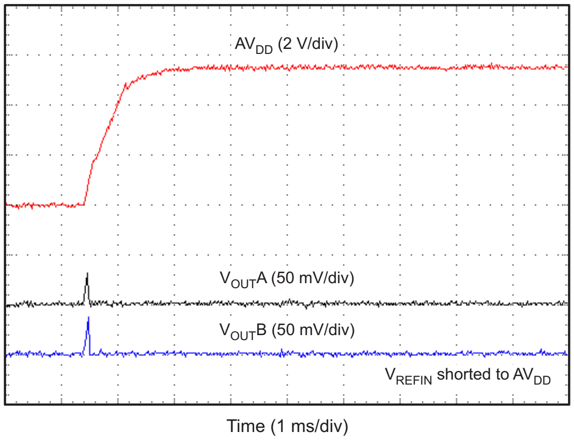


Figure 35. Power-On Glitch, Reset to Zero Scale

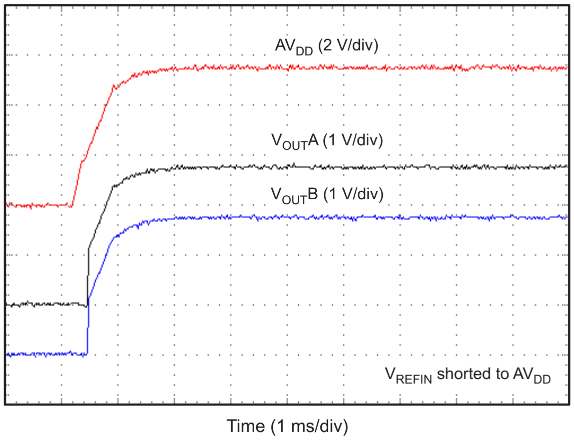


Figure 36. Power-On Glitch, Reset to Midscale

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

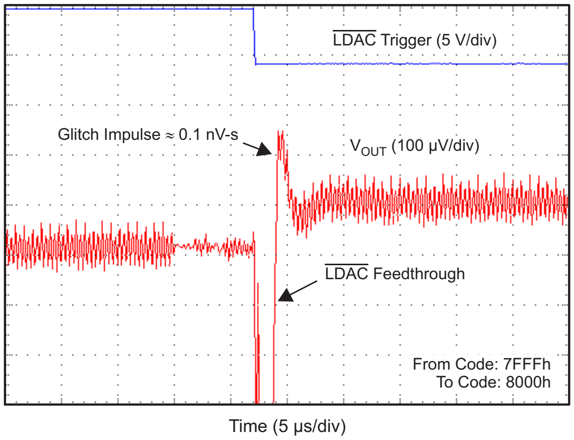


Figure 37. Glitch Impulse, Rising Edge, 1-LSB Step

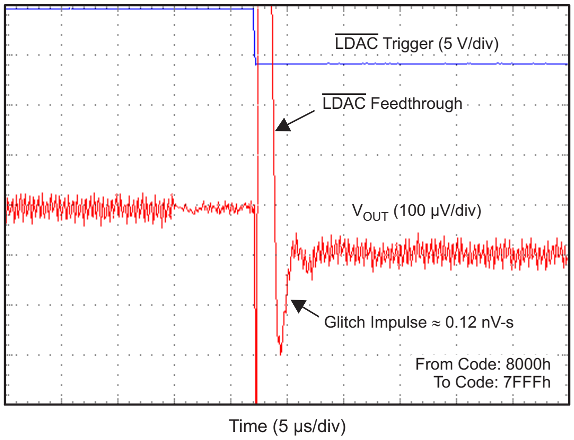


Figure 38. Glitch Impulse, Falling Edge, 1-LSB Step

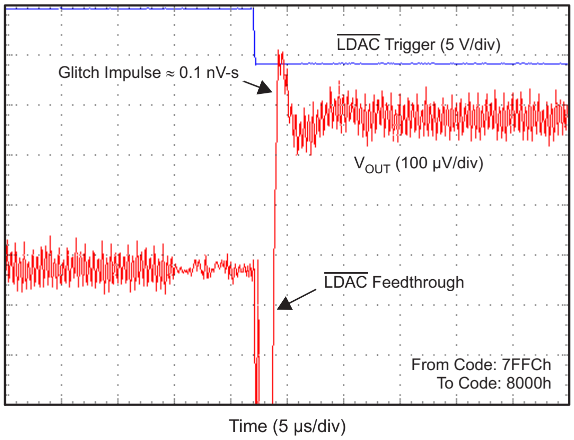


Figure 39. Glitch Impulse, Rising Edge, 4-LSB Step

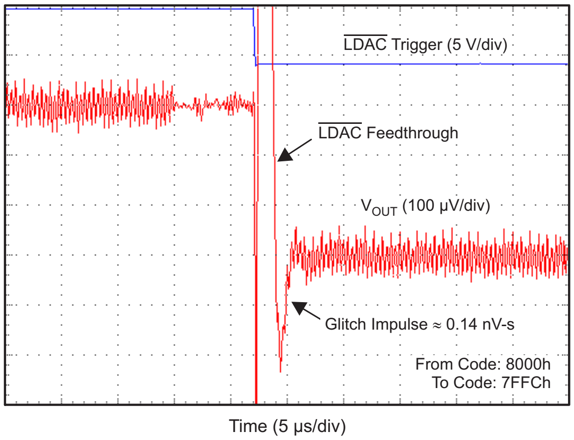


Figure 40. Glitch Impulse, Falling Edge, 4-LSB Step

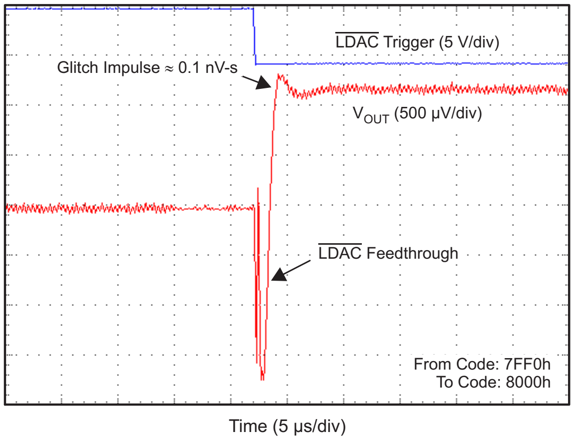


Figure 41. Glitch Impulse, Rising Edge, 16-LSB Step

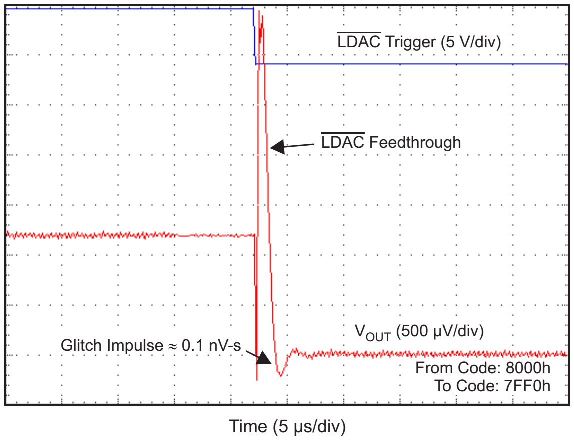


Figure 42. Glitch Impulse, Falling Edge, 16-LSB Step

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

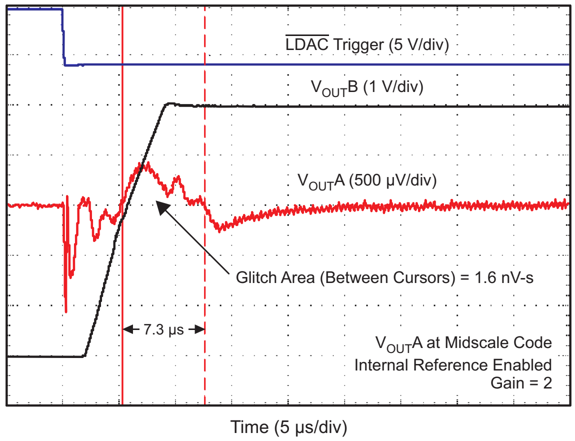


Figure 43. Channel-to-Channel Crosstalk, 5-V Rising Edge

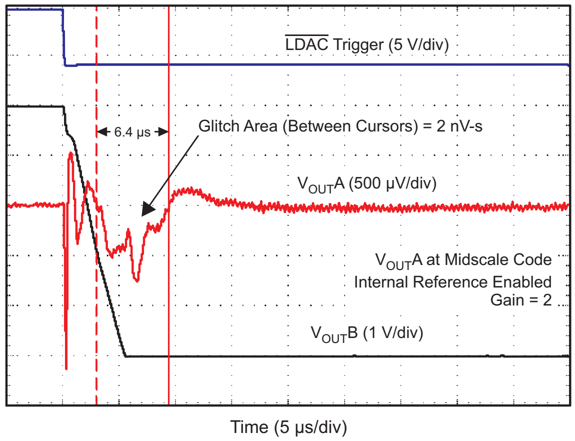


Figure 44. Channel-to-Channel Crosstalk, 5-V Falling Edge

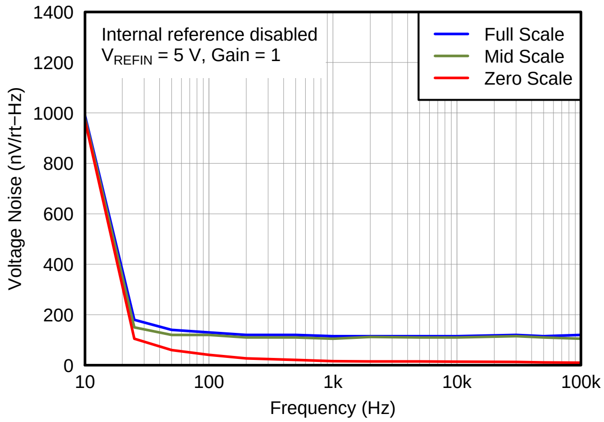


Figure 45. DAC Output Noise Density vs Frequency

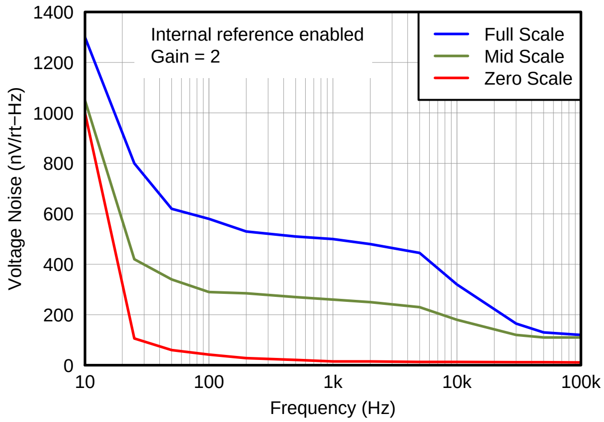


Figure 46. DAC Output Noise Density vs Frequency

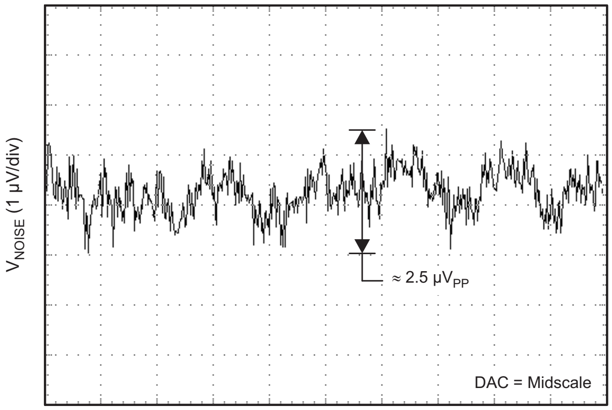


Figure 47. DAC Output Noise, 0.1 Hz to 10 Hz

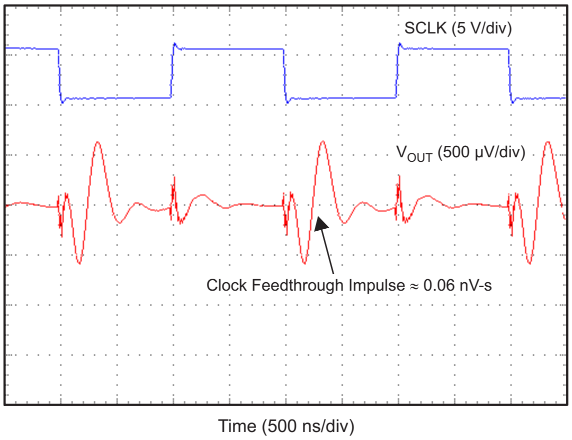


Figure 48. Clock Feedthrough, 500 kHz, Midscale

7.7.3 Typical Characteristics: DAC at AV_{DD} = 3.6 V

At T_A = 25°C, 3.3-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

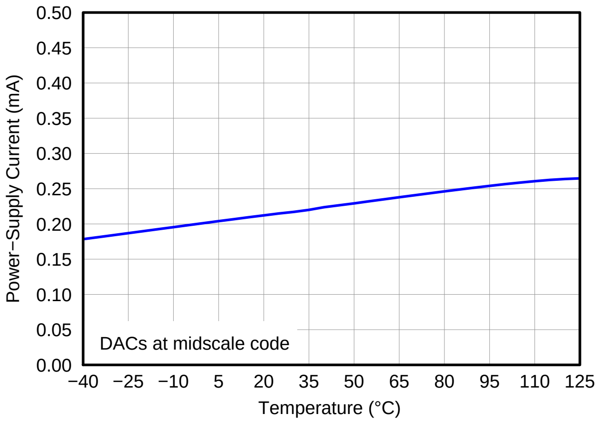


Figure 49. Power-Supply Current vs Temperature

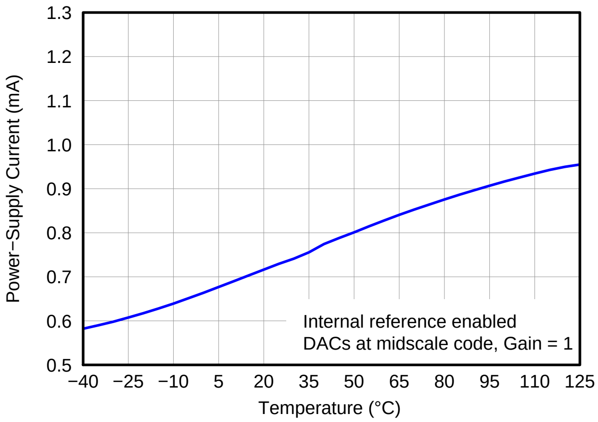


Figure 50. Power-Supply Current vs Temperature

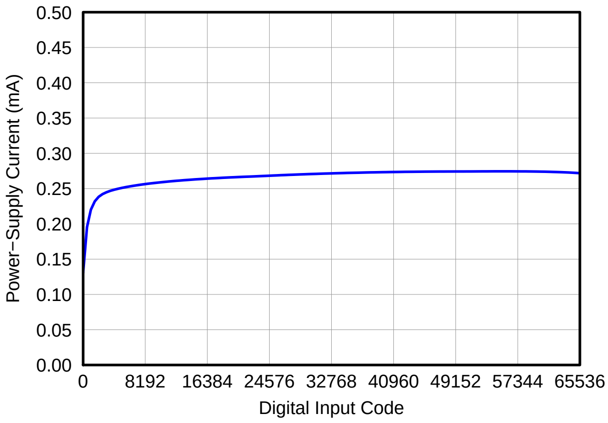


Figure 51. Power-Supply Current vs Digital Input Code

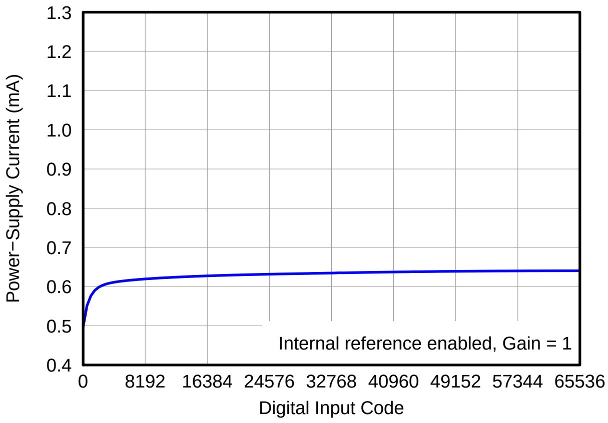


Figure 52. Power-Supply Current vs Digital Input Code

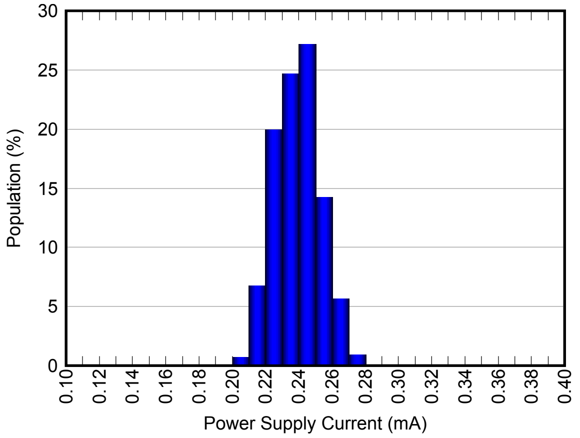


Figure 53. Power-Supply Current Histogram

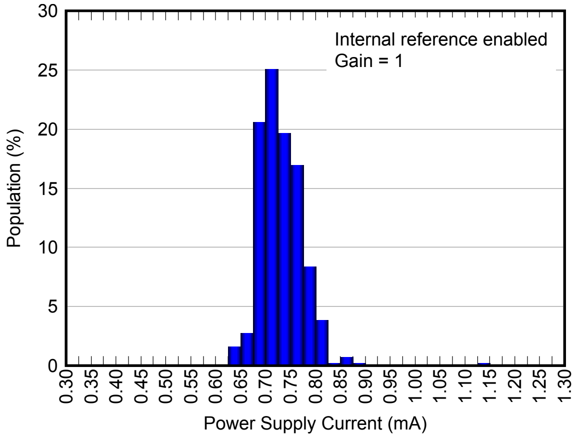


Figure 54. Power-Supply Current Histogram

7.7.4 Typical Characteristics: DAC at AV_{DD} = 2.7 V

At T_A = 25°C, 2.5-V external reference used, gain = 1, and DAC output not loaded, unless otherwise noted.

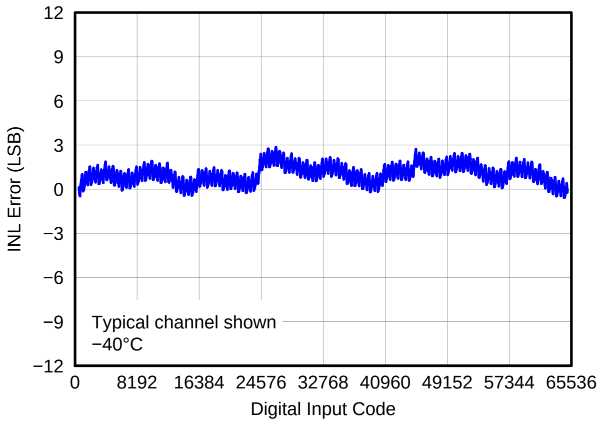


Figure 55. Linearity Error vs Digital Input Code (–40°C)

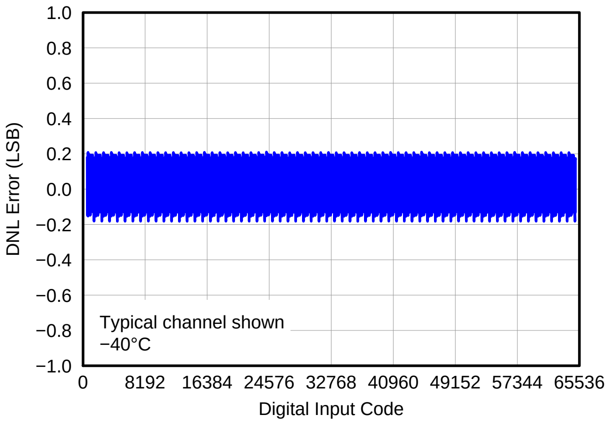


Figure 56. Differential Linearity Error vs Digital Input Code (–40°C)

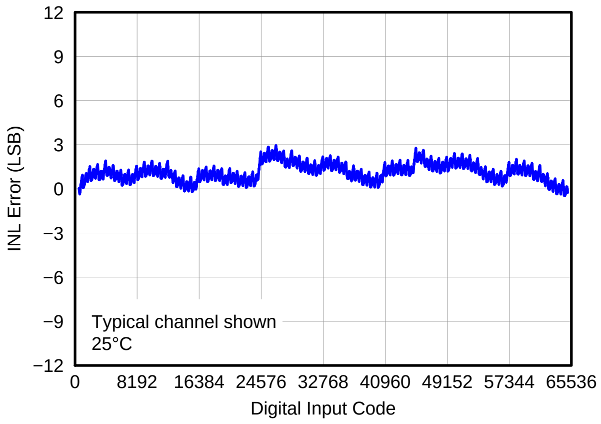


Figure 57. Linearity Error vs Digital Input Code (25°C)

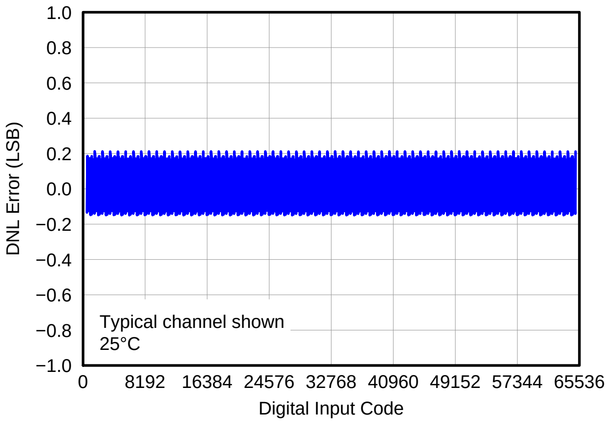


Figure 58. Differential Linearity Error vs Digital Input Code (25°C)

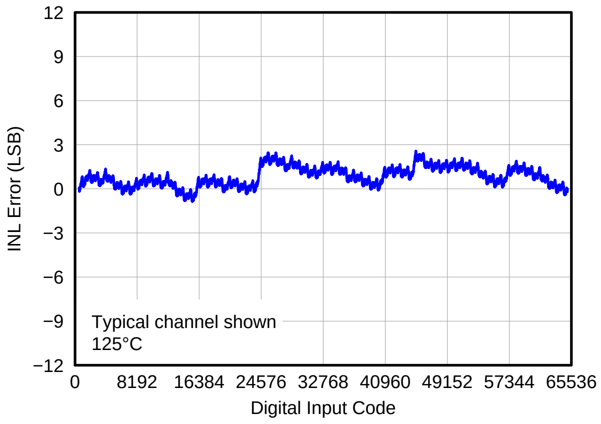


Figure 59. Linearity Error vs Digital Input Code (125°C)

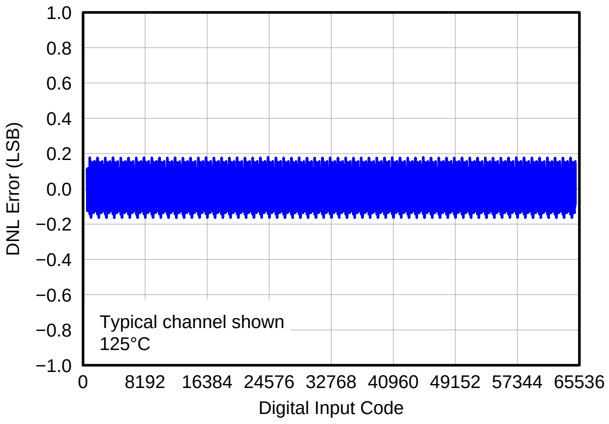


Figure 60. Differential Linearity Error vs Digital Input Code (125°C)

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1, and DAC output not loaded, unless otherwise noted.

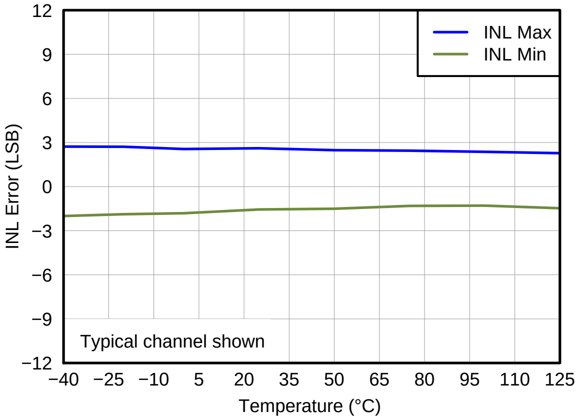


Figure 61. Linearity Error vs Temperature

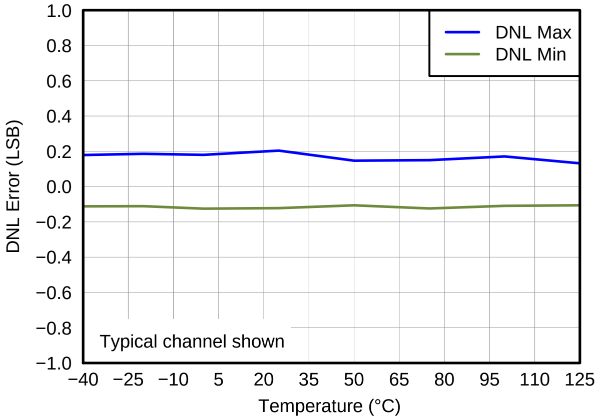


Figure 62. Differential Linearity Error vs Temperature

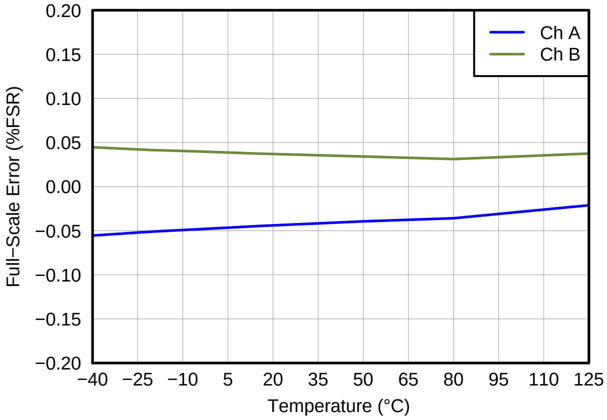


Figure 63. Full-Scale Error vs Temperature

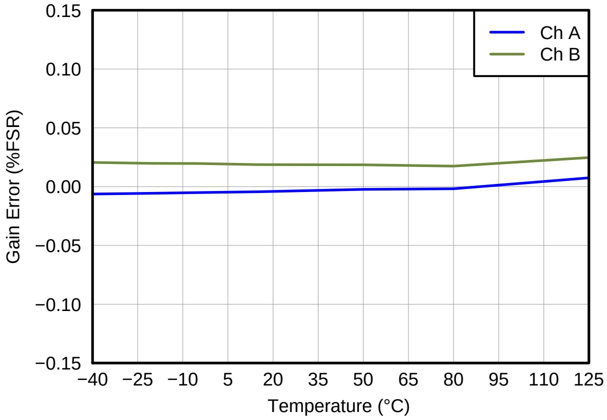


Figure 64. Gain Error vs Temperature

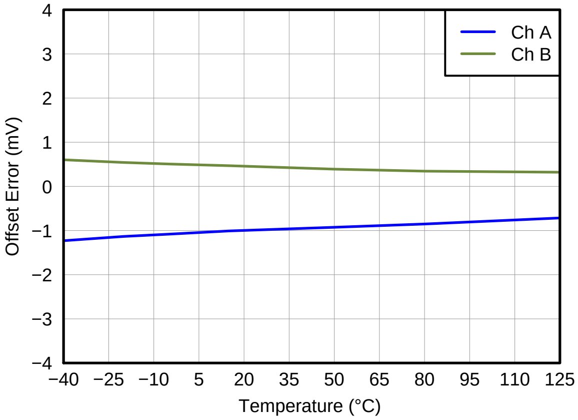


Figure 65. Offset Error vs Temperature

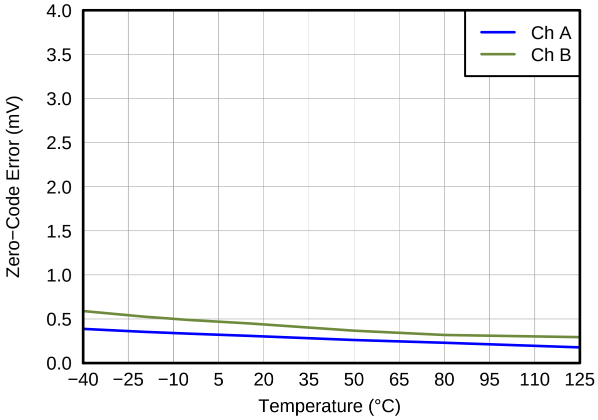


Figure 66. Zero-Code Error vs Temperature

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1, and DAC output not loaded, unless otherwise noted.

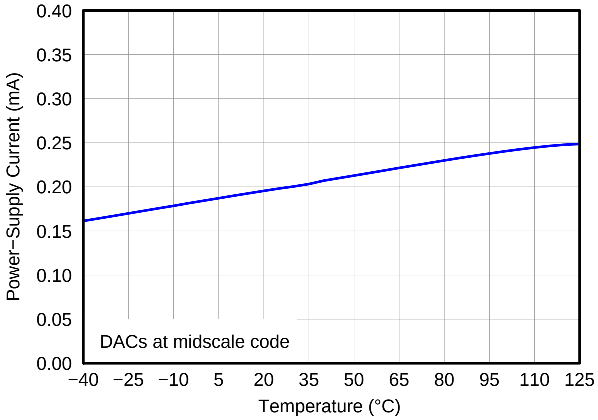


Figure 67. Power-Supply Current vs Temperature

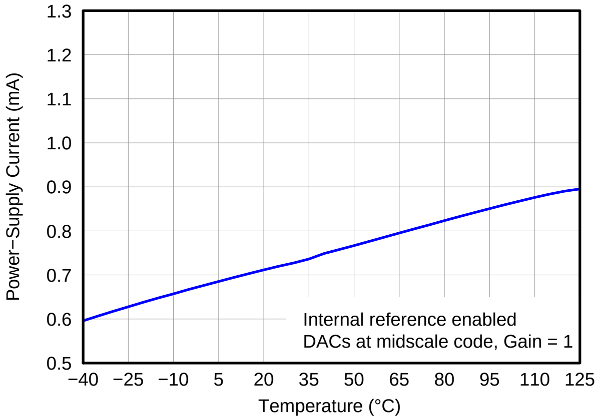


Figure 68. Power-Supply Current vs Temperature

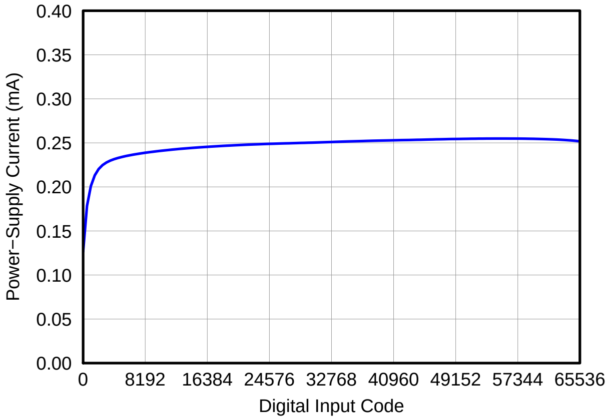


Figure 69. Power-Supply Current vs Digital Input Code

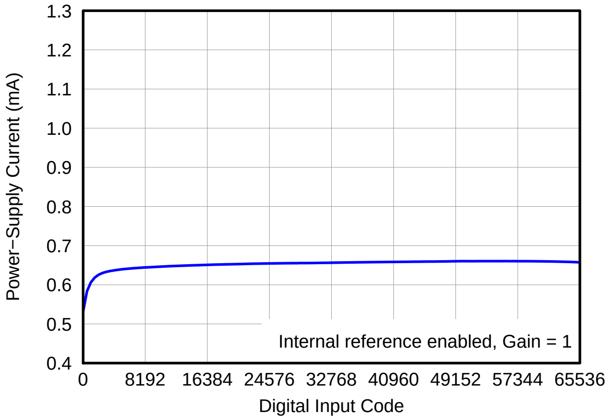


Figure 70. Power-Supply Current vs Digital Input Code

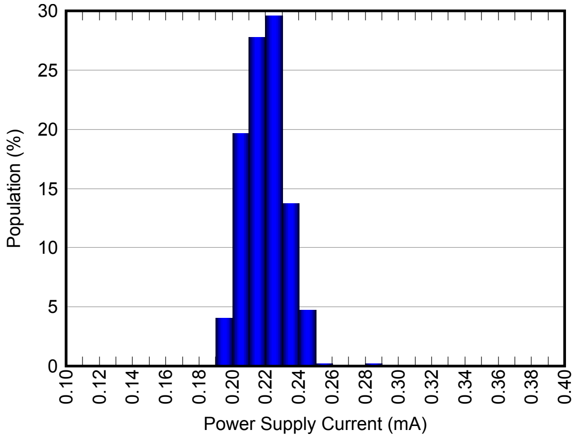


Figure 71. Power-Supply Current Histogram

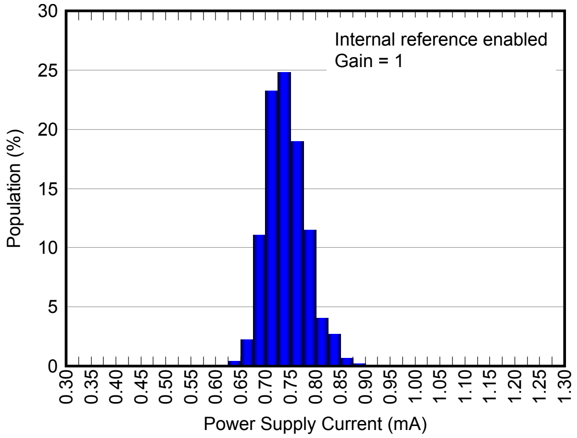


Figure 72. Power-Supply Current Histogram

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1, and DAC output not loaded, unless otherwise noted.

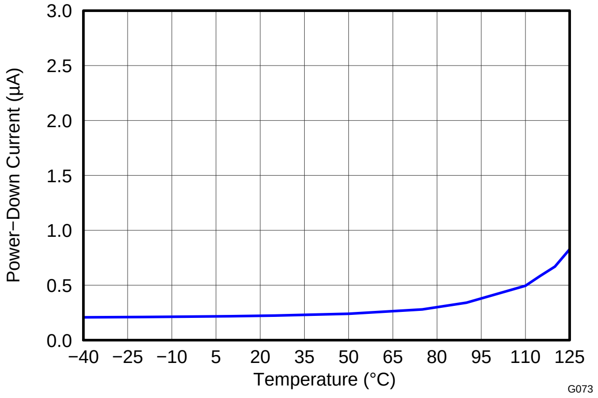


Figure 73. Power-Down Current vs Temperature

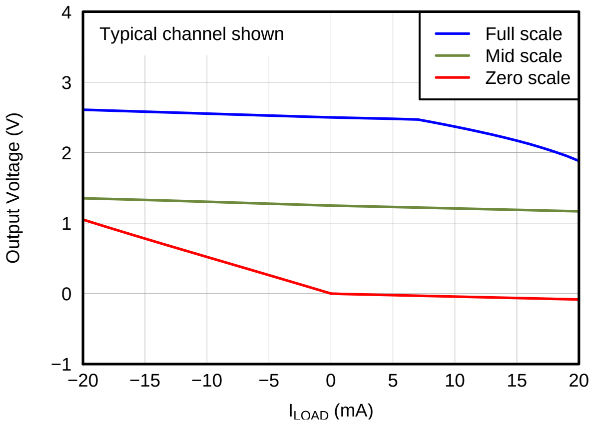


Figure 74. DAC Output Voltage vs Load Current

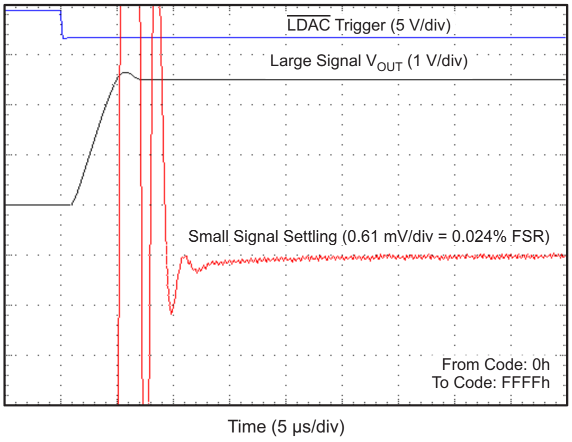


Figure 75. Full-Scale Settling Time, Rising Edge

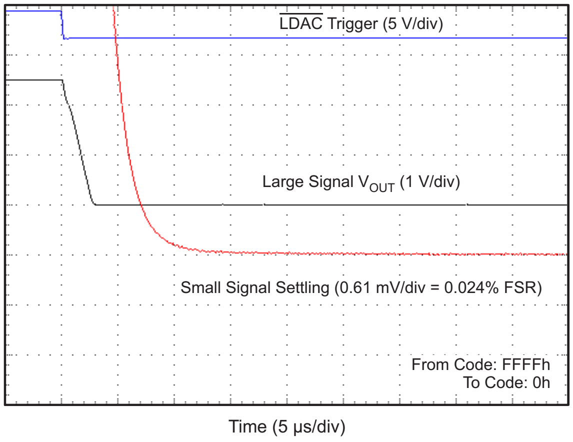


Figure 76. Full-Scale Settling Time, Falling Edge

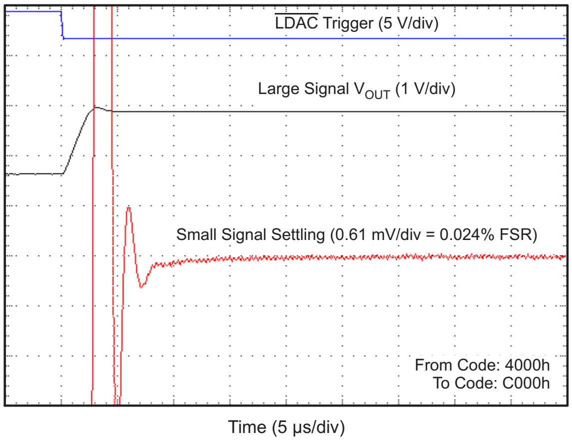


Figure 77. Half-Scale Settling Time, Rising Edge

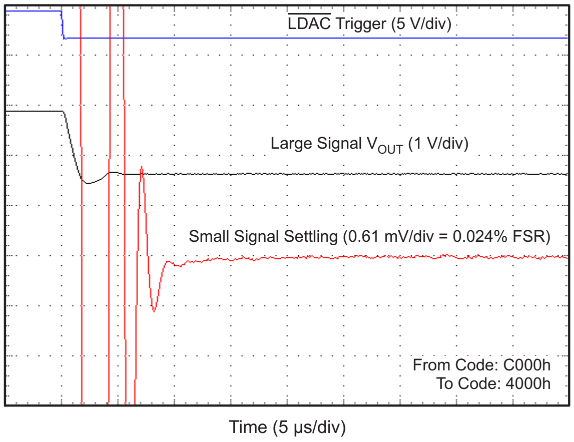


Figure 78. Half-Scale Settling Time, Falling Edge

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1, and DAC output not loaded, unless otherwise noted.

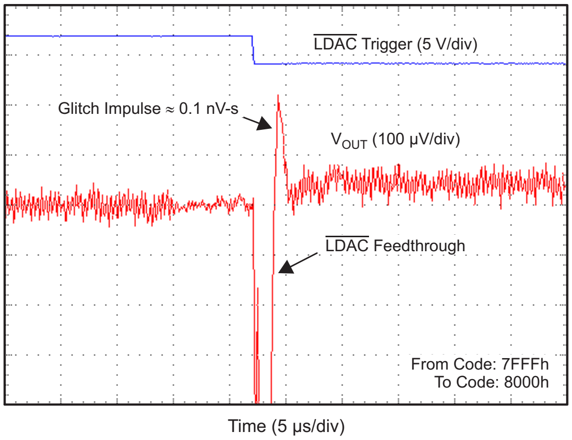


Figure 79. Glitch Impulse, Rising Edge, 1-LSB Step

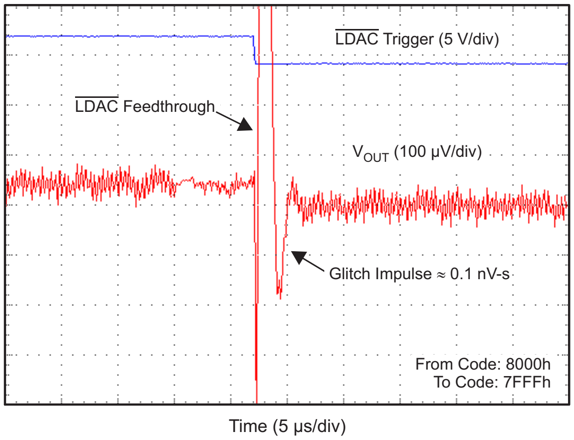


Figure 80. Glitch Impulse, Falling Edge, 1-LSB Step

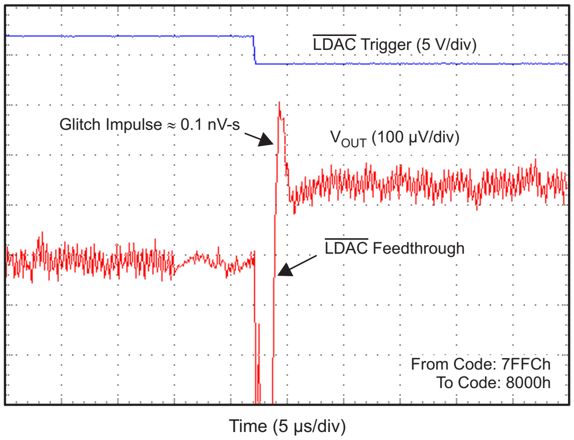


Figure 81. Glitch Impulse, Rising Edge, 4-LSB Step

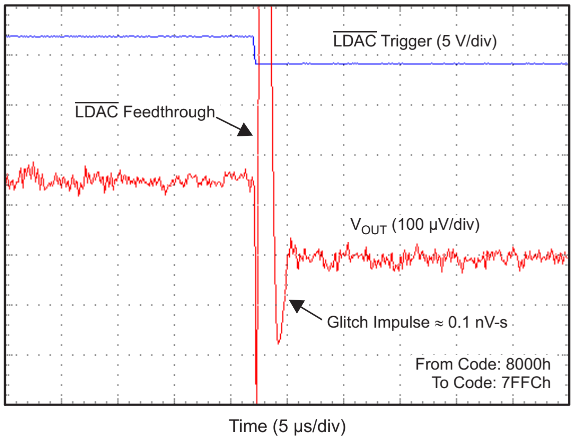


Figure 82. Glitch Impulse, Falling Edge, 4-LSB Step

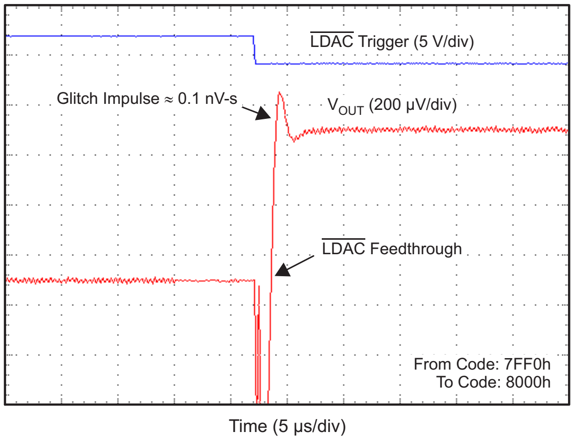


Figure 83. Glitch Impulse, Rising Edge, 16-LSB Step

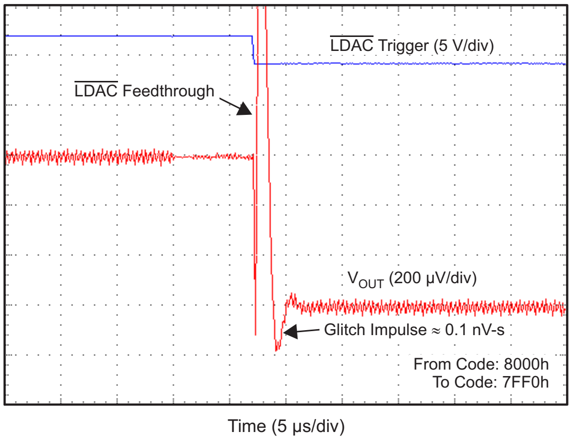


Figure 84. Glitch Impulse, Falling Edge, 16-LSB Step

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1, and DAC output not loaded, unless otherwise noted.

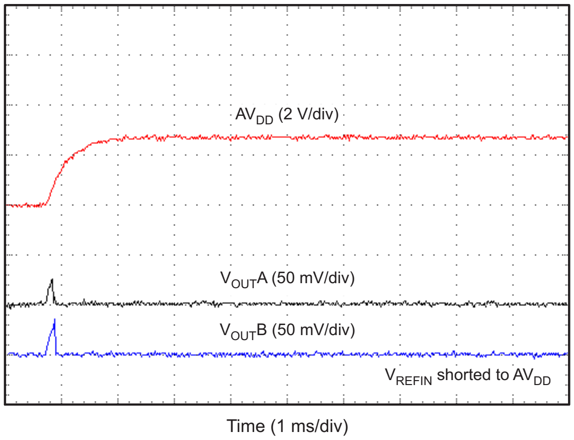


Figure 85. Power-On Glitch, Reset to Zero Scale

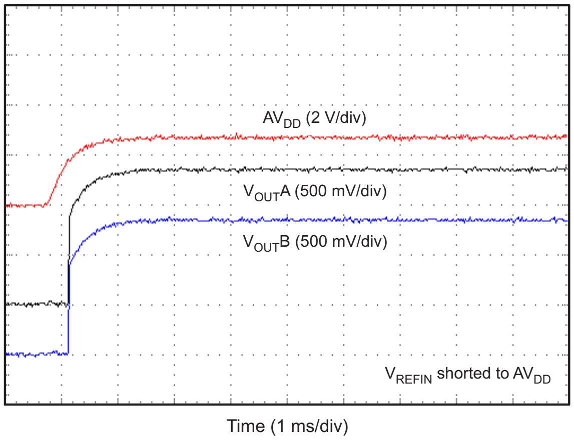


Figure 86. Power-On Glitch, Reset to Midscale

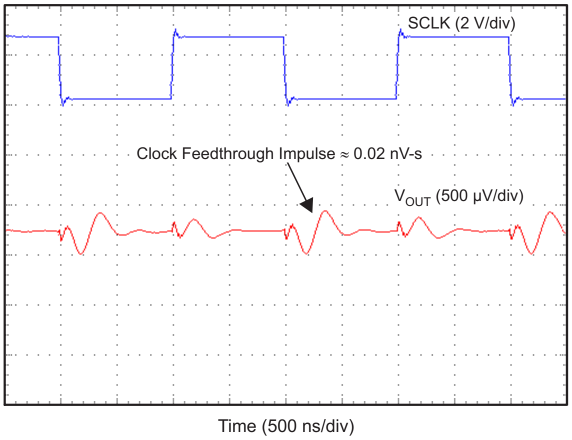


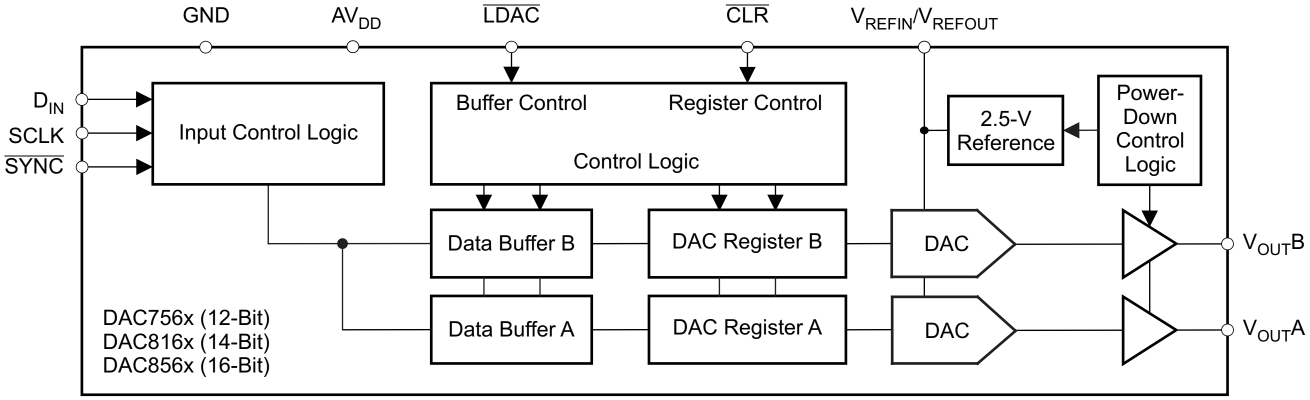
Figure 87. Clock Feedthrough, 500 kHz, Midscale

8 Detailed Description

8.1 Overview

The DAC756x, DAC816x, and DAC856x devices are low-power, voltage-output, dual-channel, 16-, 14-, and 12-bit digital-to-analog converters (DACs), respectively. These devices include a 2.5-V, 4-ppm/°C internal reference, giving a full-scale output voltage range of 2.5 V or 5 V. The internal reference has an initial accuracy of ±5 mV and can source or sink up to 20 mA at the V_{REFIN}/V_{REFOUT} pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Digital-to-Analog Converter (DAC)

The DAC756x, DAC816x, and DAC856x architecture consists of two string DACs, each followed by an output buffer amplifier. The devices include an internal 2.5-V reference with 4-ppm/°C temperature drift performance. Figure 88 shows a principal block diagram of the DAC architecture.

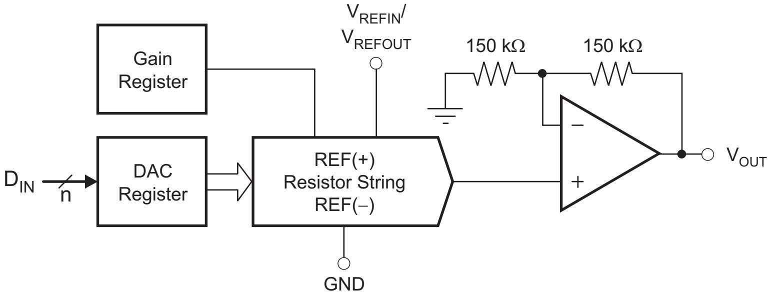


Figure 88. DAC Architecture

The input coding to the DAC756x, DAC816x, and DAC856x devices is straight binary, so the ideal output voltage is given by Equation 1:

$$V_{OUT} = \left(\frac{D_{IN}}{2^n}\right) \times V_{REF} \times \text{Gain} \tag{1}$$

where:

n = resolution in bits; either 12 (DAC756x), 14 (DAC816x) or 16 (DAC856x)

D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register. D_{IN} ranges from 0 to 2^n – 1.

V_{REF} = DAC reference voltage; either V_{REFOUT} from the internal 2.5-V reference or V_{REFIN} from an external reference.

Gain = 1 by default when internal reference is disabled (using external reference), and gain = 2 by default when using internal reference. Gain can also be manually set to either 1 or 2 using the gain register. See the *Gain Function* section for more information.

Feature Description (continued)

8.3.1.1 Resistor String

The resistor string section is shown in Figure 89. It is simply a string of resistors, each of value *R*. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. The resistor string architecture results in monotonicity. The $R_{DIVIDER}$ switch is controlled by the gain registers (see the *Gain Function* section). Because the output amplifier has a gain of 2, $R_{DIVIDER}$ is not shorted when the DAC-n gain is set to 1 (default if internal reference is disabled), and is shorted when the DAC-n gain is set to 2 (default if internal reference is enabled).

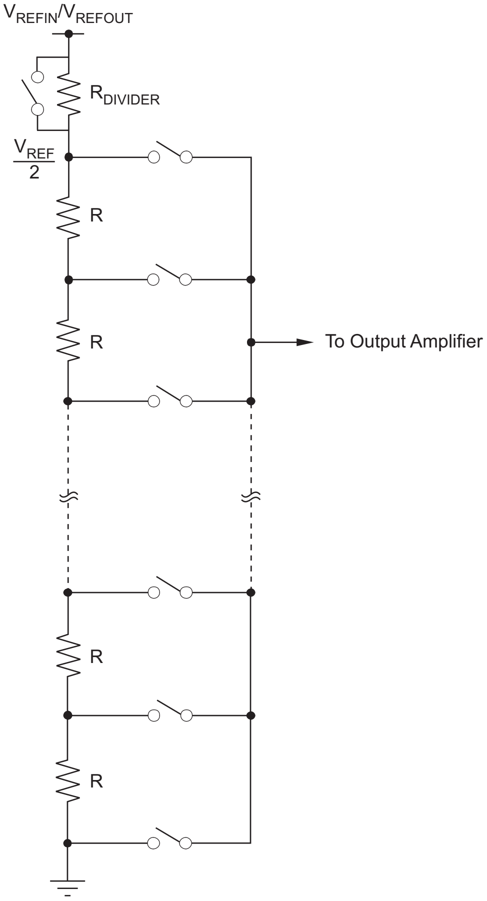


Figure 89. Resistor String

8.3.1.2 Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving a maximum output range of 0 V to AV_{DD}. It is capable of driving a load of 2 kΩ in parallel with 3 nF to GND. The typical slew rate is 0.75 V/µs, with a typical full-scale settling time of 14 µs as shown in Figure 31, Figure 32, Figure 75 and Figure 76.

Feature Description (continued)

8.3.2 Internal Reference

The DAC756x, DAC816x, and DAC856x devices include a 2.5-V internal reference that is disabled by default. The internal reference is externally available at the V_{REFIN}/V_{REFOUT} pin. The internal reference output voltage is 2.5 V and can sink and source up to 20 mA.

A minimum 150-nF capacitor is recommended between the reference output and GND for noise filtering.

The internal reference of the DAC756x, DAC816x, and DAC856x devices is a bipolar transistor-based precision band-gap voltage reference. Figure 90 shows the basic band-gap topology. Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2. The difference of the two base-emitter voltages ($V_{BE1} – V_{BE2}$) has a positive temperature coefficient and is forced across resistor R_1. This voltage is amplified and added to the base-emitter voltage of Q_2, which has a negative temperature coefficient. The resulting output voltage is virtually independent of temperature. The short-circuit current is limited by design to approximately 100 mA.

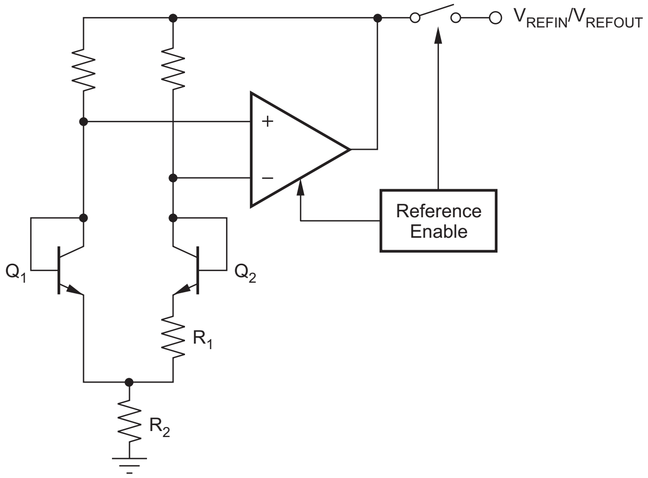


Figure 90. Band-Gap Reference Simplified Schematic

8.3.3 Power-On Reset

8.3.3.1 Power-On Reset to Zero-Scale

The DAC7562, DAC8162, and DAC8562 devices contain a power-on-reset circuit that controls the output voltage during power up. All device registers are reset as shown in Table 4. At power up, all DAC registers are filled with zeros and the output voltages of all DAC channels are set to zero volts. Each DAC channel remains that way until a valid load command is written to it. The power-on reset is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up. No device pin should be brought high before applying power to the device. The internal reference is disabled by default and remains that way until a valid reference-change command is executed.

8.3.3.2 Power-On Reset to Mid-Scale

The DAC7563, DAC8163, and DAC8563 devices contain a power-on reset circuit that controls the output voltage during power up. At power up, all DAC registers are reset to mid-scale code and the output voltages of all DAC channels are set to V_{REFIN} / 2 volts. Each DAC channel remains that way until a valid load command is written to it. The power-on reset is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up. No device pin should be brought high before applying power to the device. The internal reference is powered off or down by default and remains that way until a valid reference-change command is executed. If using an external reference, it is acceptable to power on the V_{REFIN} pin either at the same time as or after applying AV_{DD}.

Table 4. DACxx62 and DACxx63 Power-On Reset Values

REGISTER	DEFAULT SETTING	
DAC and input registers	DACxx62	Zero-scale
	DACxx63	Mid-scale
LDAC registers	$\overline{\text{LDAC}}$ pin enabled for both channels	
Power-down registers	DACs powered up	
Internal reference register	Internal reference disabled	
Gain registers	Gain = 1 for both channels	

8.3.3.3 Power-On Reset (POR) Levels

When the device powers up, a POR circuit sets the device in default mode as shown in Table 4. The POR circuit requires specific AV_{DD} levels, as indicated in Figure 91, to ensure discharging of internal capacitors and to reset the device on power up. In order to ensure a power-on reset, AV_{DD} must be below 0.7 V for at least 1 ms. When AV_{DD} drops below 2.2 V but remains above 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, TI recommends a power-on reset. When AV_{DD} remains above 2.2 V, a power-on reset does not occur.

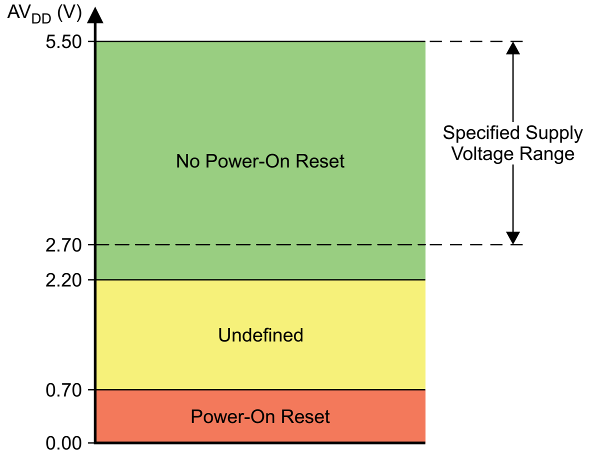


Figure 91. Relevant Voltage Levels for POR Circuit

8.4 Device Functional Modes

8.4.1 Power-Down Modes

The DAC756x, DAC816x, and DAC856x devices have two separate sets of power-down commands. One set is for the DAC channels and the other set is for the internal reference. The internal reference is forced to a powered-down state while both DAC channels are powered down, and is only enabled if any DAC channel is also in the normal mode of operation. For more information on the internal reference control, see the *Internal Reference Enable Register* section.

8.4.1.1 DAC Power-Down Commands

The DAC756x, DAC816x, and DAC856x DACs use four modes of operation. These modes are accessed by setting the serial interface command bits to 100. Once the command bits are set correctly, the four different power-down modes are software programmable by setting bits DB5 and DB4 in the shift register. Table 5 and Table 6 show the different power-down options. For more information on how to set the DAC operating mode see Table 17.

Table 5. DAC-n Operating Modes

DB5	DB4	DAC Modes of Operation
0	0	Selected DACs power up (normal mode, default)
0	1	Selected DACs power down, output 1 kΩ to GND
1	0	Selected DACs power down, output 100 kΩ to GND
1	1	Selected DACs power down, output Hi-Z to GND

Table 6. DAC-n Selection for Operating Modes

DAC-B (DB1), DAC-A (DB0)	Operating Mode
0	DAC-n does not change operating mode
1	DAC-n operating mode set to value on PD1 and PD0

It is possible to write to the DAC register or buffer of the DAC channel that is powered down. When the DAC channel is then powered up, it powers up to this new value.

The advantage of the available power-down modes is that the output impedance of the device is known while it is in power-down mode. As described in Table 5, there are three different power-down options. V_{OUT} can be connected internally to GND through a 1-kΩ resistor, a 100-kΩ resistor, or open-circuited (Hi-Z). The DAC power-down circuitry is shown in Figure 92.

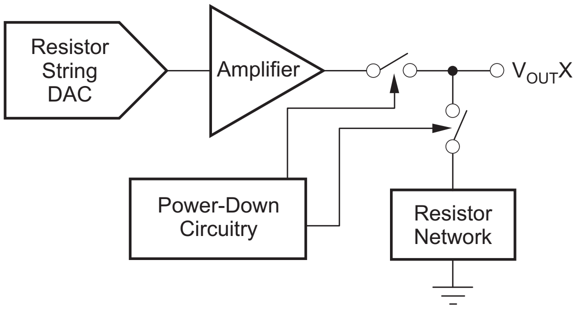


Figure 92. Output Stage

8.4.2 Gain Function

The gain register controls the GAIN setting in the DAC transfer function:

$$V_{OUT} = \left(\frac{D_{IN}}{2^n}\right) \times V_{REF} \times \text{Gain} \tag{2}$$

The DAC756x, DAC816x, and DAC856x devices have a gain register for each channel. The gain for each channel, in Equation 2, is either 1 or 2. This gain is automatically set to 2 when using the internal reference, and is automatically set to 1 when the internal reference is disabled (default). However, each channel can have either gain by setting the registers appropriately. The gain registers are accessible by setting the serial interface command bits to 000, address bits to 010, and using DB1 for DAC-B and DB0 for DAC-A. See Table 7 and Table 17 for the full command structure. The gain registers are automatically reset to provide either gain of 1 or 2 when the internal reference is powered off or on, respectively. After the reference is powered off or on, the gain register is again accessible to change the gain.

Table 7. DAC-n Selection for Gain Register Command

DB1, DB0	Value	Gain
DB0	0	DAC-A uses gain = 2 (default with internal reference)
	1	DAC-A uses gain = 1 (default with external reference)
DB1	0	DAC-B uses gain = 2 (default with internal reference)
	1	DAC-B uses gain = 1 (default with external reference)

8.4.3 Software Reset Function

The DAC756x, DAC816x, and DAC856x devices contain a software reset feature. The software reset function is accessed by setting the serial interface command bits to 101. The software reset command contains two reset modes which are software-programmable by setting bit DB0 in the shift register. Table 8 and Table 17 show the available software reset commands.

Table 8. Software Reset

DB0	Registers Reset to Default Values
0	DAC registers Input registers
1	DAC registers Input registers LDAC registers Power-down registers Internal reference register Gain registers

8.4.4 Internal Reference Enable Register

The internal reference in the DAC756x, DAC816x, and DAC856x devices is disabled by default for debugging, evaluation purposes, or when using an external reference. The internal reference can be powered up and powered down by setting the serial interface command bits to 111 and configuring DB0 (see Table 9). The internal reference is forced to a powered down state while both DAC channels are powered down, and can only be enabled if any DAC channel is in normal mode of operation. During the time that the internal reference is disabled, the DAC functions normally using an external reference. At this point, the internal reference is disconnected from the V_{REFIN}/V_{REFOUT} pin (Hi-Z output).

Table 9. Internal Reference

DB0	Internal Reference Configuration
0	Disable internal reference and reset DACs to gain = 1
1	Enable internal reference and reset DACs to gain = 2

8.4.4.1 Enabling Internal Reference

To enable the internal reference, refer to the command structure in Table 17. When performing a power cycle to reset the device, the internal reference is switched off (default mode). In the default mode, the internal reference is powered down until a valid write sequence powers up the internal reference. However, the internal reference is forced to a disabled state while both DAC channels are powered down, and remains disabled until either DAC channel is returned to the normal mode of operation. See *DAC Power-Down Commands* for more information on DAC channel modes of operation.

8.4.4.2 Disabling Internal Reference

To disable the internal reference, refer to the command structure in Table 17. When performing a power cycle to reset the device, the internal reference is disabled (default mode).

8.4.5 CLR Functionality

The edge-triggered $\overline{CLR}$ pin can be used to set the input and DAC registers immediately according to Table 10. When the $\overline{CLR}$ pin receives a falling edge signal the clear mode is activated and changes the DAC output voltages accordingly. The device exits clear mode on the 24th falling edge of the next write to the device. If the $\overline{CLR}$ pin receives a falling edge signal during a write sequence in normal operation, the clear mode is activated and changes the input and DAC registers immediately according to Table 10.

Table 10. Clear Mode Reset Values

DEVICE	DAC Output Entering Clear Mode
DAC8562, DAC8162, DAC7562	Zero-scale
DAC8563, DAC8163, DAC7563	Mid-scale

8.4.6 LDAC Functionality

The DAC756x, DAC816x, and DAC856x devices offer both a software and hardware simultaneous update and control function. The DAC double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs.

DAC756x, DAC816x, and DAC856x data updates can be performed either in *synchronous* or in *asynchronous* mode.

In *asynchronous* mode, the $\overline{\text{LDAC}}$ pin is used as a negative edge-triggered timing signal for simultaneous DAC updates. Multiple single-channel writes can be done in order to set different channel buffers to desired values and then make a falling edge on $\overline{\text{LDAC}}$ pin to simultaneously update the DAC output registers. Data buffers of all channels must be loaded with desired data before an $\overline{\text{LDAC}}$ falling edge. After a high-to-low $\overline{\text{LDAC}}$ transition, all DACs are simultaneously updated with the last contents of the corresponding data buffers. If the content of a data buffer is not changed, the corresponding DAC output remains unchanged after the $\overline{\text{LDAC}}$ pin is triggered. $\overline{\text{LDAC}}$ must be returned high before the next serial command is initiated.

In *synchronous* mode, data are updated with the falling edge of the 24th SCLK cycle, which follows a falling edge of $\overline{\text{SYNC}}$. For such *synchronous* updates, the $\overline{\text{LDAC}}$ pin is not required, and it must be connected to GND permanently or asserted and held low before sending commands to the device.

Alternatively, all DAC outputs can be updated simultaneously using the built-in software function of LDAC. The LDAC register offers additional flexibility and control by allowing the selection of which DAC channel(s) should be updated simultaneously when the $\overline{\text{LDAC}}$ pin is being brought low. The LDAC register is loaded with a 2-bit word (DB1 and DB0) using command bits C2, C1, and C0 (see Table 17). The default value for each bit, and therefore for each DAC channel, is zero. If the LDAC register bit is set to 1, it overrides the $\overline{\text{LDAC}}$ pin (the $\overline{\text{LDAC}}$ pin is internally tied low for that particular DAC channel) and this DAC channel updates synchronously after the falling edge of the 24th SCLK cycle. However, if the LDAC register bit is set to 0, the DAC channel is controlled by the $\overline{\text{LDAC}}$ pin.

The combination of software and hardware simultaneous update functions is particularly useful in applications when updating a DAC channel, while keeping the other channel unaffected; see Table 11 and Table 17 for more information.

Table 11. DAC-n Selection for LDAC Register Command

DB1, DB0	Value	$\overline{\text{LDAC}}$ Pin Functionality
DB0	0	DAC-A uses $\overline{\text{LDAC}}$ pin
	1	DAC-A operates in synchronous mode
DB1	0	DAC-B uses $\overline{\text{LDAC}}$ pin
	1	DAC-B operates in synchronous mode

8.5 Programming

The DAC756x, DAC816x, and DAC856x devices have a three-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and D_{IN}; see the table) compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See the Serial Write Operation timing diagram (Figure 1) for an example of a typical write sequence.

The DAC756x, DAC816x, or DAC856x input shift register is 24 bits wide, consisting of two *don't care* bits (DB23 to DB22), three command bits (DB21 to DB19), three address bits (DB18 to DB16), and 16 data bits (DB15 to DB0). All 24 bits of data are loaded into the DAC under the control of the serial clock input, SCLK. DB23 (MSB) is the first bit that is loaded into the DAC shift register. DB23 is followed by the rest of the 24-bit word pattern, left-aligned. This configuration means that the first 24 bits of data are latched into the shift register, and any further clocking of data is ignored.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the D_{IN} line are clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the DAC756x, DAC816x, and DAC856x devices compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked into the shift register and the shift register locks. Further clocking does not change the shift register data.

After receiving the 24th falling clock edge, the DAC756x, DAC816x, and DAC856x devices decode the three command bits, three address bits and 16 data bits to perform the required function, without waiting for a $\overline{\text{SYNC}}$ rising edge. After the 24th falling edge of SCLK is received, the $\overline{\text{SYNC}}$ line may be kept low or brought high. In either case, the minimum delay time from the 24th falling SCLK edge to the next falling $\overline{\text{SYNC}}$ edge must be met in order to begin the next cycle properly; see the Serial Write Operation timing diagram (Figure 1).

A rising edge of $\overline{\text{SYNC}}$ before the 24-bit sequence is complete resets the SPI interface; no data transfer occurs. A new write sequence starts at the next falling edge of $\overline{\text{SYNC}}$. To assure the lowest power consumption of the device, care should be taken that the levels are as close to each rail as possible.

8.5.1 $\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line stays low for at least 24 falling edges of SCLK and the addressed DAC register updates on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 23rd falling edge, it acts as an interrupt to the write sequence; the shift register resets and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents, nor a change in the operating mode occurs (as shown in Figure 93).

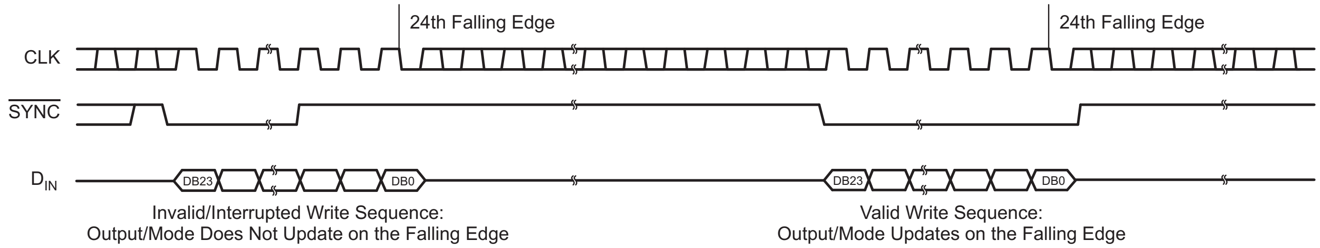


Figure 93. $\overline{\text{SYNC}}$ Interrupt Facility

Programming (continued)

8.5.2 DAC Register Configuration

When the DAC registers are being written to, the DAC756x, DAC816x, and DAC856x devices receive all 24 bits of data, ignore DB23 and DB22, and decode the next three bits (DB21 to DB19) in order to determine the DAC operating or control mode (see Table 12). Bits DB18 to DB16 are used to address the DAC channels (see Table 13).

Table 12. Commands for the DAC756x, DAC816x, and DAC856x Devices

C2 (DB21)	C1 (DB20)	C0 (DB19)	Command
0	0	0	Write to input register n (Table 13)
0	0	1	Software LDAC, update DAC register n (Table 13)
0	1	0	Write to input register n (Table 13) and update all DAC registers
0	1	1	Write to input register n and update DAC register n (Table 13)
1	0	0	Set DAC power up or -down mode
1	0	1	Software reset
1	1	0	Set LDAC registers
1	1	1	Enable or disable the internal reference

Table 13. Address Select for the DAC756x, DAC816x, and DAC856x Devices

A2 (DB18)	A1 (DB17)	A0 (DB16)	Channel (n)
0	0	0	DAC-A
0	0	1	DAC-B
0	1	0	Gain (only use with command 000)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	DAC-A and DAC-B

When writing to the DAC input registers the next 16, 14, or 12 bits of data that follow are decoded by the DAC to determine the equivalent analog output (see Table 14 through Table 16) . The data format is straight binary, with all 0s corresponding to 0-V output and all 1s corresponding to full-scale output. For all documentation purposes, the data format and representation used here is a true 16-bit pattern (that is, FFFFh data word for full scale) that the DAC756x, DAC816x, and DAC856x devices require.

Table 14. DAC856x Data Input Register Format

		COMMAND			ADDRESS			DATA															
X(1)	X	C2	C1	C0	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DB23																							DB0

(1) X' denotes *don't care* bits.

Table 15. DAC816x Data Input Register Format

		COMMAND			ADDRESS			DATA															
X	X	C2	C1	C0	A2	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X
DB23																							DB0

Table 16. DAC756x Data Input Register Format

		COMMAND			ADDRESS			DATA															
X	X	C2	C1	C0	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
DB23																							DB0

In additon to DAC input register updates, the DAC756x, DAC816x, and DAC856x devices support a number of functional mode commands (such as write to LDAC register, power down DACs and so on). The complete set of functional mode commands is shown in Table 17.

Table 17. Command Matrix for the DAC756x, DAC816x, and DAC856x Devices

DB23-DB22	Command			Address			Data						DESCRIPTION
	C2	C1	C0	A2	A1	A0	DB15-DB6	DB5	DB4	DB3-DB2	DB1	DB0	
X[1]	0	0	0	0	0	0	16-, 14-, or 12-bit DAC data						Write to DAC-A input register
				0	0	1	16-, 14-, or 12-bit DAC data						Write to DAC-B input register
				1	1	1	16-, 14-, or 12-bit DAC data						Write to DAC-A and DAC-B input registers
X	0	1	0	0	0	0	16-, 14-, or 12-bit DAC data						Write to DAC-A input register and update all DACs
				0	0	1	16-, 14-, or 12-bit DAC data						Write to DAC-B input register and update all DACs
				1	1	1	16-, 14-, or 12-bit DAC data						Write to DAC-A and DAC-B input register and update all DACs
X	0	1	1	0	0	0	16-, 14-, or 12-bit DAC data						Write to DAC-A input register and update DAC-A
				0	0	1	16-, 14-, or 12-bit DAC data						Write to DAC-B input register and update DAC-B
				1	1	1	16-, 14-, or 12-bit DAC data						Write to DAC-A and DAC-B input register and update all DACs
X	0	0	1	0	0	0	X						Update DAC-A
				0	0	1	X						Update DAC-B
				1	1	1	X						Update all DACs
X	0	0	0	0	1	0	X				0	0	Gain: DAC-B gain = 2, DAC-A gain = 2 (default with internal V_{REF})
											0	1	Gain: DAC-B gain = 2, DAC-A gain = 1
											1	0	Gain: DAC-B gain = 1, DAC-A gain = 2
											1	1	Gain: DAC-B gain = 1, DAC-A gain = 1 (power-on default)
X	1	0	0	X			X	0	0	X	0	1	Power up DAC-A
											1	0	Power up DAC-B
											1	1	Power up DAC-A and DAC-B
X	1	0	0	X			X	0	1	X	0	1	Power down DAC-A; 1 kΩ to GND
											1	0	Power down DAC-B; 1 kΩ to GND
											1	1	Power down DAC-A and DAC-B; 1 kΩ to GND
X	1	0	0	X			X	1	0	X	0	1	Power down DAC-A; 100 kΩ to GND
											1	0	Power down DAC-B; 100 kΩ to GND
											1	1	Power down DAC-A and DAC-B; 100 kΩ to GND
X	1	0	0	X			X	1	1	X	0	1	Power down DAC-A; Hi-Z
											1	0	Power down DAC-B; Hi-Z
											1	1	Power down DAC-A and DAC-B; Hi-Z
X	1	0	1	X			X				X	0	Reset DAC-A and DAC-B input register and update all DACs
											X	1	Reset all registers and update all DACs (Power-on-reset update)
X	1	1	0	X			X				0	0	$\overline{\text{LDAC}}$ pin active for DAC-B and DAC-A
											0	1	$\overline{\text{LDAC}}$ pin active for DAC-B; inactive for DAC-A
											1	0	$\overline{\text{LDAC}}$ pin inactive for DAC-B; active for DAC-A
											1	1	$\overline{\text{LDAC}}$ pin inactive for DAC-B and DAC-A
X	1	1	1	X			X				X	0	Disable internal reference and reset DACs to gain = 1
											X	1	Enable internal reference and reset DACs to gain = 2

(1) *X* denotes *don't care* bits.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 DAC Internal Reference

The internal reference of the DAC756x, DAC816x, and DAC856x devices does not require an external load capacitor for stability because it is stable without any capacitive load. However, for improved noise performance, an external load capacitor of 150 nF or larger connected to the V_{REFIN}/V_{REFOUT} output is recommended. Figure 94 shows the typical connections required for operation of the DAC756x, DAC816x, and DAC856x internal reference. A supply bypass capacitor at the AV_{DD} input is also recommended.

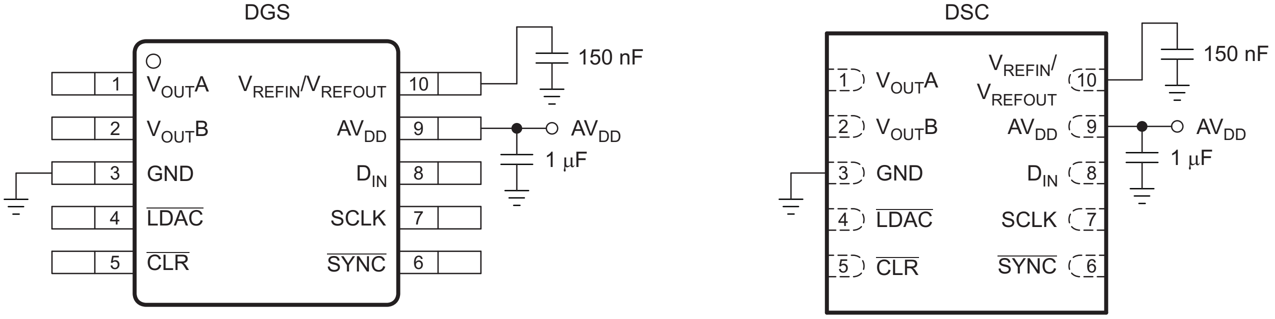


Figure 94. Typical Connections for Operating the DAC756x, DAC816x, and DAC856x Internal Reference

9.1.1.1 Supply Voltage

The internal reference features an extremely low dropout voltage. It can be operated with a supply of only 5 mV above the reference output voltage in an unloaded condition. For loaded conditions, see the *Load Regulation* section. The stability of the internal reference with variations in supply voltage (line regulation, dc PSRR) is also exceptional. Within the specified supply voltage range of 2.7 V to 5.5 V, the variation at V_{REFIN}/V_{REFOUT} is typically 50 µV/V; see Figure 7.

9.1.1.2 Temperature Drift

The internal reference is designed to exhibit minimal drift error, defined as the change in reference output voltage over varying temperature. The drift is calculated using the box method described by Equation 3:

$$\text{Drift Error} = \left(\frac{V_{REF\_MAX} - V_{REF\_MIN}}{V_{REF} \times T_{RANGE}} \right) \times 10^6 \, (\text{ppm}/^\circ\text{C}) \quad (3)$$

where:

V_{REF_MAX} = maximum reference voltage observed within temperature range T_{RANGE}.
V_{REF_MIN} = minimum reference voltage observed within temperature range T_{RANGE}.
V_{REF} = 2.5 V, target value for reference output voltage.
T_{RANGE} = the characterized range from –40°C to 125°C (165°C range)

The internal reference features an exceptional typical drift coefficient of 4 ppm/°C from –40°C to 125°C. Characterizing a large number of units, a maximum drift coefficient of 10 ppm/°C is observed. Temperature drift results are summarized in Figure 3.

Application Information (continued)

9.1.1.3 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise and noise spectral density performance are listed in the *Electrical Characteristics*. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade the ac performance. The output noise spectrum at the V_{REFIN}/V_{REFOUT} pin, both unloaded and with an external 4.7-µF load capacitor, is shown in Figure 6. Internal reference noise impacts the DAC output noise when the internal reference is used.

9.1.1.4 Load Regulation

Load regulation is defined as the change in reference output voltage as a result of changes in load current. The load regulation of the internal reference is measured using force and sense contacts as shown in Figure 95. The force and sense lines reduce the impact of contact and trace resistance, resulting in accurate measurement of the load regulation contributed solely by the internal reference. Measurement results are shown in Figure 4. Force and sense lines should be used for applications that require improved load regulation.

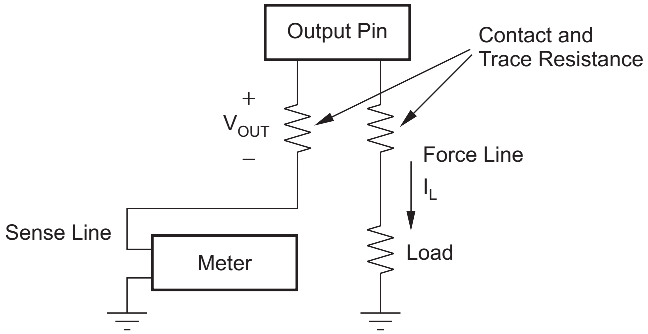


Figure 95. Accurate Load Regulation of the DAC756x, DAC816x, and DAC856x Internal Reference

9.1.1.4.1 Long-Term Stability

Long-term stability or aging refers to the change of the output voltage of a reference over a period of months or years. This effect lessens as time progresses. The typical drift value for the internal reference is listed in the *Electrical Charateristics* and measurement results are shown in Figure 5. This parameter is characterized by powering up multiple devices and measuring them at regular intervals.

9.1.1.5 Thermal Hysteresis

Thermal hysteresis for a reference is defined as the change in output voltage after operating the device at 25°C, cycling the device through the operating temperature range, and returning to 25°C. Hysteresis is expressed by Equation 4:

$$V_{HYST} = \left[\frac{V_{REF\_PRE} - V_{REF\_POST}}{V_{REF\_NOM}}\right] \times 10^6 (\text{ppm}/°\text{C}) \quad (4)$$

where:

V_{HYST} = thermal hysteresis.
V_{REF_PRE} = output voltage measured at 25°C pre-temperature cycling.
V_{REF_POST} = output voltage measured after the device cycles through the temperature range of –40°C to 125°C, and returns to 25°C.
V_{REF_NOM} = 2.5 V, target value for reference output voltage.

9.1.2 DAC Noise Performance

Output noise spectral density at the V_{OUT}-n pin versus frequency is depicted in Figure 45 and Figure 46 for full-scale, mid-scale, and zero-scale input codes. The typical noise density for mid-scale code is 90 nV/√Hz at 1 kHz. High-frequency noise can be improved by filtering the reference noise. Integrated output noise between 0.1 Hz and 10 Hz is close to 2.5 µV_{PP} (mid-scale), as shown in Figure 47.

9.2 Typical Applications

9.2.1 Combined Voltage and Current Analog Output Module Using the XTR300

The design features two independent outputs that can source and sink voltage and current over the standard industrial output ranges. The possible outputs of the design include: –24 mA to 24 mA, 4 mA–20 mA, 0 mA to 24 mA, 0 V to 5 V, 0 V to 10 V, –5 V to5 V, and –10 V to 10 V.

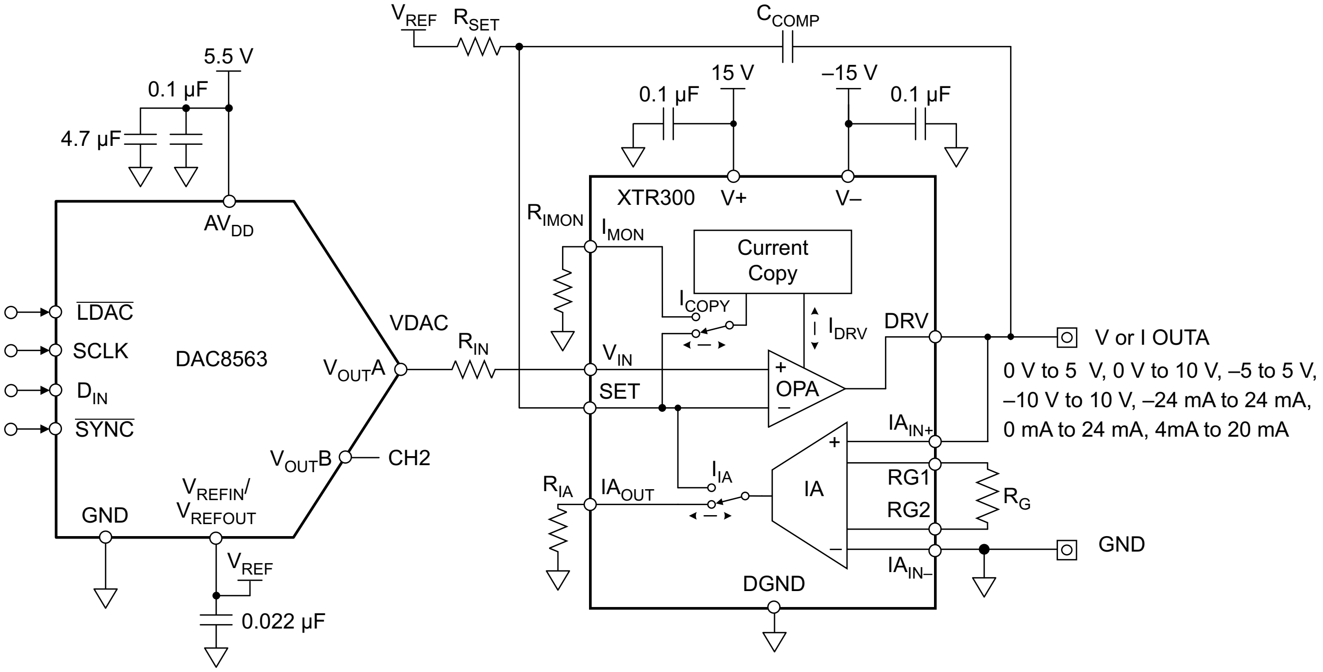


Figure 96. DAC8563 and XTR300 Discrete Analog Output Module

9.2.1.1 *Design Requirements*

The design uses a DAC and a current-or-voltage output driver to create a discrete analog output design that can output either voltage or current from the same pin while focusing on high-accuracy specifications. The choice of the DAC8563 device takes advantage of its 16-bit resolution as well as its low typical offset error of 1 mV and gain error of 0.01% FSR. The choice of the XTR300 device is based on its strong dc performance, having a typical error of 400 µV and 0.04% FSR gain error. The XTR300 device allows a variety of both current and voltage outputs on the same pin while providing load monitoring and error status pins.

The power-on reset-to-midscale feature of the DAC8563 makes the bipolar output of the XTR300 power up at 0 V or 0 A. If using a unipolar output, the recommended device to achieve a system power-on output of 0 V, 0 A or 4 mA is the DAC8562 device.

A recommendation for minimizing the introduction of errors into the system is to use ±0.01% tolerance RG and RSET resistors. The bypass capacitors on AV_{DD}, VREF, V+ and V– should have values between 100 nF and 10 µF. Smaller capacitors filter fast low-energy transients, whereas the large capacitors filter the slow high-energy transients. If there is an expectation of both types of signals in the system, the recommendation is to use a pair of small and large values as shown on the AV_{DD} pin of the DAC8563 device in Figure 96.

9.2.1.2 *Detailed Design Procedure*

When configured for voltage mode, the output of the instrumentation amplifier (IA), internal to the XTR300 device, is routed to the SET pin. The SET output provides feedback for the IA based on the IA input voltage. The feedback from the IA provides high-impedance remote sensing of the voltage at the output load. Using the output voltage can overcome errors from PCB traces and protection component impedances. The DAC provides a unipolar input voltage to the VIN pin of the XTR300 device. The XTR300 device offsets the VDAC range by a negative V_{REF} and amplifies the difference by a value set by the R_G and R_{SET} resistors, as shown in Equation 5.

Typical Applications (continued)

$$V_{OUT} = \frac{R_G}{2} \times \left(\frac{V_{DAC} - V_{REF}}{R_{SET}} \right) \tag{5}$$

When configured for current mode, the XTR300 routes the internal output of its current copy circuitry to the SET pin. This provides feedback for the internal OPA driver based on 1 / 10th of the output current, resulting in a voltage-to-current transfer function. Generating bipolar current outputs from the single-ended DAC output voltage, VDAC, requires the application of an offset to the XTR300 SET pin. Connect the R_{SET} resistor from the SET pin to V_{REF} to apply the offset and obtain the transfer function shown in Equation 6.

$$I_{OUT} = 10 \times \left(\frac{V_{DAC} - V_{REF}}{R_{SET}} \right) \tag{6}$$

The desired output ranges for VDAC and V_{REF} voltages determine the R_{SET} and R_G resistor values, calculated using Equation 7 and Equation 8. The system design requires a VDAC voltage range of 0.04 V to 4.96 V in order to operate the DAC8563 in the specified linear output range from codes 512 to 65 024.

$$R_{SET} = 10 \times \left(\frac{V_{DAC} - V_{REF}}{I_{OUT}} \right) = 10 \times \left(\frac{4.96\ \text{V} - 2.5\ \text{V}}{0.024\ \text{A}} \right) = 1025\ \Omega \tag{7}$$

$$R_G = \frac{2 \times V_{OUT\_MAX} \times R_{SET}}{V_{DAC} - V_{REF}} = \frac{2 \times 10\ \text{V} \times 1020\ \Omega}{4.96\ \text{V} - 2.5\ \text{V}} = 8292\ \Omega \tag{8}$$

I_{MON} and IA_{OUT} accomplish load monitoring. The sizing of R_{IMON} and R_{IA} determine the monitoring output voltage across the resistors. Size the resistors according to Equation 9 and Equation 10 and the expected output load current I_{DRV}.

$$R_{IMON} = \frac{10 \times V_{IMON}}{I_{DRV}} \tag{9}$$

$$R_{IA} = \frac{10 \times V_{IA}}{I_{IA}} \tag{10}$$

For more detailed information about the design procedure of this circuit and how to isolate it, see *Two-Channel Source/Sink Combined Voltage & Current Output, Isolated, EMC/EMI Tested Reference Design* (TIDU434).

Typical Applications (continued)

9.2.1.3 Application Curves

Figure 97 shows the transfer function for the bipolar ±10 V voltage range. This design also supports output voltage ranges of 0–5 V, 0–10 V and ±5 V. Figure 98 shows the transfer function for the unipolar 0–24 mA current range. This design also supports output current ranges of ±24 mA and 4 mA–20 mA.

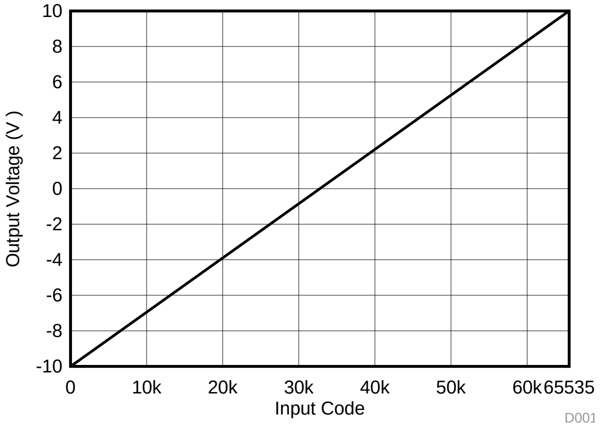


Figure 97. Output Voltage vs Input Code

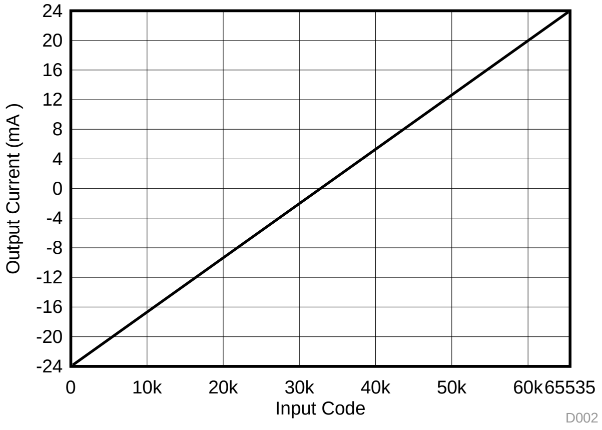


Figure 98. Output Current vs Input Code

Typical Applications (continued)

9.2.2 Up to ±15-V Bipolar Output Using the DAC8562

The DAC8562 is designed to be operate from a single power supply providing a maximum output range of AV_{DD} volts. However, the DAC can be placed in the configuration shown in Figure 99 in order to be designed into bipolar systems. Depending on the ratio of the resistor values, the output of the circuit can range anywhere from ±5 V to ±15 V. The design example below shows that the DAC is configured to have its internal reference enabled and the DAC8562 internal gain set to 2, however, an external 2.5-V reference could also be used (with DAC8562 internal gain set to 2).

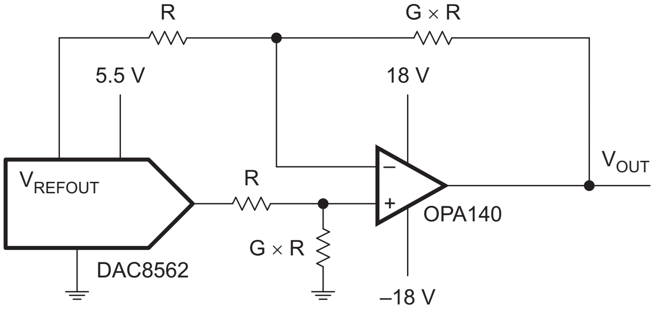


Figure 99. Bipolar Output Range Circuit Using DAC8562

The transfer function shown in Equation 5 can be used to calculate the output voltage as a function of the DAC code, reference voltage and resistor ratio:

$$V_{OUT} = G \times V_{REFOUT}\left(2 \times \frac{D_{IN}}{65{,}536} - 1\right) \tag{11}$$

where:

D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register, ranging from 0 to 65,535 for DAC8562 (16 bit).

V_{REFOUT} = reference output voltage with the internal reference enabled from the DAC V_{REFIN}/V_{REFOUT} pin

G = ratio of the resistors

An example configuration to generate a ±10-V output range is shown below in Equation 6 with G = 4 and V_{REFOUT} = 2.5 V:

$$V_{OUT} = 20 \times \frac{D_{IN}}{65{,}536} - 10\text{ V} \tag{12}$$

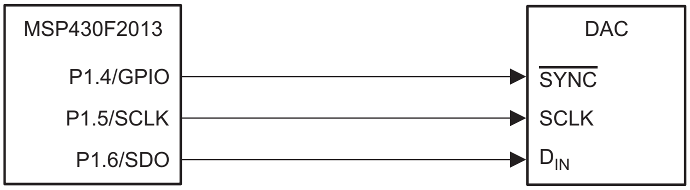
In this example, the range is set to ±10 V by using a resistor ratio of four, V_{REFOUT} of 2.5 V, and DAC8562 internal gain of 2. The resistor sizes must be selected keeping in mind the current sink or source capability of the DAC8562 internal reference. Using larger resistor values, for example, R = 10 kΩ or larger, is recommended. The op amp is selectable depending on the requirements of the system.

The DAC8562EVM and DAC7562EVM boards have the option to evaluate the bipolar output application by installing the components on the pre-placed footprints. For more information see either the DAC8562EVM or DAC7562EVM product folder.

9.3 System Examples

9.3.1 MSP430 Microprocessor Interfacing

Figure 100 shows a serial interface between the DAC756x, DAC816x, or DAC856x device and a typical MSP430 USI port such as the one found on the MSP430F2013. The port is configured in SPI master mode by setting bits 3, 5, 6, and 7 in USICTL0. The USI counter interrupt is set in USICTL1 to provide an efficient means of SPI communication with minimal software overhead. The serial clock polarity, source, and speed are controlled by settings in the USI clock control register (USICKCTL). The $\overline{\text{SYNC}}$ signal is derived from a bit-programmable pin on port 1; in this case, port line P1.4 is used. When data are to be transmitted to the DAC756x, DAC816x, or DAC856x device, P1.4 is taken low. The USI transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P1.4 is left low after the first eight bits are transmitted; then, a second write cycle is initiated to transmit the second byte of data. P1.4 is taken high following the completion of the third write cycle.

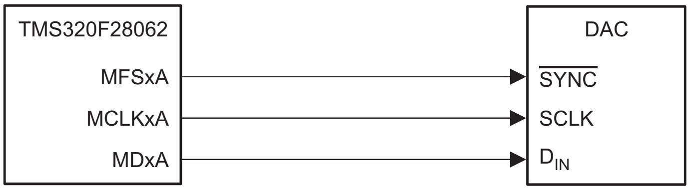


NOTE: Additional pins omitted for clarity.

Figure 100. DAC756x, DAC816x, or DAC856x Device to MSP430 Interface

9.3.2 TMS320 McBSP Microprocessor Interfacing

Figure 101 shows an interface between the DAC756x, DAC816x, or DAC856x device and any TMS320 series DSP from Texas Instruments with a multi-channel buffered serial port (McBSP). Serial data are shifted out on the rising edge of the serial clock and are clocked into the DAC756x, DAC816x, or DAC856x device on the falling edge of the SCLK signal.

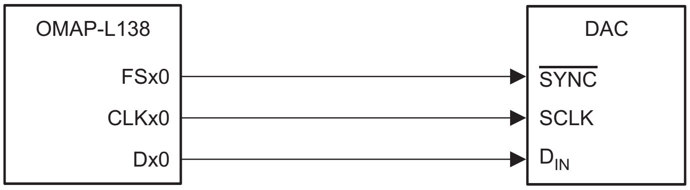


NOTE: Additional pins omitted for clarity.

Figure 101. DAC756x, DAC816x, or DAC856x Device to TMS320 McBSP Interface

9.3.3 OMAP-L1x Processor Interfacing

Figure 102 shows a serial interface between the DAC756x, DAC816x, or DAC856x device and the OMAP-L138 processor. The transmit clock CLKx0 of the L138 drives SCLK of the DAC756x, DAC816x, or DAC856x device, and the data transmit (Dx0) output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from the frame sync transmit (FSx0) line, similar to the TMS320 interface.



NOTE: Additional pins omitted for clarity.

Figure 102. DAC756x, DAC816x, or DAC856x Device to OMAP-L1x Processor

10 Power Supply Recommendations

These devices can operate within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to AV_{DD} should be well-regulated and low-noise. In order to further minimize noise from the power supplies, a strong recommendation is to include a pair of 100-pF and 1-nF capacitors and a 0.1-μF to 1-μF bypass capacitor. The current consumption of the AV_{DD} pin, the short-circuit current limit, and the load current for these devices are listed in the *Electrical Characteristics* table. Choose the power supplies for these devices to meet the aforementioned current requirements.

11 Layout

11.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The DAC756x, DAC816x, and DAC856x devices offer single-supply operation, and are often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output. As a result of the single ground pin of the DAC756x, DAC816x, and DAC856x devices, all return currents (including digital and analog return currents for the DAC) must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system. The power applied to AV_{DD} should be well-regulated and low noise. Switching power supplies and dc-dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. As with the GND connection, AV_{DD} should be connected to a power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a pair of 100-pF to 1-nF capacitors and a 0.1-μF to 1-μF bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100-μF electrolytic capacitor or even a pi filter made up of inductors and capacitors – all designed essentially to provide low-pass filtering for the supply and remove the high-frequency noise.

11.2 Layout Example

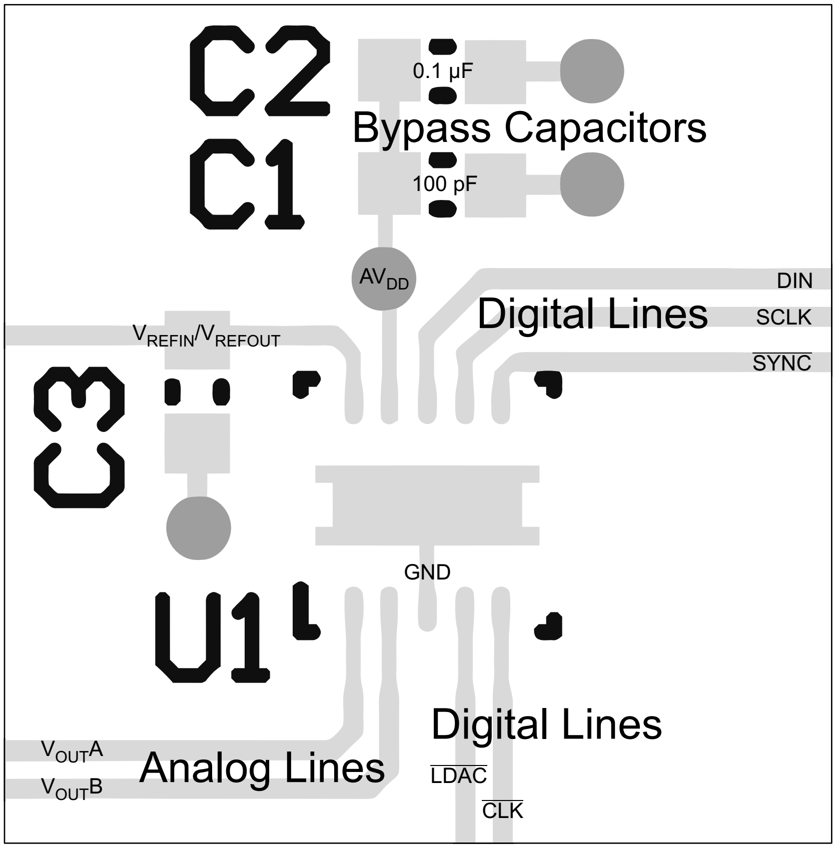


Figure 103. DACxx6x Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 18. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DAC7562	Click here	Click here	Click here	Click here	Click here
DAC7563	Click here	Click here	Click here	Click here	Click here
DAC8162	Click here	Click here	Click here	Click here	Click here
DAC8163	Click here	Click here	Click here	Click here	Click here
DAC8562	Click here	Click here	Click here	Click here	Click here
DAC8563	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
SPI, QSPI are trademarks of Motorola, Inc.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7562SDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7562	Samples
DAC7562SDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7562	Samples
DAC7562SDSCR	ACTIVE	WSON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7562	Samples
DAC7562SDSCT	ACTIVE	WSON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7562	Samples
DAC7563SDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	7563	Samples
DAC7563SDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	7563	Samples
DAC7563SDSCR	ACTIVE	WSON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	7563	Samples
DAC7563SDSCT	ACTIVE	WSON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	7563	Samples
DAC8162SDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8162	Samples
DAC8162SDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8162	Samples
DAC8162SDSCR	ACTIVE	WSON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8162	Samples
DAC8162SDSCT	ACTIVE	WSON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8162	Samples
DAC8163SDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8163	Samples
DAC8163SDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8163	Samples
DAC8163SDSCR	ACTIVE	WSON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8163	Samples
DAC8163SDSCT	ACTIVE	WSON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8163	Samples
DAC8562SDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8562	Samples

PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8562SDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8562	Samples
DAC8562SDSCR	ACTIVE	WSON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8562	Samples
DAC8562SDSCT	ACTIVE	WSON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8562	Samples
DAC8563SDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8563	Samples
DAC8563SDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8563	Samples
DAC8563SDSCR	ACTIVE	WSON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8563	Samples
DAC8563SDSCT	ACTIVE	WSON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8563	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF DAC8562 :

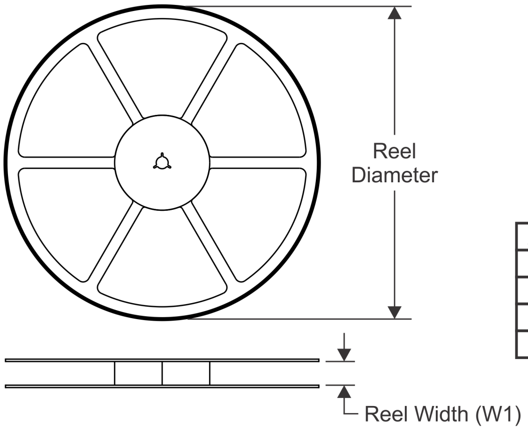
- Automotive: DAC8562-Q1

NOTE: Qualified Version Definitions:

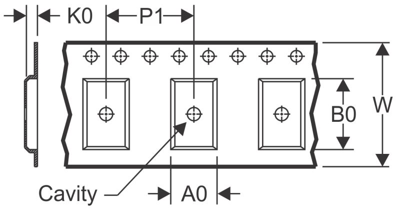
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

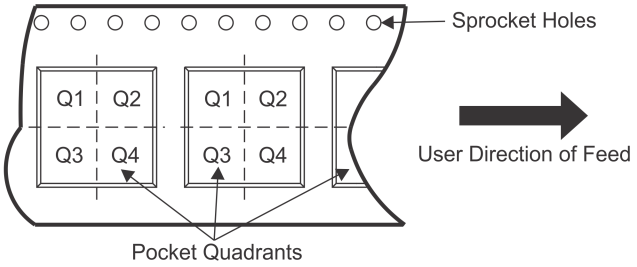


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

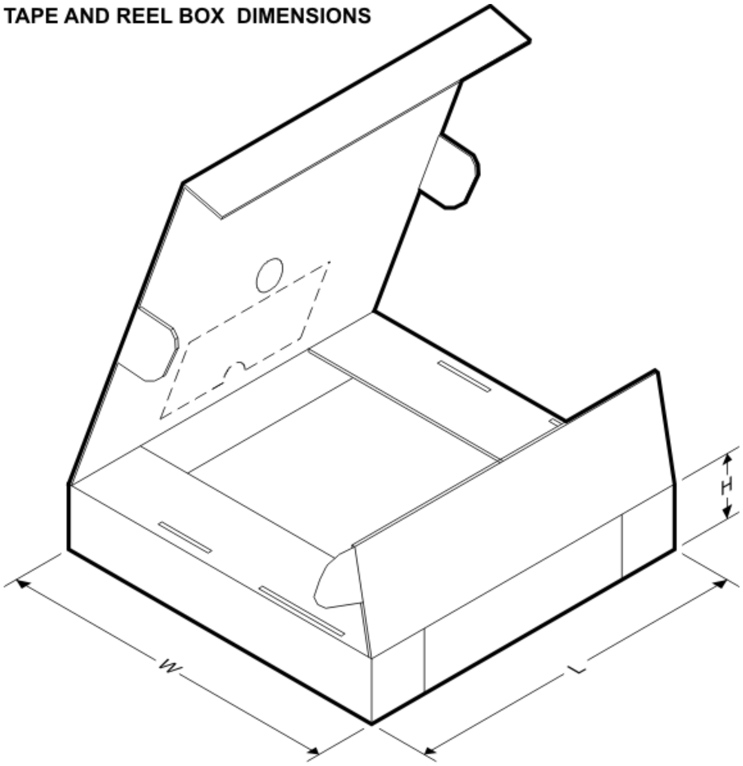


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7562SDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC7562SDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC7562SDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC7562SDSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC7563SDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC7563SDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC7563SDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC7563SDSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8162SDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8162SDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8162SDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8162SDSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8163SDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8163SDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8163SDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8163SDSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8562SDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8562SDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8562SDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8562SDSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8563SDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8563SDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8563SDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8563SDSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

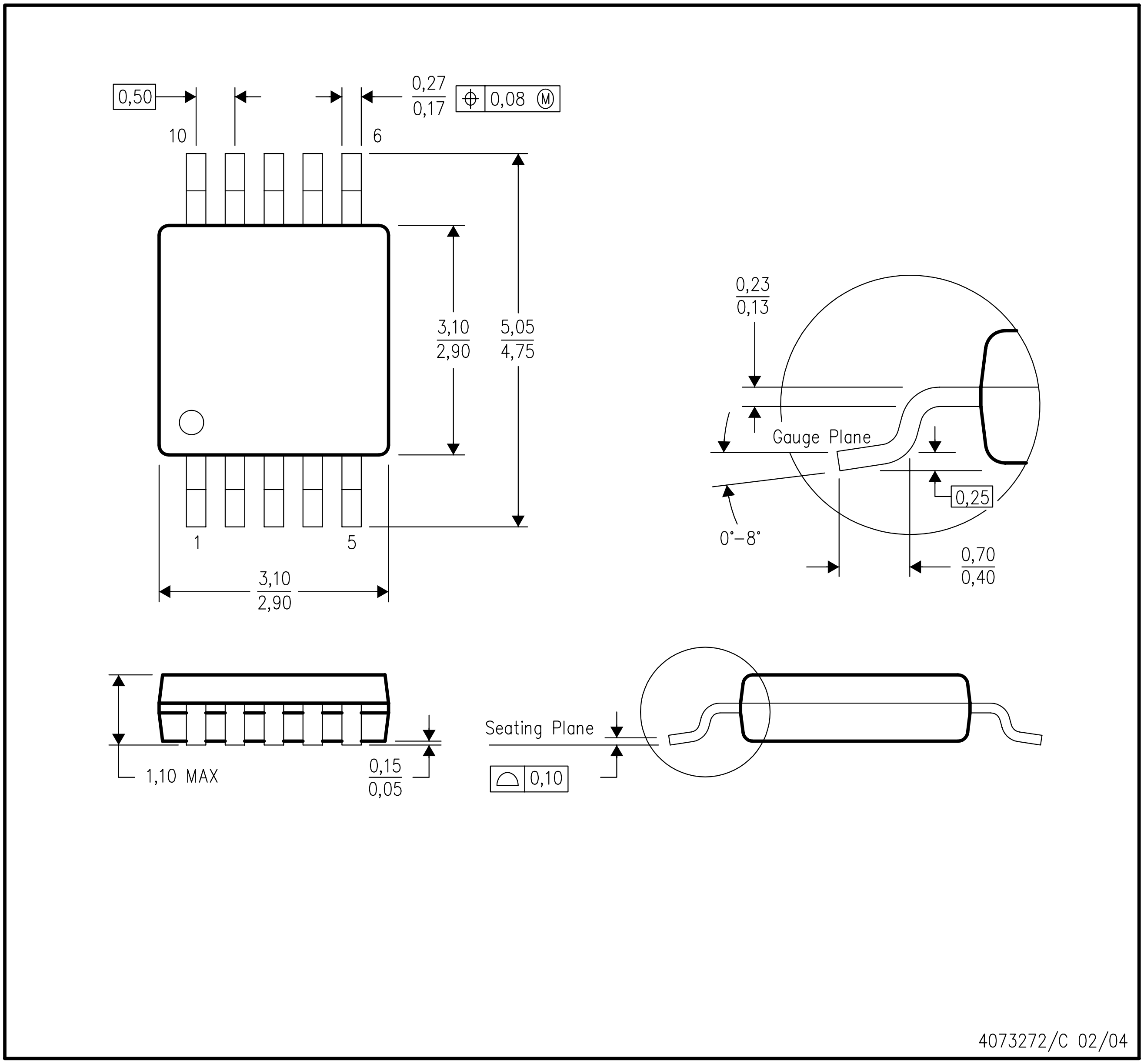


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7562SDGSR	VSSOP	DGS	10	2500	370.0	355.0	55.0
DAC7562SDGST	VSSOP	DGS	10	250	195.0	200.0	45.0
DAC7562SDSCR	WSON	DSC	10	3000	367.0	367.0	35.0
DAC7562SDSCT	WSON	DSC	10	250	210.0	185.0	35.0
DAC7563SDGSR	VSSOP	DGS	10	2500	370.0	355.0	55.0
DAC7563SDGST	VSSOP	DGS	10	250	220.0	205.0	50.0
DAC7563SDSCR	WSON	DSC	10	3000	367.0	367.0	35.0
DAC7563SDSCT	WSON	DSC	10	250	210.0	185.0	35.0
DAC8162SDGSR	VSSOP	DGS	10	2500	370.0	355.0	55.0
DAC8162SDGST	VSSOP	DGS	10	250	220.0	205.0	50.0
DAC8162SDSCR	WSON	DSC	10	3000	367.0	367.0	35.0

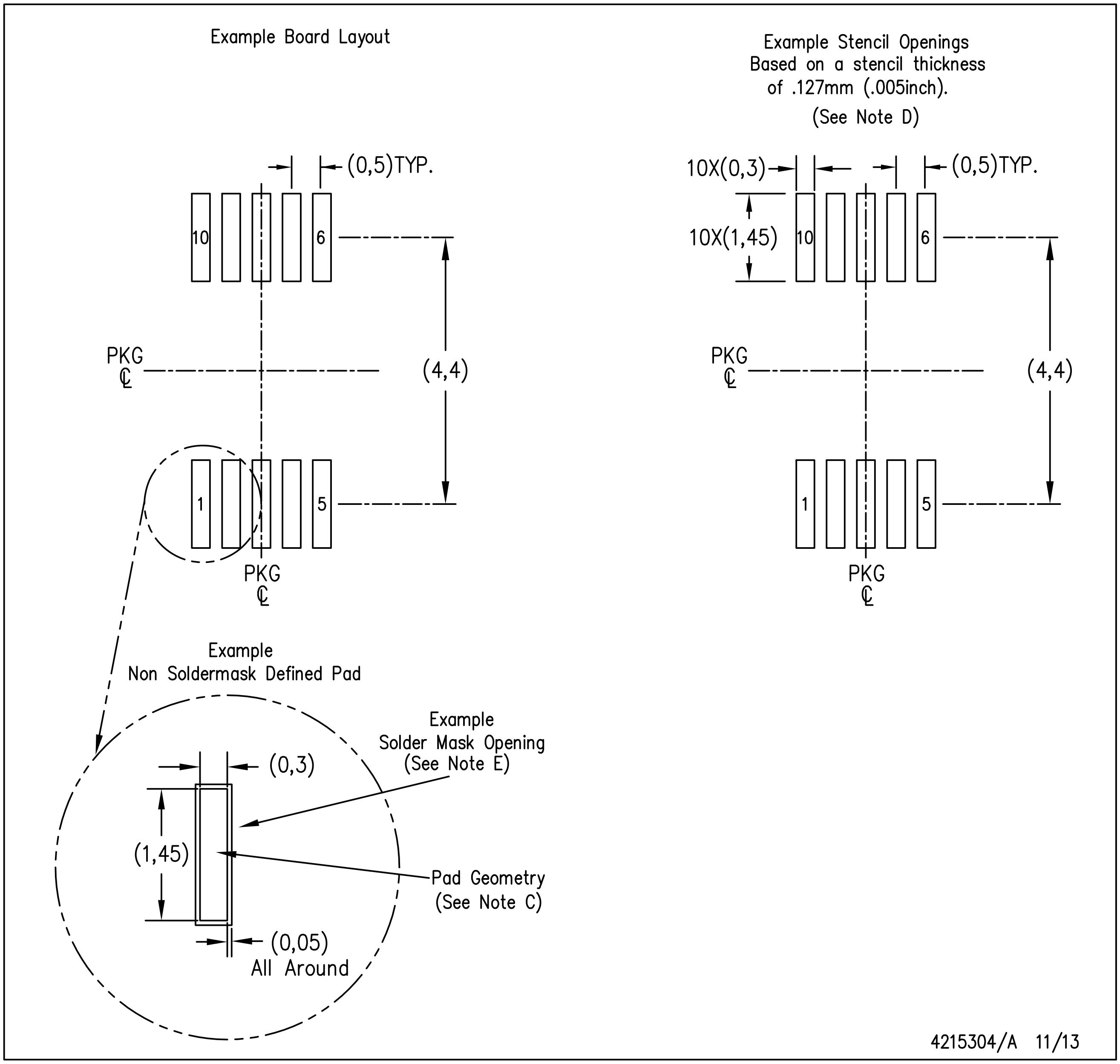
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8162SDSCT	WSON	DSC	10	250	210.0	185.0	35.0
DAC8163SDGSR	VSSOP	DGS	10	2500	370.0	355.0	55.0
DAC8163SDGST	VSSOP	DGS	10	250	220.0	205.0	50.0
DAC8163SDSCR	WSON	DSC	10	3000	367.0	367.0	35.0
DAC8163SDSCT	WSON	DSC	10	250	210.0	185.0	35.0
DAC8562SDGSR	VSSOP	DGS	10	2500	370.0	355.0	55.0
DAC8562SDGST	VSSOP	DGS	10	250	220.0	205.0	50.0
DAC8562SDSCR	WSON	DSC	10	3000	367.0	367.0	35.0
DAC8562SDSCT	WSON	DSC	10	250	210.0	185.0	35.0
DAC8563SDGSR	VSSOP	DGS	10	2500	370.0	355.0	55.0
DAC8563SDGST	VSSOP	DGS	10	250	220.0	205.0	50.0
DAC8563SDSCR	WSON	DSC	10	3000	367.0	367.0	35.0
DAC8563SDSCT	WSON	DSC	10	250	210.0	185.0	35.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



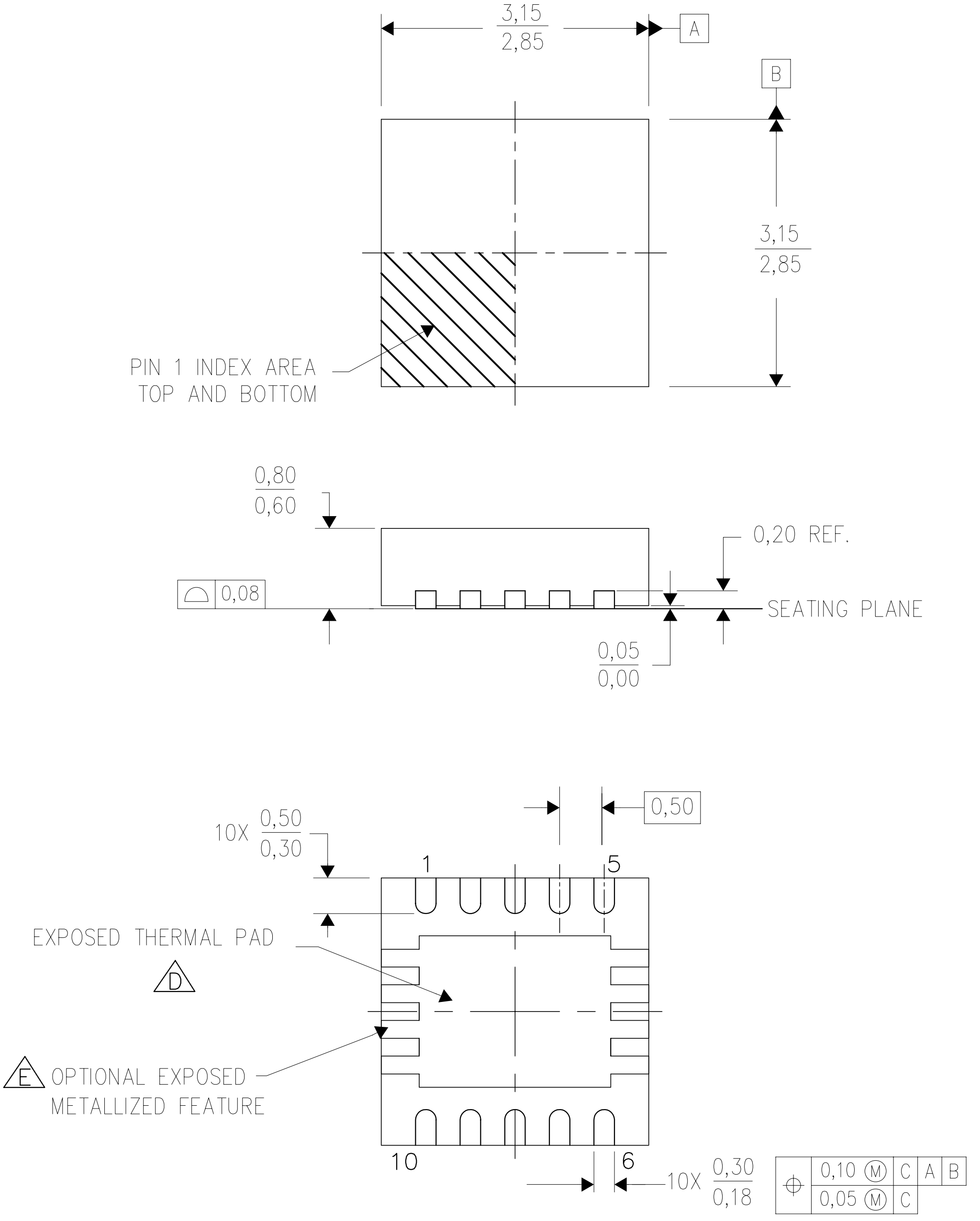
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DSC (S-PWSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



4207383/E 01/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

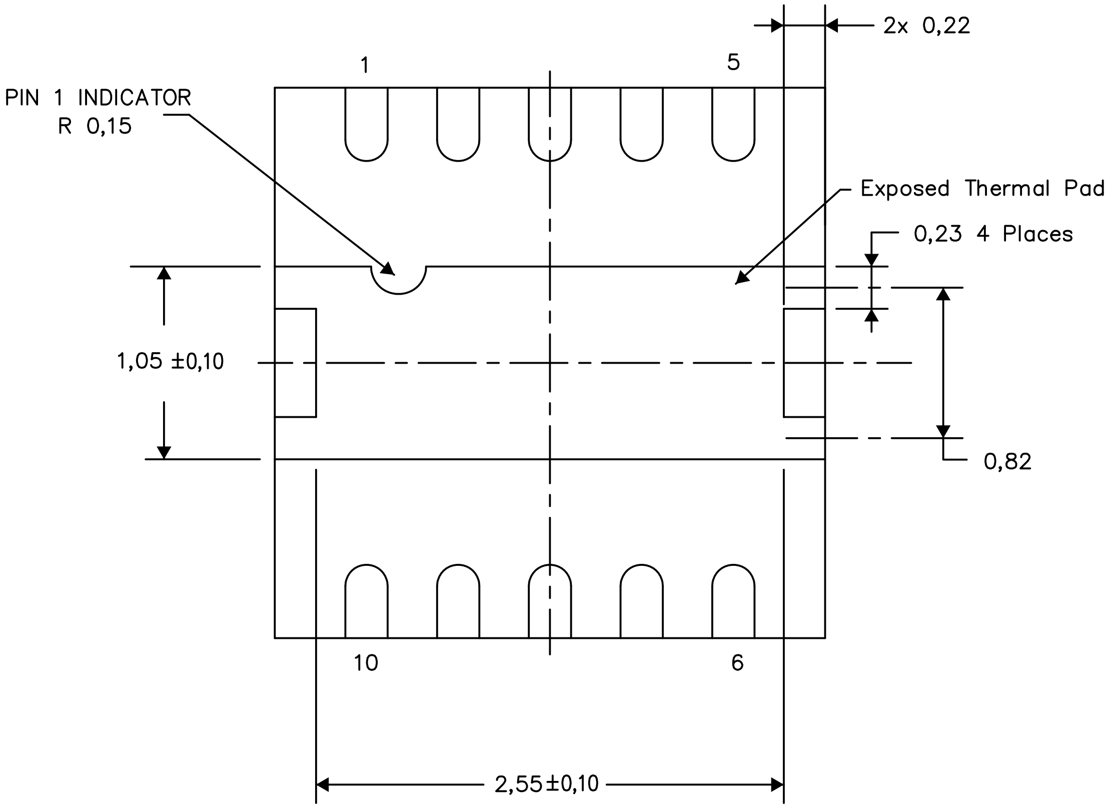
DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



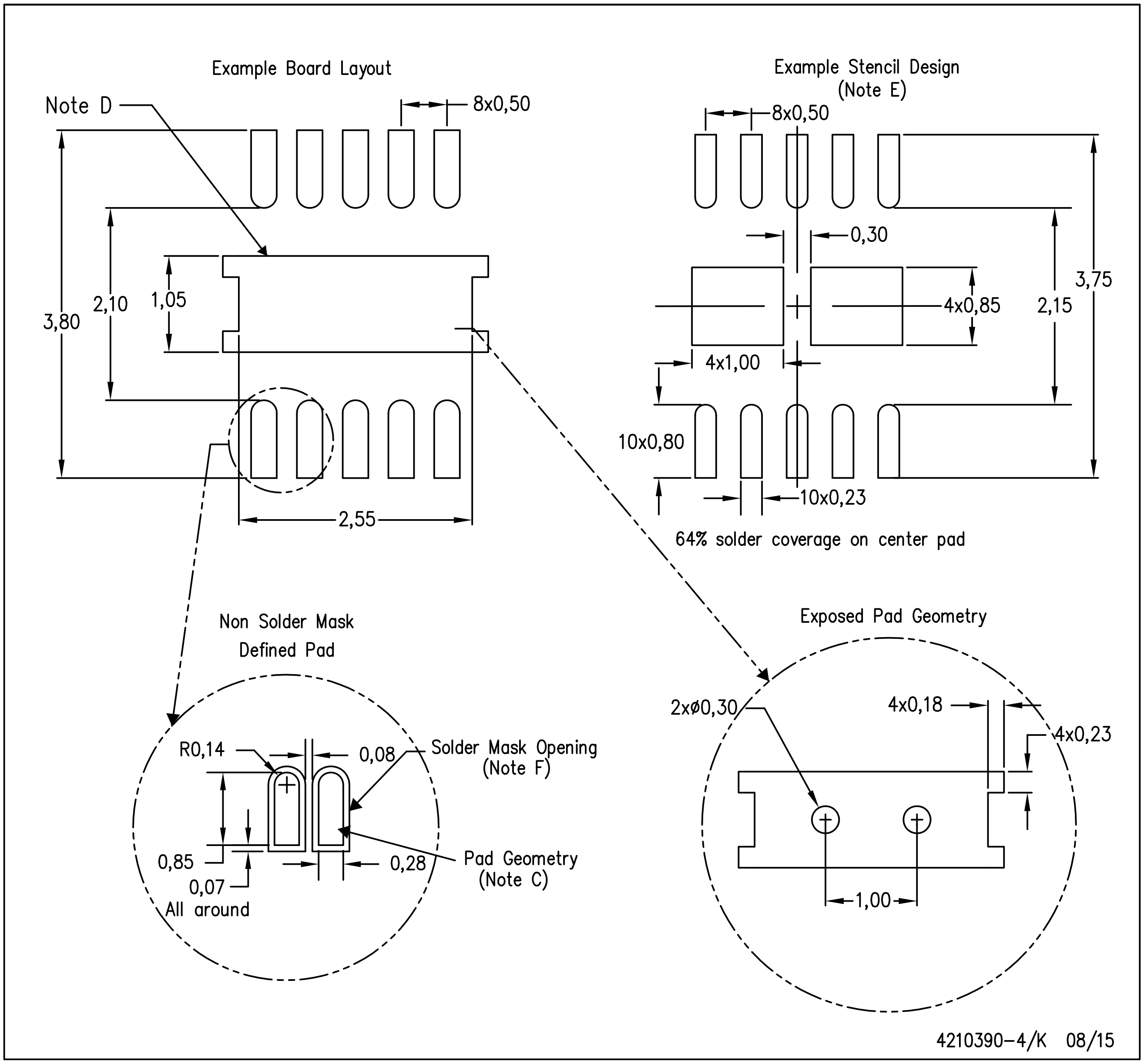
Bottom View

Exposed Thermal Pad Dimensions

4210391–4/Q 08/15

NOTE: A. All linear dimensions are in millimeters

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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