CD54HC4351, CD74HC4351, CD74HCT4351, CD74HC4352

High-Speed CMOS Logic Analog Multiplexers/Demultiplexers with Latch

Data sheet acquired from Harris Semiconductor
SCHS213C

September 1998 - Revised July 2003

Features

- **Wide Analog Input Voltage Range** . . . . . **±5V (Max)**
- **Low "On" Resistance**
  - **V_{CC} - V_{EE} = 4.5V. . . . . 70Ω (Typ)**
  - **V_{CC} - V_{EE} = 9V . . . . . 40Ω (Typ)**
- **Low Crosstalk Between Switches**
- **Fast Switching and Propagation Speeds**
- **"Break-Before-Make" Switching**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **HC Types**
  - **2V to 6V Operation, Control; 0V to 10V Switch**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation, Control; 0V to 10V Switch**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The 'HC4351, CD74HCT4351, and CD74HC4352 are digitally controlled analog switches which utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers are, in essence, the HC/HCT4015 and HC4052 preceded by address latches that are controlled by an active low Latch Enable input ($\overline{LE}$). Two Enable inputs, one active low ($\overline{E1}$), and the other active high (E2) are provided allowing enabling with either input voltage level.

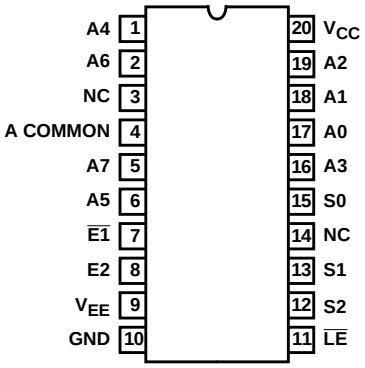
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4351F3A	-55 to 125	20 Ld CERDIP
CD74HC4351E	-55 to 125	20 Ld PDIP
CD74HC4351M	-55 to 125	20 Ld SOIC
CD74HC4351M96	-55 to 125	20 Ld SOIC
CD74HCT4351E	-55 to 125	20 Ld PDIP
CD74HC4352E	-55 to 125	20 Ld PDIP

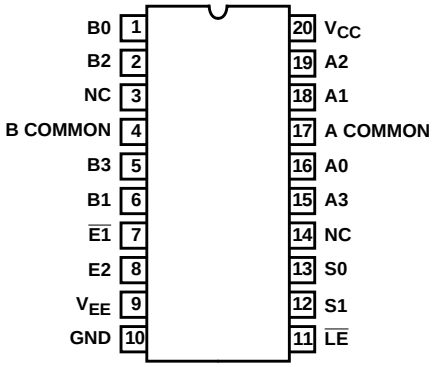
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

Pinouts

CD54HC4351
(CERDIP)
CD74HC4351
(PDIP, SOIC)
CD74HCT4351
(PDIP)
TOP VIEW



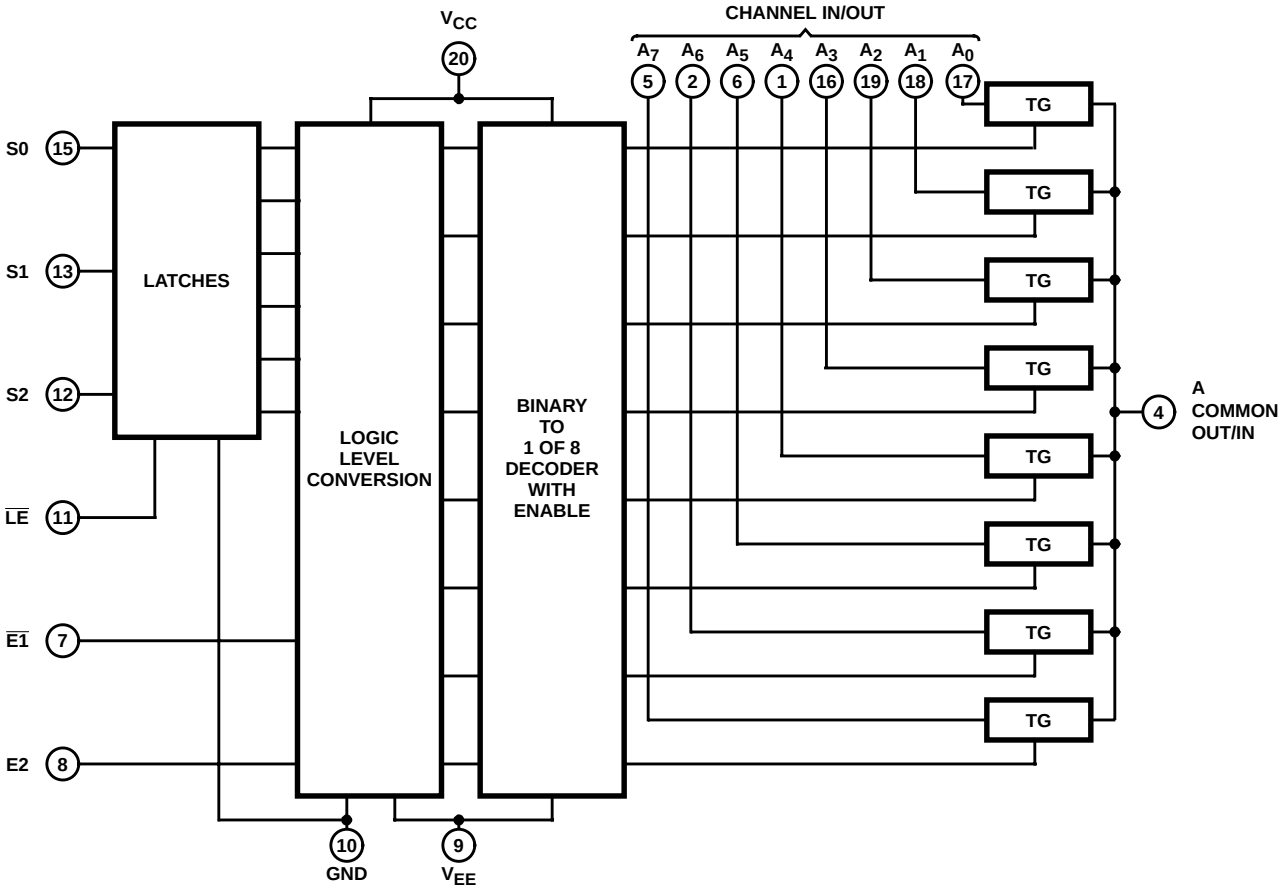
CD74HC4352
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram

'HC4351, CD74HCT4351



TRUTH TABLE
'HC4351, CD74HCT4351

INPUT STATES					(NOTE 1) "ON" SWITCHES
$\overline{E1}$	E2	S2	S1	S0	$\overline{LE}$ = H
L	H	L	L	L	A_0
L	H	L	L	H	A_1
L	H	L	H	L	A_2
L	H	L	H	H	A_3
L	H	H	L	L	A_4
L	H	H	L	H	A_5
L	H	H	H	L	A_6
L	H	H	H	H	A_7
H	L	X	X	X	None

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

NOTE:

1. When $\overline{LE}$ is low S0-S2 data are latched and switches cannot change state.

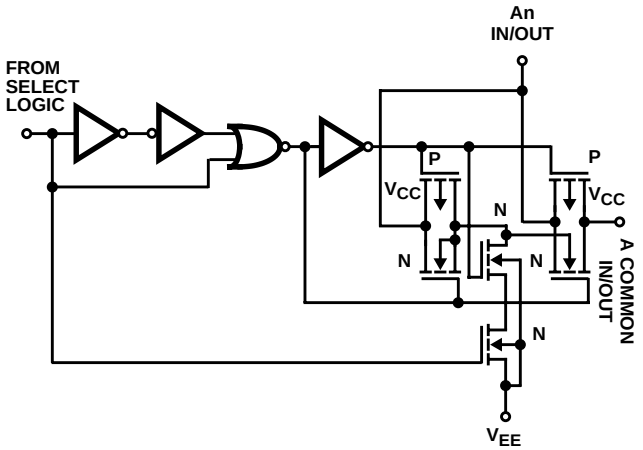
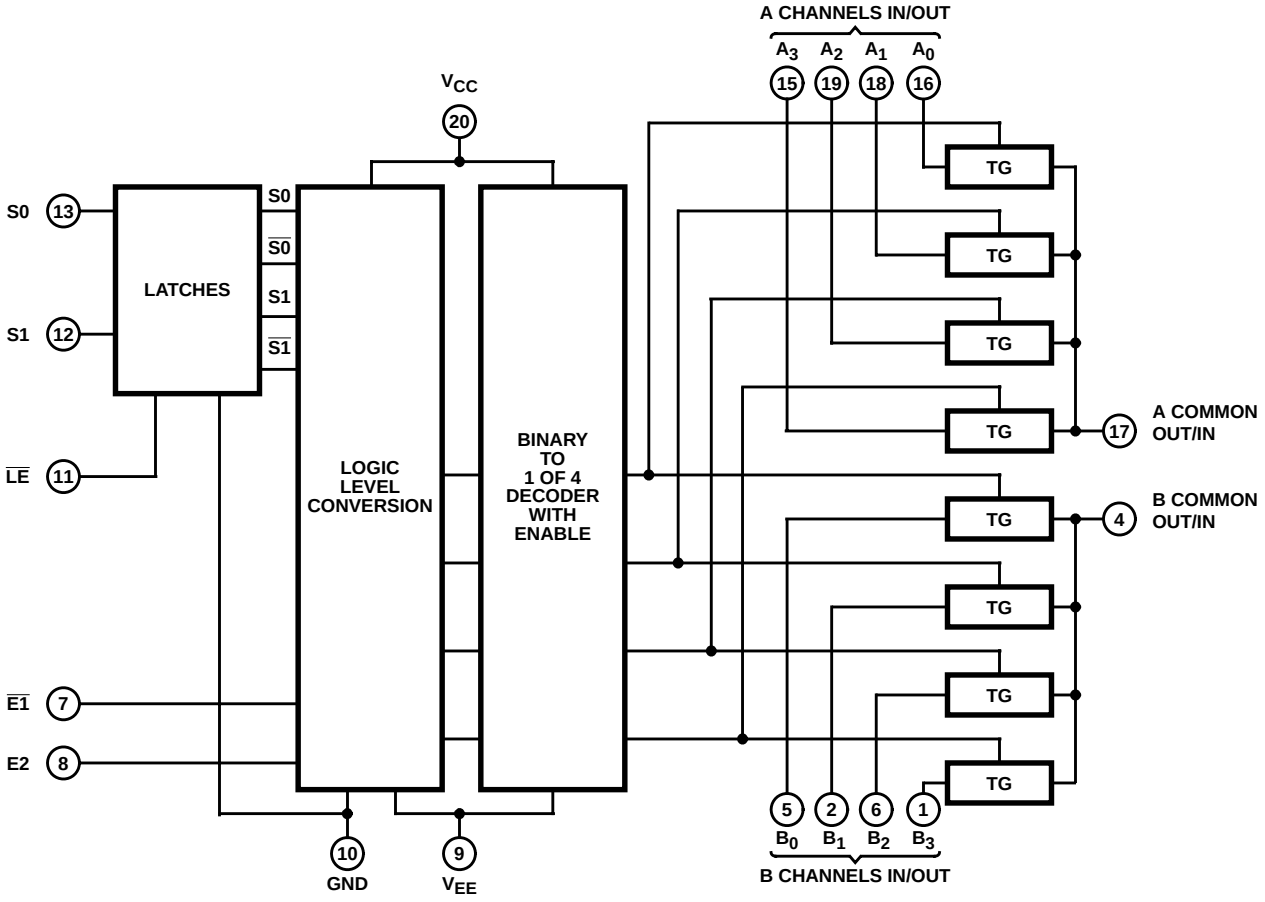


FIGURE 1. DETAIL OF ONE HC/HCT4351 SWITCH

Functional Diagram

CD74HC4352



TRUTH TABLE
CD74HC4352

INPUT STATES				(NOTE 2) "ON" SWITCHES
$\overline{E1}$	E2	S1	S0	$\overline{LE}$ = H
L	H	L	L	A_0, B_0
L	H	L	H	A_1, B_1
L	H	H	L	A_2, B_2
L	H	H	H	A_3, B_3
H	L	X	X	None

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

NOTE:

2. When Latch Enable is "Low" channel-select data is latched and switches cannot change state.

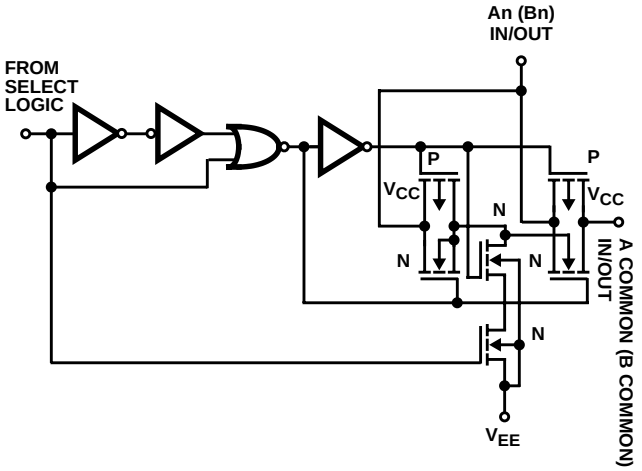


FIGURE 2. DETAIL OF ONE CD74HC4352 SWITCH

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Supply Voltage, V_{CC} - V_{EE} . . . . . -0.5V to 10.5V
DC Supply Voltage, V_{EE} . . . . . 0.5V to -7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} 0.5V. . . . . ±20mA
DC Switch Diode Current, I_{OK}
For V_I < V_{EE} -0.5V or V_I < V_{CC} + 0.5V . . . . . ±25mA
DC Switch Current, I_{OK} (Note 3)
For V_I > V_{EE} -0.5V or V_I < V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55^oC to 125^oC
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
Supply Voltage Range, V_{CC} - V_{EE}
HC, HCT Types (Figure 3) . . . . . 2V to 10V
Supply Voltage Range, V_{EE}
HC, HCT Types (Figure 4) . . . . . 0V to -6V
DC Input or Output Voltage, V_I . . . . . GND to V_{CC}
Analog Switch I/O Voltage, V_{IS} . . . . . V_{EE} (Min)
. . . . . V_{CC} (Max)
Input Rise and Fall Time, t_r, t_f
2V . . . . . 1000ns (Max)
4.5V . . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} ($^oC/W$)
E (PDIP) Package	69
M (SOIC) Package	58

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. In certain applications, the external load-resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from R_{ON} values shown in the DC Electrical Specifications table). No V_{CC} current will flow through R_L if the switch current flows into terminal 3 on the 'HC4351 and CD74HCT4351; terminals 3 and 13 on the CD74HC4352.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Area as a Function of Supply Voltage

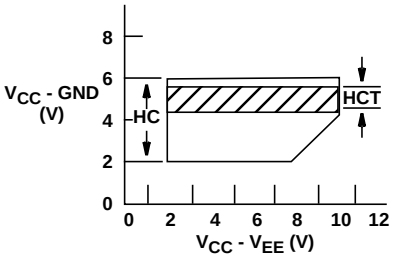


FIGURE 3.

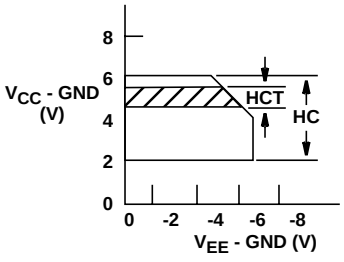


FIGURE 4.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS				25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)	V_{EE} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES													
High Level Input Voltage	V_{IH}	-	-	-	2	1.5	-	-	1.5	-	1.5	-	V
					4.5	3.15	-	-	3.15	-	3.15	-	V
					6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	-	2	-	-	0.5	-	0.5	-	0.5	V
					4.5	-	-	1.35	-	1.35	-	1.35	V
					6	-	-	1.8	-	1.8	-	1.8	V
"ON" Resistance I_O = 1mA Figure 9	R_{ON}	V_{IH} or V_{IL}	V_{CC} or V_{EE}	0	4.5	-	70	160	-	200	-	240	Ω
				0	6	-	60	140	-	175	-	210	Ω
				-4.5	4.5	-	40	120	-	150	-	180	Ω
			V_{CC} to V_{EE}	0	4.5	-	90	180	-	225	-	270	Ω
				0	6	-	80	160	-	200	-	240	Ω
				-4.5	4.5	-	45	130	-	162	-	195	Ω
Maximum "ON" Resistance Between Any Two Channels	ΔR_{ON}	-	-	0	4.5	-	10	-	-	-	-	-	Ω
				0	6	-	8.5	-	-	-	-	-	Ω
				-4.5	4.5	-	5	-	-	-	-	-	Ω
Switch On/Off Leakage Current 4 Channels (4352)	I_{IZ}	V_{IH} or V_{IL}	For Switch OFF: When $V_{IS} = V_{CC}$ $V_{OS} = V_{EE}$; When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$ For Switch ON: All Applicable Combinations of V_{IS} and V_{OS} Voltage Levels	0	6	-	-	±0.1	-	±1	-	±1	µA
				-5	5	-	-	±0.2	-	±2	-	±2	µA
Switch On/Off Leakage Current 8 Channels (4351)				0	6	-	-	±0.2	-	±2	-	±2	µA
				-5	5	-	-	±0.4	-	±4	-	±4	µA
Control Input Leakage Current	I_{IL}	V_{CC} or GND	-	0	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current I_O = 0	I_{CC}	V_{CC} or GND	When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$, When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$	0	6	-	-	8	-	80	-	160	µA
				-5	5	-	-	16	-	160	-	320	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS				25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)	V_{EE} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES													
High Level Input Voltage	V_{IH}	-	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
"ON" Resistance I_O = 1mA Figure 9	R_{ON}	V_{IH} or V_{IL}	V_{CC} or V_{EE}	0	4.5	-	70	160	-	200	-	240	Ω
				-4.5	4.5	-	40	120	-	150	-	180	Ω
			V_{CC} to V_{EE}	0	4.5	-	90	180	-	225	-	270	Ω
				-4.5	4.5	-	45	130	-	162	-	195	Ω
Maximum "ON" Resistance Between Any Two Channels	ΔR_{ON}	-	-	0	4.5	-	10	-	-	-	-	-	Ω
				-4.5	4.5	-	5	-	-	-	-	-	Ω
Switch On/Off Leakage Current 4 Channels (4352)	I_{IZ}	V_{IH} or V_{IL}	For Switch OFF: When $V_{IS} = V_{CC}$ $V_{OS} = V_{EE}$; When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$ For Switch ON: All Applicable Combinations of V_{IS} and V_{OS} Voltage Levels	0	6	-	-	±0.1	-	±1	-	±1	µA
				-5	5	-	-	±0.2	-	±2	-	±2	µA
Switch On/Off Leakage Current 8 Channels (4351)				0	6	-	-	±0.2	-	±2	-	±2	µA
				-5	5	-	-	±0.4	-	±4	-	±4	µA
Control Input Leakage Current	I_I	V_{CC} or GND	-	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current I_O = 0	I_{CC}	Any Voltage Between V_{CC} and GND	When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$, When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$	0	5.5	-	-	8	-	80	-	160	µA
				-4.5	5.5	-	-	16	-	160	-	320	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 5)	V_{CC} -2.1	-	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

5. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

TYPE	INPUT	UNIT LOADS
All	$\overline{E1}$, E2, Sn	0.5
(4351, 4352)	$\overline{LE}$	1.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{EE} (V)	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
Propagation Delay, Switch In to Switch Out	t_{PLH}, t_{PHL}	C_L = 50pF	0	2	-	-	35	-	45	-	55	ns
			0	4.5	-	-	7	-	9	-	11	ns
			0	6	-	-	6	-	8	-	9	ns
			-4.5	4.5	-	-	5	-	7	-	8	ns
Maximum Switch Turn “ON” Delay 4351 $\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	t_{PZH}, t_{PZL}	C_L = 50pF	0	2	-	-	300	-	375	-	450	ns
			0	4.5	-	-	60	-	75	-	90	ns
			0	6	-	-	51	-	64	-	77	ns
			-4.5	4.5	-	-	55	-	69	-	83	ns
		C_L = 15pF	-	5	-	27	-	-	-	-	-	ns
Maximum Switch Turn “ON” Delay 4352 $\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	t_{PZH}, t_{PZL}	C_L = 50pF	0	2	-	-	350	-	440	-	525	ns
			0	4.5	-	-	70	-	88	-	105	ns
			0	6	-	-	60	-	75	-	90	ns
			-4.5	4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	-	5	-	35	-	-	-	-	-	ns
Maximum Switch Turn “ON” Delay 4351 Sn to V_{OS}	t_{PZH}, t_{PZL}	C_L = 50pF	0	2	-	-	300	-	375	-	450	ns
			0	4.5	-	-	60	-	75	-	90	ns
			0	6	-	-	51	-	64	-	77	ns
			-4.5	4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	-	5	-	27	-	-	-	-	-	ns
Maximum Switch Turn “ON” Delay 4352 Sn to V_{OS}	t_{PZH}, t_{PZL}	C_L = 50pF	0	2	-	-	375	-	470	-	565	ns
			0	4.5	-	-	75	-	94	-	113	ns
			0	6	-	-	64	-	80	-	96	ns
			-4.5	4.5	-	-	55	-	69	-	83	ns
		C_L = 15pF	-	5	-	35	-	-	-	-	-	ns
Maximum Switch Turn “OFF” Delay 4351 $\overline{E1}$ to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	2	-	-	250	-	315	-	375	ns
			0	4.5	-	-	50	-	63	-	75	ns
			0	6	-	-	43	-	54	-	64	ns
			-4.5	4.5	-	-	40	-	50	-	60	ns
		C_L = 15pF	-	5	-	21	-	-	-	-	-	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{EE} (V)	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Maximum Switch Turn “OFF” Delay 4351 E2 to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	2	-	-	250	-	315	-	375	ns
			0	4.5	-	-	50	-	63	-	75	ns
			0	6	-	-	43	-	54	-	64	ns
			-4.5	4.5	-	-	40	-	50	-	60	ns
		C_L = 15pF	-	5	-	21	-	-	-	-	-	ns
Maximum Switch Turn “OFF” Delay 4351 $\overline{LE}$ to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	2	-	-	275	-	345	-	415	ns
			0	4.5	-	-	55	-	69	-	83	ns
			0	6	-	-	47	-	59	-	71	ns
			-4.5	4.5	-	-	45	-	56	-	68	ns
Maximum Switch Turn “OFF” Delay 4351 Sn to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	2	-	-	275	-	345	-	415	ns
			0	4.5	-	-	55	-	69	-	83	ns
			0	6	-	-	47	-	59	-	71	ns
			-4.5	4.5	-	-	48	-	60	-	71	ns
		C_L = 15pF	-	5	-	21	-	-	-	-	-	ns
Maximum Switch Turn “OFF” Delay 4352 $\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	2	-	-	275	-	345	-	415	ns
			0	4.5	-	-	55	-	69	-	83	ns
			0	6	-	-	47	-	59	-	71	ns
			-4.5	4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	-	5	-	21	-	-	-	-	-	ns
Setup Time 4351 Sn to $\overline{LE}$	t_{SU}	C_L = 50pF	0	2	-	-	60	-	75	-	90	ns
			0	4.5	-	-	12	-	15	-	18	ns
			0	6	-	-	10	-	13	-	15	ns
			-4.5	4.5	-	-	18	-	23	-	27	ns
Hold Time 4351 and 4352 Sn to $\overline{LE}$	t_H	C_L = 50pF	0	2	5	-	-	5	-	5	-	ns
			0	4.5	5	-	-	5	-	5	-	ns
			0	6	5	-	-	5	-	5	-	ns
			-4.5	4.5	5	-	-	5	-	5	-	ns
Pulse Width 4351 and 4352 $\overline{LE}$	t_W	C_L = 50pF	0	2	100	-	-	125	-	150	-	ns
			0	4.5	20	-	-	25	-	30	-	ns
			0	6	17	-	-	21	-	26	-	ns
			-4.5	4.5	25	-	-	31	-	38	-	ns
Input (Control) Capacitance	C_I	-	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 6, 7) 4351	C_{PD}	-	-	5	-	50	-	-	-	-	-	pF

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{EE} (V)	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Power Dissipation Capacitance (Notes 6, 7) 4352	C_{PD}	-	-	5	-	74	-	-	-	-	-	pF
HCT TYPES												
Propagation Delay, Switch In to Switch Out	t_{PLH}, t_{PHL}	C_L = 50pF	0	4.5	-	-	7	-	9	-	11	ns
			-4.5	4.5	-	-	5	-	7	-	8	ns
Maximum Switch Turn "ON" Delay 4351 $\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	t_{PZH}, t_{PZL}	C_L = 50pF	0	4.5	-	-	75	-	94	-	113	ns
			-4.5	4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	-	5	-	35	-	-	-	-	-	ns
Maximum Switch Turn "ON" Delay 4351 Sn to V_{OS}	t_{PZH}, t_{PZL}	C_L = 50pF	0	4.5	-	-	75	-	94	-	113	ns
			-4.5	4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	-	5	-	35	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4351 $\overline{E1}$ to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	4.5	-	-	55	-	69	-	83	ns
			-4.5	4.5	-	-	40	-	50	-	60	ns
		C_L = 15pF	-	5	-	23	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4351 E2 to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	4.5	-	-	60	-	75	-	90	ns
			-4.5	4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	-	5	-	23	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4351 $\overline{LE}$ to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	4.5	-	-	60	-	75	-	90	ns
			-4.5	4.5	-	-	55	-	69	-	83	ns
Maximum Switch Turn "OFF" Delay 4351 Sn to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	4.5	-	-	65	-	81	-	98	ns
			-4.5	4.5	-	-	55	-	69	-	83	ns
		C_L = 15pF	-	5	-	23	-	-	-	-	-	ns
Setup Time 4351 Sn to $\overline{LE}$		C_L = 50pF	0	4.5	-	-	12	-	15	-	18	ns
			-4.5	4.5	-	-	14	-	18	-	21	ns
Hold Time 4351 and 4352 Sn to $\overline{LE}$		C_L = 50pF	0	4.5	5	-	-	5	-	5	-	ns
			-4.5	4.5	5	-	-	5	-	5	-	ns
Pulse Width 4351 $\overline{LE}$	t_W	C_L = 50pF	0	4.5	25	-	-	31	-	28	-	ns
			-4.5	4.5	25	-	-	31	-	38	-	ns
Input (Control) Capacitance	C_I	-	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 6, 7) 4351	C_{PD}	-	-	5	-	52	-	-	-	-	-	pF

NOTES:

6. C_{PD} is used to determine the dynamic power consumption, per package.
7. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Analog Channel Specifications $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS	TYPE	V_{EE} (V)	V_{CC} (V)	HC/HCT	UNITS
Switch Input Capacitance	C_I		All	-	-	5	pF
Common Capacitance	C_{COM}		4351	-	-	25	pF
			4352	-	-	12	pF
Minimum Switch Frequency Response at -3dB (Figure 6, 8)	f_{MAX}	See Figure 11 (Notes 8, 9)	4351	-	-	145	MHz
			4352	-2.25	2.25	165	MHz
			4351	-	-	180	MHz
			4352	-4.5	4.5	185	MHz
Crosstalk Between Any Two Switches (Note 11)		See Figure 10 (Notes 9, 10)	4351	-	-	N/A	dB
			4352	-2.25	2.25	(TBE)	dB
			4351	-	-	N/A	dB
			4352	-4.5	4.5	(TBE)	dB
Sine-Wave Distortion		See Figure 12	All	-2.25	2.25	0.035	%
			All	-4.5	4.5	0.018	%
$\overline{E}$ or S to Switch Feedthrough Noise		See Figure 13 (Notes 9, 10)	4351	-	-	-	mV
			4352	-2.25	2.25	(TBE)	mV
			4351	-	-	-	mV
			4352	-4.5	4.5	(TBE)	mV
Switch “OFF” Signal Feedthrough (Figure 6, 8)		See Figure 14 (Notes 9, 10)	4351	-	-	-73	dB
			4352	-2.25	2.25	-65	dB
			4351	-	-	-75	dB
			4352	-4.5	4.5	-67	dB

NOTES:

8. Adjust input voltage to obtain 0dBm at V_{OS} for, f_{in} = 1MHz.
9. V_{IS} is centered at $(V_{CC} - V_{EE})/2$.
10. Adjust input for 0dBm.
11. Not applicable for ’HC4351 and CD74HCT4351.

Typical Performance Curves

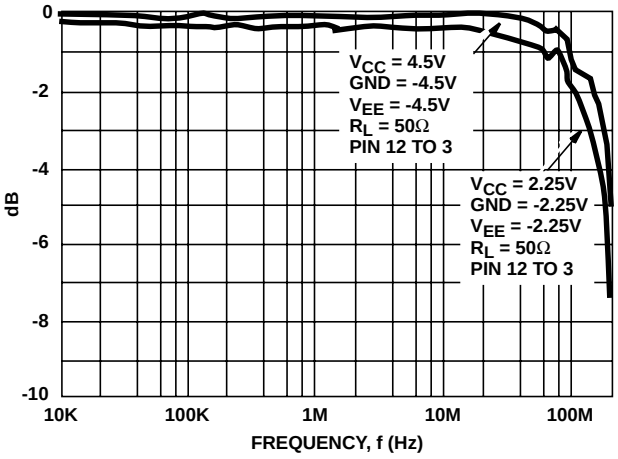


FIGURE 5. CHANNEL ON BANDWIDTH ('HC4351, CD74HCT4351)

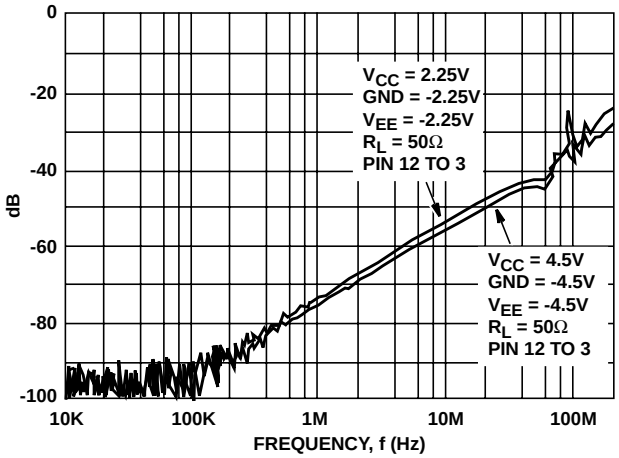


FIGURE 6. CHANNEL OFF FEEDTHROUGH ('HC4351, CD74HCT4351)

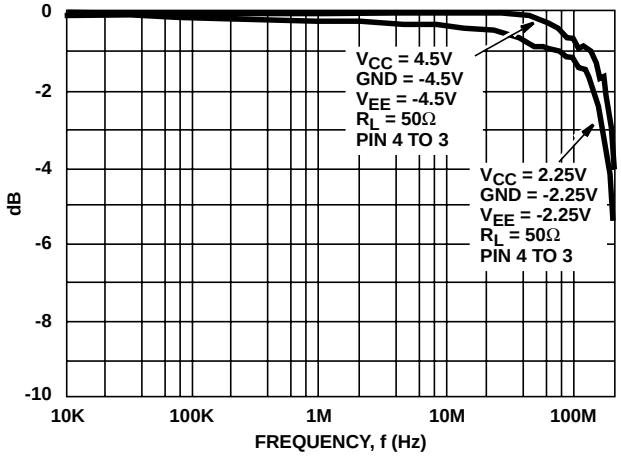


FIGURE 7. CHANNEL ON BANDWIDTH (CD74HC4352)

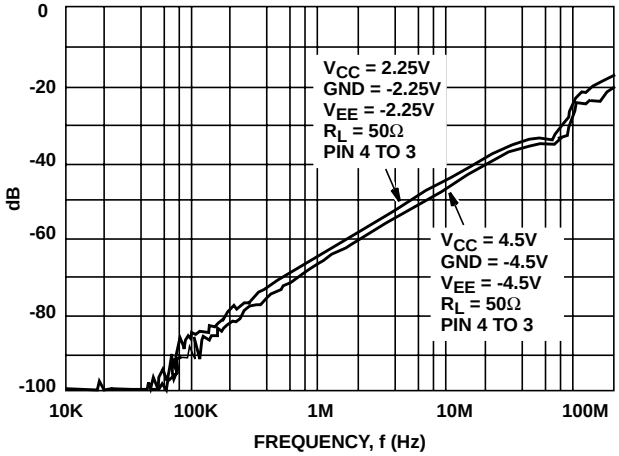


FIGURE 8. CHANNEL OFF FEEDTHROUGH (CD74HC4352)

Typical Performance Curves (Continued)

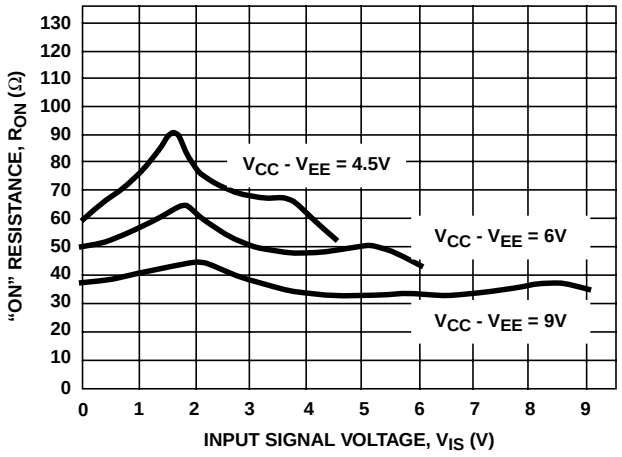


FIGURE 9. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE

Analog Test Circuits

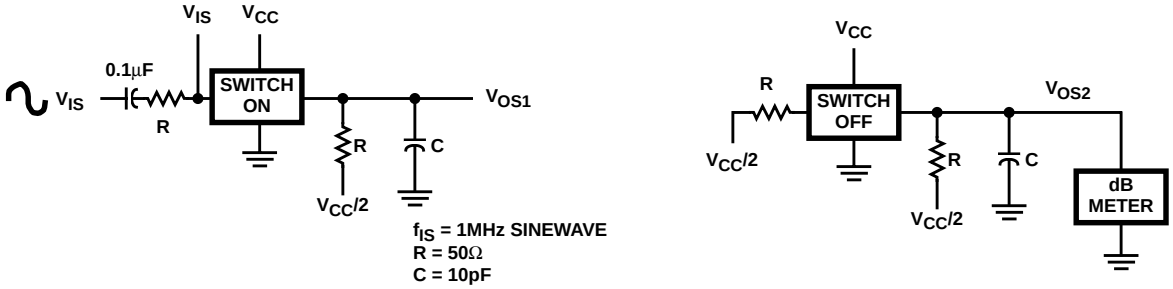


FIGURE 10. CROSSTALK BETWEEN TWO SWITCHES TEST CIRCUIT

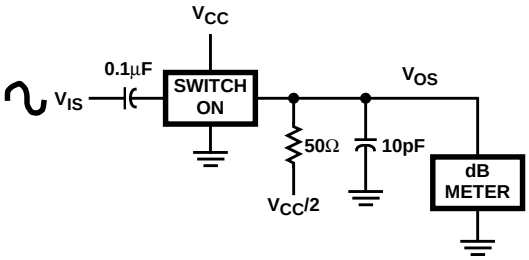


FIGURE 11. FREQUENCY RESPONSE TEST CIRCUIT

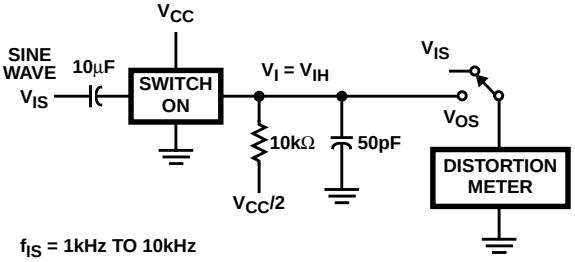


FIGURE 12. TOTAL HARMONIC DISTORTION TEST CIRCUIT

Analog Test Circuits (Continued)

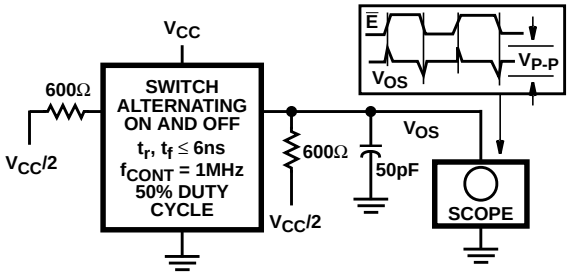


FIGURE 13. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

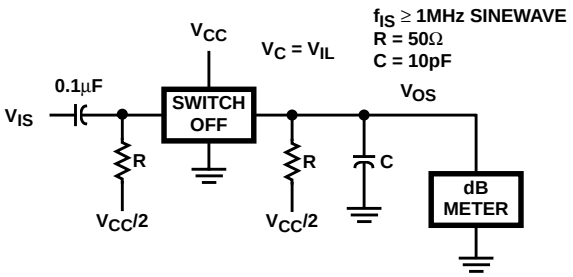
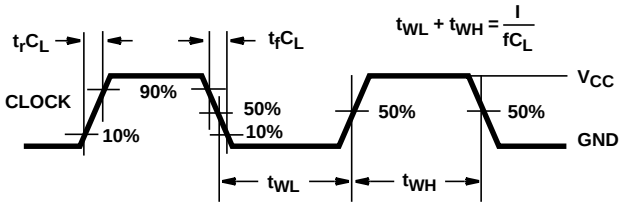


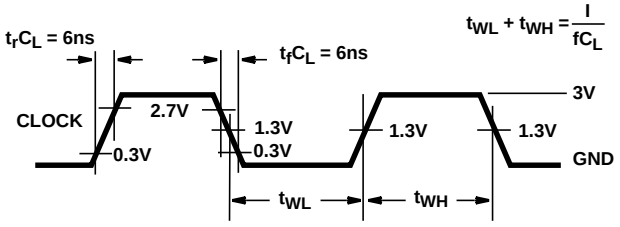
FIGURE 14. SWITCH OFF SIGNAL FEEDTHROUGH

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 15. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 16. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

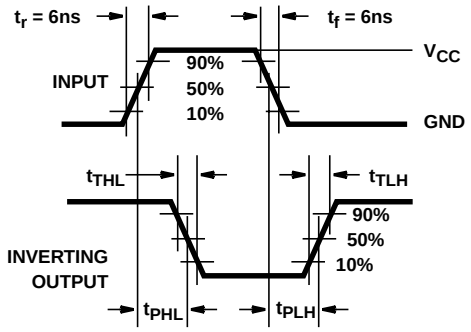


FIGURE 17. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

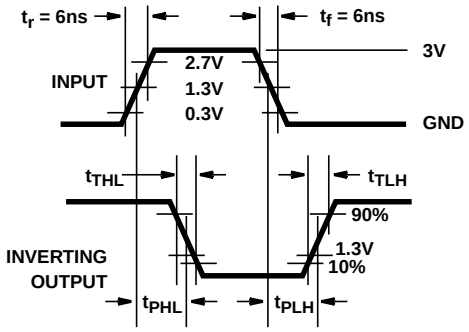


FIGURE 18. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

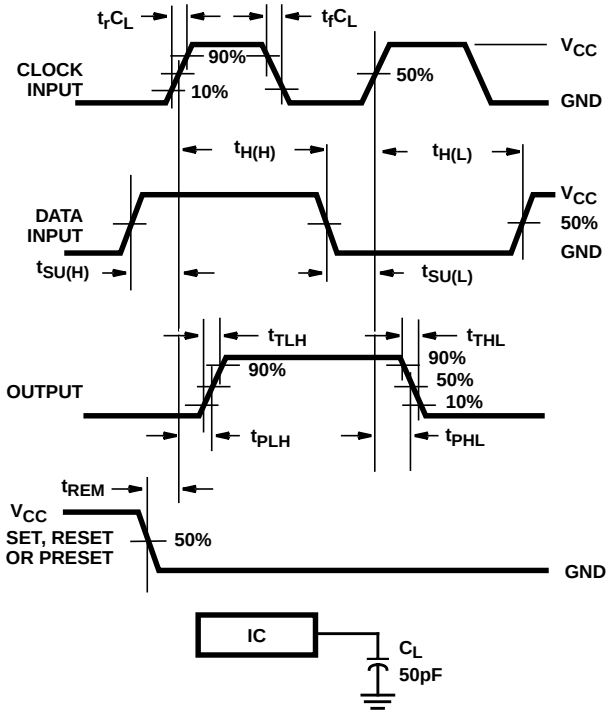


FIGURE 19. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

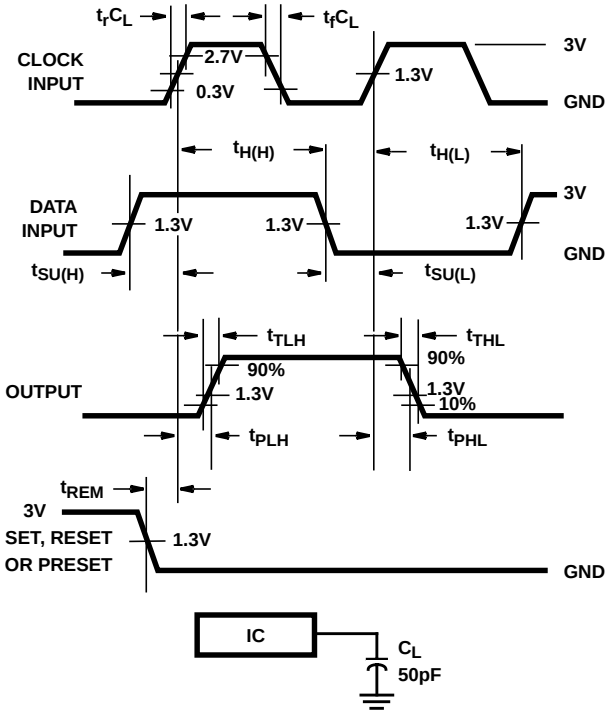


FIGURE 20. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued)

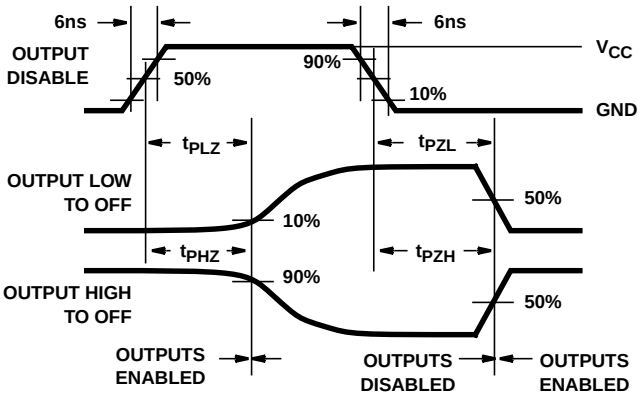


FIGURE 21. HC THREE-STATE PROPAGATION DELAY WAVEFORM

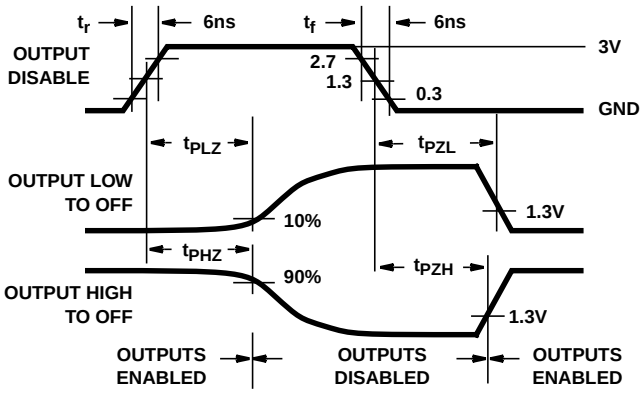
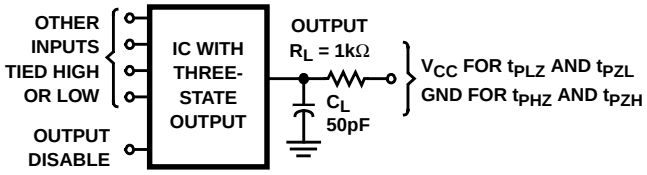


FIGURE 22. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

FIGURE 23. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54HC4351F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4351F3A	Samples
CD74HC4351E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4351E	Samples
CD74HC4351EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4351E	Samples
CD74HC4351M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4351M	Samples
CD74HC4351M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4351M	Samples
CD74HC4351ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4351M	Samples
CD74HC4352E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4352E	Samples
CD74HCT4351E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4351E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD54HC4351, CD74HC4351 :

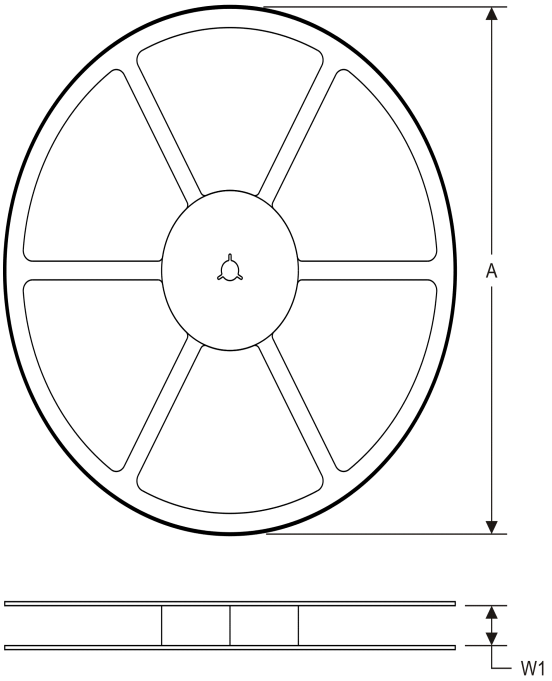
- Catalog: CD74HC4351
- Military: CD54HC4351

NOTE: Qualified Version Definitions:

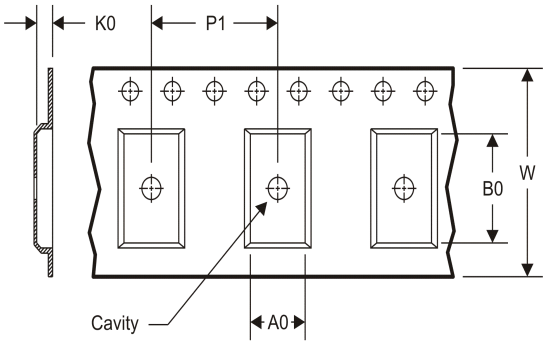
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



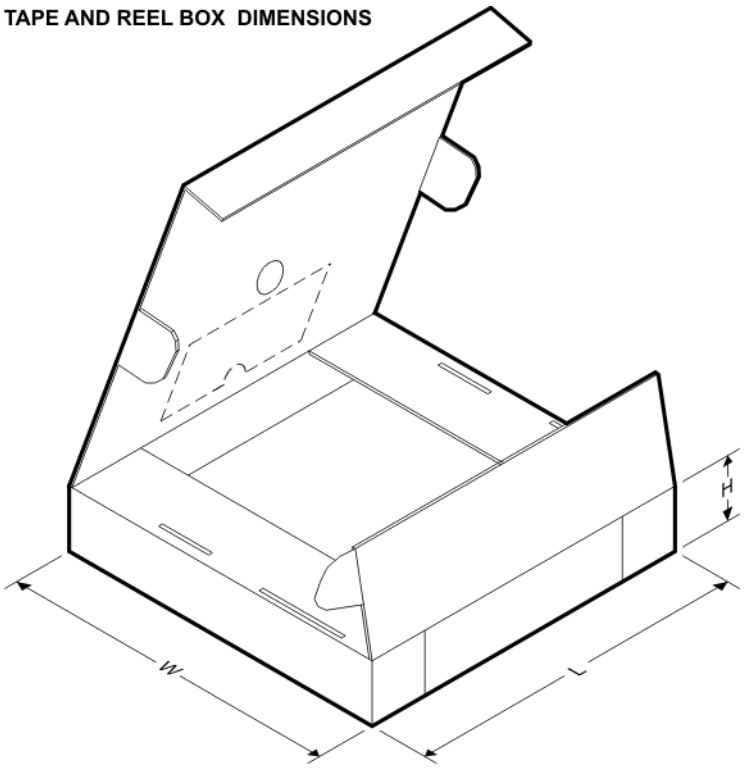
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4351M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



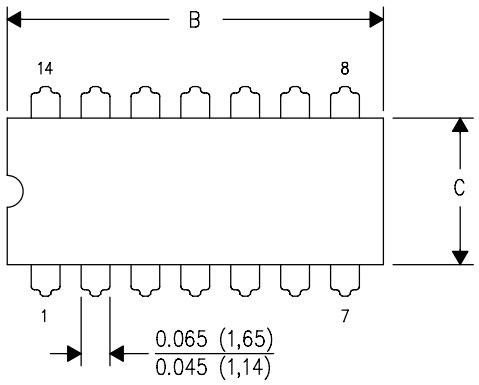
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4351M96	SOIC	DW	20	2000	367.0	367.0	45.0

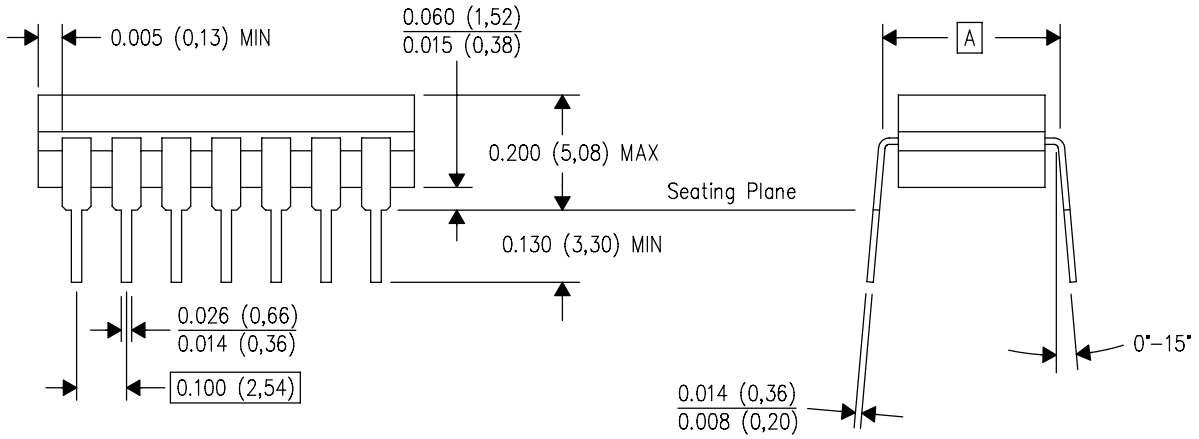
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



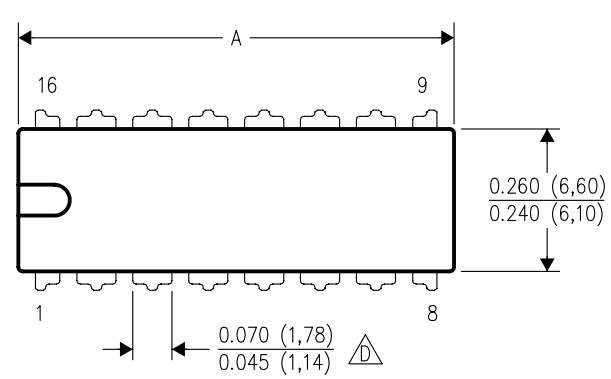
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

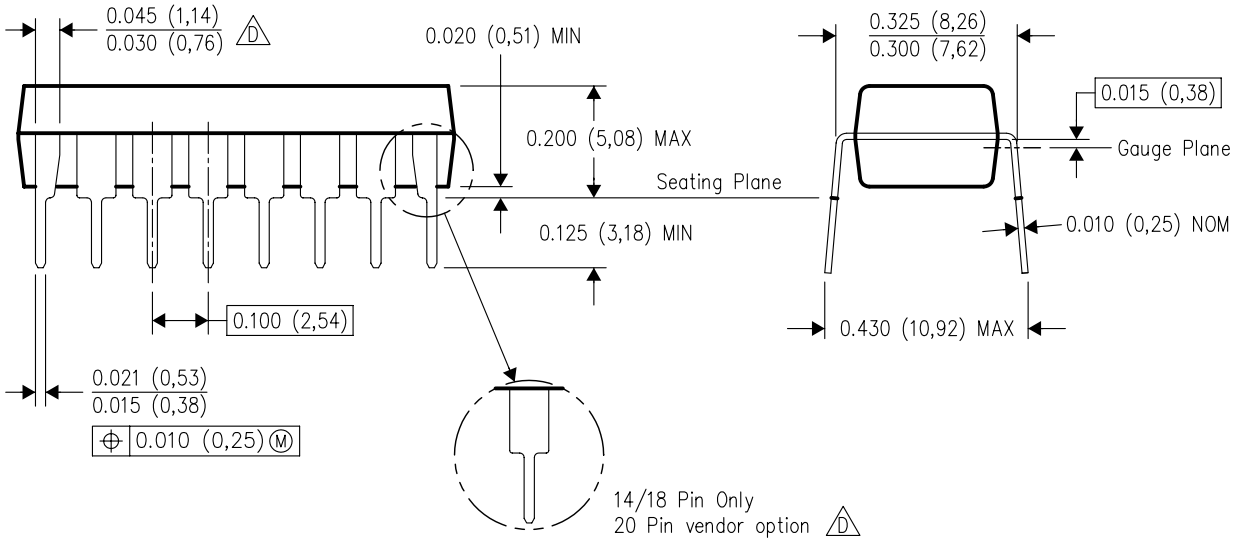
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

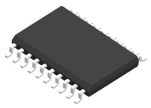


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

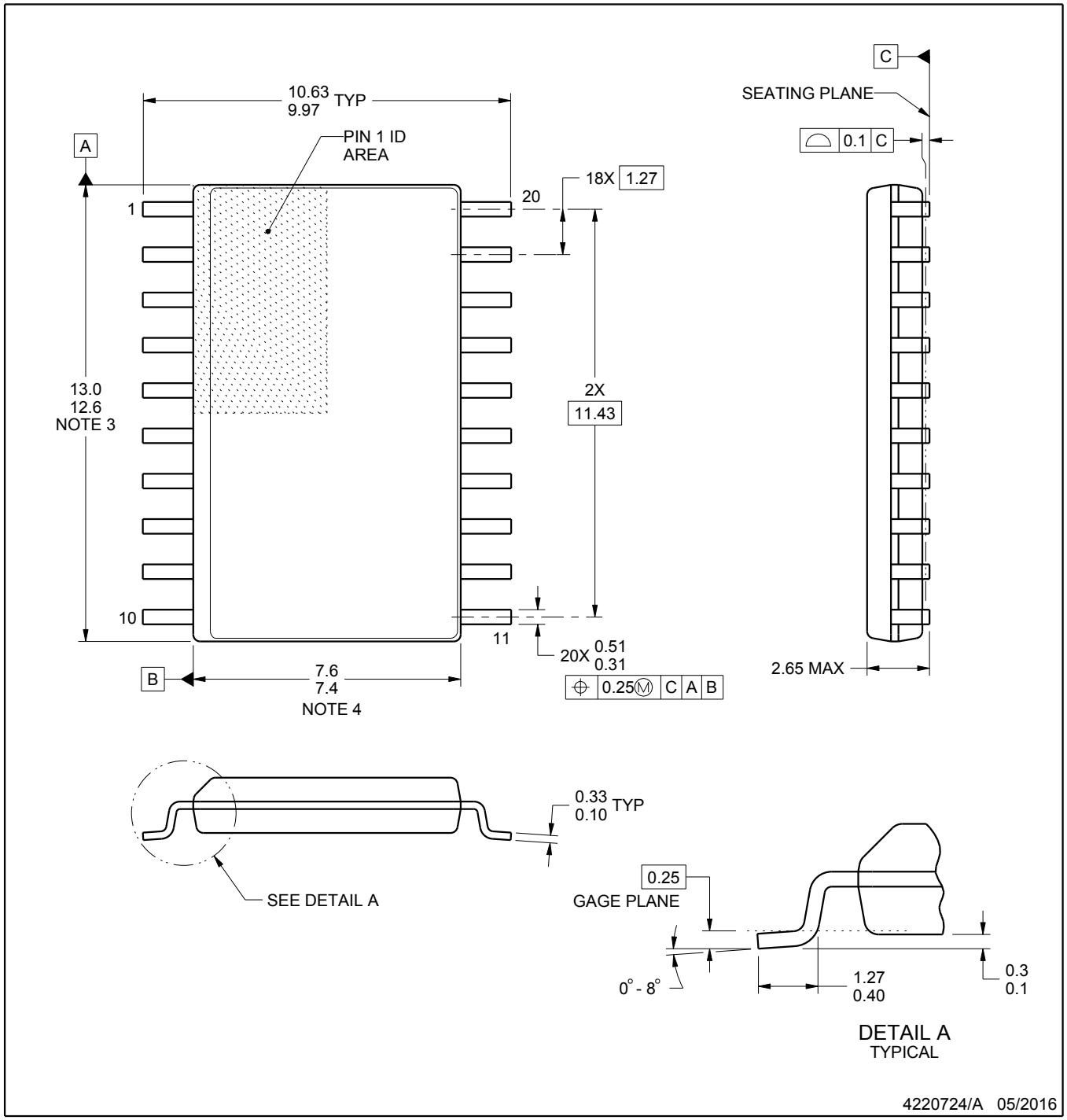


PACKAGE OUTLINE

DW0020A

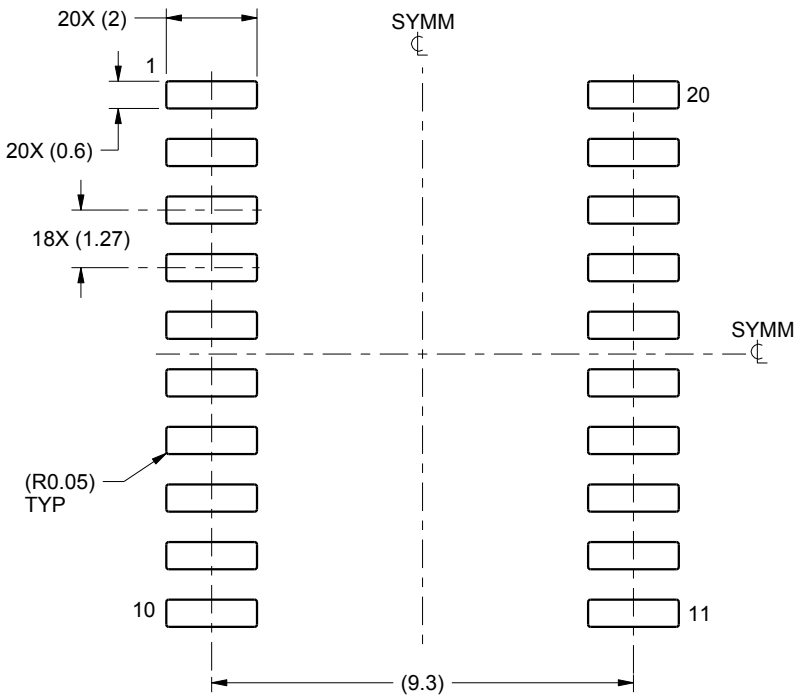
SOIC - 2.65 mm max height

SOIC

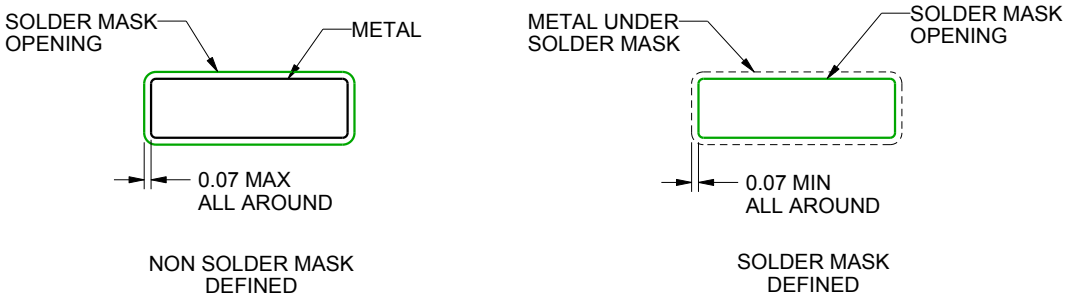


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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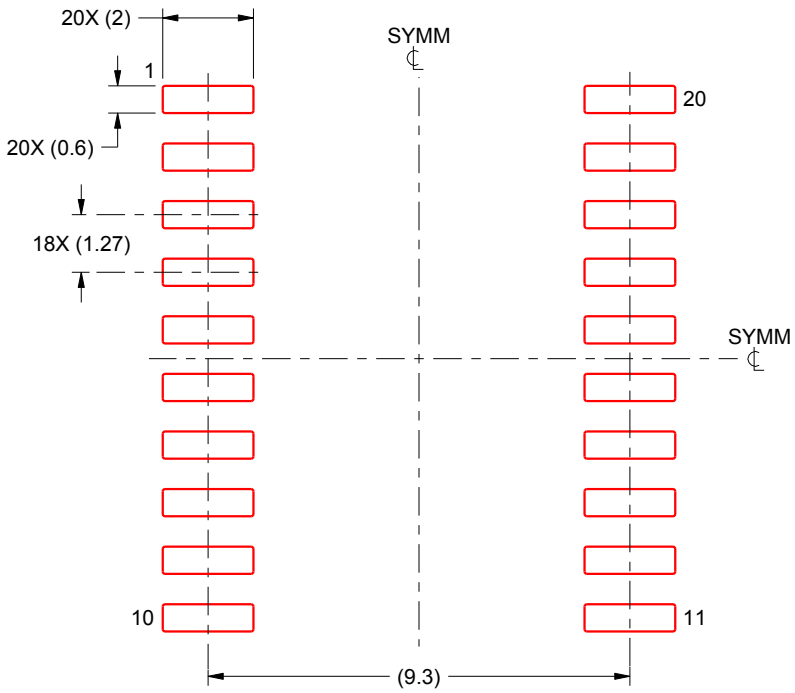
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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