



## 64-Channel, Current-Input Analog-to-Digital Converter

Check for Samples: [DDC264](#)

### FEATURES

- **Single-Chip Solution to Directly Measure 64 Low-Level Currents**
- **Proven High-Precision, True Integrating Architecture with 100% Charge Collection**
- **Easy Upgrade for Existing DDC Family Applications**
- **Very Low Power: 3mW/channel**
- **Extremely Linear:**  
INL =  $\pm 0.025\%$  of Reading  $\pm 1.0\text{ppm}$  of FSR
- **Low Noise: 6.3ppm of FSR**
- **Adjustable Full-Scale Range**
- **Adjustable Speed**
  - Data Rates up to 6kSPS with 20-bit Performance
  - Integration Times as low as 160 $\mu\text{s}$
- **Daisy-Chainable Serial Interface**
- **In-Package Bypass Capacitors Simplify PCB Design**

### APPLICATIONS

- **CT Scanner DAS**
- **Photodiode Sensors**
- **X-Ray Detection Systems**

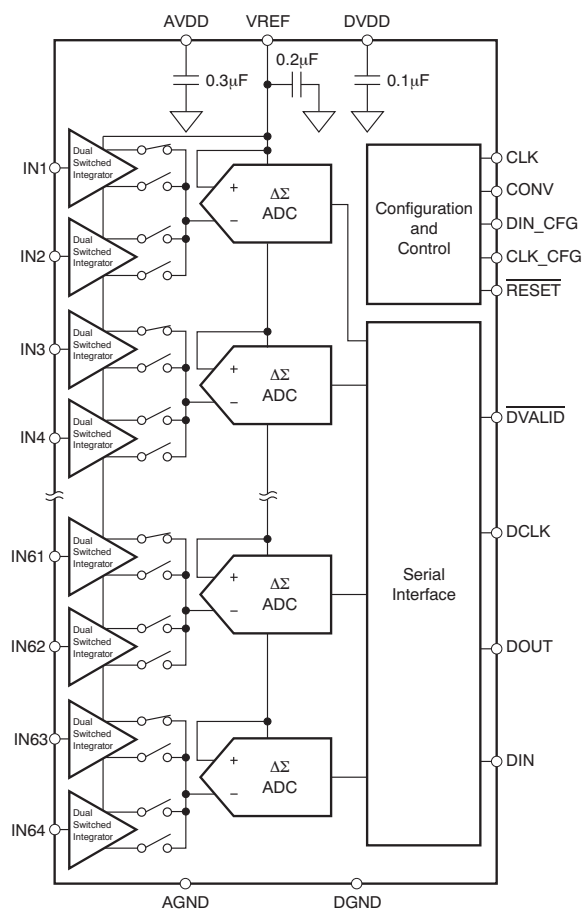
### DESCRIPTION

The DDC264 is a 20-bit, 64-channel, current-input analog-to-digital (A/D) converter. It combines both current-to-voltage and A/D conversion so that 64 separate low-level current output devices, such as photodiodes, can be directly connected to its inputs and digitized.

For each of the 64 inputs, the DDC264 uses the proven dual switched integrator front-end. This configuration allows for continuous current integration: while one integrator is being digitized by the onboard A/D converter, the other is integrating the input current. This architecture provides both a very stable offset and a loss-less collection of the input current. Adjustable integration times range from 160 $\mu\text{s}$  to 1s, allowing currents from fAs to  $\mu\text{As}$  to be continuously measured with outstanding precision.

The DDC264 has a serial interface designed for daisy-chaining in multi-device systems. Simply connect the output of one device to the input of the next to create the chain. Common clocking feeds all the devices in the chain so that the digital overhead in a multi-DDC264 system is minimal.

The DDC264 uses a +5V analog supply and a +2.7V to +3.6V digital supply. Bypass capacitors within the DDC264 package help minimize the external component requirements. Operating over the temperature range of 0°C to +70°C, the DDC264 BGA-100 package is offered in two versions: the DDC264C for low-power applications, and the DDC264CK when higher speeds are required.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### DDC FAMILY OVERVIEW

PRODUCT	NO. OF CHANNELS	FULL-SCALE	MAXIMUM DATA RATE	POWER/CHANNEL	PACKAGE-LEAD
<a href="#">DDC112</a>	2	1000pC	20kSPS	40mW	SO-28
<a href="#">DDC112K</a>	2	1000pC	3.3kSPS	40mW	TQFP-32
<a href="#">DDC114</a>	4	350pC	3.3kSPS	13mW	QFN-48
<a href="#">DDC118</a>	8	350pC	3.3kSPS	13mW	QFN-48
<a href="#">DDC316</a>	16	12pC	100kSPS	28mW	BGA-64
<a href="#">DDC232C</a>	32	350pC	3.1kSPS	7mW	BGA-64
<a href="#">DDC232CK</a>	32	350pC	6.2kSPS	10mW	BGA-64
<b>DDC264C</b>	64	150pC	3.1kSPS	3mW	BGA-100
<b>DDC264CK</b>	64	150pC	6.2kSPS	5.5mW	BGA-100

### ORDERING INFORMATION

For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

AVDD to AGND		–0.3V to +6V
DVDD to DGND		–0.3V to +3.6V
AGND to DGND		±0.2V
VREF Input to AGND		2.0V to AVDD + 0.3V
Analog Input to AGND		–0.3V to +0.7V
Digital Input Voltage to DGND		–0.3V to DVDD + 0.3V
Digital Output Voltage to DGND		–0.3V to DVDD + 0.3V
Operating Temperature		0°C to +70°C
Storage Temperature		–60°C to +150°C
Junction Temperature (T <sub>J</sub> )		+150°C
ESD Ratings:	Human Body Model (HBM) JEDEC standard 22, test method A114-C.01, all pins	4kV
	Charged Device Model (CDM) JEDEC standard 22, test method A114-C.01, all pins	1kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## ELECTRICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $AVDD = +5\text{V}$ ,  $DVDD = +3.0\text{V}$ ,  $VREF = +4.096\text{V}$ ,  $t_{\text{INT}} = 333\mu\text{s}$  for DDC264C or  $166\mu\text{s}$  for DDC264CK, and Range = 3 (150pC), unless otherwise noted.

PARAMETER	TEST CONDITIONS	DDC264C			DDC264CK			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>ANALOG INPUT RANGE</b>								
Range 0		10.5	12.5	14.5	10.5	12.5	14.5	pC
Range 1		47.5	50	52.5	47.5	50	52.5	pC
Range 2		95	100	105	95	100	105	pC
Range 3		142.5	150	157.5	142.5	150	157.5	pC
Negative Full-Scale Range		–0.4% of Positive Full-Scale Range			–0.4% of Positive Full-Scale Range			pC
<b>DYNAMIC CHARACTERISTICS</b>								
Data Rate			3	3.125		6	6.25	kSPS
Integration Time, $t_{\text{INT}}$		320	333	1,000,000	160	166	1,000,000	$\mu\text{s}$
System Clock (CLK)	Clkdiv = 0	1		5	1		10	MHz
	Clkdiv = 1	4		20	4		40	MHz
Data Clock (DCLK)				32			32	MHz
Configuration Clock (CLK_CFG)				20			20	MHz
<b>ACCURACY</b>								
Noise, Low-Level Input <sup>(1)</sup>	Range = 3, $C_{\text{SENSOR}}^{(2)} = 35\text{pF}$		6.3			6.3		ppm of FSR <sup>(3)</sup> , rms
Integral Linearity Error <sup>(4)</sup>		$\pm 0.025\%$ Reading $\pm 1.0\text{ppm}$ FSR, typ			$\pm 0.025\%$ Reading $\pm 1.0\text{ppm}$ FSR, typ			
		$\pm 0.05\%$ Reading $\pm 1.5\text{ppm}$ FSR, max			$\pm 0.05\%$ Reading $\pm 1.5\text{ppm}$ FSR, max			
Resolution	No Missing Codes, Format = 1	20			20			Bits
	No Missing Codes, Format = 0	16			16			Bits
Input Bias Current	$T_A = +25^\circ\text{C}$ to $+45^\circ\text{C}$		$\pm 0.5$	$\pm 5$		$\pm 0.5$	$\pm 5$	pA
Range Error Match <sup>(5)</sup>			0.1	0.5		0.1	0.5	% of FSR
Range Sensitivity to VREF	$VREF = 4.096 \pm 0.1\text{V}$		1:1			1:1		
Offset Error			$\pm 500$	$\pm 1000$		$\pm 500$	$\pm 1000$	ppm of FSR
Offset Error Match <sup>(5)</sup>			$\pm 150$			$\pm 150$		ppm of FSR
DC Bias Voltage <sup>(6)</sup>	Low-Level Input (< 1% FSR)		$\pm 0.1$	$\pm 1$		$\pm 0.1$	$\pm 1$	mV
Power-Supply Rejection Ratio	At dc		100	$\pm 300$		100	$\pm 300$	ppm of FSR/V

- (1) Input is less than 1% of full-scale.
- (2)  $C_{\text{SENSOR}}$  is the capacitance seen at the DDC264 inputs from wiring, photodiode, etc.
- (3) FSR is full-scale range.
- (4) A best-fit line is used in measuring nonlinearity.
- (5) Matching between side A and side B of the same input.
- (6) Voltage produced by the DDC264 at its input that is applied to the sensor.

## ELECTRICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $AVDD = +5\text{V}$ ,  $DVDD = +3.0\text{V}$ ,  $VREF = +4.096\text{V}$ ,  $t_{\text{INT}} = 333\mu\text{s}$  for DDC264C or  $166\mu\text{s}$  for DDC264CK, and Range = 3 (150pC), unless otherwise noted.

PARAMETER	TEST CONDITIONS	DDC264C			DDC264CK			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
<b>PERFORMANCE OVER TEMPERATURE</b>									
Offset Drift	$T_A = +25^\circ\text{C}$ to $+45^\circ\text{C}$		$\pm 0.5$	$5^{(7)}$		$\pm 0.5$	$5^{(7)}$	ppm of FSR/ $^\circ\text{C}$	
Offset Drift Stability			$\pm 0.2$	$2^{(7)}$		$\pm 0.2$	$2^{(7)}$	ppm of FSR/minute	
DC Bias Voltage Drift <sup>(8)</sup>				$\pm 3$			$\pm 3$	$\mu\text{V}/^\circ\text{C}$	
Input Bias Current Drift				0.01	$1^{(7)}$		0.01	$1^{(7)}$	$\text{pA}/^\circ\text{C}$
Range Drift <sup>(9)</sup>				25	50		25	50	ppm/ $^\circ\text{C}$
Range Drift Match <sup>(10)</sup>				$\pm 5$			$\pm 5$		ppm/ $^\circ\text{C}$
<b>REFERENCE</b>									
Voltage	Average Value with $t_{\text{INT}} = 333\mu\text{s}$ Average Value with $t_{\text{INT}} = 166\mu\text{s}$	4.000	4.096	4.200	4.000	4.096	4.200	V	
Input Current <sup>(11)</sup>				825			1650		$\mu\text{A}$ $\mu\text{A}$
<b>DIGITAL INPUT/OUTPUT</b>									
Logic Levels	$I_{\text{OH}} = -500\mu\text{A}$ $I_{\text{OL}} = 500\mu\text{A}$ $0 < V_{\text{IN}} < DVDD$	0.8 DVDD -0.1 DVDD - 0.4		DVDD + 0.1 0.2 DVDD 0.4 $\pm 10$	0.8 DVDD -0.1 DVDD - 0.4		DVDD + 0.1 0.2 DVDD 0.4 $\pm 10$	V V V V $\mu\text{A}$	
$V_{\text{IH}}$									
$V_{\text{IL}}$									
$V_{\text{OH}}$									
$V_{\text{OL}}$									
Input Current ( $I_{\text{IN}}$ )									
Data Format <sup>(12)</sup>	Straight Binary			Straight Binary					
<b>POWER-SUPPLY REQUIREMENTS</b>									
Analog Power-Supply Voltage (AVDD)		4.75	5.0	5.25	4.9	5.0	5.1	V	
Digital Power-Supply Voltage (DVDD)		2.7	3.3	3.6	2.7	3.3	3.6	V	
Supply Current									
Analog Current			34			60		mA	
Digital Current			7.5			15		mA	
Total Power Dissipation			192	256		350		mW	
Per Channel Power Dissipation			3	4		5.5		mW/Channel	

(7) Ensured by design; not production tested.

(8) Voltage produced by the DDC264 at its input that is applied to the sensor.

(9) Range drift does not include external reference drift.

(10) Matching between side A and side B of the same input.

(11) Input reference current decreases with increasing  $t_{\text{INT}}$  (see the [Voltage Reference](#) section).

(12) Data format is Straight Binary with a small offset. The number of bits in the output word is controlled by the Format bit.

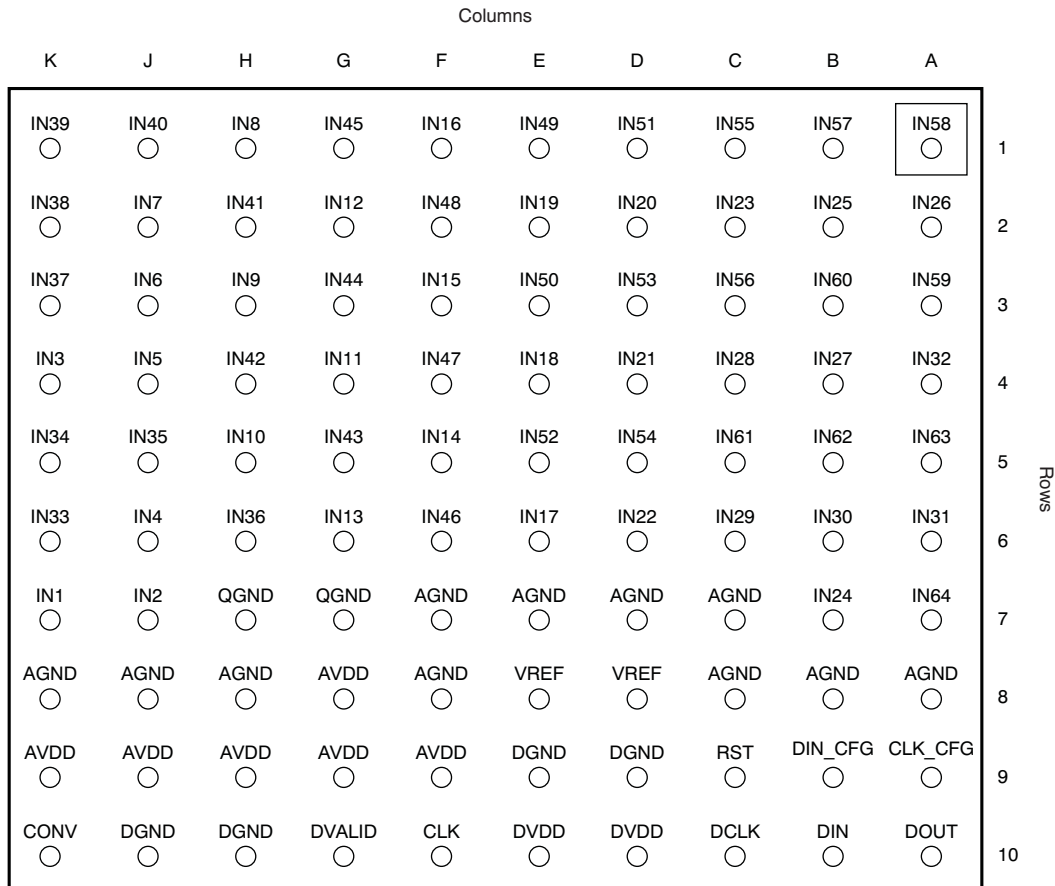
## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		DDC264C, DDC264CK	UNITS
		ZAW Package	
		100 Balls	
$\theta_{\text{JA}}$	Junction-to-ambient thermal resistance	25.7	$^\circ\text{C}/\text{W}$
$\theta_{\text{JCTop}}$	Junction-to-case (top) thermal resistance	9.8	
$\theta_{\text{JB}}$	Junction-to-board thermal resistance	7.1	
$\psi_{\text{JT}}$	Junction-to-top characterization parameter	0.1	
$\psi_{\text{JB}}$	Junction-to-board characterization parameter	7.0	
$\theta_{\text{JCbott}}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## PIN CONFIGURATION

### ZAW PACKAGE 9mm × 9mm BGA (TOP VIEW)



## PIN DESCRIPTIONS

PIN	LOCATION	FUNCTION	DESCRIPTION
IN1-IN64	Rows 1-6, A7, B7, J7, K7	Analog input	Analog inputs for channels 1 to 64
QGND	G7, H7	Analog	Quiet analog ground; see the guidelines described in the <a href="#">Layout</a> section
AGND	A8, B8, C7, C8, D7, E7, F7, F8, H8, J8, K8	Analog	Analog ground
DGND	D9, E9, H10, J10	Digital	Digital ground
AVDD	F9, G8, G9, H9, J9, K9	Analog	Analog power supply, +5V nominal
VREF	D8, E8	Analog input	External voltage reference input, +4.096V nominal
DVALID	G10	Digital output	Data valid output, active low
DIN_CFG	B9	Digital input	Configuration register data input
CLK_CFG	A9	Digital input	Configuration register clock input
RESET	C9	Digital input	Digital reset, active low
DVDD	D10, E10	Digital	Digital power supply, +3.3V nominal
CONV	K10	Digital input	Conversion control input: 0 = integrate on side B; 1 = integrate on side A
DIN	B10	Digital input	Serial data input
DOUT	A10	Digital output	Serial data output
CLK	F10	Digital input	Master clock input
DCLK	C10	Digital input	Serial data clock input

### TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ , unless otherwise indicated.

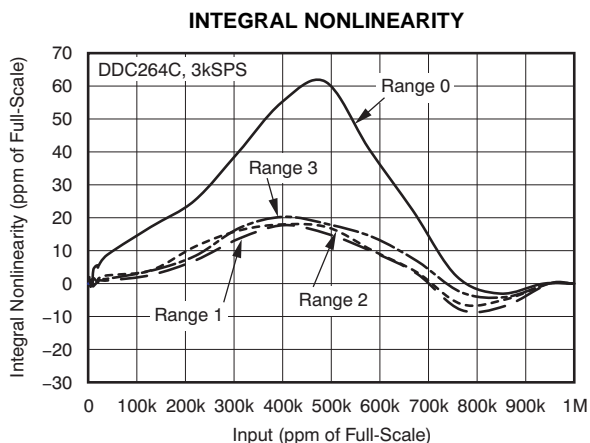


Figure 1.

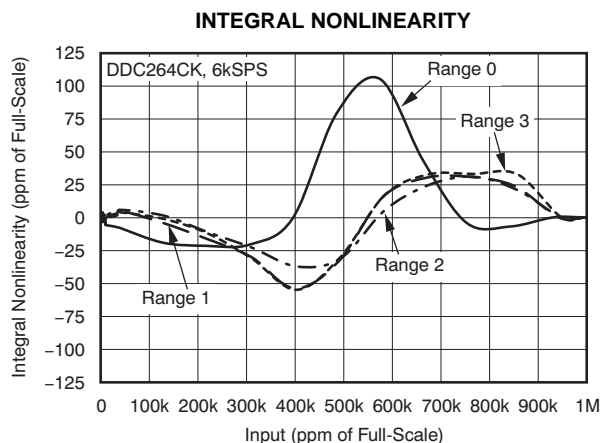


Figure 2.

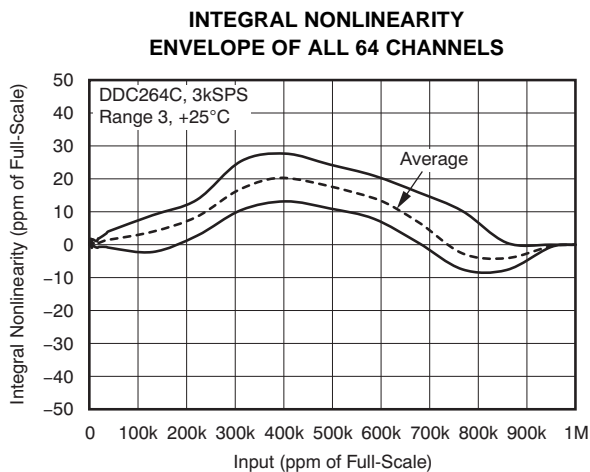


Figure 3.

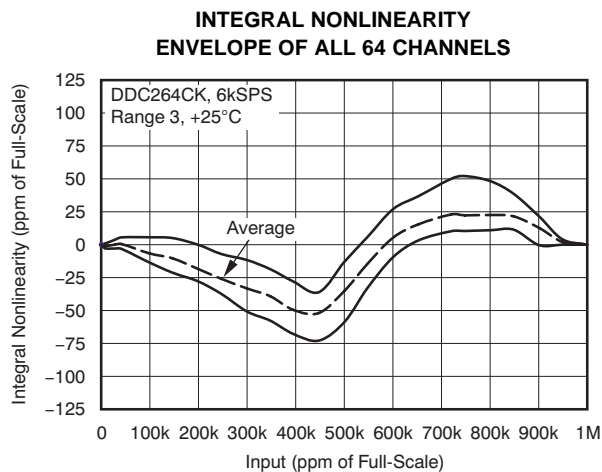


Figure 4.

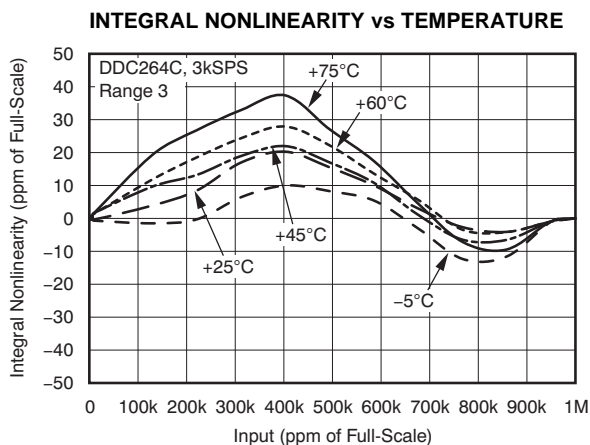


Figure 5.

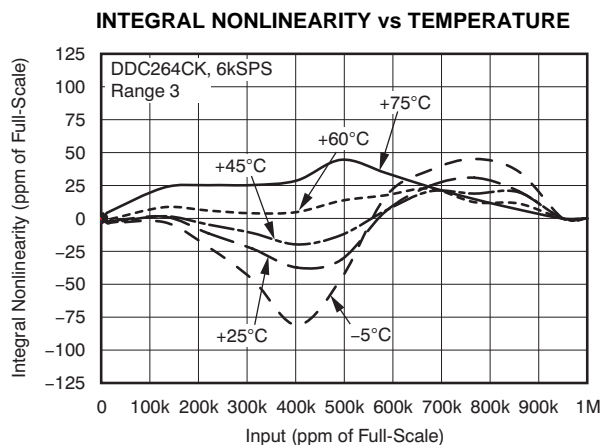


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise indicated.

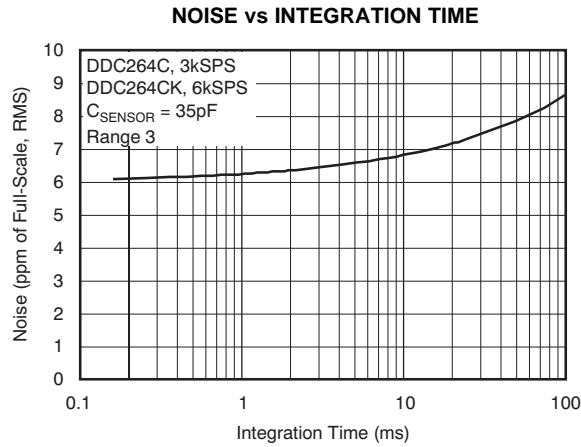


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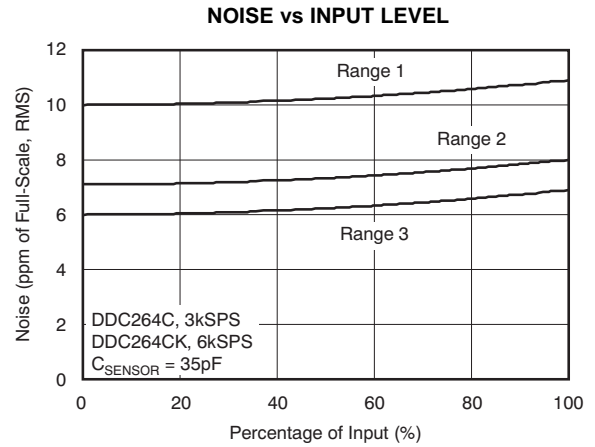


Figure 8.

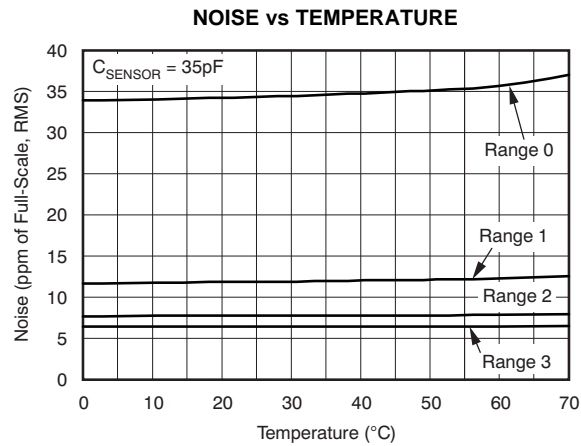


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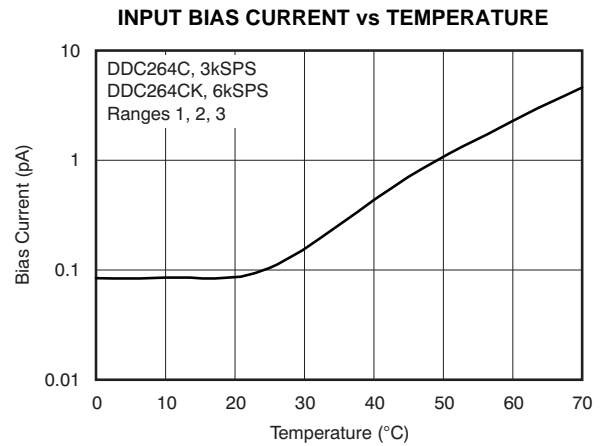


Figure 10.

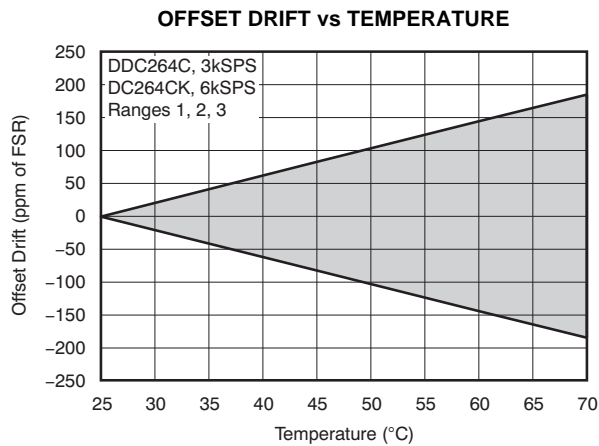


Figure 11.

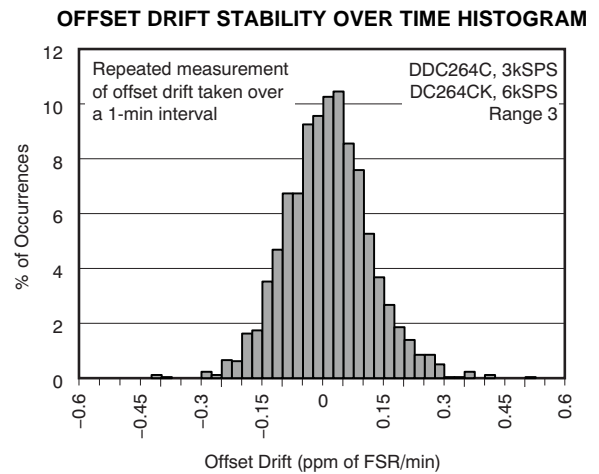
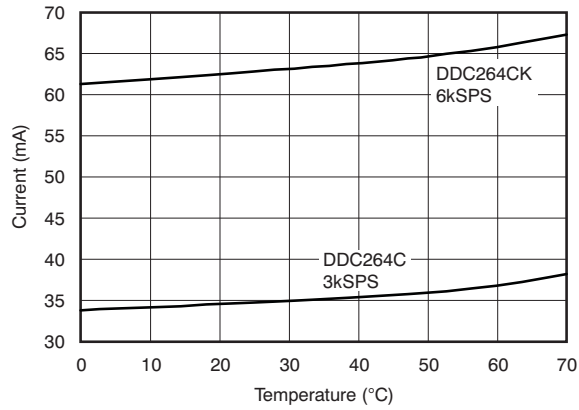


Figure 12.

**TYPICAL CHARACTERISTICS (continued)**

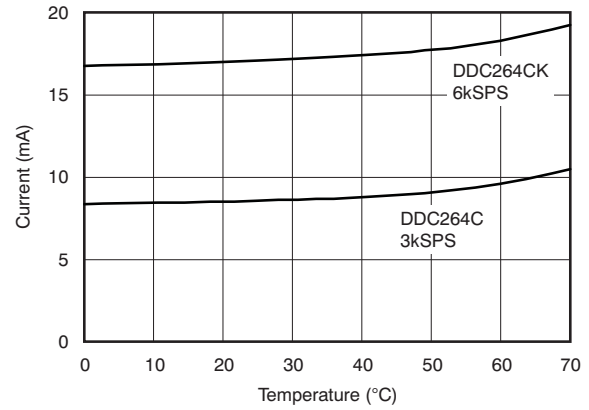
At  $T_A = +25^\circ\text{C}$ , unless otherwise indicated.

**ANALOG SUPPLY CURRENT vs TEMPERATURE**



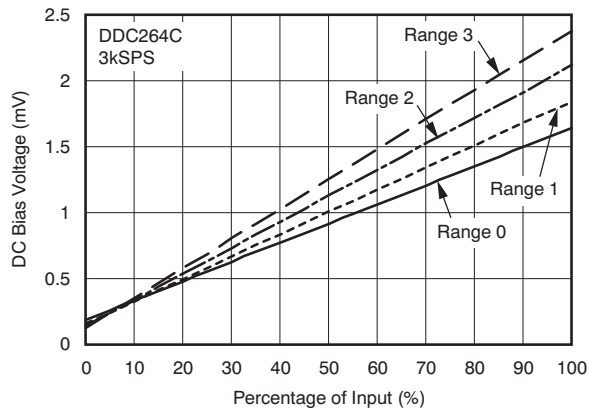
**Figure 13.**

**DIGITAL SUPPLY CURRENT vs TEMPERATURE**



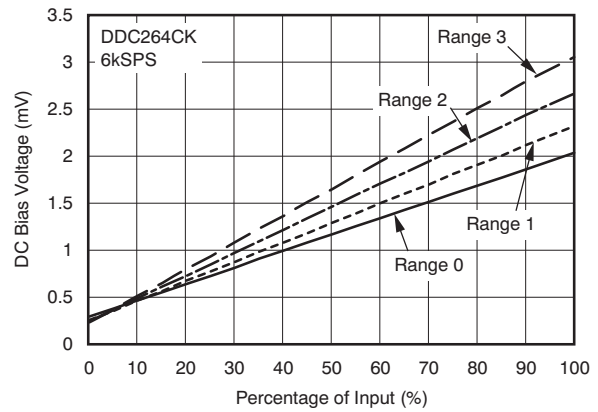
**Figure 14.**

**DC BIAS VOLTAGE vs INPUT PERCENTAGE**



**Figure 15.**

**DC BIAS VOLTAGE vs INPUT PERCENTAGE**



**Figure 16.**



Figure 17. NOISE vs  $C_{\text{SENSOR}}$

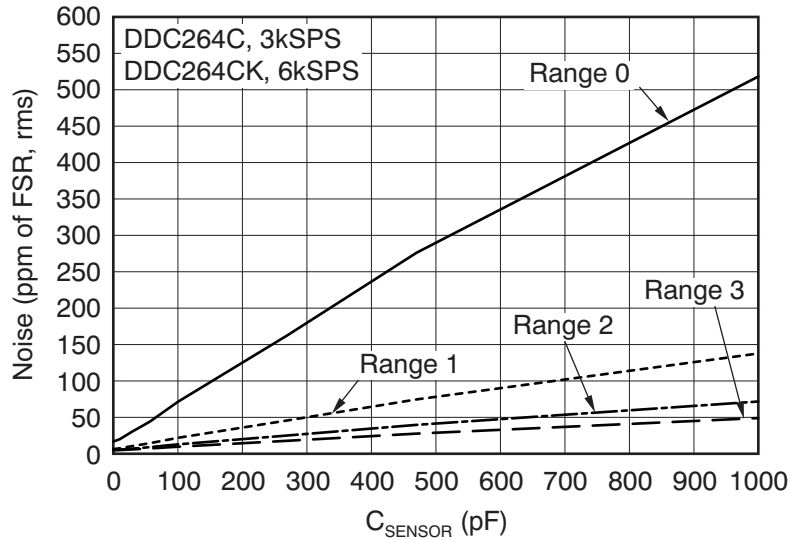


Figure 18.

Table 1. NOISE vs  $C_{\text{SENSOR}}$  <sup>(1)</sup>

RANGE	$C_{\text{SENSOR}}$								
	0pF	10pF	30pF	43pF	57pF	100pF	270pF	470pF	1000pF
ppm of FSR, rms									
Range 0: 12.5pC	16	20	30	37	44	71	160	270	510
Range 1: 50pC	6.4	7.4	10	12	14	21	45	74	130
Range 2: 100pC	5.1	5.5	7.1	8	9.1	12	25	39	71
Range 3: 150pC	4.8	5	6	6.5	7.2	9.6	17	27	49
fC, rms									
Range 0: 12.5pC	0.20	0.25	0.38	0.46	0.55	0.89	2.0	3.38	6.38
Range 1: 50pC	0.32	0.37	0.53	0.62	0.73	1.09	2.29	3.73	6.88
Range 2: 100pC	0.51	0.55	0.71	0.80	0.91	1.28	2.50	3.97	7.16
Range 3: 150pC	0.72	0.75	0.90	0.98	1.08	1.45	2.67	4.14	7.36
Electrons, rms									
Range 0: 12.5pC	1250	1560	2340	2890	3430	5540	12480	21070	39790
Range 1: 50pC	2010	2310	3340	3910	4570	6800	14200	23300	42900
Range 2: 100pC	3220	3440	4450	5000	5680	7990	15600	24800	44700
Range 3: 150pC	4530	4730	5610	6120	6770	9050	16700	25800	45900

(1) Noise in Table 1 is expressed in three different units for reader convenience. The first section lists noise in units of parts per million of full-scale range; the second section shows noise as an equivalent input charge (in fC); and the third section converts noise to electrons.

## THEORY OF OPERATION

### General Description

A dual switched integrator input channel for the DDC264 is shown in Figure 19. The DDC264 contains 64 identical input channels that perform the function of current-to-voltage integration followed by a multiplexed A/D conversion. Each input has two integrators so that the current-to-voltage integration can be continuous in time. The DDC264 continuously integrates the input signal by switching integrations between side A and side B.

For example, while side A integrates the input signal, the side B outputs are digitized by the onboard ADC. This integration and A/D conversion process is controlled by the convert pin, CONV. The results from side A and side B of each signal input are stored in a serial output shift register. The  $\overline{\text{DVALID}}$  output goes low when the shift register data are ready to be retrieved.

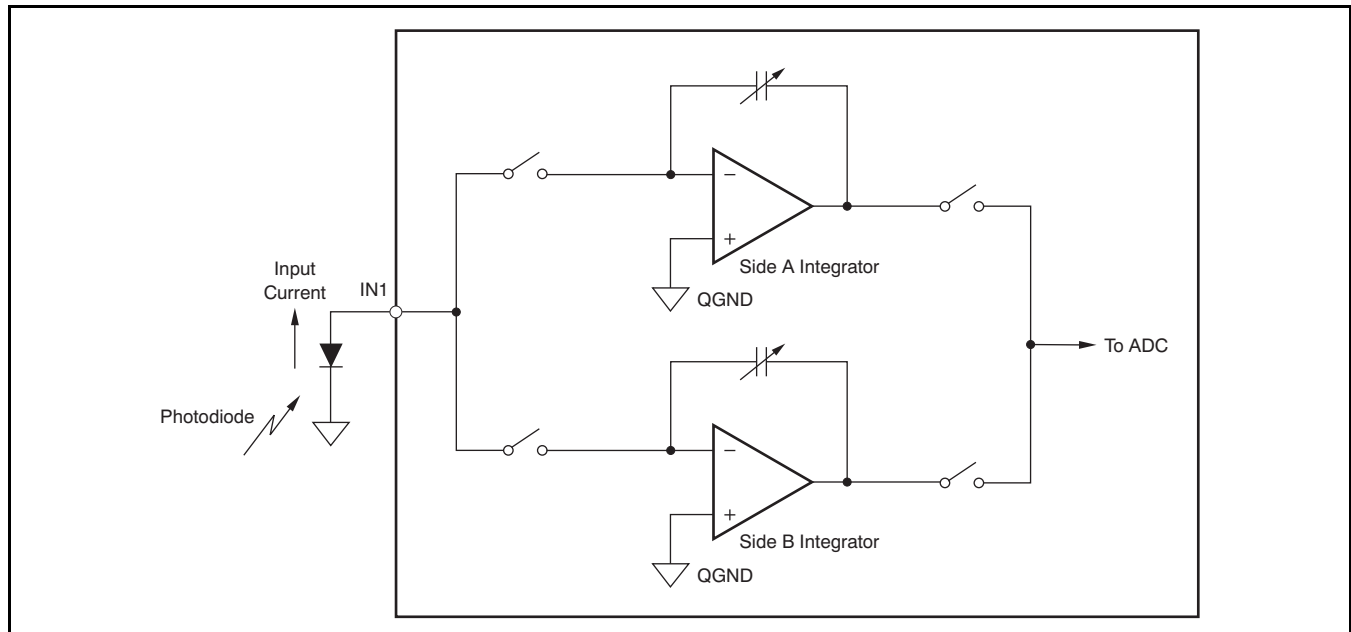


Figure 19. Dual Switched Integrator Architecture

## Basic Integration Cycle

The topology of the front end of the DDC264 is an analog integrator as shown in Figure 20. In this diagram, only input IN1 is shown. The input stage consists of an operational amplifier, a selectable feedback capacitor network ( $C_F$ ), and several switches that implement the integration cycle. The timing relationships of all of the switches shown in Figure 20 are illustrated in Figure 21. Figure 21 conceptualizes the operation of the integrator input stage of the DDC264 and should not be used as an exact timing tool for design.

See Figure 22 for the block diagrams of the reset, integrate, wait, and convert states of the integrator section of the DDC264. This internal switching network is controlled externally with the convert pin (CONV) and the system clock (CLK). For the best noise performance, CONV must be synchronized with the falling edge of CLK. It is recommended that CONV toggle within  $\pm 10\text{ns}$  of the falling edge of CLK.

The noninverting inputs of the integrators are connected to the QGND pin. Consequently, the DDC264 analog ground, QGND, should be as clean as possible. In Figure 20, the feedback capacitors ( $C_F$ ) are shown in parallel between the inverting input and output of the operational amplifier. At the beginning of a conversion, the switches  $S_{A/D}$ ,  $S_{INTA}$ ,  $S_{INTB}$ ,  $S_{REF1}$ ,  $S_{REF2}$ , and  $S_{RESET}$  are set (see Figure 21).

At the completion of an A/D conversion, the charge on the integration capacitor ( $C_F$ ) is reset with  $S_{REF1}$  and  $S_{RESET}$  (see Figure 21 and Figure 22a). This process is done during reset. In this manner, the selected capacitor is charged to the reference voltage, VREF. Once the integration capacitor is charged,  $S_{REF1}$  and  $S_{RESET}$  are switched so that VREF is no longer connected to the amplifier circuit while it waits to begin integrating (see Figure 22b). With the rising edge of CONV,  $S_{INTA}$  closes, which begins the integration of side A. This process puts the integrator stage into its integrate mode (see Figure 22c).

Charge from the input signal is collected on the integration capacitor, causing the voltage output of the amplifier to decrease. The falling edge of CONV stops the integration by switching the input signal from side A to side B ( $S_{INTA}$  and  $S_{INTB}$ ). Prior to the falling edge of CONV, the signal on side B was converted by the A/D converter and reset during the time that side A was integrating. With the falling edge of CONV, side B starts integrating the input signal. At this point, the output voltage of the side A operational amplifier is presented to the input of the A/D converter (see Figure 22d).

A special electrostatic discharge (ESD) structure protects the inputs but does not increase current leakage on the input pins.

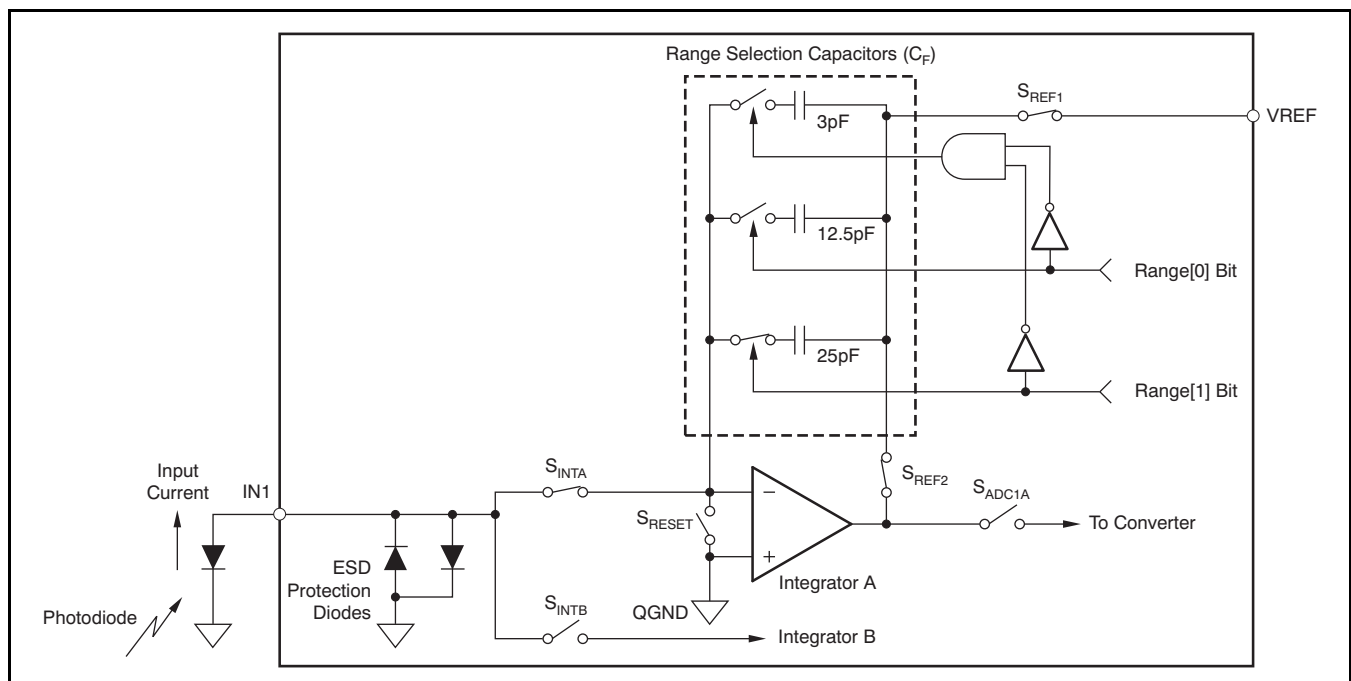


Figure 20. Basic Integration Configuration

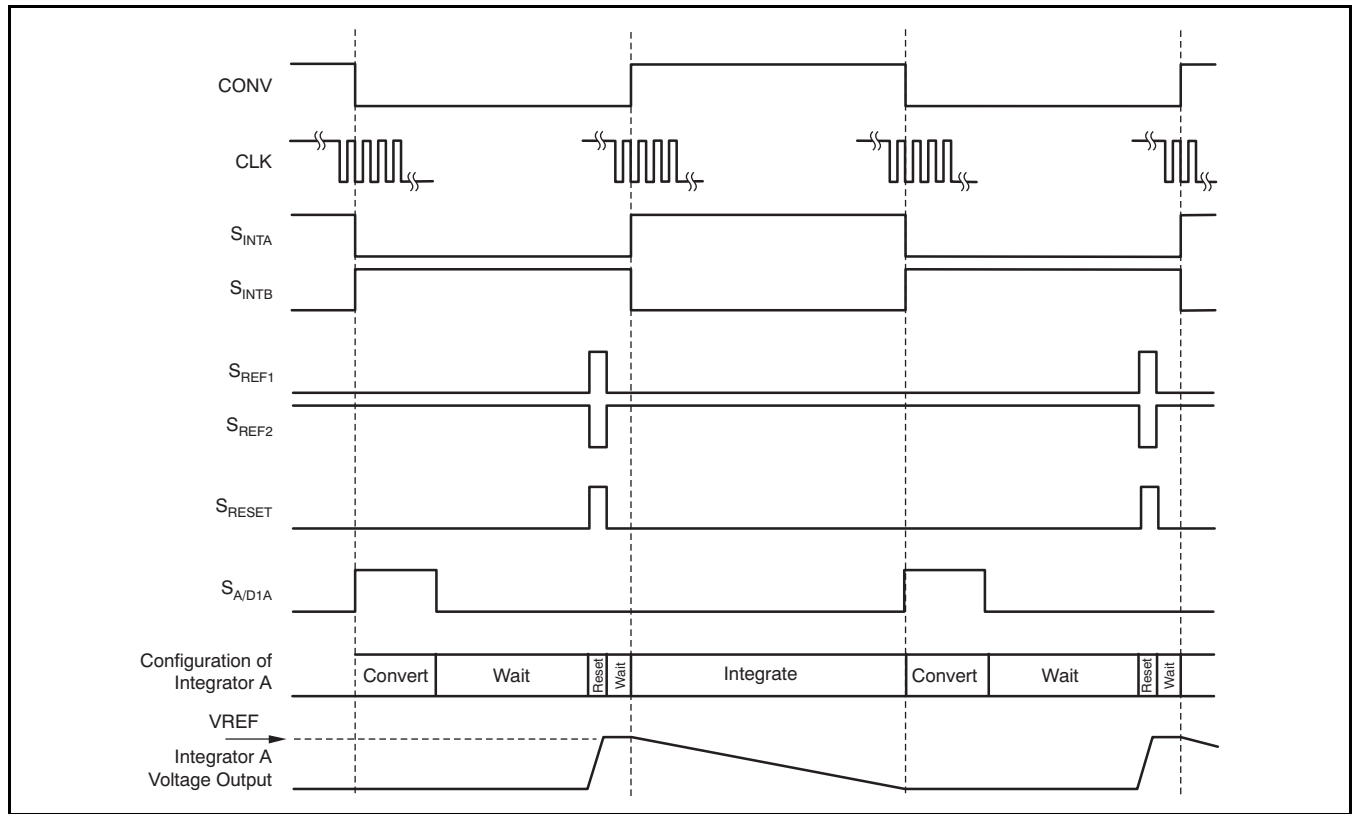


Figure 21. Integration Timing (see Figure 20)

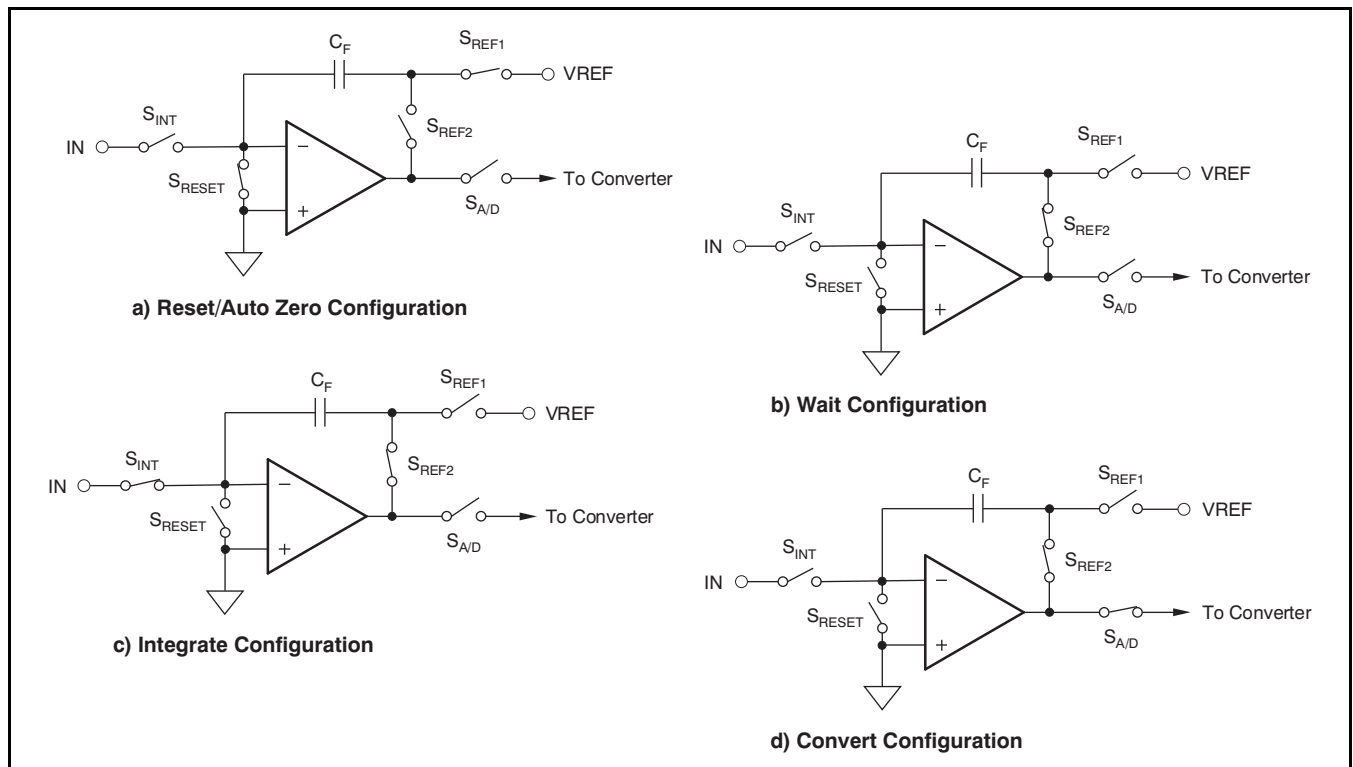


Figure 22. Four Configurations of the Front-End Integrators

## Integration Capacitors

There are four different capacitor configurations available on-chip for both sides of every channel in the DDC264. These internal capacitors are trimmed in production to achieve the specified performance for range error of the DDC264. The range control bits (Range[1:0]) set the capacitor value for all integrators. Consequently, all inputs and both sides of each input always have the same full-scale range. Table 2 shows the capacitor value selected for each range selection.

Table 2. Range Selection

RANGE	RANGE CONTROL BITS		C <sub>F</sub>	INPUT RANGE
	Range[1]	Range[0]		
0	0	0	3pF	-0.04 to 12.5pC
1	0	1	12.5pF	-0.2 to 50.0pC
2	1	0	25pF	-0.4 to 100pC
3	1	1	37.5pF	-0.6 to 150pC

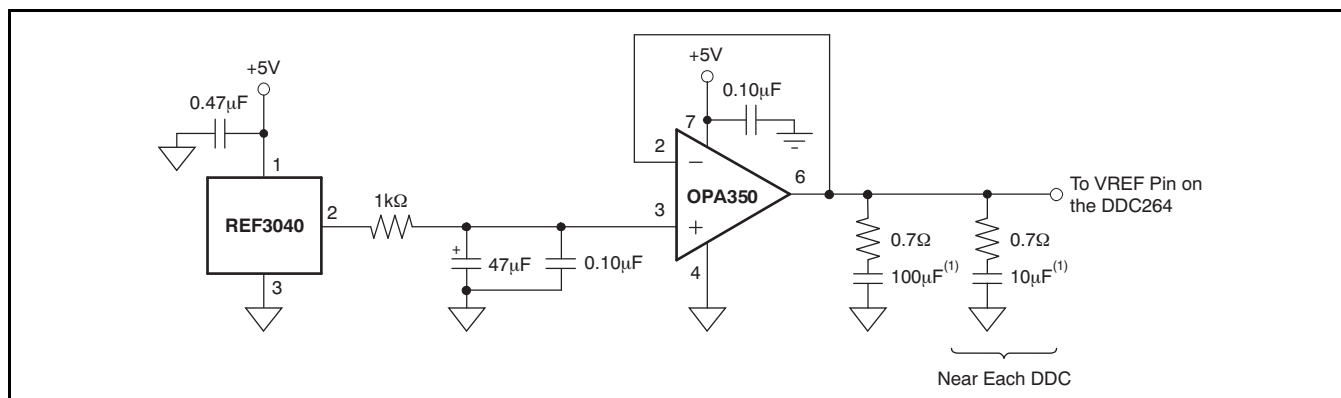
## Voltage Reference

The external voltage reference is used to reset the integration capacitors before an integration cycle begins. It is also used by the A/D converter while the converter is measuring the voltage stored on the integrators after an integration cycle ends. During this sampling, the external reference must supply the charge needed by the A/D converter. For an integration time of 333μs, this charge translates to an average VREF current of approximately 825μA. The

amount of charge needed by the A/D converter is independent of the integration time; therefore, increasing the integration time lowers the average current. For example, an integration time of 800μs lowers the average VREF current to 340μA.

It is critical that VREF be stable during the different modes of operation (see Figure 22). The A/D converter measures the voltage on the integrator with respect to VREF. Because the integrator capacitors are initially reset to VREF, any drop in VREF from the time the capacitors are reset to the time when the converter measures the integrator output introduces an offset. It is also important that VREF be stable over longer periods of time because changes in VREF correspond directly to changes in the full-scale range. Finally, VREF should introduce as little additional noise as possible.

For these reasons, it is strongly recommended that the external reference source be buffered with an operational amplifier, as shown in Figure 23. In this circuit, the voltage reference is generated by a +4.096V reference. A low-pass filter to reduce noise connects the reference to an operational amplifier configured as a buffer. This amplifier should have low noise and input/output common-mode ranges that support VREF. Even though the circuit in Figure 23 might appear to be unstable because of the large output capacitors, it works well for the OPA350. It is **not** recommended that series resistance be placed in the output lead to improve stability because this can cause a drop in VREF, which produces large offsets.

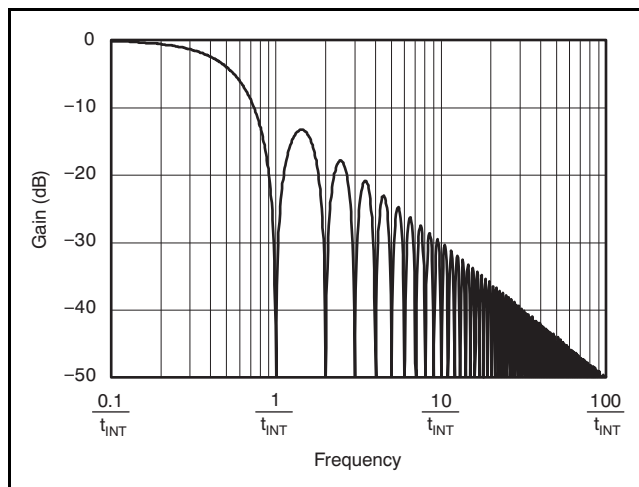


(1) Ceramic X5R capacitors are recommended.

Figure 23. Recommended External Voltage Reference Circuit for Best Low-Noise Operation

## Frequency Response

The frequency response of the DDC264 is set by the front-end integrators and is that of a traditional continuous time integrator, as shown in [Figure 24](#). By adjusting the integration time,  $t_{INT}$ , the user can change the 3dB bandwidth and the location of the notches in the response. The frequency response of the A/D converter that follows the front-end integrator is of no consequence because the converter samples a held signal from the integrators. That is, the input to the A/D converter is always a dc signal. The output of the front-end integrators are sampled; therefore, aliasing can occur. Whenever the frequency of the input signal exceeds one-half of the sampling rate, the signal folds back down to lower frequencies.



**Figure 24. Frequency Response**

## DIGITAL INTERFACE

The digital interface of the DDC264 sends the digital results via a synchronous serial interface that consists of a data clock (DCLK), a valid data pin ( $\overline{DVALID}$ ), a serial data output pin (DOUT), and a serial data input pin (DIN). The integration and conversion process is fundamentally independent of the data retrieval process. Consequently, the CLK and DCLK frequencies need not be the same, though for best performance, it is highly recommended that they be derived from the same clocking source to keep the phase relationship constant. DIN is only used when multiple converters are cascaded and should be tied to DGND otherwise. Depending on  $t_{INT}$ , CLK, and DCLK, it is possible to daisy-chain multiple converters. This option greatly simplifies the interconnection and routing of the digital outputs in those applications where a large number of converters are needed. Configuration of the DDC264 is set by a dedicated register addressed using the DIN\_CFG and CLK\_CFG pins.

## System and Data Clocks (CLK and DCLK)

The system clock is supplied to CLK and the data clock is supplied to DCLK. It is recommended that the CLK pin be driven by a free-running clock source (that is, do not start and stop CLK between conversions). Make sure the clock signals are clean—avoid overshoot or ringing. For best performance, generate both clocks from the same clock source. Disable DCLK by taking it low after the data have been shifted out and while CONV is transitioning.

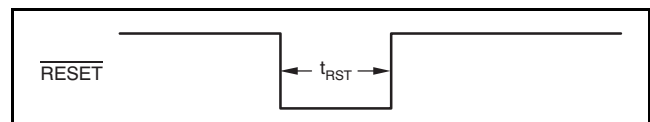
When using multiple DDC264s, pay close attention to the DCLK distribution on the printed circuit board (PCB). In particular, make sure to minimize skew in the DCLK signal because this can lead to timing violations in the serial interface specifications. See the [Cascading Multiple Converters](#) section for more details.

## Data Valid ( $\overline{DVALID}$ )

The  $\overline{DVALID}$  signal indicates that data are ready. Data retrieval may begin after  $\overline{DVALID}$  goes low. This signal is generated using an internal clock divided down from the system clock, CLK. The phase relationship between this internal clock and CLK is set when power is first applied and is random. Because the user must synchronize CONV with CLK, the  $\overline{DVALID}$  signal has a random phase relationship with CONV. This uncertainty is  $\pm 1/f_{CLK}$ . Polling  $\overline{DVALID}$  eliminates any concern about this relationship. If the data readback is timed from CONV, make sure to wait for the required amount of time.

## Reset ( $\overline{RESET}$ )

The DDC264 is reset asynchronously by taking the  $\overline{RESET}$  input low, as shown in [Figure 25](#). Make sure the release pulse is a minimum of  $t_{RST}$  wide. It is very important that  $\overline{RESET}$  is glitch-free to avoid unintentional resets. The Configuration Register must be programmed immediately afterwards. After programming the DDC264, wait at least four conversions before using the data.



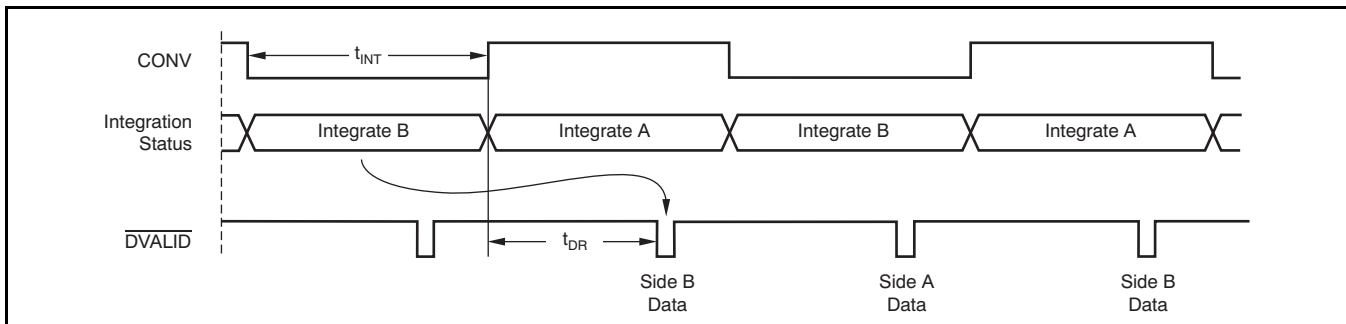
**Figure 25. Reset Timing**

**TIMING EXAMPLES**

Figure 26 shows a few integration cycles beginning after the device has been powered up, reset, and the Configuration Register has been programmed. The top signal is CONV and is supplied by the user. The integration status trace indicates which side is integrating. As described in the data sheet,  $\overline{DVALID}$  goes active low when data are ready to be retrieved from the DDC264. It stays low until DCLK is taken high and then back low by the user. The text below the  $\overline{DVALID}$  pulse indicates the side of the data available to be read. The arrow is used to match the data to the corresponding integration. Table 3 shows the timing specifications for Figure 26.

**Integration Time**

The minimum  $t_{INT}$  depends on which device is being used. The minimum time scales directly with the internal clock frequency. For the DDC264C, with an internal clock frequency of 5MHz, the minimum time is 320 $\mu$ s. For the DDC264CK, with an internal clock frequency of 10MHz, the minimum time is 166 $\mu$ s. If the minimum integration time is violated, the DDC264 stops continuously integrating the input signal. To return to normal operation (that is, continuous integration) after a violation of the minimum  $t_{INT}$  specification, perform three integrations that each last for a minimum of 5000 internal clock periods. In other words, integrate three times with each integration lasting for at least 1ms when using an internal clock frequency of 5MHz. During this time, ignore the  $\overline{DVALID}$  pin. Once the three integrations complete, normal continuous operation resumes, and data can be retrieved.



**Figure 26. Integration Sequence Timing**

**Table 3. Timing Specifications for Figure 26**

SYMBOL	DESCRIPTION	DDC264C Internal Clock Frequency = 5MHz			DDC264CK Internal Clock Frequency = 10MHz			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{INT}$	Integration time	320		1,000,000	160			$\mu$ s
$t_{DR}$	Time until data ready		276.4 $\pm$ 0.4			138.2 $\pm$ 0.2		$\mu$ s

### DATA FORMAT

The serial output data are provided in an offset binary code as shown in Table 4. The Format bit in the Configuration Register selects how many bits are used in the output word. When Format = 1, 20 bits are used. When Format = 0, the lower four bits are truncated so that only 16 bits are used. Note that the LSB size is 16 times bigger when Format = 0. An offset is included in the output to allow slightly negative inputs (for example, from board leakages) from clipping the reading. This offset is approximately 0.4% of the positive full-scale.

### DATA RETRIEVAL

The data from the last conversion are available for retrieval on the falling edge of  $\overline{\text{DVALID}}$  (see Figure 27 and Table 5). Data are shifted out on the falling edge of the data clock, DCLK.

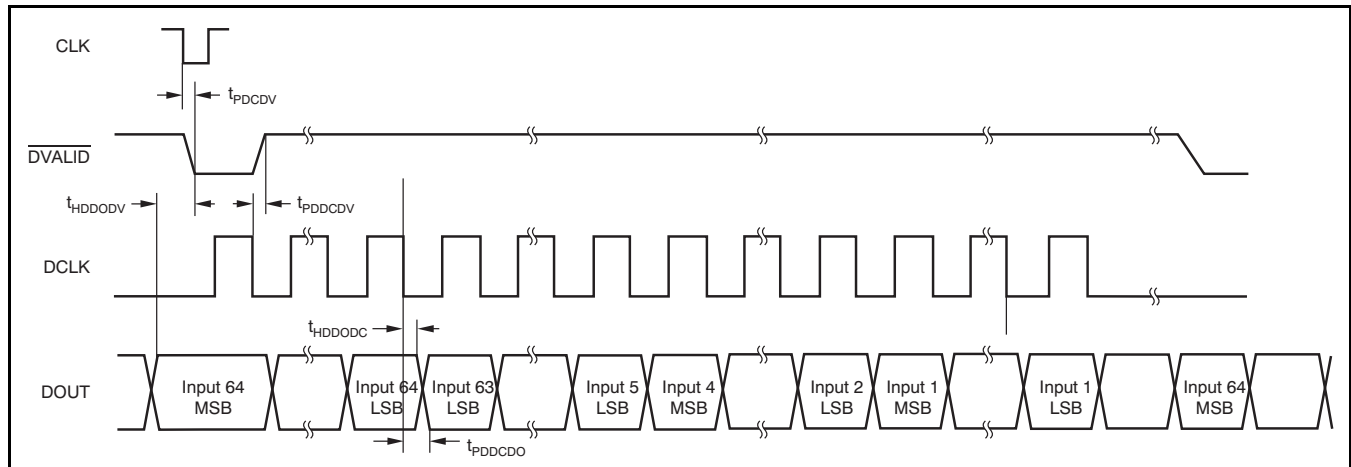
Make sure not to retrieve data around changes in CONV because this change can introduce noise. Stop activity on DCLK at least 2 $\mu\text{s}$  before or after a CONV transition.

Setting the Format bit = 0 (16-bit output word) reduces the time needed to retrieve data by 20% because there are fewer bits to shift out. This technique can be useful in multichannel systems requiring only 16 bits of resolution.

**Table 4. Ideal Output Code<sup>(1)</sup> vs Input Signal**

INPUT SIGNAL	IDEAL OUTPUT CODE FORMAT = 1	IDEAL OUTPUT CODE FORMAT = 0
$\geq 100\%$ FS	1111 1111 1111 1111 1111	1111 1111 1111 1111
0.001531% FS	0000 0001 0000 0001 0000	0000 0001 0000 0001
0.001436% FS	0000 0001 0000 0000 1111	0000 0001 0000 0000
0.000191% FS	0000 0001 0000 0000 0010	0000 0001 0000 0000
0.000096% FS	0000 0001 0000 0000 0001	0000 0001 0000 0000
0% FS	0000 0001 0000 0000 0000	0000 0001 0000 0000
-0.3955% FS	0000 0000 0000 0000 0000	0000 0000 0000 0000

(1) Excludes the effects of noise, INL, offset, and gain errors.



**Figure 27. Digital Interface Timing Diagram for Data Retrieval From a Single DDC264**

**Table 5. Timing for DDC264 Data Retrieval**

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{\text{PDCDV}}$	Propagation delay from falling edge of CLK to $\overline{\text{DVALID}}$ Low	10			ns
$t_{\text{PDDCDV}}$	Propagation delay from falling edge of DCLK to $\overline{\text{DVALID}}$ High	5			ns
$t_{\text{HDDODV}}$	Hold time that DOUT is valid before the falling edge of $\overline{\text{DVALID}}$		400		ns
$t_{\text{HDDODC}}$	Hold time that DOUT is valid after falling edge of DCLK	4			ns
$t_{\text{PDDCDO}}^{(1)}$	Propagation delay from falling edge of DCLK to valid DOUT			25	ns

(1) With a maximum load of one DDC264 (4pF typical) with an additional load of 5pF.

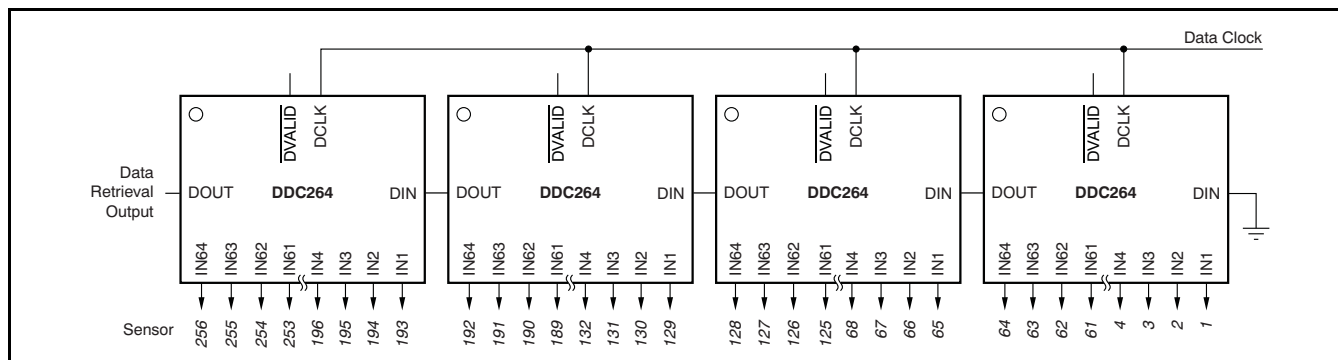


**Cascading Multiple Converters**

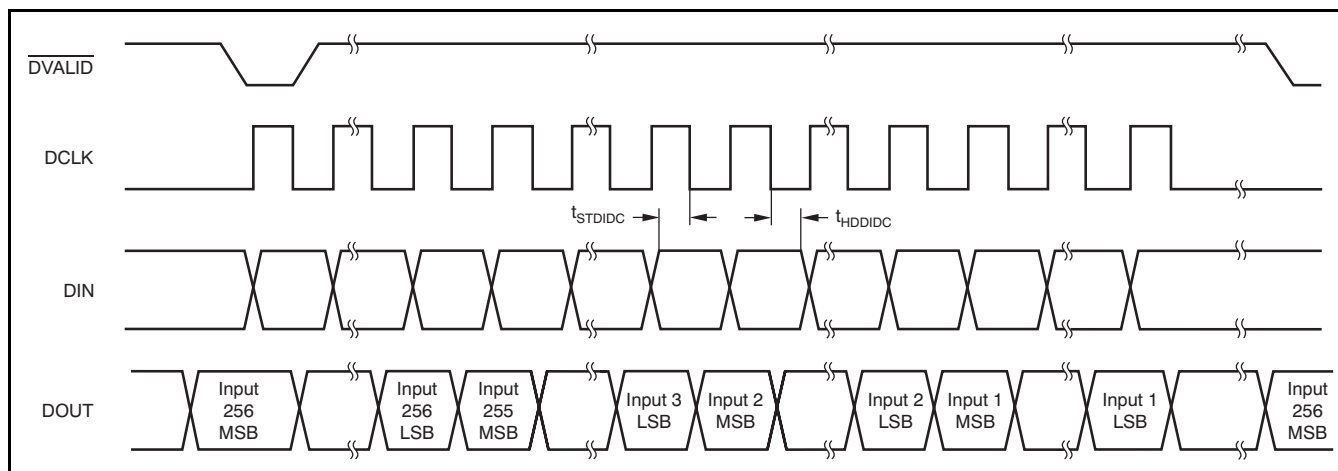
Multiple DDC264 devices can be connected in a serial configuration; see [Figure 28](#).

DOUT can be used with DIN to daisy-chain multiple DDC264 devices together to minimize wiring. In this mode of operation, the serial data output is shifted through multiple DDC264s; see [Figure 28](#).

[Figure 29](#) shows the timing diagram when the DIN input is used to daisy-chain several devices. [Table 6](#) gives the timing specification for data retrieval using DIN.



**Figure 28. Daisy-Chained DDC264s**



**Figure 29. Timing Diagram When Using DDC264 DIN Function; See [Figure 28](#)**

**Table 6. Timing for DDC264 Data Retrieval Using DIN**

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{STDIDC}$	Set-up time from DIN to falling edge of DCLK	10			ns
$t_{HDDIDC}$	Hold time for DIN after falling edge of DCLK	10			ns

## Retrieval Before CONV Toggles

Data retrieval should occur before CONV toggles. Data retrieval begins soon after DVALID goes low and finishes before CONV toggles, as shown in Figure 30. For best performance, data retrieval must stop  $t_{SDCV}$  before CONV toggles. This method is most appropriate for longer integration times. The maximum time available for readback is  $(t_{INT} - t_{CMDR} - t_{SDCV})$ . The maximum number of DDC264s that can be daisy-chained together (Format = 1) is calculated by Equation 1:

$$\frac{t_{INT} - (t_{DR} + t_{SDCV})}{(20 \times 64)\tau_{DCLK}} \quad (1)$$

**NOTE:**  $(16 \times 64)\tau_{DCLK}$  is used for Format = 0, where  $\tau_{DCLK}$  is the period of the data clock. For example, if  $t_{INT} = 1000\mu\text{s}$  and  $DCLK = 20\text{MHz}$ , the maximum number of DDC264s with Format = 1 is shown in Equation 2:

$$\frac{1000\mu\text{s} - 278.4\mu\text{s}}{(1280)(50\text{ns})} = 11.5 \rightarrow 11 \text{ DDC264s} \quad (2)$$

(or 14 DDC264s for Format = 0)

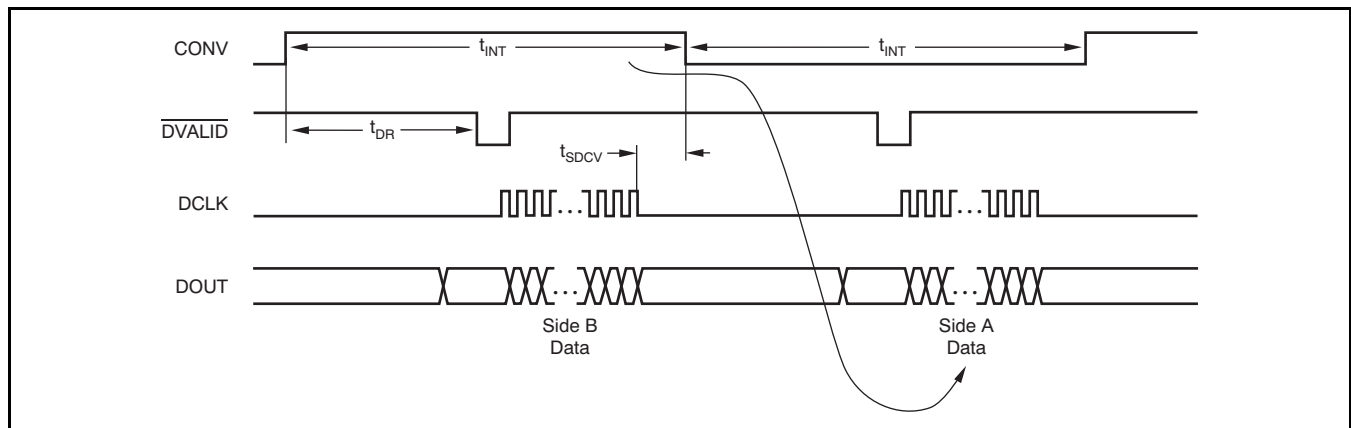


Figure 30. Readback Before CONV Toggles

Table 7. Timing for Readback

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{SDCV}$	Data retrieval shutdown before or after edge of CONV	2			$\mu\text{s}$

### Retrieval After CONV Toggles

For shorter integration times, more time is available if data retrieval begins after CONV toggles and ends before the new data are ready. Data retrieval must wait  $t_{SDCV}$  after CONV toggles before beginning. See Figure 31 for an example of this timing sequence. The maximum time available for retrieval is  $t_{DR} - (t_{SDCV} + t_{HDDODV})$ , regardless of  $t_{INT}$ . The maximum number of DDC264s that can be daisy-chained together with Format = 1 is calculated by Equation 3:

$$\frac{274\mu\text{s}}{(20 \times 64)\tau_{DCLK}} \quad (3)$$

**NOTE:**  $(16 \times 64)\tau_{DCLK}$  is for Format = 0.

For DCLK = 20MHz, the maximum number of DDC264s is four (or five for Format = 0).

### Retrieval Before and After CONV Toggles

For the absolute maximum time for data retrieval, data can be retrieved before and after CONV toggles. Nearly all of  $t_{INT}$  is available for data retrieval. Figure 32 illustrates how this process is done by combining the two previous methods. Pause the retrieval during CONV toggling to prevent digital noise, as discussed previously, and finish before the next data are ready. The maximum number of DDC264s that can be daisy-chained together with Format = 1 is:

$$\frac{t_{INT} - (t_{SDCV} + t_{SDCV} + t_{HDDODV})}{(20 \times 64)\tau_{DCLK}} \quad (4)$$

**NOTE:**  $(16 \times 64)\tau_{DCLK}$  is used for Format = 0.

For  $t_{INT} = 400\mu\text{s}$  and DCLK = 20MHz, the maximum number of DDC264s is six (or seven for Format = 0).

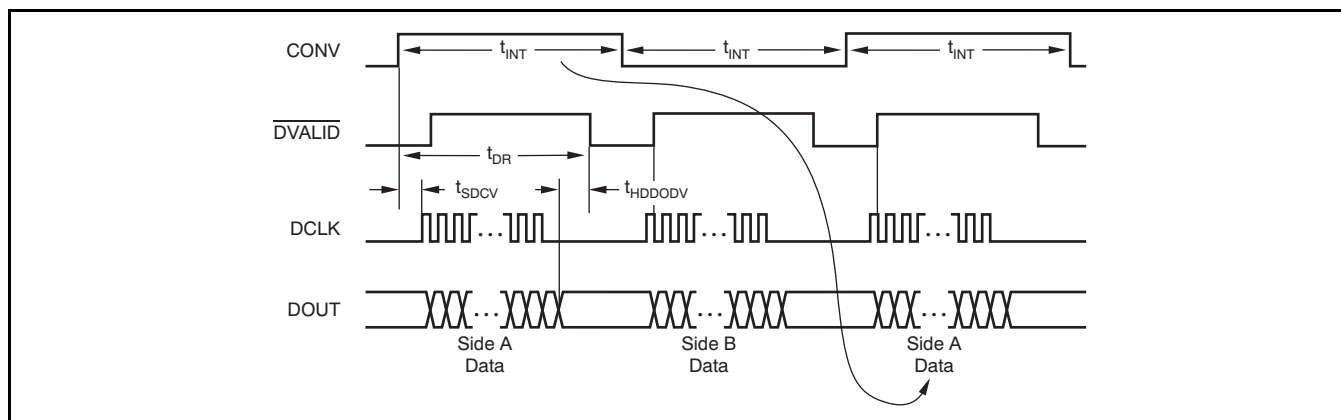


Figure 31. Readback After CONV Toggles

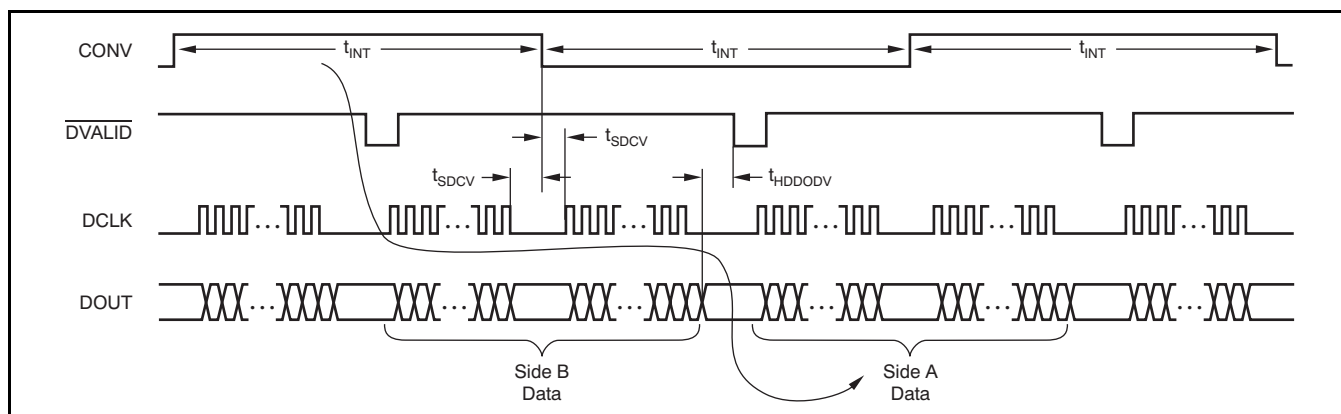


Figure 32. Readback Before and After CONV Toggles

## CONFIGURATION REGISTER Read and Write Operations

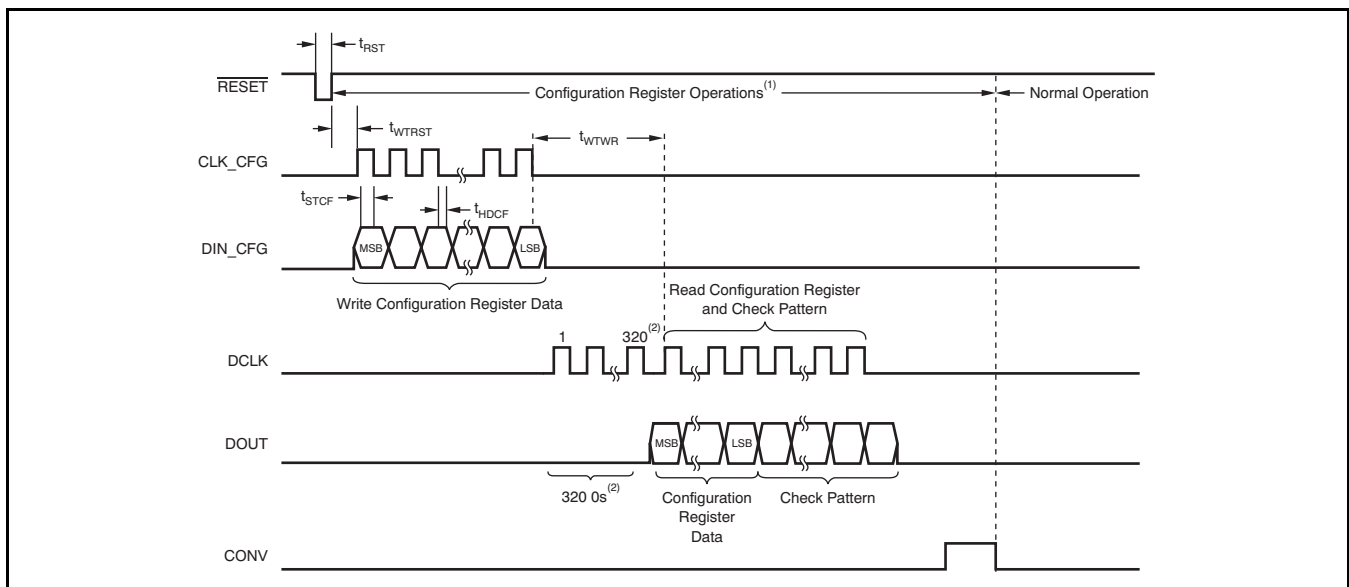
The Configuration Register must be programmed after power-up or a device reset. The DIN\_CFG, CLK\_CFG, and RESET pins are used to write to this register. When beginning a write operation, hold CONV low and strobe RESET; see Figure 33. Then begin shifting in the configuration data on DIN\_CFG. Data are written to the Configuration Register most significant bit first. The data are internally latched on the falling edge of CLK\_CFG. Partial writes to the Configuration Register are not allowed—make sure to send all 16 bits when updating the register.

Optional readback of the Configuration Register is available immediately after the write sequence. During readback, 320 '0's, then the 16-bit configuration data followed by a 4-bit revision ID and the check pattern are shifted out on the DOUT pin on the rising edge of DCLK. The check pattern can be used to check or verify the DOUT functionality.

**NOTE:** With Format = 1, the check pattern is 300 bits, with only the last 72 bits non-zero. This sequence of outputs is repeated twice for each DDC264 and daisy-chaining is supported in configuration readback. Table 8 shows the check pattern configuration during readback. Table 9 shows the timing for the Configuration Register read and write operations. Strobe CONV to begin normal operation.

**Table 8. Check Pattern During Readback**

Format Bit	Check Pattern (Hex)	Total Readback Bits
0	180 0s, 30F066012480F6h	1024
1	228 0s, 30F066012480F69055h	1280



- (1) CLK must be running during Configuration Register write and read operations.  
 (2) In 16-bit mode (FORMAT = 0), only 256 0s are read before the Configuration Register write and read operations.

**Figure 33. Configuration Register Write and Read Operations**

**Table 9. Timing for the Configuration Register Read/Write**

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{WTRST}$	Wait Required from Reset High to First Rising Edge of CLK_CFG	2			$\mu$ s
$t_{WTWR}$	Wait Required from Last CLK_CFG of Write Operation to First DCLK of Read Operation	2			$\mu$ s
$t_{STCF}$	Set-Up Time from DIN_CFG to Falling Edge of CLK_CFG	10			ns
$t_{HDCF}$	Hold Time for DIN_CFG After Falling Edge of CLK_CFG	10			ns
$t_{RST}$	Pulse Width for RESET Active	1			$\mu$ s

**Configuration Register Bit Assignments**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0	0	Clkdiv	0	0	Range[1]	Range[0]	Format
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Version	0	0	Reserved	0	0	0	Test

**Bits 15:14** These bits must always be set to '0'.

**Bit 13** **Clkdiv**

The Clkdiv input enables an internal divider on the system clock as shown in [Table 10](#). When Clkdiv = 1, the system clock is divided by 4. This configuration allows a system clock that is faster by a factor of four, which in turn provides a finer quantization of the integration time, because the CONV signal must be synchronized with the system clock for the best performance.

0 = Internal clock divider set to 1

1 = Internal clock divider set to 4

**Table 10. Clkdiv Operation**

Clkdiv Bit	CLK Divider Value	CLK Frequency	Internal Clock Frequency
0	1	5MHz	5MHz
1	4	20MHz	5MHz

**Bits 12:11** These bits must always be set to '0'.

**Bits 10:9** **Range[1:0]**

These bits set the full-scale range.

00 = Range 0 = 12.5pC

01 = Range 1 = 50.0pC

10 = Range 2 = 100.0pC

11 = Range 3 = 150.0pC

**Bit 8** **Format**

Format selects how many bits are used in the data output word.

0 = 16-bit output

1 = 20-bit output

**Bit 7** **Version**

This bit must be set to match the device being used.

Must be set to '0' for DDC264C.

Must be set to '1' for DDC264CK.

**Bits 6:5** These bits must always be set to '0'.

**Bit 4** **Reserved**

This bit is reserved and must be set to '0'.

**Bits 3:1** These bits must always be set to '0'.

**Bit 0** **Test**

When Test Mode is used, the inputs (IN1 through IN64) are disconnected from the DDC264 integrators to enable the user to measure a *zero* input signal regardless of the current supplied to the inputs.

0 = TEST mode off

1 = TEST mode on

## LAYOUT

### Power Supplies and Grounding

Both AVDD and DVDD should be as quiet as possible. It is particularly important to eliminate noise from AVDD that is non-synchronous with the DDC264 operation. Figure 34 illustrates how to supply power to the DDC264. Each DDC264 has internal bypass capacitors on AVDD and DVDD; therefore, the only external bypass capacitors typically needed are 10 $\mu$ F ceramic capacitors, one per PCB. It is recommended that both the analog and digital grounds (AGND and DGND) be connected to a single ground plane on the PCB.

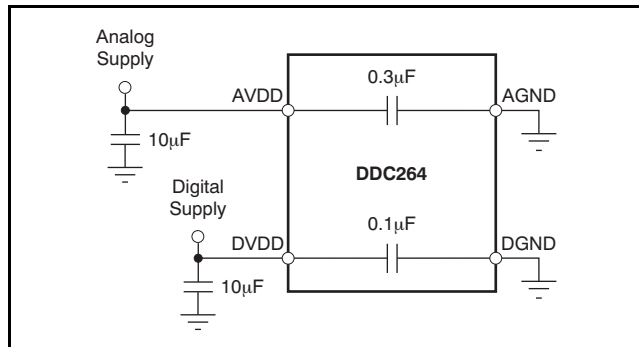


Figure 34. Power-Supply Connections

### Shielding Analog Signal Paths

As with any precision circuit, careful PCB layout ensures the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins and QGND. The analog input pins are high-impedance and extremely sensitive to extraneous noise. The QGND pin should be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the input bias current of the DDC264 if shielding is not implemented. Digital signals should be kept as far as possible from the analog input signals on the PCB.

## POWER-UP SEQUENCING

Before device power-up, all digital and analog inputs must be low. At the time of power-up, all of these signals should remain low until the power supplies have stabilized, as shown in Figure 35. The analog supply must come up before or at the same time as the digital supply. At this time, begin supplying the master clock signal to the CLK pin. Wait for time  $t_{POR}$ , then give a RESET pulse. After releasing RESET, the Configuration Register must be written to. Table 11 shows the timing for the power-up sequence.

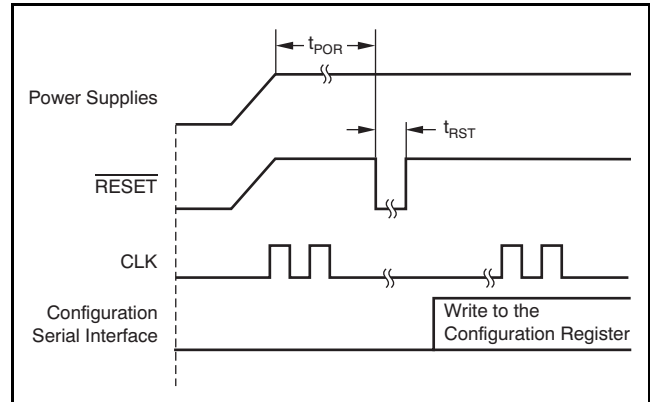


Figure 35. DDC264 Timing Diagram at Power-Up

Table 11. Timing for DDC264 Power-Up Sequence

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{POR}$	Wait after power-up until reset	250			ms

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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### Changes from Revision B (January, 2011) to Revision C Page

- Updated [Table 1](#); revised values for Range 0 performance in fC and Electrons ..... 9
- 

### Changes from Revision A (January, 2011) to Revision B Page

- Changed second paragraph of [Basic Integration Cycle](#) section to correct CONV timing description error ..... 11
-

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DDC264CKZAW	ACTIVE	NFBGA	ZAW	100	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 70	DDC264K	<a href="#">Samples</a>
DDC264CKZAWR	ACTIVE	NFBGA	ZAW	100	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 70	DDC264K	<a href="#">Samples</a>
DDC264CZAW	ACTIVE	NFBGA	ZAW	100	168	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 70	DDC264	<a href="#">Samples</a>
DDC264CZAWR	ACTIVE	NFBGA	ZAW	100	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 70	DDC264	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

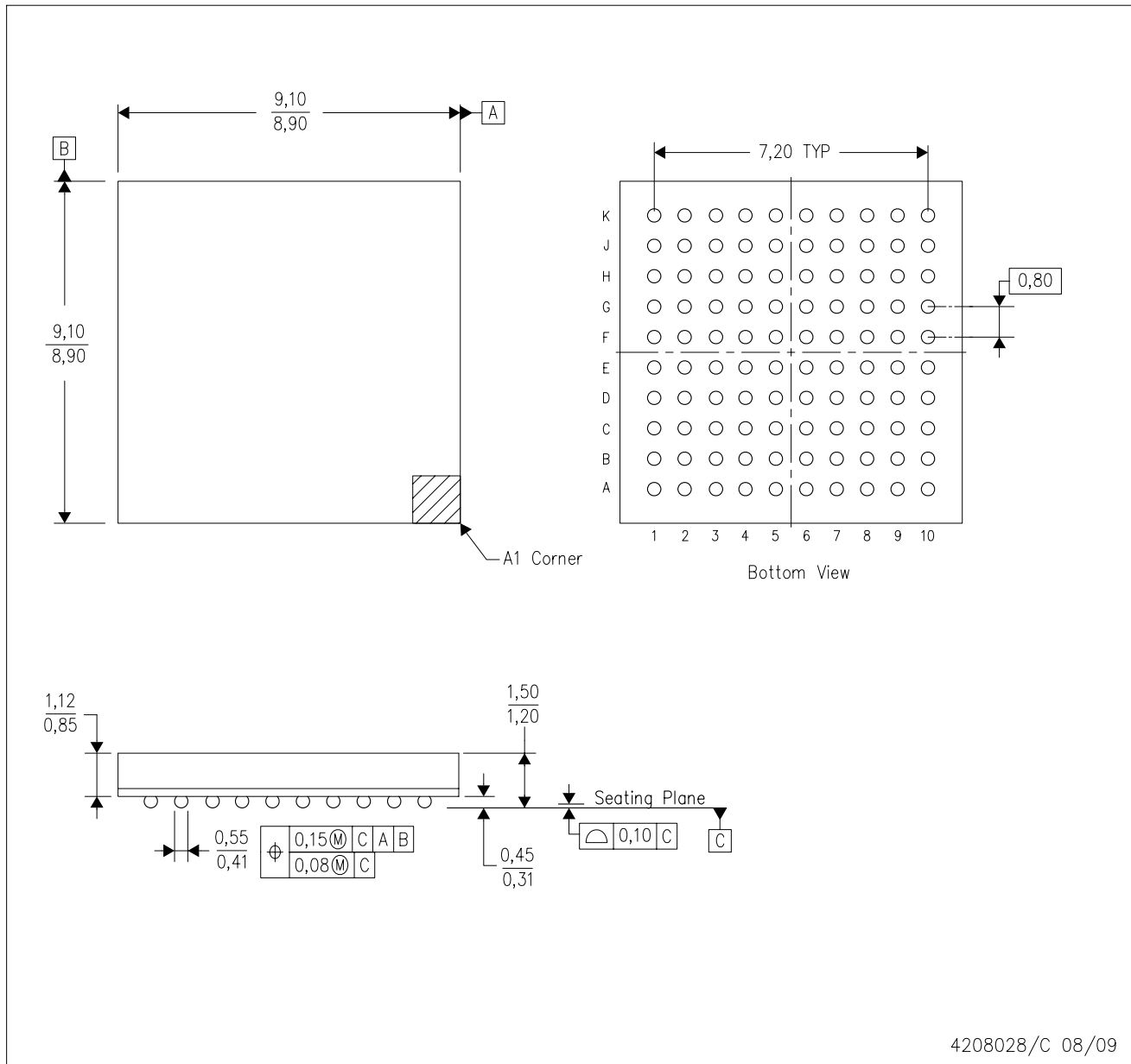


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ZAW (S-PBGA-N100)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. This is a Pb-free solder ball design.

## IMPORTANT NOTICE

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