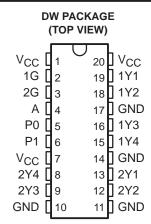
- Low Output Skew, Low Pulse Skew for **Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Eight Outputs**
- Distributed V_{CC} and Ground Pins Reduce **Switching Noise**
- High-Drive Outputs (-48-mA IOH, 48-mA I_{OI})
- State-of-the-Art *EPIC-IIB™* BiCMOS Design **Significantly Reduces Power Dissipation**
- **Packaging Options Include Plastic** Small-Outline (DW) Packages



description

The CDC341 is a high-performance clock-driver circuit that distributes one (A) input signal to eight (Y) outputs with minimum skew for clock distribution. Through the use of the control pins (1G and 2G), the outputs can be placed in a low state regardless of the A input.

The propagation delays are adjusted at the factory using the P0 and P1 pins. These pins are not intended for customer use and should be strapped to GND.

The CDC341 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

	INPUTS		OUTPUTS				
1G	2G	Α	1Y1-1Y4	2Y1-2Y4			
Х	Х	L	L	L			
L	L	Н	L	L			
L	Н	Н	L	Н			
н	L	Н	Н	L			
Н	Н	Н	Н	Н			

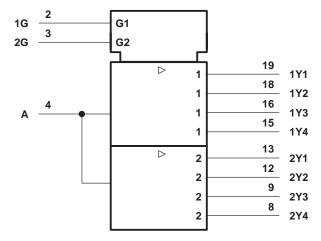


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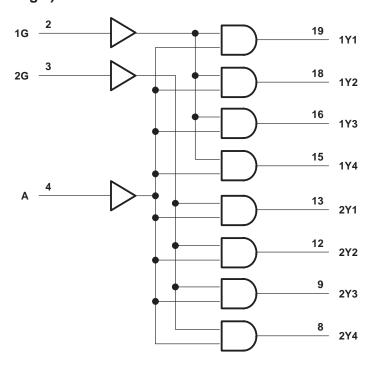


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state,	
V _O (see Note 1)	-0.5 V to $V_{CC} + 0.5 \text{ V}$
Current into any output in the low state, IO	96 mA
Input clamp current, I _{IK} (V _I < 0)	–18 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2)	1.6 W
Storage temperature range, T _{stq}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage	4.75	5.25	V	
VIH	High-level input voltage	2		V	
VIL	Low-level input voltage		0.8	V	
VI	Input voltage	0	VCC	V	
lOH	High-level output current		-48	mA	
loL	Low-level output current			48	mA
f	Input clock frequency	One output bank loaded		80	MHz
fclock	input clock frequency		40	IVITIZ	
TA	Operating free-air temperature				°C

NOTE 3: Unused pins (input or I/O) must be held high or low.

^{2.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	т	Т	A = 25°C	;	MIN	MAX	UNIT		
PARAWETER	"	MIN	TYP [†]	MAX	IVIIIV	IVIAA	UNIT		
VIK	$V_{CC} = 4.75 \text{ V},$	I _I = -18 mA				-1.2		-1.2	V
	$V_{CC} = 4.75 \text{ V},$	$I_{OH} = -3 \text{ mA}$		2.5			2.5		
Voн	$V_{CC} = 5 V$,	$I_{OH} = -3 \text{ mA}$		3			3		V
	$V_{CC} = 4.75 \text{ V},$	$I_{OH} = -48 \text{ mA}$		2			2		
V _{OL}	$V_{CC} = 4.75 \text{ V},$	$I_{OL} = 48 \text{ mA}$						0.5	V
lį	$V_{CC} = 5.25 \text{ V},$	$V_I = V_{CC}$ or GND				±1		±1	μΑ
lo [‡]	$V_{CC} = 5.25 \text{ V},$	V _O = 2.5 V		-50	-100	-200	-50	-200	mA
laa	$V_{CC} = 5.25 \text{ V},$	$I_{O} = 0$,	Outputs high		2			3.5	mA
lcc	V _I = V _{CC} or GND		Outputs low		24	·		33	IIIA
Ci	$V_{ } = 2.5 \text{ V or } 0.5 \text{ V}$				3				pF

[†] All typical values are at $V_{CC} = 5 \text{ V}$.

switching characteristics, C_L = 50 pF (see Figures 1 and 2)

PARAMETER	FROM	TO (OUTPUT)	V ₍	CC = 5 V 4 = 25°C	', ;	V _{CC} = 4.75 T _A = 0°	5 V to 5.25 V, C to 70°C	UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	
^t PLH	А	V	3.5		4.5	3.1	4.9	ns
^t PHL	Α	'			4.3	3.1	4.9	115
^t PLH	G	V	2		3.8	2	4	ns
^t PHL	9	·	2		3.8	2	4	115
tsk(o)				0.3	0.5		0.6	
^t sk(p)	Α	Υ		0.6	0.8		0.9	ns
^t sk(pr)					1		1	
t _r	А	Υ					1.5	ns
t _f	А	Y					1.5	ns

t_{pd} performance information relative to V_{CC} and temperature variation (see Note 4)

Dt _{PLH(TA)} †	Temperature drift of tpLH from 0°C to 70°C	-41 ps/10°C
Dt _{PHL(TA)} †	Temperature drift of tpHL from 0°C to 70°C	−52 ps/10°C
Dt _{PLH(VCC)} ‡	V _{CC} drift of t _{PLH} from 4.75 V to 5.25 V	28 ps/100 mV
Dt _{PHL(VCC)} ‡§	V _{CC} drift of t _{PHL} from 4.75 V to 5.25 V	20 ps/100 mV

[†] Virtually independent of V_{CC}

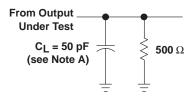
NOTE 4: The data extracted is from a wide range of characterization material.



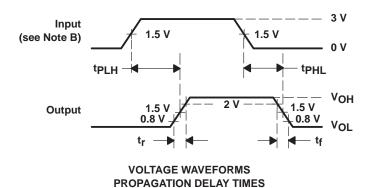
[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[‡] Virtually independent of temperature

PARAMETER MEASUREMENT INFORMATION



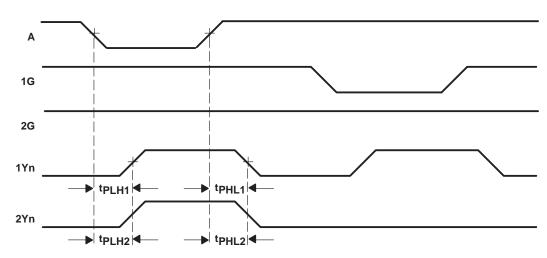
LOAD CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms



NOTES: A. Output skew, $t_{Sk(0)}$, is calculated as the greater of:

- The difference between the fastest and slowest of tp_{LHn} (n = 1, 2)
 The difference between the fastest and slowest of tp_{HLn} (n = 1, 2)
- B. Pulse skew, $t_{Sk(p)}$, is calculated as the greater of $|t_{PLHn} t_{PHLn}|$ (n = 1, 2).
- C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
 - The difference bétween the fastest and slowest of tpLHn (n = 1, 2) across multiple devices under identical operating conditions
 - The difference between the fastest and slowest of tpHLn (n = 1, 2) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

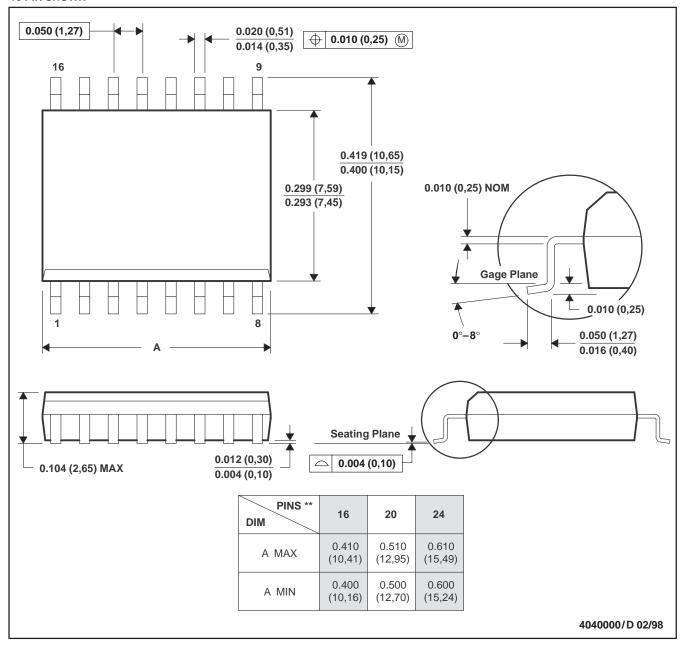


MECHANICAL INFORMATION

DW (R-PDSO-G**)

16 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013







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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDC341DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
CDC341DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC341DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC341DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC341DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC341NSR	OBSOLETE	SO	NS	20		TBD	Call TI	Call TI
CDC341NSRG4	OBSOLETE	SO	NS	20		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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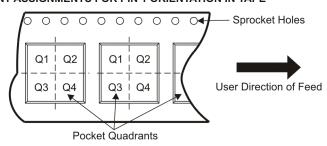
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC341DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1





*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CI	C341DWR	SOIC	DW	20	2000	346.0	346.0	41.0

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