LMH6525/LMH6526 Four–Channel Laser Diode Driver with Dual Output

Check for Samples: LMH6525, LMH6526

FEATURES

- **Fast Switching: Rise and Fall Times: 0.6/1.0 ns.**
- **Low Voltage Differential Signaling (LVDS) Channels Enable Interface for the Fast Switching Lines**
- **Low Output Current Noise: 0.24 nA/$\sqrt{Hz}$**
- **Dual Output: Selectable by SELA/B Pin (Active HIGH)**
  - **SELA = LMH6526 SEB = LMH6525**
- **Four Independent Current Channels**
  - **Gain of 300, 300 mA Write Channel**
  - **Gain of 150, 150 mA Low-Noise Read Channel**
  - **Two Gain of 150, 150 mA Write Channels**
  - **600 mA Minimum Combined Output Current**
- **Integrated AC Coupled HFM Oscillator**
  - **Selectable Frequency and Amplitude Setting**
  - **By External Resistors**
  - **200 MHz to 600 MHz Frequency Range**
  - **Amplitude to 100 mA Peak-to-Peak Modulation**
- **Complete Shutdown by ENABLE Pin**
- **5V Single-Supply Operation**
- **Logic inputs TTL and CMOS compatible**
- **Space Saving Package (OFN)**
- **LMH6525 has Differential Enable Oscillator Inputs**
- **LMH6526 has Single Ended Enable Oscillator Inputs**

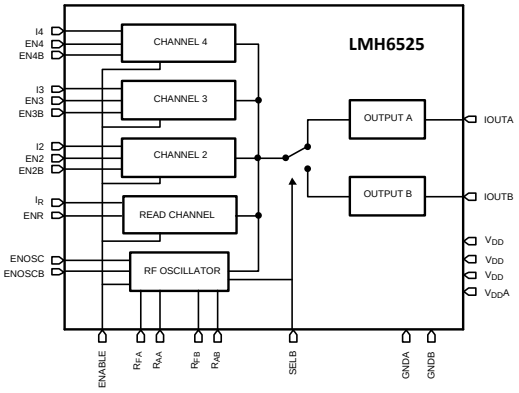
APPLICATIONS

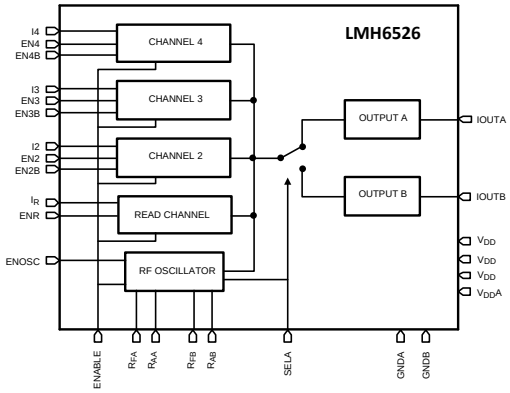
- **Combination DVD/CD Recordable and Rewritable Drives**
- **DVD Camcorders**
- **DVD Recorders**

DESCRIPTION

The LMH™6525/6526 is a laser diode driver for use in combination DVD/CD recordable and rewritable systems. The part contains two high-current outputs for reading and writing the DVD (650 nm) and CD (780 nm) lasers. Functionality includes read, write and erase through four separate switched current channels. The channel currents are summed together at the selected output to generate multilevel waveforms for reading, writing and erasing of optical discs. The LVDS interface delivers DVD write speeds of 16x and higher while minimizing noise and crosstalk. The LMH6525/6526 is optimized for both speed and power consumption to meet the demands of next generation systems. The part features a 150 mA read channel plus one 300 mA and two 150 mA write channels, which can be summed to allow a total output current of 600 mA or greater. The channel currents are set through four independent current inputs.

Block Diagrams





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

An on-board High-Frequency Modulator (HFM) oscillator helps reduce low-frequency noise of the laser and is enabled by applying LVDS levels on the ENOSC pins for the LMH6525, while the LMH6526 is enabled by applying an asymmetrical signal on the ENOSC pin. The fully differential oscillator circuit minimizes supply line noise, easing FCC approval of the overall system. The SELA/B pin (active HIGH) selects the output channel and oscillator settings. External resistors determine oscillator frequency and amplitude for each setting. The write and erase channels can be switched on and off through dedicated LVDS interface pins.

Absolute Maximum Ratings (1)(2)

ESD Tolerance	Human Body Model (3)	2 KV
	Machine Model (4)	200V
Supply Voltages $V^+ - V^-$		5.5V
Differential Input Voltage		±5.5V
Output Short Circuit to Ground (5)		Continuous
Input Common Mode Voltage		V^- to V^+
Storage Temperature Range		−65°C to +150°C
Junction Temperature (6)		+150°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications, see the Electrical Characteristics tables.
(3) For testing purposes, ESD was applied using "Human Body Model"; 1.5 kΩ in series with 100 pF.
(4) Machine Model, 0Ω in series with 200 pF.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} — T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board..

Operating Ratings

Supply Voltage ($V^+ - V^-$)	$4.5V \le V_S \le 5.5V$
Operating Temperature Range (T_A) (1)	$-40°C \le T_A \le 85°C$
Package Thermal Resistance (2), (1)	QFN Package

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Parametric performance is as indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications section for information on temperature de-rating of this device.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} — T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board..

Operating Ratings (continued)

(θ_{JC})	3°C/W
(θ_{JA}) (no heatsink)	42°C/W
(θ_{JA}) (no heatsink see (3))	30.8°C/W
$I_{INR/3/4}$	1.5 mA (Max)
I_{IN2}	1.0 mA (Max)
R_{FREQ}	1000 Ω (Min)
R_{AMP}	1000 Ω (Min)
F_{OSC}	100-600 MHz
A_{OSC}	10-100 mA_{PP}

(3) This figure is taken from a thermal modeling result. The test board is a 4 layer FR-4 board measuring 101 mm x 101 mm x 1.6 mm with a 3 x 3 array of thermal vias. The ground plane on the board is 50 mm x 50 mm. Ambient temperature in simulation is 22°C, still air. Power dissipation is 1W.

+5V DC Electrical Characteristics (1)

Unless otherwise specified, all limits specified for T_J = 25°C, R_L = 10Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
LVDS						
V_I	Input Voltage Range	$\|V_{GPD}\|$ < 50 mV (4)	0	1.7	2.4	V
V_{IDTH}	Input Diff. Threshold	$\|V_{GPD}\|$ < 50 mV (4)	–100	0	100	mV
V_{HYST}	Input Diff. Hysteresis	$V_{IDTHH} - V_{IDTHL}$	25	0		mV
R_{IN}	Input Diff. Impedance		95	115	135	Ω
I_{IN}	Input Current	Excluding R_{IN} Current , V_{CM} = 1.25V		8	20	µA
Current Channels						
R_{IN}	Input Resistance all Channels	R_{IN} to Ground	475	580	675	Ω
I_{OS2}	Current Offset Channel 2	Channel R,3,4 Off I_{IN} = 0, EN = High		2.1	16	mA
$I_{OS,R,3,4}$	Current Offset Channel R,3,4	All Channels Off I_{IN} = 0, EN = High		1.2	9	mA
A_{IW}	Current Gain	Channel 2	345	386	430	A/A
A_{IR}	Current Gain	Channel Read	135	159	180	A/A
$A_{I,3,4}$	Current Gain	Channel 3 and 4	160	182	200	A/A
$I_{LIN-R,2,3,4}$	Output Current Linearity	200 µA < I_{IN} < 1000 µA; R_{LOAD} = 5Ω Channels Read, 2,3 and 4		1.7	3	%
$IOUT_W$	Output Current	Channel 2 @ 1 mA input current	285	300		mA
$IOUT_R$	Output Current	Channel Read @ 1 mA input current	140	162		mA
$IOUT_{3,4}$	Output Current	Channel 3 and 4 @ 1 mA input current	160	183		mA
$IOUT_{TOTAL}$	Total Output Current	All Channels (5)	600			mA
V_{TLO}	TTL Low Voltage	Input (H to L), ENR ENOSC (LMH6526)		1.29	0.8	V
V_{TLO}	TTL Low Voltage	Input (H to L) B-Select (LMH6525) A-Select (LMH6526)		1.40	0.8	V
V_{ELO}	Enable Low Voltage	Enable Input (H to L)		1.98	0.8	V
V_{THI}	TTL High Voltage	Input (L to H), ENR ENOSC (LMH6526)	2	1.27		V
V_{THI}	TTL High Voltage	Input (L to H) B-Select (LMH6525) A-Select (LMH6526)	2	1.51		V
V_{EHI}	Enable High Voltage	Enable Input (L to H)	2.8	2.13		V
I_{Spd}	Supply Current, Power Down	Enable = Low		0.003	**0.1**	mA
I_{Sr1}	Supply Current, Read Mode, Oscillator Disabled	ENOSC = Low; ENOSCB = High I2 = I3 = I4 = I_R = 125 µA		81.5	**100**	mA
I_{Sr2}	Supply Current, Read Mode, Oscillator Enabled	ENOSC = High; ENOSCB = Low I2 = I3 = I4 = I_R = 125 µA R_{FA} = 3.5 kΩ		81.5	**100**	mA
I_{Swr}	Supply Current, Write Mode	EN2 = EN3 = EN4 = High; I2 = I3 = I4 = I_R = 125 µA		180	**210**	mA
I_S	Supply Current	All Channels disable, no input current. SELA/B = Low R_{AA}, R_{AB}, R_{FA}, R_{FB} = ∞		33	**40**	mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Parametric performance is as indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications section for information on temperature de-rating of this device.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) V_{GPD} = ground potential difference voltage between driver and receiver
(5) Total input current is 4 mA (all 4 channels equal) and output currents are summed together (see typical performance characteristics).

+5V AC ELECTRICAL CHARACTERISTICS

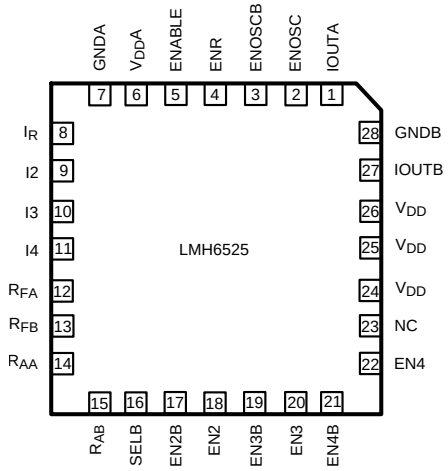
Unless otherwise specified, all limits specified for T_J = 25°C, I_{OUT} = 40 mA DC and 40 mA pulse, R_L = 50Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
t_r	Write Rise Time	I_{OUT} = 40 mA (Read) + 40 mA (10% to 90%) R_{LOAD} = 5Ω		0.6		ns
t_f	Write Fall Time	I_{OUT} = 40 mA (Read) + 40 mA (90% to 10%) R_{LOAD} = 5Ω		1.6		ns
t_r	Write Rise Time	I_{OUT} = 100 mA (Read) + 100 mA (10% to 90%) R_{LOAD} = 5Ω		0.6		ns
t_f	Write Fall Time	I_{OUT} = 100 mA (Read) + 100 mA (90% to 10%) R_{LOAD} = 5Ω		1.0		ns
t_r	Write Rise Time	I_{OUT} = 150 mA (Read) + 150 mA (10% to 90%) R_{LOAD} = 5Ω		0.6		ns
t_f	Write Fall Time	I_{OUT} = 150 mA (Read) + 150 mA (90% to 10%) R_{LOAD} = 5Ω		1.0		ns
OS	Output Current Overshoot	I_{OUT} = 40 mA (Read) + 40 mA (3)		18		%
IN_0	Output Current Noise	I_{OUT} = 40 mA; R_{LOAD} = 50Ω; f = 50 MHz; ENOSC = Low		0.24		nA/√Hz
t_{ON}	I_{OUT} ON Prod. Delay	Switched on EN2 and EN2B		3.1		ns
t_{OFF}	I_{OUT} OFF Prop. Delay	Switched on EN2 and EN2B		3.3		ns
t_{disr}	Disable Time, Read Channel	Switched on ENR		3.5		as
T_{enr}	Enable Time, Read Channel	Switched on ENR		2.8		ns
t_{dis}	Disable Time (Shutdown)	Enable = High to Low		37		ns
t_{en}	Enable Time (Shutdown)	Enable = Low to High		4.5		µs
BW_C	Channel Bandwidth, −3 dB	I_{OUT} = 50 mA, All Channels		250		KHz
F_{OSC}	Oscillator Frequency	R_F = 3.48 kΩ Range 200 MHz to 600 MHz	**290**	360	**430**	MHz
T_{DO}	Disable Time Oscillator	LMH6525		5		ns
T_{EO}	Enable Time Oscillator	LMH6525		4		ns
T_{DO}	Disable Time Oscillator	LMH6526		7		ns
T_{EO}	Enable Time Oscillator	LMH6526		4		ns

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) This is the average between the positive and negative overshoot.

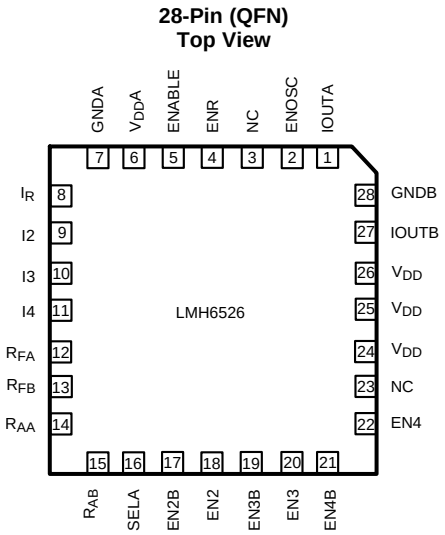
CONNECTION DIAGRAMS

28-Pin (QFN)
Top View



See Package Number NJD0028A

28-Pin (QFN)
Top View



See Package Number NJD0028A

Table 1. Pin Description

Pin #	Description	Remarks
1.	Laser driver output channel A	
2.	LVDS Oscillator Enable pin	Internal Oscillator activated if logical input is high
3.	LVDS Oscillator Enable pin B (only LMH6525)	Internal Oscillator activated if logical input is low
4.	Read Channel Enable pin	Read Channel active if pin is high
5.	Chip Enable pin	Chip Enabled if pin is high
6.	Supply Voltage A	
7.	Ground Connection A	
8.	Read Channel current setting	1 mA input current result in 150 mA output current
9.	Channel 2 current setting	1 mA input current result in 300 mA output current
10.	Channel 3 current setting	1 mA input current result in 150 mA output current
11.	Channel 4 current setting	1 mA input current result in 150 mA output current
12.	Oscillator Frequency setting Channel A	Set by external resistor to ground
13.	Oscillator Frequency setting Channel B	Set by external resistor to ground
14.	Oscillator Amplitude setting Channel A	Set by external resistor to ground
15.	Oscillator Amplitude setting Channel B	Set by external resistor to ground
16.	Channel select B (LMH6525) Channel select A (LMH6526)	Channel selected if pin is high
17.	LVDS input Channel 2B	Channel 2 active if logical input is low
18.	LVDS input Channel 2	Channel 2 active if logical input is high
19.	LVDS input Channel 3B	Channel 3 active if logical input is low
20.	LVDS input Channel 3	Channel 3 active if logical input is high
21.	LVDS input Channel 4B	Channel 4 active if logical input is low
22.	LVDS input Channel 4	Channel 4 active if logical input is high
23.	NC	
24.	Supply Voltage	
25.	Supply Voltage	

Table 1. Pin Description (continued)

Pin #	Description	Remarks
26.	Supply Voltage	
27.	Laser driver output channel B	
28.	Ground Connection B	

Truth Tables

Table 2. IOUT Control

ENABLE	ENR	EN2	EN3	EN4	IOUT
0	X	X	X	X	OFF
1	0	0	0	0	OFF
1	1	0	0	0	$A_R * I_{INR}$
1	1	1	0	0	$A_R * I_{INR} + A_2 * I_{IN2}$
1	1	0	1	0	$A_R * I_{INR} + A_3 * I_{IN3}$
1	1	0	0	1	$A_R * I_{INR} + A_4 * I_{IN4}$

Table 3. Oscillator Control

ENABLE	ENOSC	ENR	EN2	EN3	EN 4	OSCILLATOR
0	X	X	X	X	X	OFF
1	0	X	X	X	X	OFF
1	1	X	X	X	X	ON

NOTE

Note: EN2, EN3, EN4 AND ENOSC are LVDS SIGNALS USING THE LMH6525.

EN2, EN3 and EN4 are LVDS signals using the LMH6526.

Waveforms

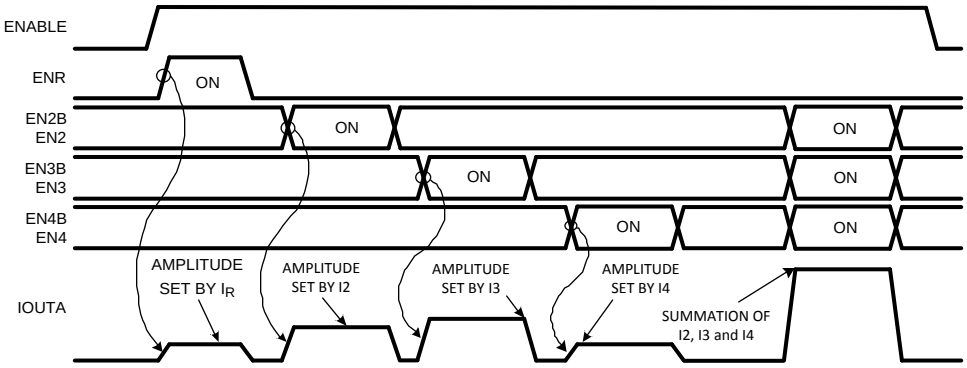


Figure 1. Functional Timing Diagram

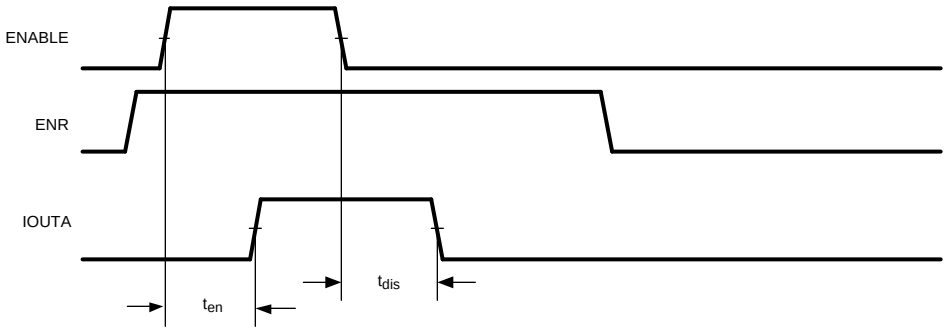


Figure 2. Enable Timing

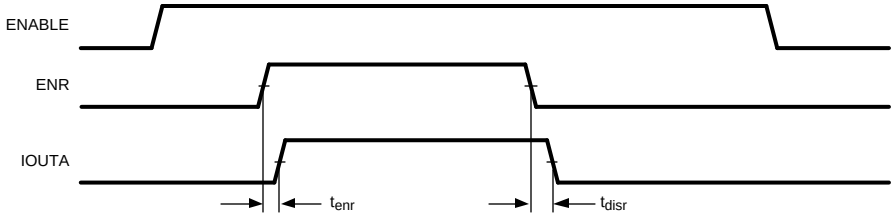


Figure 3. Read Timing

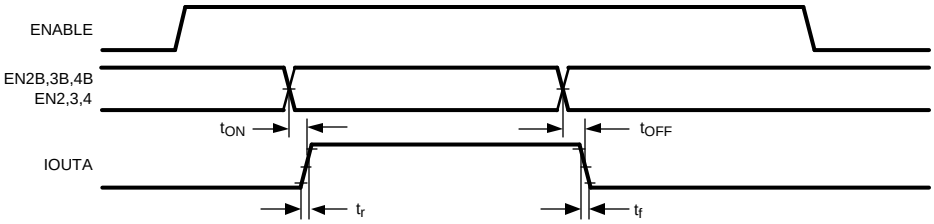


Figure 4. Write Timing

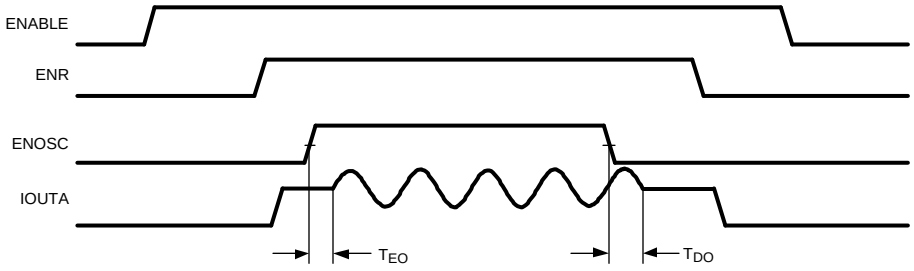
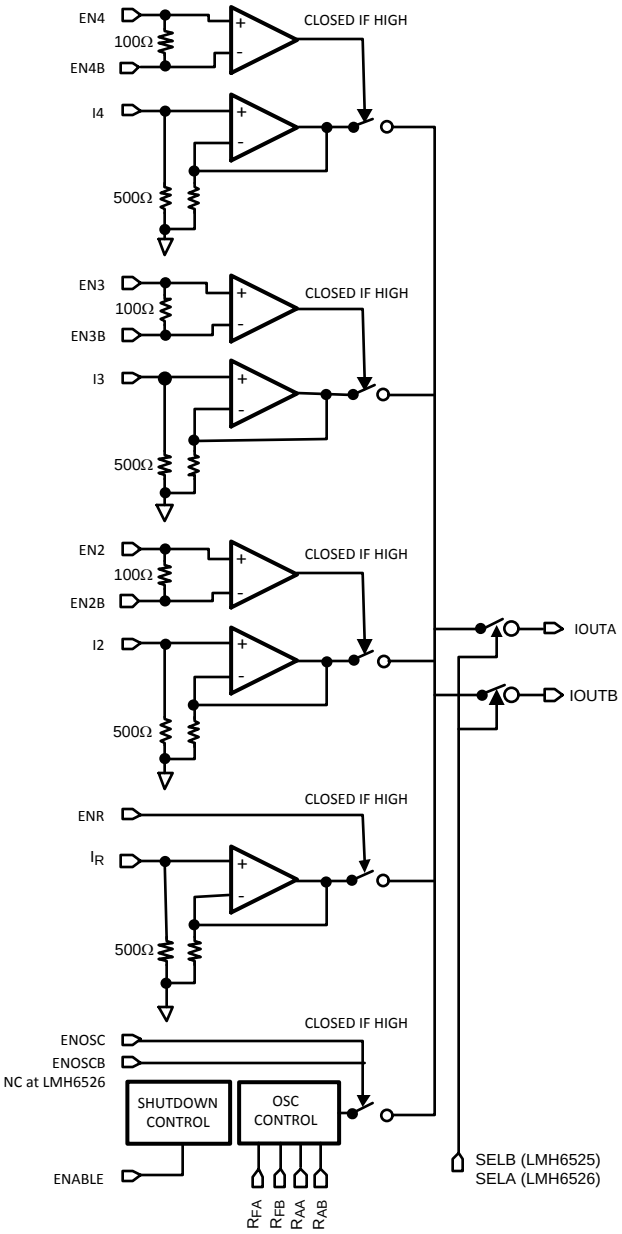
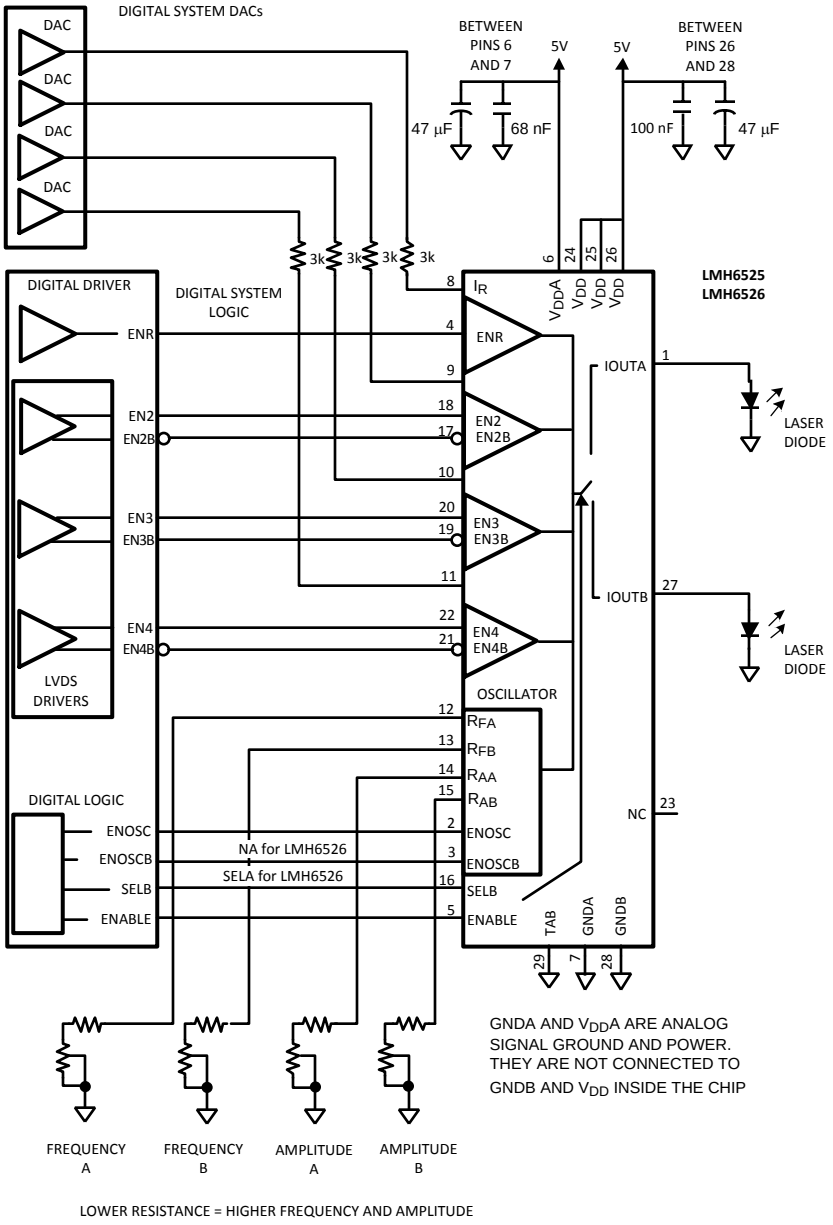


Figure 5. Oscillator Timing

Detailed Block Diagram



Application Schematic



Typical Performance Characteristics

(T_J = 25°C, V^+ = ±5V, V^- = 0V; Unless Specified).

Oscillator Amplitude vs. R_A

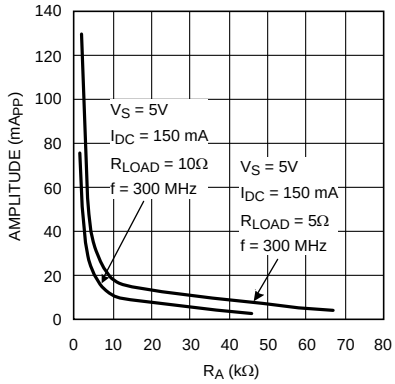


Figure 6.

Oscillator Amplitude vs. R_A

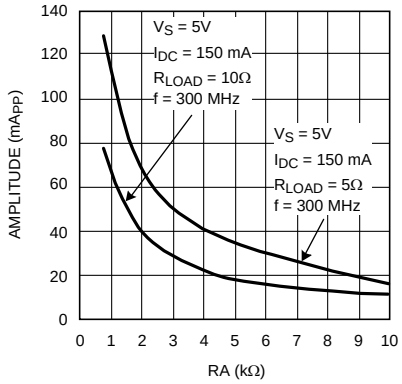


Figure 7.

Oscillator Frequency vs. R_F

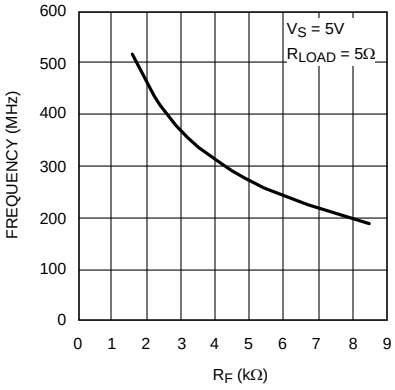


Figure 8.

Pulse Response

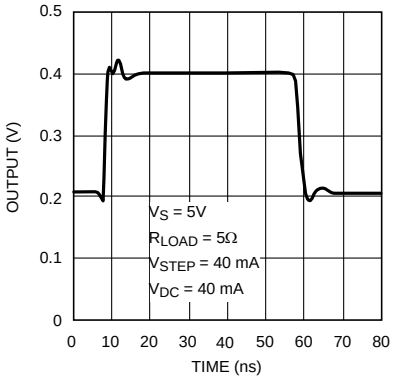


Figure 9.

Noise vs. Frequency

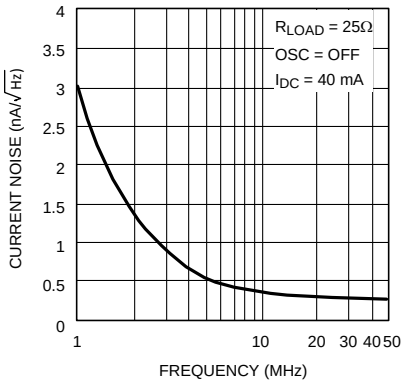


Figure 10.

Headroom & Output Current vs. Total Input Current

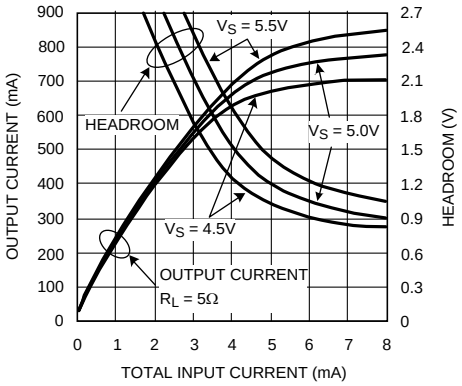


Figure 11.

APPLICATION INFORMATION

CIRCUIT DESCRIPTION

General & Spec

The LMH6525/6526 is a 4-channel-input, dual-output laser driver. The dual outputs are meant to drive two different laser diodes, one for CD reading and writing and one for DVD reading and writing. The part has an oscillator that can be set for both amplitude and frequency. The oscillator has four input pins for setting both the amplitude and frequency by connecting external resistors to ground. The part operates at 5V and is capable to deliver a minimum total output current of 500 mA.

INPUTS

Current-Setting Inputs

The 4 input channels are transconductance-type inputs. This means the output current of the channel is proportional to the current (not voltage) sourced into the input pin. That is why these pins are designated by the letter "I" to indicate the current input nature of the pin. The read channel current-setting pin is "I_R", the Channel 2 current-setting pin is "I2" and so on. Using a transconductance-type input eliminates the high-impedance inputs associated with a voltage input amplifier. The lower input impedances of the input nodes lowers the susceptibility of the part to EMI/RFI. The Read Channel (I_R) and Channel 3 (I3) and 4 (I4) current-setting inputs have a gain of 150. The Channel 2 input (I2) has a current gain of 300. Sourcing one milliampere into the pins I_R, I3 or I4, will result in 150 mA at the output for each Channel, while 1 mA into I2 will result in 300 mA at the output for Channel 2. These currents of 150 mA and 300 mA are the maximum allowable currents per channel. The total allowable output current from all the channels operating together exceeds 500 mA.

Channel Enable Inputs

Each of the four channels has one (read) or two enable inputs that allow the channel to be turned on or off. The read channel enable (ENR) is a single-ended TTL/CMOS compatible input. A single-ended signal is adequate for this channel because the read channel is generally enabled the entire time the drive is reading or writing. The three write/erase channels need to be operated much faster so these channel enables are LVDS (Low Voltage Differential Signal) inputs. Each channel has two inputs, such as EN2 and EN2B. Following the standard an LVDS output consists of a current source of 3.5 mA, and this current produces across the internal termination resistor of 100Ω in the LMH6525 or LMH6526 a voltage of 350 mV. The polarity of the current through the resistor can change very quickly thus switching the channel current on or off. The bias level of the LVDS signal is about 1.2V, so the operating levels are 175 mV above and below this bias level. The ENxB inputs act as the not input so if the other input is at logical '1' state and the not input at '0' state the channel is activated. The internal 100Ω resister provides a proper termination for the LVDS signals, saving space and simplifying layout and assembly.

Control Inputs

There are two other control inputs (next to the oscillator enable which is covered in the next section). There are the global chip Enable and output select pin SELA or SELB. Setting the Enable pin to a level above 2V will enable the part. This means the supply current raises from sleep mode value to the normal operating values. The SELA or SELB input (TTL/ CMOS levels) controls which output is active. When at logical '1' state the output indicated by it's name is active. The mode of this pin also controls the oscillator circuitry which means that the appropriate setting resistors become active as described in the next section.

Oscillator Inputs

The oscillator section can be switched on or off by a LVDS signal for the LMH6525 and by a TTL/ CMOS signal for the LMH6526. When switched on the oscillator will modulate the output current. The settings of the frequency and amplitude are done by 4 resistors, two for every channel. R_{FA} and R_{FB} pins set the oscillator frequency for the A and B outputs respectively. The R_{AA} and R_{AB} pins set the oscillator amplitude for the A and B channels respectively. These 4 inputs work by having current drawn out of the pin by a setting resistor or potentiometer. The frequency and amplitude increase by decreasing setting resistor value. There are two charts in the Typical Performance Characteristics section that relates the setting resistor value to the resulting frequency or amplitude. Normally the settings for the frequency and amplitude are done by connecting the pin via a resistor to ground. If needed to program this settings it is possible to connect these R_{Fx} and R_{Ax} pins via a current limiting resistor to

the output of an op amp or DAC. When using such a circuitry the output can be held at a negative voltage, which means even if the channel pins R_{Fx} and R_{Ax} are not selected, current is drawn from the pin. This is only true when the negative voltage has such a value that the internal transistors connected to the pin will conduct. This will influence the settings of the active pins R_{Fx} and R_{Ax}. Due to this effect it is recommended, when using a negative voltage lower as -0.5V, to disable this voltage simultaneously with the channel.

OUTPUT

The outputs can source currents in excess of 600 mA. The output pins have been designed to have minimal series inductance in order to minimize current overshoot on fast pulses. The outputs have a saturation voltage of about 1V. The table below shows the typical output saturation Voltages into a 5Ω load at various supply voltages.

Table 4. Output Saturation

Supply Voltage (V)	Maximum Output (mA) 5Ω	Saturation Voltage (V)
4.5V	700	0.8
5.0V	777	0.89
5.5V	846	1.02

As can be seen, even with a 4.5V supply voltage the part can deliver 700 mA while the saturation voltage is at 0.8V. This means the output voltage of the part can be at maximum 700e-3*5 = 3.5V. With a saturated output voltage (see Figure 12) of 0.8V the voltage on the supply pin of the part is 4.3V. The used supply voltage is 4.5V so there is a supply voltage loss of 0.2V over the supply line resistance, but nevertheless the part can drive laser diodes with a forward voltage up to 3.5V with currents over 500 mA. When operating at 5.5V the part can deliver currents over 800 mA. In this case the output at the anode of the laser diode is 846e-3*5 = 4.23V, combined with the saturated output voltage of 1.02V the supply voltage of the part at the power pin is 5.25V and this means the supply line loss is 0.25V. So at 5.5V supply voltage the part can drive laser diodes with a forward voltage in access of 4V.

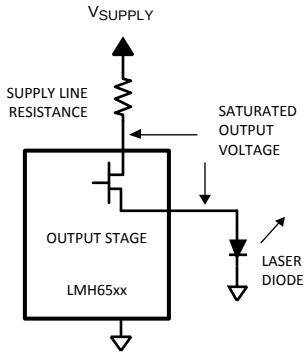


Figure 12. Output Configuration

Application Hints

SUPPLY SEQUENCING

As the LMH6525/6526 is fabricated in the CMOS7 process, latch-up concerns are minimal. Be aware that applying a low impedance input to the part when it has no supply voltage will forward bias the ESD diode on the input pin and then source power into the part's V_{DD} pin. If the potential exists for sustained operation with active inputs and no supply voltage, all the active inputs should have series resistors to limit the current into the input pins to levels below a few milliamperes.

DECOUPLING

The LMH6525/6526 has very high output currents changing within a nanosecond. This makes decoupling especially important. High performance, low impedance ceramic capacitors should be located as close as possible to the supply pins. The LMH6525/6526 needs two decoupling capacitors, one for the analog power and ground V_{DD}A, GNDA) and one for the power side supply and ground (3xV_{DD} and GNDB). The high level of output current dictates the power side decoupling capacitor should be 0.1 microfarads minimum. Larger values may improve rise times depending on the layout and trace impedances of the connections. The capacitors should have direct connection across the supply pins on the top layer, preferably with small copper-pour planes. These planes can connect to the bottom side ground and/or power planes with vias but there should be a topside low impedance path with no vias if possible. (see also Figure 15 Decoupling Capacitors).

OVERSHOOT

As the LMH6525/6526 has fast rise times of less then a nanosecond, any inductance in the output path will cause overshoot. This includes the inductance in the laser diode itself as well as any trace inductance. A series connection of a resistor and a capacitor across the laser diode could be helpful to reduce unwanted overshoot or to reduce the very high peaks caused by the relaxation oscillations of a laser diode when driven from below the knee voltage. But keep always in mind that this causes a slower rise and/ or fall time. Typical values are 10Ω and 100 pF. The actual values required depend on the laser diode used and the circuit layout and should be determined empirically.

THERMAL

General

The LMH6525/6526 is a very high current output device. This means that the device must have adequate heat-sinking to prevent the die from reaching its absolute maximum rating of 150°C. The primary way heat is removed from the LMH6525/6526 is through the Die Attach Pad, the large center pad on the bottomside of the device. Heat is also carried out of the die through the bond wires to the traces. The outputs and the V_{DD} pads of the device have double bond wires on this device so they will conduct about twice as much heat to the pad. In any event, the heat able to be transferred out the bond wires is far less than that which can be conducted out of the die attach pad. Heat can also be removed from the top of the part but the plastic encapsulation has worse thermal conductivity then copper. This means a heat sink on top of the part is less effective than the same copper area on the circuit board that is thermally attached to the Die Attach Pad.

PBC Heatsinks

In order to remove the heat from the die attach pad there must be a good thermal path to large copper pours on the circuit board. If the part is mounted on a dual-layer board the simplest method is to use 6 or 8 vias under the die attach pad to connect the pad thermally (as well as electrically, of course) to the bottomside of the circuit board. The vias can then conduct heat to a copper pour area with a size as large as possible. Please see application note AN-1187 (Literature Number SNOA401) for guidelines about these vias and QFN packaging in general.

Derating

It is essential to keep the LMH6525/6526 die under 150°C. This means that if there is inadequate heat sinking the part may overheat at maximum load while at maximum operating ambient of 85°C. How much power (current) the part can deliver to the load at elevated ambient temperatures is purely dependent on the amount of heat sinking the part is provided with.

LAYOUT

Inputs

Critical inputs are the LVDS lines. These are two coupled lines of a certain impedance, mostly 100Ω. For some reason those lines could have another value but in that case the termination resistance must have the same value. The differential input resistance of the LMH6525 and LMH6526 is 100Ω and normally the impedance of the incoming transmission line matches that value. When using a flexible flat cable it is important to know the impedance of two parallel wires in that cable. Flex cables can have different pitch distances, but a commonly

used cable has a pitch of 0.5 mm. When verified by TDR equipment, the measurements show an impedance of about 142Ω. It is possible to calculate the impedance of such a cable when some parameters are known. Needed parameters are the pitch (a) of the wires, the thickness (d) en r (see Figure 13). When Checked under a microscope: the thickness of the wires is 0.3 mm. The pitch is 0.5 mm, while the ;r must be 1 for air. The impedance of two parallel wires is given by this formula,

$$Z = (276/r) * \log\{(2*a)/d\} \quad (1)$$

With the data above filled in this formula the result is:

$$Z = 144\Omega \quad (2)$$

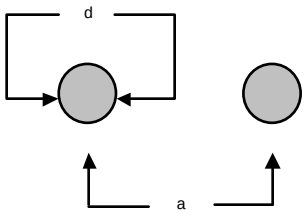


Figure 13. Parallel Wires

Both the measured and the calculated numbers match very closely. The impedance of the flex cable is a physical parameter so when designing a transmission path using this flex cable, the impedance of the total path must be based on 140Ω. There is another parameter which is the termination resistance inside the LMH6525 or LMH6526 which is 100Ω. When terminating the 140Ω transmission path with an impedance of 100Ω a mismatch will occur causing reflections on the transmission line. To solve this problem it is possible to connect directly at the input terminals of the part two resistors of 20Ω one on every pin to keep it symmetrical. Normally this causes signal loss over the total extra series resistance of 40Ω when using a voltage source for driving the transmission line. An advantage of a LVDS source is it's current nature. The current of a LVDS output is 3.5 mA and this current produces across a resistor of 140Ω a voltage of 490 mV, while this voltage across the 100Ω internal termination resistor of the part remains at 350 mV, which is conform the LVDS standard. With the usage of a series resistance of 40Ω and the termination resistor of 100Ω the total termination resistance now matches the line impedance and reflections will be as low as possible. A helpful tool for calculating impedances of transmission lines is the: 'Transmission Line Rapidesigner' available from the Texas Instruments Interface Products Group. Application Note AN-905 (Literature Number SNLA035) details the use of this handy software tool.

The Read Enable and Enable inputs are slower and much less critical. The Oscillator Enable input is toggled in combination with the write pulse so special attention should be given to this signal to insure it is routed cleanly. It may be desirable to put a termination resistor close to the LMH6526 for the Enable Oscillator line, to achieve the best turn-on and turn-off performance of the oscillator.

OUTPUTS

In order to achieve the fastest output rise times the layout of the output lines should be short and tight (see Figure 14). It is intended that the Output B trace be routed under the decoupling capacitor and that the ground return for the laser be closely coupled to the output and terminated at the ground side of the decoupling capacitor.

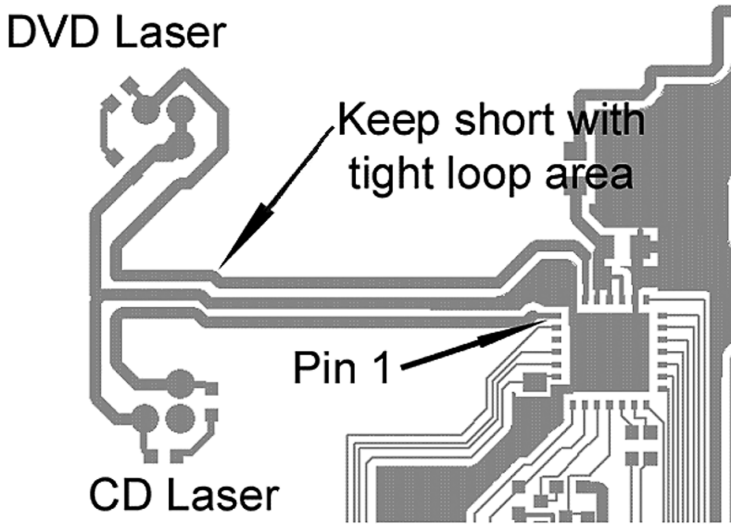


Figure 14. Laser Connection

The capacitance on the output lines should also be reduced as much as possible. As always the loop area of the laser current should be minimized and keep in mind that it is important not to have vias in the current path of the output lines. Via's will introduce some inductance which lead to extra overshoot on the pulse shape.

DECOUPLING CAPACITORS

As mentioned before, the decoupling capacitors are critical to the performance of the part. The output section above mentioned that the power-side decoupling capacitor should be as close as possible to the V_{DD} and GND pins and that the B output should pass under the decoupling capacitor. Similarly the analog-side decoupling capacitor should be as close as possible to the $V_{DD}A$ and GNDA pins. Figure 15 shows a layout where the analog ($V_{DD}A$ and GNDA) decoupling cap C1 is placed next to pins 6 and 7. (Note the layout is rotated 90 degrees from the last figure.) The ground extends into a plane that should connect to the oscillator amplitude and current setting resistors. C2 is the power-side decoupling capacitor and it can be seen placed as close to the V_{DD} and GNDB pins as possible while straddling the B output trace. This layout has also provided for a second power decoupling capacitor C3 that connects from V_{DD} to a different GND copper pour. It must be noted that the two ground planes extending from C2 and C3 must be tied together. This will be shown in the thermal section below. Bear in mind that the closeness of the parts to the LMH6525/6526 may be dictated by manufacturing rework considerations such that the LMH6525/6526 can be de-soldered with a hot-air rework station without the need to remove the capacitors. The relevant manufacturing organization can provide guidelines for this minimum spacing.

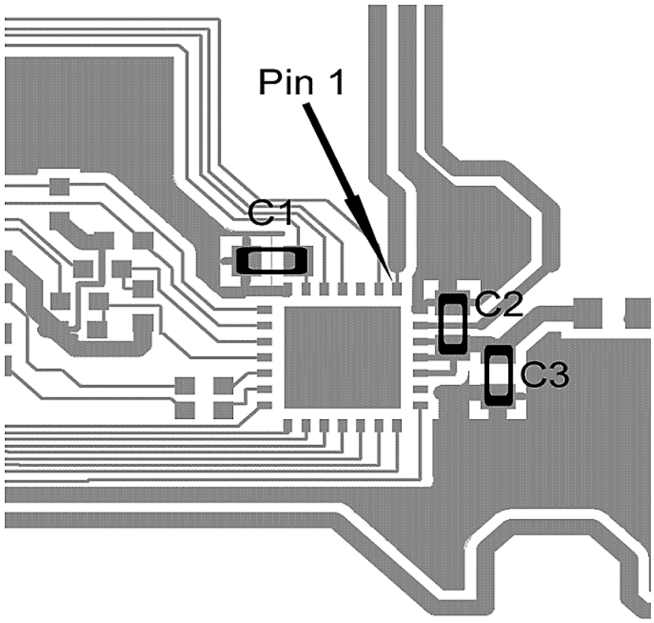


Figure 15. Decoupling Capacitors

OSCILLATOR RESISTORS

The resistors and/or potentiometers used to set oscillator frequency or amplitude should be as close to the part as possible. If the grounds are split when using a single-sided flex circuit, it is essential that these resistors and potentiometers share the same ground as the GNDA pin and decoupling capacitor.

THERMAL

As mentioned previously, the primary way to get heat out of the QFN package is by the large Die Attach Pad at the center of the part's underside. On two-layer circuits this can be done with vias. On single-sided circuits the pad should connect with a copper pour to either the GND pin or, if a better thermal path can be achieved, with the V_{DD} pins. Be aware that the unused pins on the part can also be used to connect a copper pour area to the Die Attach Pad. Figure 16 Heat Sinking (with the same orientation as the first layout example) shows using the unused pin to provide a thermal path to copper pour heat sinks. In this layout the analog ground has been separated from the power ground so pin 7 is not connected to the Die Attach Paddle even though it would help remove heat from the part. The above layout is based on a single-sided circuit board. If a dual-sided circuit board was used there would also be vias on the Die Attach Pad that would conduct heat to a copper plane on the bottom side of the board.

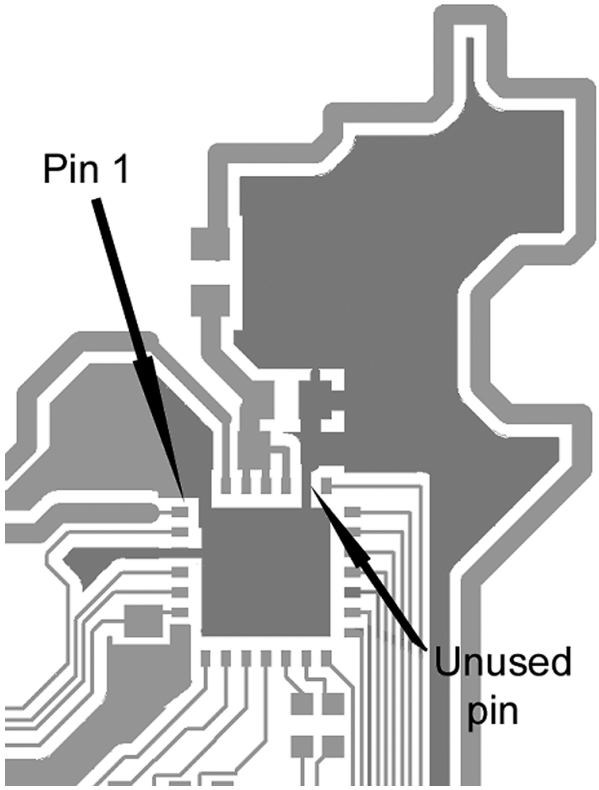


Figure 16. Heat Sinking

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6525SP/NOPB	ACTIVE	UQFN	NJD	28	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L6525SP	Samples
LMH6526SP/NOPB	ACTIVE	UQFN	NJD	28	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L6526SP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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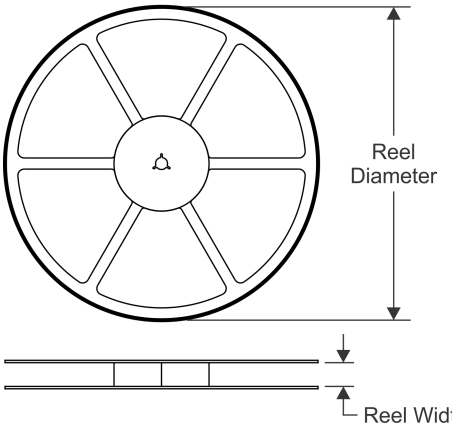
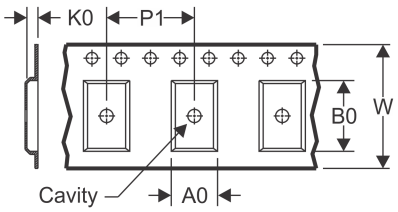
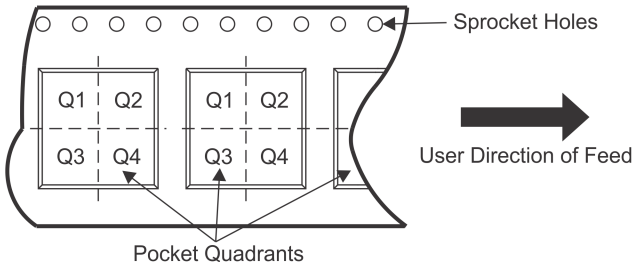


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

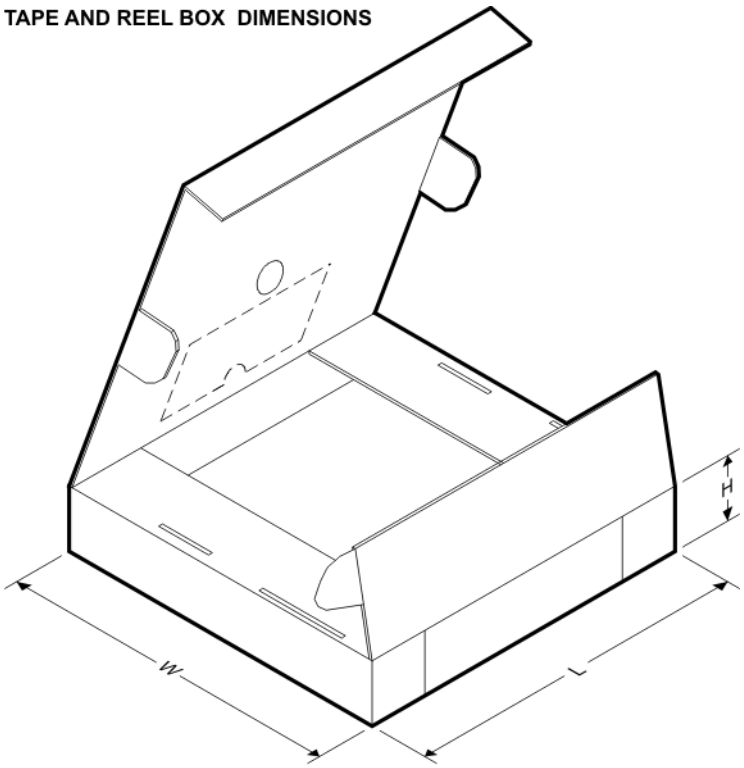
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6525SP/NOPB	UQFN	NJD	28	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMH6526SP/NOPB	UQFN	NJD	28	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

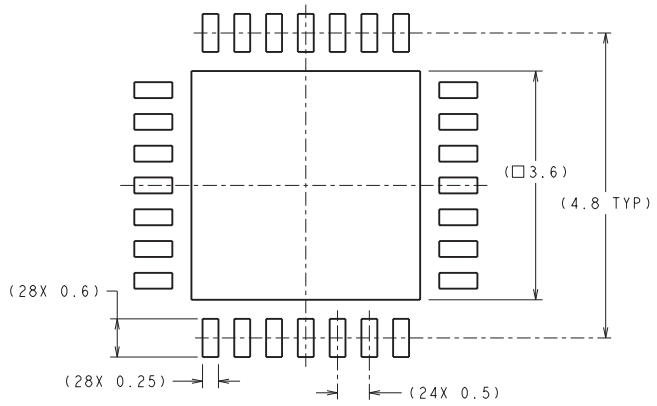
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

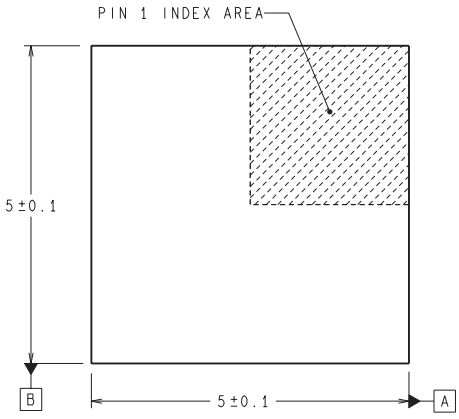
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6525SP/NOPB	UQFN	NJD	28	1000	210.0	185.0	35.0
LMH6526SP/NOPB	UQFN	NJD	28	1000	210.0	185.0	35.0

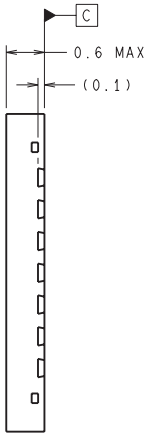
NJD0028A

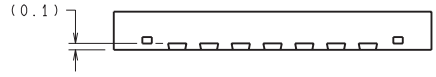


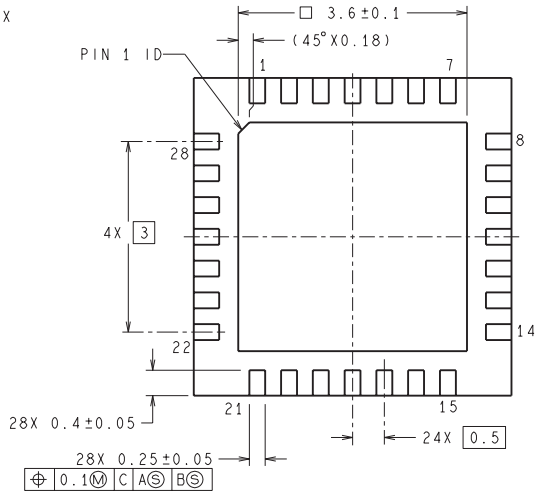
RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY









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