LMH6572 Triple 2:1 High Speed Video Multiplexer

Check for Samples: LMH6572

FEATURES

- 350 MHz, 250 mV −3 dB Bandwidth
- 290 MHz, 2 V_{PP} −3 dB Bandwidth
- 10 ns Channel Switching Time
- 90 dB Channel to Channel Isolation @ 5 MHz
- 0.02%, 0.02° Diff. Gain, Phase
- 0.1 dB Gain Flatness to 140 MHz
- 1400 V/µs Slew Rate
- Wide Supply Voltage Range: 6V (±3V) to 12V (±6V)
- −78 dB HD2 @ 10 MHz
- −75 dB HD3 @ 10 MHz

APPLICATIONS

- RGB Video Router
- Multi Input Video Monitor
- Fault Tolerant Data Switch

Connection Diagram

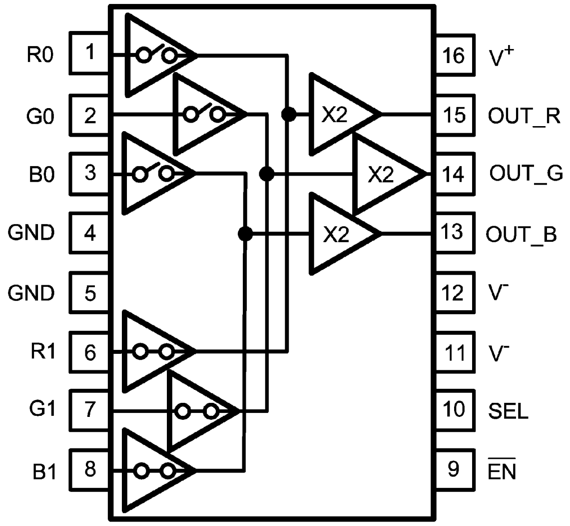

**Figure 1. 16-Pin SSOP Package
See Package Number DBQ0016A
Top View**

DESCRIPTION

The LMH™ 6572 is a high performance analog multiplexer optimized for professional grade video and other high fidelity, high bandwidth analog applications. The LMH6572 provides a 290MHz bandwidth at 2 V_{PP} output signal levels. The 140 MHz of .1 dB bandwidth and a 1500 V/µs slew rate make this part suitable for High Definition Television (HDTV) and High Resolution Multimedia Video applications.

The LMH6572 supports composite video applications with its 0.02% and 0.02° differential gain and phase errors for NTSC and PAL video signals while driving a single, back terminated 75Ω load. The LM6572 can deliver 80 mA linear output current for driving multiple video load applications.

The LMH6572 has an internal gain of 2 V/V (+6 dBv) for driving back terminated transmission lines at a net gain of 1 V/V (0 dBv).

The LMH6572 is available in the SSOP package.

Truth Table

SEL	$\overline{EN}$	OUT
0	0	CH 1
1	0	CH 0
X	1	Disable

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

ESD Tolerance[3]	Human Body Model	2000V
	Machine Model	200V
Supply Voltage ($V^+ - V^-$)		13.2V
I_{OUT}[4]		130 mA
Input Voltage Range		±(V_S)
Maximum Junction Temperature		+150°C[3]
Storage Temperature Range		−65°C to +150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, 1.5 kΩ in series with 100 pF. Machine Model 0Ω In series with 200 pF.
(4) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations. See the Power Dissipation section of the Application Section for more details. A short circuit condition should be limited to 5 seconds or less.

Operating Ratings[1]

Operating Temperature			−40 °C to 85 °C
Supply Voltage Range			6V to 12V
Thermal Resistance			
Package	16-Pin SSOP	(θ_{JA})	125°C/W
		(θ_{JC})	36°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.

±5V Electrical Characteristics

Unless otherwise specified, V_S = ±5V, R_L = 100Ω.

Symbol	Parameter	Conditions [1]	Min	Typ	Max	Units
Frequency Domain Performance						
SSBW	−3 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		350		MHz
LSBW	–3 dB Bandwidth [2]	V_{OUT} = 2 V_{PP}	250	290		MHz
.1 dBBW	0.1 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		140		MHz
DG	Differential Gain	R_L = 150Ω, f = 4.43 MHz		0.02		%
DP	Differential Phase	R_L = 150Ω, f = 4.43MHz		0.02		deg
Time Domain Response						
TRS	Channel to Channel Switching Time	Logic Transition to 90% Output		10		ns
	Enable and Disable Times	Logic Transition to 90% or 10% Output		11		ns
TRL	Rise and Fall Time	2V Step		1.5		ns
TSS	Settling Time to 0.05%	2V Step		17		ns
OS	Overshoot	4V Step		5		%
SR	Slew Rate [2]	4V Step	1200	1400		V/μs
Distortion						
HD2	2nd Harmonic Distortion	2 V_{PP} , 10 MHz		−78		dBc
HD3	3rd Harmonic Distortion	2 V_{PP} , 10 MHz		−75		dBc
IMD	3rd Order Intermodulation Products	10 MHz, Two tones 2 V_{PP} at Output		−80		dBc
Equivalent Input Noise						
VN	Voltage	>1 MHz, Input Referred		5		nV√Hz
ICN	Current	>1 MHz, Input Referred		5		pA/√Hz
Static, DC Performance						
GAIN	Voltage Gain			2.0		V/V
	Gain Error [3]	No load, with respect to nominal gain of 2.00 V/V.		±0.3	±0.5 **±0.7**	%
	Gain Error	R_L = 50Ω, with respect to nominal gain of 2.00 V/V		0.3		%
VIO	Output Offset Voltage [3]	V_{IN} = 0V		1	±14 **±17.5**	mV
DVIO	Average Drift			27		μV/°C
IBN	Input Bias Current [3] [4]	V_{IN} = 0V		−1.4	±5.0 **±5.6**	μA
DIBN	Average Drift			7		nA/°C
PSRR	Power Supply Rejection Ratio [3]	DC, Input referred	50 **48**	54		dB
ICC	Supply Current [3]	No load	20	23	25 **28.5**	mA
	Supply Current Disabled [3]	No load		2.0	2.2 **2.3**	mA
VIH	Logic High Threshold [3]	Select & Enable Pins	2.0			V
VIL	Logic Low Threshold [3]	Select & Enable Pins			0.8	V
IiL	Logic Pin Input Current Low [4]	Logic Input = 0V		−1	±5.0 **±15**	μA
IiH	Logic Pin Input Current High [4]	Logic Input = 2.0V	112 **100**	150	200 **210**	μA

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(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Applications Section for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

(2) Parameters ensured by design.

(3) Parameters ensured by electrical testing at 25° C.

(4) Positive Value is current into device.

±5V Electrical Characteristics (continued)

Unless otherwise specified, V_S = ±5V, R_L = 100Ω.

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Units
Miscellaneous Performance						
RF	Internal Feedback and Gain Set Resistor Values		650 **620**	800	940 **1010**	Ω
RODIS	Disabled Output Resistance	Internal Feedback and Gain Set Resistors in Series to Ground	1.3	1.6	1.88	kΩ
RIN+	Input Resistance			100		kΩ
CIN	Input Capacitance			0.9		pF
ROUT	Output Resistance			0.26		Ω
VO	Output Voltage Range	No Load	±3.83 **±3.80**	±3.9		V
VOL		R_L = 100Ω	±3.52 **±3.5**	±3.53		V
CMIR	Input Voltage Range		±2	±2.5		V
IO	Linear Output Current(3)(4)	V_{IN} = 0V	+70 40	±80		mA
ISC	Short Circuit Current(5)	V_{IN} = ±2V, Output Shorted to Ground		±230		mA
XTLK	Channel to Channel Crosstalk	V_{IN} = 2 V_{PP} @5 MHz		-90		dBc
XTLK	Channel to Channel Crosstalk	V_{IN} = 2 V_{PP} @ 100 MHz		-54		dBc
XTLK	All Hostile Crosstalk	In A, C. Out B, V_{IN} = 2 V_{PP} @ 5 MHz		-95		dBc

(5) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations. See the Power Dissipation section of the Application Section for more details. A short circuit condition should be limited to 5 seconds or less.

±3.3V Electrical Characteristics

Unless otherwise specified, V_S = ±3.3V, R_L = 100Ω.

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Units
Frequency Domain Performance						
SSBW	−3 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		360		MHz
LSBW	−3 dB Bandwidth	V_{OUT} = 2.0 V_{PP}		270		MHz
0.1 dBBW	0.1 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		80		MHz
GFP	Peaking	DC to 200 MHz		0.3		dB
DG	Differential Gain	R_L = 150Ω, f=4.43 MHz		0.02		%
DP	Differential Phase	R_L = 150Ω, f=4.43 MHz		0.03		deg
Time Domain Response						
TRL	Rise and Fall Time	2V Step		2.0		ns
TSS	Settling Time to 0.05%	2V Step		15		ns
OS	Overshoot	2V Step		5		%
SR	Slew Rate	2V Step		1000		V/µs
Distortion						
HD2	2nd Harmonic Distortion	2 V_{PP}, 10 MHz		−70		dBc
HD3	3rd Harmonic Distortion	2 V_{PP}, 10 MHz		−74		dBc
IMD	3rd Order Intermodulation Products	10 MHz, Two tones 2 V_{PP} at Output		-79		dBc
Static, DC Performance						
GAIN	Voltage Gain			2.0		V/V
VIO	Output Offset Voltage	V_{IN} = 0V		1		mV
DVIO	Average Drift			36		µV/°C
IBN	Input Bias Current[2]	V_{IN} = 0V		2		µA
DIBN	Average Drift			24		nA/°C
PSRR	Power Supply Rejection Ratio	DC, Input Referred		54		dB
ICC	Supply Current	RL = ∞		20		mA
VIH	Logic High Threshold	Select & Enable Pins			1.3	V
VIL	Logic Low Threshold	Select & Enable Pins	0.4			V
Miscellaneous Performance						
RIN+	Input Resistance			100		kΩ
CIN	Input Capacitance			0.9		pF
ROUT	Output Resistance			0.27		Ω
VO	Output Voltage Range	No Load		±2.5		V
VOL		R_L = 100Ω		±2.2		V
CMIR	Input Voltage Range			±1.2		V
IO	Linear Output Current	V_{IN} = 0V		±60		mA
ISC	Short Circuit Current	V_{IN} = ±1V, Output Shorted to Ground		±150		mA
XTLK	Channel to Channel Crosstalk	5 MHz		-90		dBc

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Applications Section for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

(2) Positive Value is current into device.

Typical Performance Characteristics

Unless otherwise specified, $V_S = \pm 5V$, $R_L = 100\Omega$.

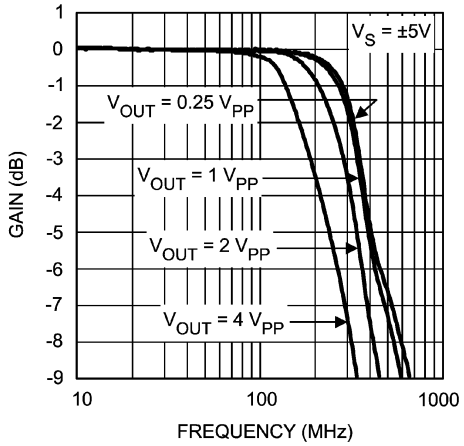
Frequency Response vs. V_{OUT}

Figure 2.

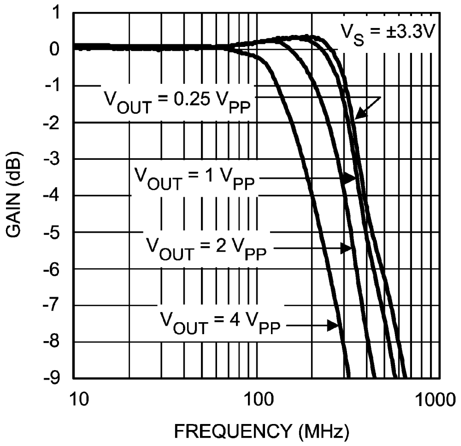
Frequency Response vs. V_{OUT}

Figure 3.

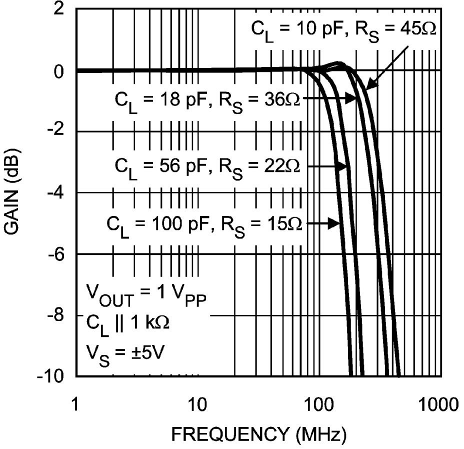
Frequency Response vs. Capacitive Load

Figure 4.

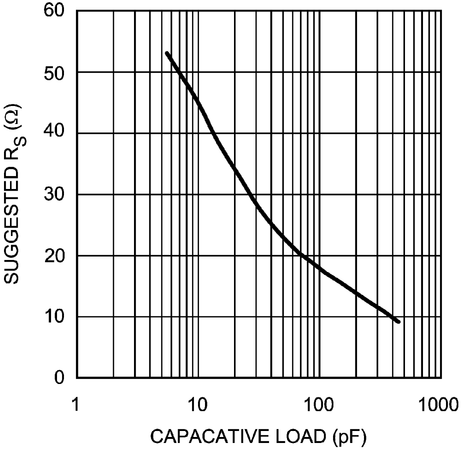
Suggested R_S vs. Capacitative Load
Load = 1kΩ || C_L

Figure 5.

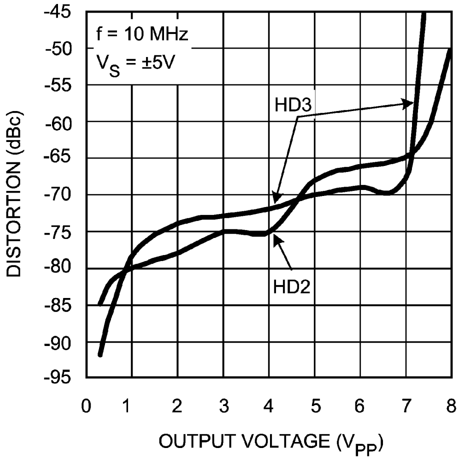
Harmonic Distortion vs. Output Voltage

Figure 6.

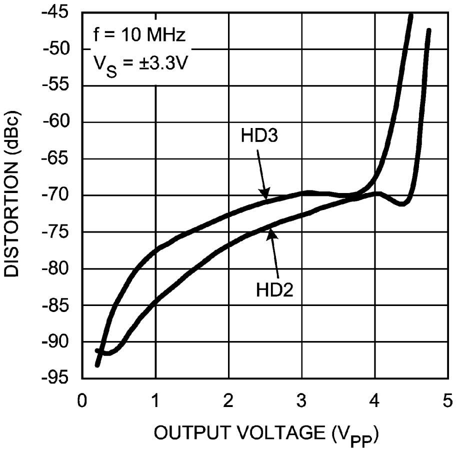
Harmonic Distortion vs. Output Voltage

Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = ±5V, R_L = 100Ω.

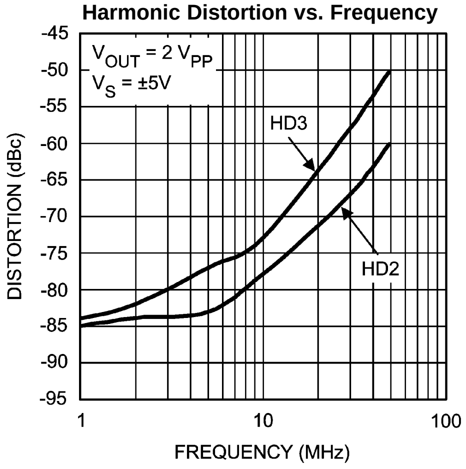

Figure 8.

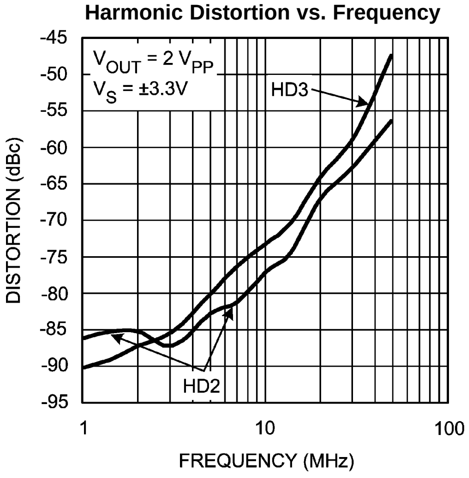

Figure 9.

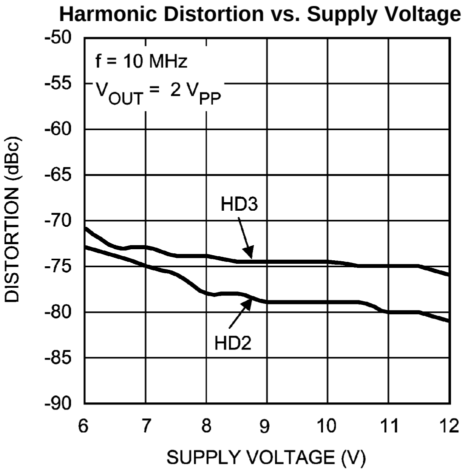

Figure 10.

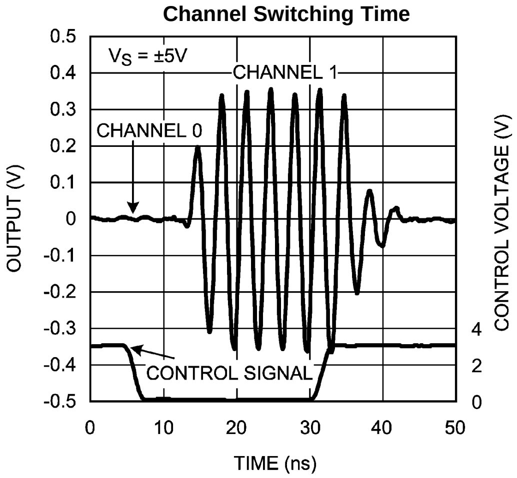

Figure 11.

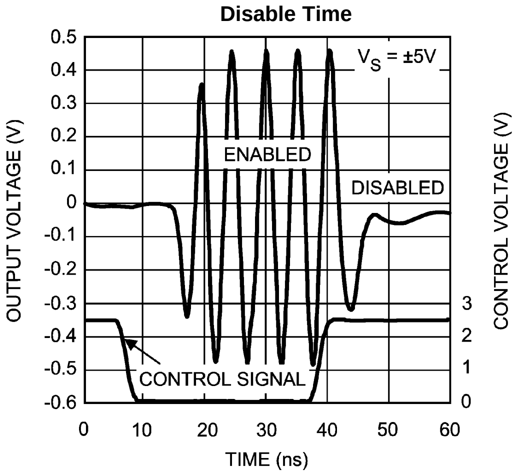

Figure 12.

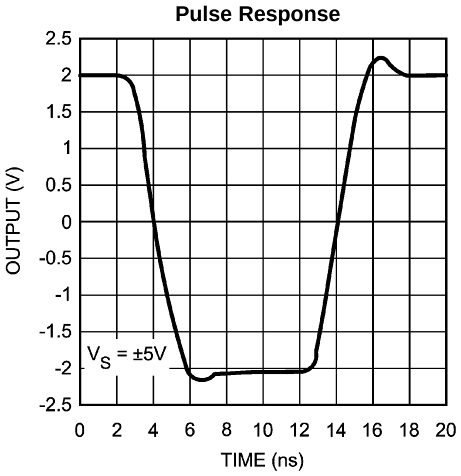

Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise specified, $V_S = \pm5V$, $R_L = 100\Omega$.

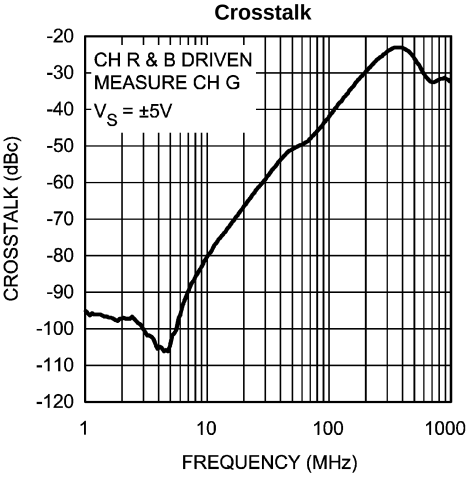

Figure .

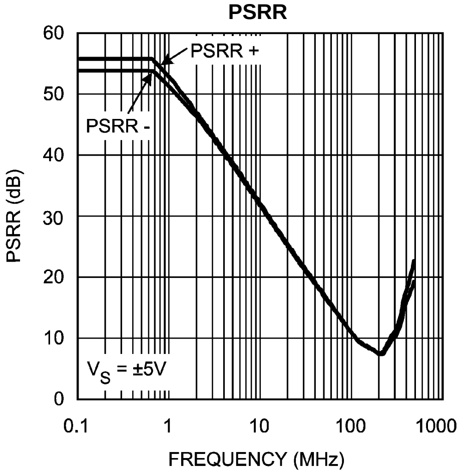

Figure 14.

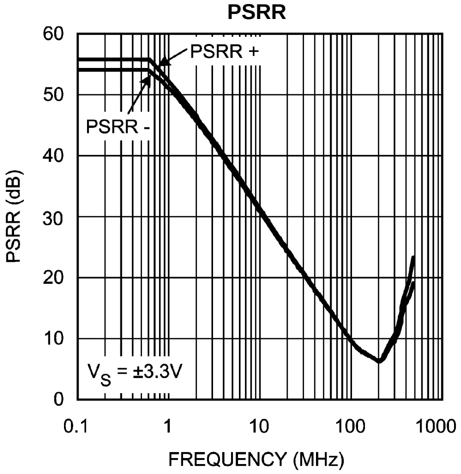

Figure 15.

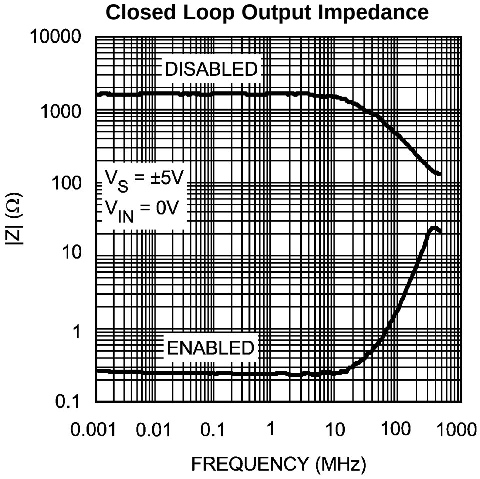

Figure 16.

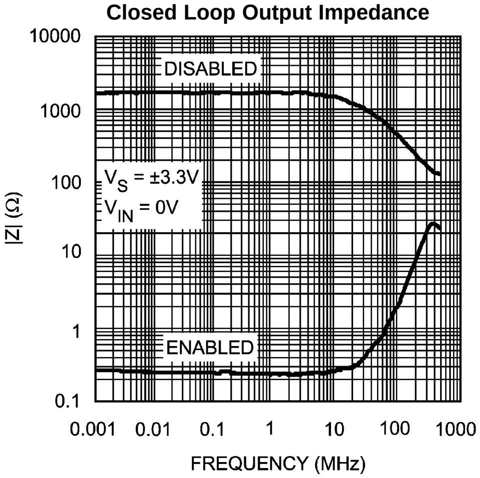

Figure 17.

APPLICATION NOTES

General Information

The LMH6572 is a high-speed triple 2:1 analog multiplexer, optimized for very high speed and low distortion. With a fixed gain of 2 and excellent AC performance, the LMH6572 is ideally suited for switching high resolution, presentation grade video signals. The LMH6572 has no internal ground reference. Single or split supply configurations are both possible. The LMH6572 features very high speed channel switching and disable times. When disabled the LMH6572 output is high impedance, making multiplexer expansion possible by combining multiple devices.

Single Supply Operation

The LMH6572 uses mid-supply referenced circuits for the select and disable pins. In order to use the LMH6572 in single supply configuration, it is necessary to use a circuit similar to Figure 19. In this configuration the logical inputs are compatible with high breakdown open collector TTL, or open drain CMOS logic. In addition, the default logic state is reversed since there is a pull-up resistor on those pins. Single supply operation also requires the input to be biased to within the common mode input range of roughly ±2V from the mid-supply point.

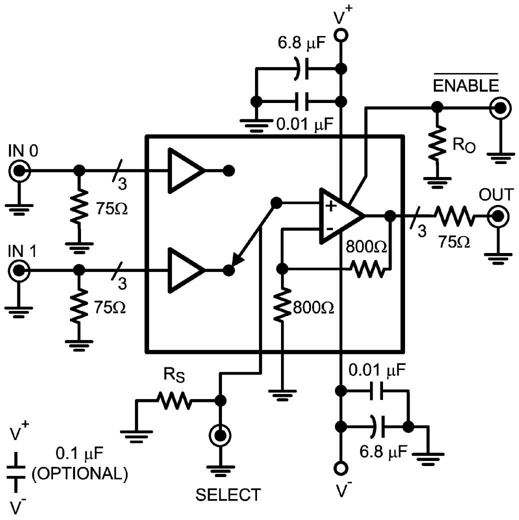

Figure 18. Typical Application

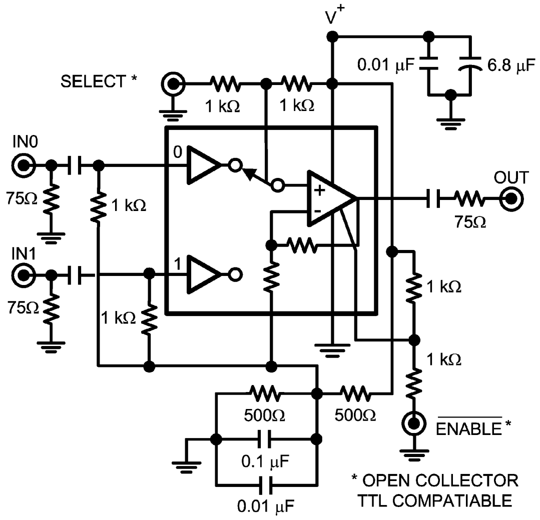

Figure 19. Single Supply Application

Video Performance

The LMH6572 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. Figure 18 shows a typical configuration for driving a 75Ω cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.

Gain Accuracy

The gain accuracy of the LMH6572 is accurate to ±0.5% (0.3% typical) and stable over temperature. The internal gain setting resistors, RF and RG, match very well; however, over process and temperature their absolute value will change.

Expanding the Multiplexer

It is possible to build higher density multiplexers by paralleling several LMH6572s. Figure 20 shows a 4:1 RGB MUX using two LMH6572s:

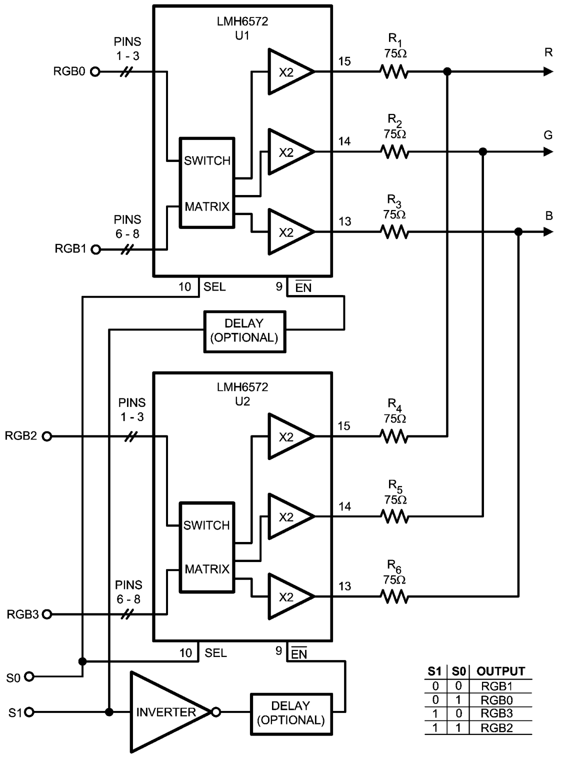

Figure 20. RGB MUX Using Two LMH6572's

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added prior to the ENABLE($\overline{\text{EN}}$) pin of each device, as shown. Figure 21 shows one possible approach to this delay circuit. The delay circuit shown will delay $\overline{\text{ENABLE}}$'s H to L transitions (R_1 and C_1 decay) but will not delay its L to H transition.

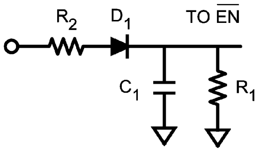

Figure 21. Delay Circuit Implementation

R_2 should be kept small compared to R_1 in order to not reduce the $\overline{\text{ENABLE}}$ voltage and to produce little or no delay to the $\overline{\text{ENABLE}}$ L to H transition.

With the $\overline{\text{ENABLE}}$ pin putting the output stage into a high impedance state, several LMH6572's can be tied together to form a larger input MUX. However, there is a slight loading effect on the active output caused by the off-channel feedback and gain set resistors, as shown in Figure 21. Figure 22 is assuming there are four LMH6572 devices tied together to form a triple 8:1 MUX. With the internal resistors valued at approximately 800Ω, the gain error is about -0.57 dB, or about −6%.

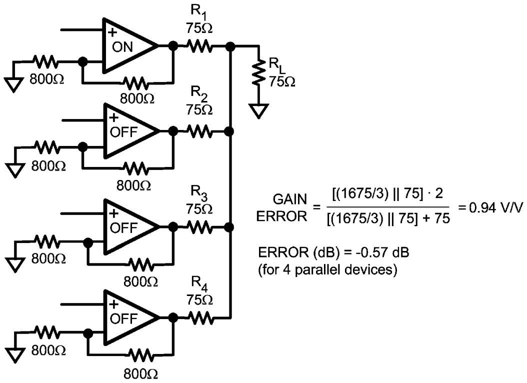

Figure 22. Multiplexer Input Expansion by Combining Outputs

An alternate approach would be to tie the outputs directly together and let all devices share a common back termination resistor in order to alleviate the gain error issue above.

The drawback in this case is the increased capacitive load presented to the output of each LMH6572 due to the offstate capacitance of the LMH6572.

Other Applications

The LMH6572 may be utilized in systems that involve a single RGB channel as well whenever there is a need to switch between different “flavors” of a single RGB input.

Here are some examples:

1. RGB positive polarity, negative polarity switch
2. RGB full resolution, high-pass filter switch

In each of these applications, the same RGB input occupies one set of inputs to the LMH6572 and the other “flavor” would be tied to the other input set.

Driving Capacitive Loads

Capacitive output loading applications will benefit from the use of a series output resistor. Figure 23 shows the use of a series output resistor, R_{OUT}, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Figure 24 gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for .5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

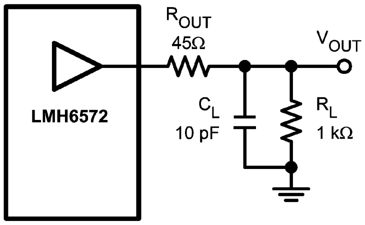

Figure 23. Decoupling Capacitive Loads

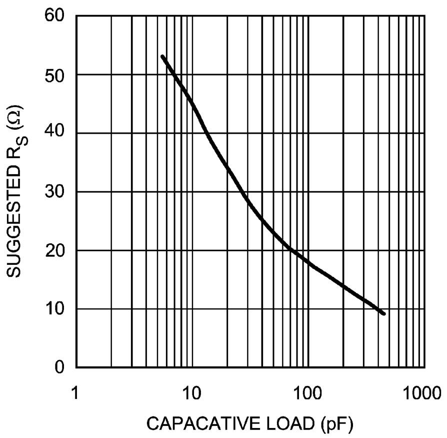

Figure 24. Recommended R_{OUT} vs. Capacitive Load

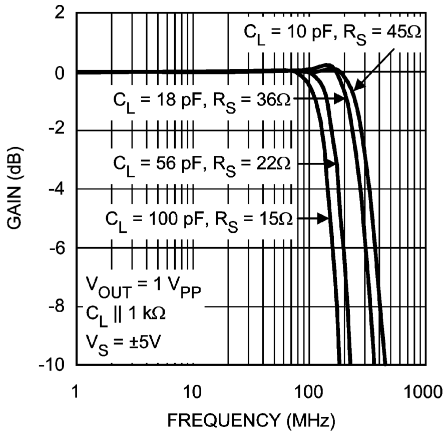

Figure 25. Frequency Response vs. Capacitive Load

Layout Considerations

Whenever questions about layout arise, use the LMH730151 evaluation board as a guide. To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device; however, the smaller ceramic capacitors should be placed as close to the device as possible. In Figure 18 and Figure 19, the capacitor between V^+ and V^- is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of .01 µF and 0.1 µF ceramic capacitors for each supply bypass.

Power Dissipation

The LMH6572 is optimized for maximum speed and performance in the small form factor of the standard SSOP package. To achieve its high level of performance, the LMH6572 consumes 23 mA of quiescent current, which cannot be neglected when considering the total package power dissipation limit. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6572:

1. Calculate the quiescent (no-load) power:

$P_{AMP} = I_{CC} * (V_S)$

where

- $V_S = V^+ - V^-$ (1)

2. Calculate the RMS power dissipated in the output stage:

P_D (rms) = rms $((V_S - V_{OUT}) * I_{OUT})$

where

- V_{OUT} and I_{OUT} are the voltage across and the current through the external load
- V_S is the total supply voltage (2)

3. Calculate the total RMS power:

$P_T = P_{AMP} + P_D$ (3)

The maximum power that the LMH6572 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° – T_{AMB})/ \theta_{JA}$

where

- T_{AMB} = Ambient temperature (°C)
- θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)
- For the SSOP package θ_{JA} is 125 °C/W (4)

PRODUCT PREVIEW

ESD Protection

The LMH6572 is protected against electrostatic discharge (ESD) on all pins. The LMH6572 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6572 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Shorting the power pins to each other will prevent the chip from being powered up through the input.

Evaluation Boards

Texas Instruments provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the datasheet plots were measured with these boards.

Device	Package	Evaluation Board Part Number
LMH6572	SSOP	LMH730151

An evaluation board can be shipped when a device sample request is placed with Texas Instruments.

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6572MQ/NOPB	ACTIVE	SSOP	DBQ	16	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LH65 72MQ	Samples
LMH6572MQX/NOPB	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LH65 72MQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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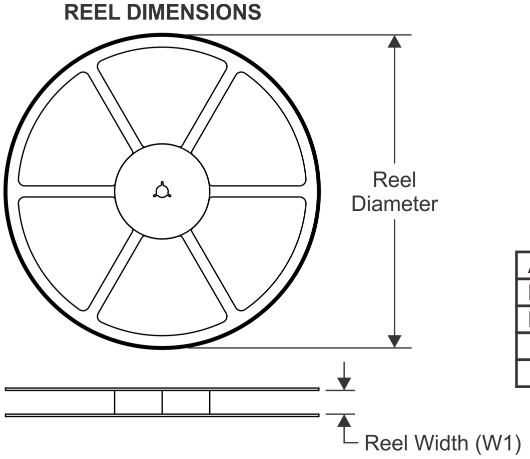
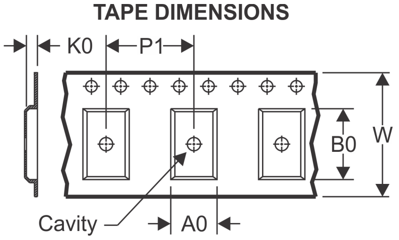
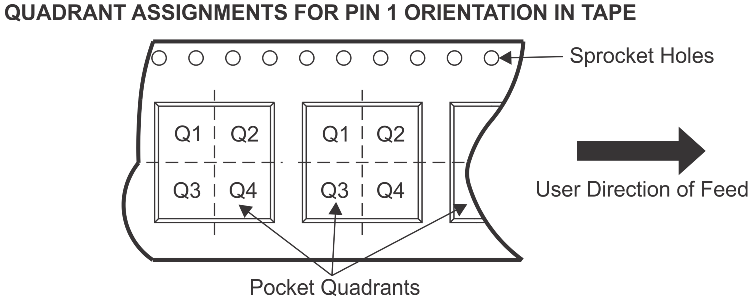
TAPE AND REEL INFORMATION





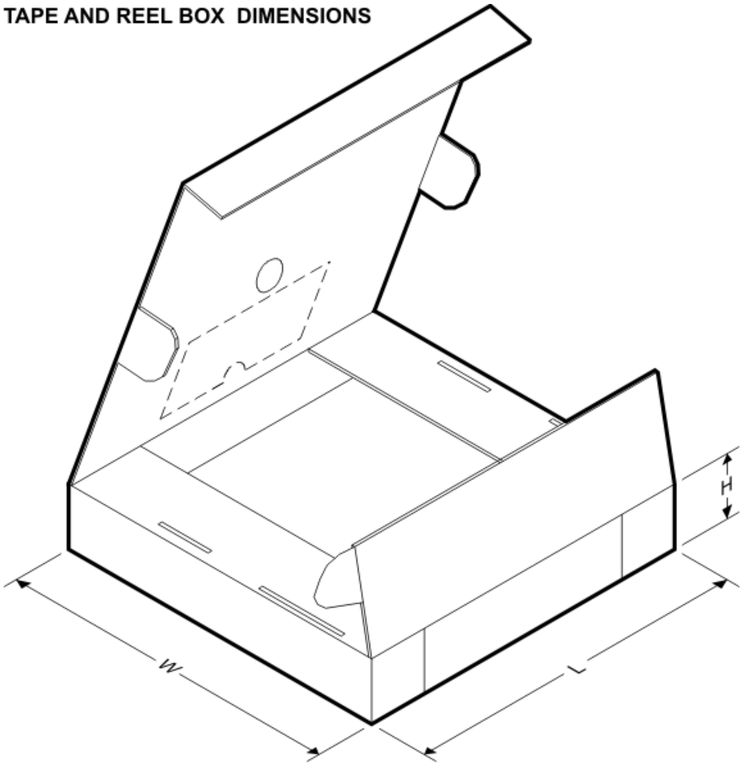
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6572MQX/NOPB	SSOP	DBQ	16	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

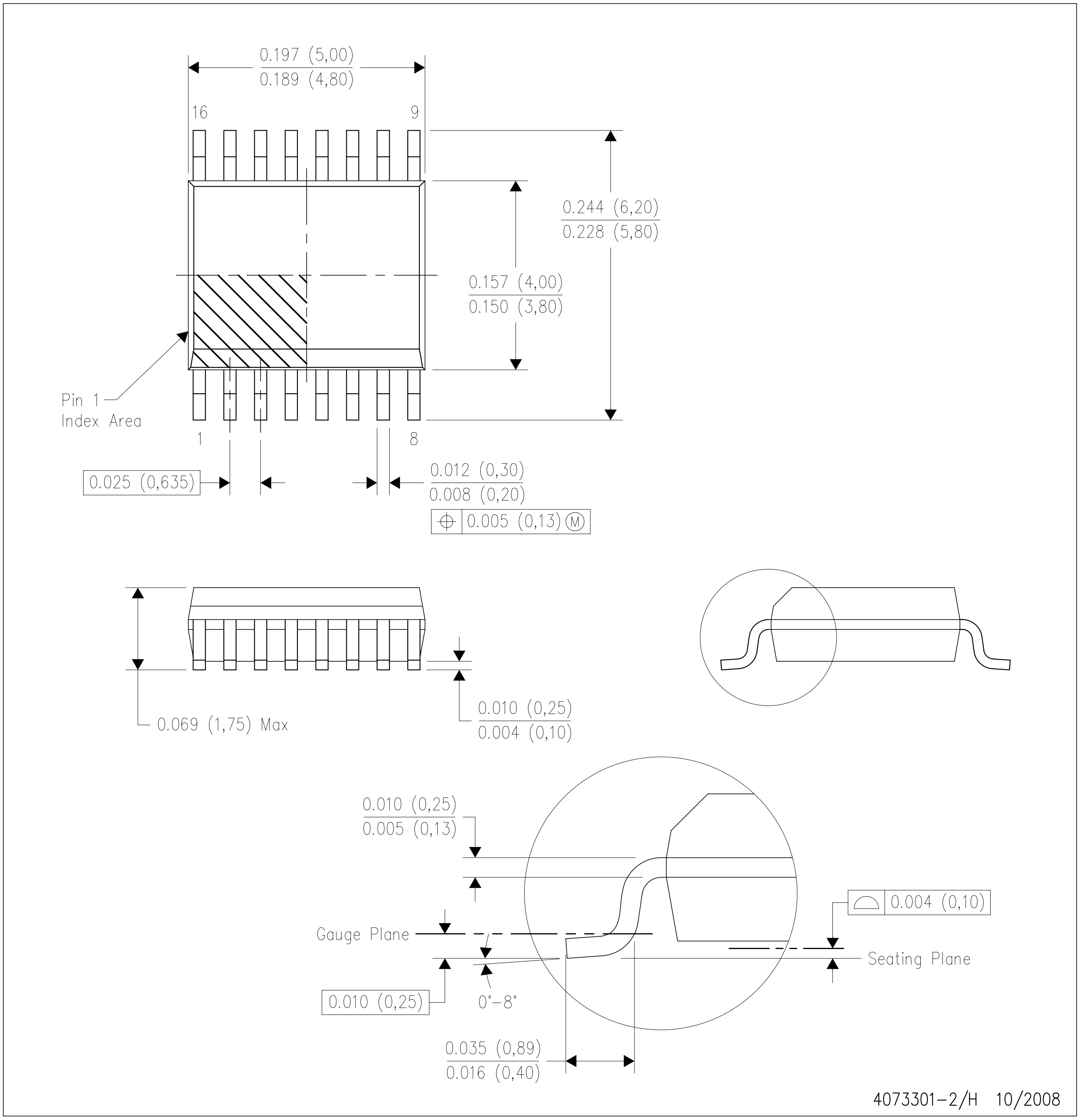
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6572MQX/NOPB	SSOP	DBQ	16	2500	367.0	367.0	35.0

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO–137 variation AB.

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