LM5165-Q1 3-V to 65-V Input, 150-mA Synchronous Buck Converter with Ultra-Low I_Q

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40ºC to 125ºC Ambient Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- Wide Input Voltage Range of 3 V to 65 V
- Fixed (3.3 V, 5 V) or Adjustable Output Voltages
- Maximum Output Current as High as 150 mA
- 10.5-µA No Load Quiescent Current
- –40°C to 150°C Junction Temperature Range
- Selectable PFM or COT Mode Operation
- Switching Frequency as High as 600 kHz
- Integrated 2-Ω PMOS Buck Switch
  - Supports 100% Duty Cycle for Low Dropout
- Integrated 1-Ω NMOS Synchronous Rectifier
  - Eliminates External Rectifier Diode
- Programmable Current Limit Setpoint (4 Levels)
- 900-µs Internal or Programmable Soft Start
- Monotonic Startup into Pre-Biased Output
- No Loop Compensation or Bootstrap Components
- Precision Enable/Input UVLO with Hysteresis
- Open-Drain Power Good Indicator
- Active Slew Rate Control for Low EMI
- Thermal Shutdown Protection with Hysteresis
- 10-Lead, 3-mm x 3-mm VSON Package

2 Applications

- Automotive and Battery-powered Equipment
- High-voltage LDO Replacement
- General Purpose Bias Supplies

3 Description

The LM5165-Q1 is a compact, easy-to-use, 3-V to 65-V, ultra-low I_Q synchronous buck converter with high efficiency over wide input voltage and load current ranges. With integrated high-side and low-side power MOSFETs, up to 150-mA of output current can be delivered at fixed output voltages of 3.3 V or 5 V, or an adjustable output. The converter is designed to simplify implementation while providing options to optimize the performance the target application. Pulse Frequency Modulation (PFM) mode is selected for optimal light-load efficiency or Constant On-Time (COT) control for nearly constant operating frequency. Both control schemes do not require loop compensation while providing excellent line and load transient response and short PWM on-time for large step-down conversion ratios.

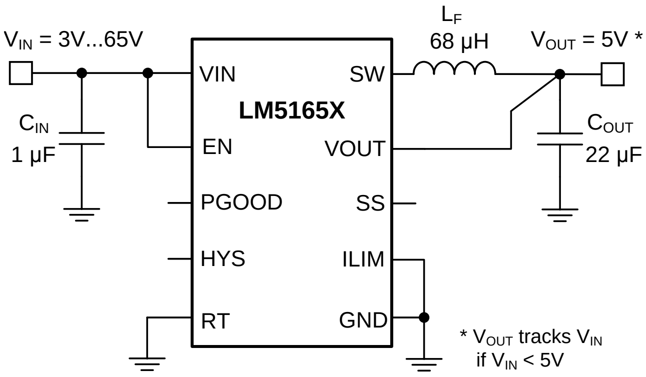
The high-side p-channel MOSFET can operate at 100% duty cycle for lowest dropout voltage and does not require a bootstrap capacitor for gate drive. Also, the current limit setpoint is adjustable to optimize inductor selection for a particular output current requirement. Selectable/adjustable startup timing options include minimum delay (no soft start), internally fixed (900 µs), and externally programmable soft start via an external capacitor. An open-drain PGOOD indicator can be used for sequencing and output voltage monitoring. The LM5165-Q1 is qualified to automotive AEC-Q100 grade 1 and is available in a VSON-10 package with 0.5-mm pin pitch.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5165-Q1	VSON (10)	3 mm x 3 mm
LM5165X-Q1		
LM5165Y-Q1		

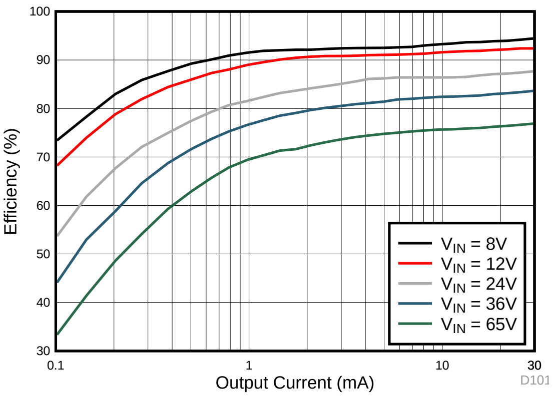
(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Schematic, Fixed Output



* V_{OUT} tracks V_{IN} if V_{IN} < 5V

Typical Efficiency, V_{OUT} = 5 V



4 Revision History

Changes from Original (February 2016) to Revision A	**Page**
• Product Preview to Production Data Release	1

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Device Comparison Table(1)(2)

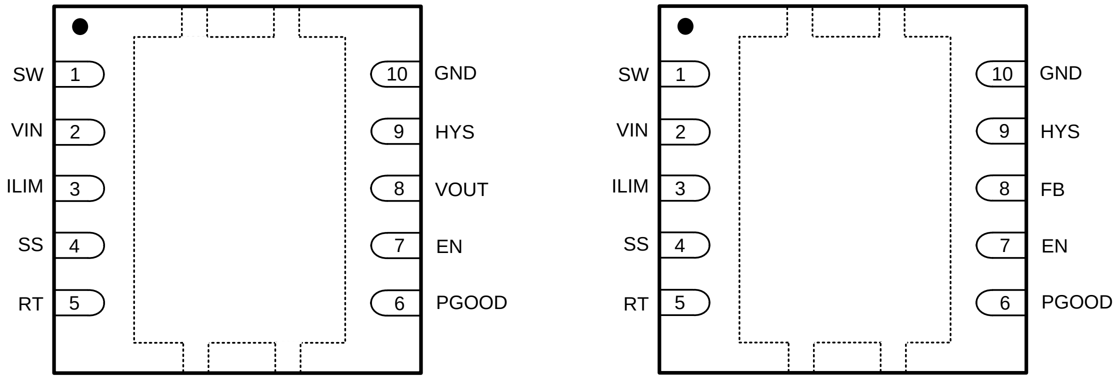
PART NUMBER	VOLTAGE OPTION	PACKAGE QUANTITY
LM5165XQDRCRQ1	5.0V	3000
LM5165XQDRCTQ1		250
LM5165YQDRCRQ1	3.3V	3000
LM5165YQDRCTQ1		250
LM5165QDRCRQ1	Adjustable	3000
LM5165QDRCTQ1		250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or refer to the *TI website*.

(2) Package drawings, thermal data and symbolization are available at *www.ti.com/packaging*.

5 Pin Configuration and Functions

DRC Package
10-Pin VSON with Exposed Thermal Pad
Top View



LM5165X, LM5165Y
Fixed Output Versions

LM5165
Adjustable Output Version

Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
SW	1	P	Switching node that is internally connected to the drain of the high-side PMOS buck switch and the drain of the low-side NMOS synchronous rectifier. Connect to the switching side of the power inductor.
VIN	2	P	Regulator supply input pin to high-side power MOSFET and internal bias rail LDO. Connect to input supply and input capacitor C_{IN}. Path from VIN to the input capacitor must be as short as possible.
ILIM	3	I	Programming pin for current limit. Connecting the appropriate resistor from ILIM to GND selects one of four pre-set current limit options. Short ILIM to GND for the maximum current setting.
SS	4	I	Programming pin for the soft-start time. If a 100-kΩ resistor is connected from SS to GND, the internal soft-start circuit is disabled and the FB comparator reference steps immediately from zero to full value when the regulator is enabled by the EN input. If the SS pin is left open, the internal soft-start circuit ramps the FB reference from zero to full value in 900 µs. If an appropriate capacitance is connected to the SS pin, the soft-start time can be programmed as required.
RT	5	I	Mode selection and on-time programming pin for Constant On-Time (COT) control. Short RT to GND to select PFM (pulse frequency modulation) operation. Connect a resistor from RT to GND to program the on-time, which sets the switching frequency for COT.
PGOOD	6	O	Power Good output flag pin. PGOOD is connected to the drain of an NFET that holds the pin low when either FB or VOUT is below the regulation target. Use a pull-up resistor of 10 kΩ to 100 kΩ to the system voltage rail or VOUT (no higher than 12 V).
EN	7	I	Input pin of the precision enable / UVLO comparator. The converter is enabled when the EN voltage is greater than 1.212V.
VOUT/FB	8	I	Feedback input to voltage regulation loop. The VOUT pin connects the internal feedback resistor divider to the regulator output voltage for fixed 3.3V and 5V options. The FB pin connects the internal feedback comparator to an external resistor divider for the adjustable output voltage option. The FB comparator reference voltage is nominally 1.223V.
HYS	9	O	Drain of an internal NFET that is turned off when the EN input is greater than the EN threshold. An external resistor from HYS to the EN pin UVLO resistor divider programs the input UVLO hysteresis voltage.
GND	10	G	Regulator ground return.
PAD	-	P	Exposed pad. Connect to the GND pin and system ground on PCB. Path to C_{IN} must be as short as possible.

(1) P = Power, G = Ground, I = Input, O = Output.

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).(1)

PARAMETER		MIN	MAX	UNIT
VIN to GND		–0.3	68	V
EN to GND		–0.3	VIN + 0.3	
SW to GND		–0.7	VIN + 0.3	
	20-ns transient	–3		
PGOOD, VOUT(3) to GND	Survives short to automotive battery voltage	–0.3	16	
HYS to GND		–0.3	7	
ILIM, SS, RT, FB(4) to GND		–0.3	3.6	
T_J	Maximum junction temperature(5)	–40	150	°C
T_{stg}	Storage temperature range	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Fixed output versions.
(4) Adjustable output version.
(5) High junction temperatures degrade operating lifetime. Operating lifetime is derated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)(2)		±2000	V
		Charged device model (CDM), per AEC Q100-011(3)	Corner pins (SW, RT, PGOOD, GND)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).

	PARAMETER	MIN	NOM	MAX	UNIT
Input voltages	VIN	3		65	V
	EN	–0.3		V_{VIN}	
	PGOOD	–0.3		12	
	HYS	–0.3		5	
Output current	I_{OUT} (COT mode)	0		150	mA
	I_{OUT} (PFM mode)	0		100	mA
Temperature	Operating junction temperature(2)	–40		150	°C

(1) Operating Ratings are conditions under which the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC(1)		LM5165-Q1	UNIT
		VSON	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	22.1	
Ψ_{JT}	Junction-to-top characterization parameter	1.0	
Ψ_{JB}	Junction-to-board characterization parameter	22.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to +125°C junction temperature range. V_{IN} = 12 V (unless otherwise noted).(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
$I_{Q\text{-}SHD}$	VIN DC supply current, shutdown	V_{EN} = 0 V, T_A = 25°C		4.6	6.0	µA
$I_{Q\text{-}SLEEP}$	VIN DC supply current, no load	V_{FB} = 1.5 V, T_A = 25°C		10.5	15.0	
$I_{Q\text{-}SLEEP\text{-}VINMAX}$	VIN DC supply current, no load, VIN = 65V	V_{FB} = 1.5 V, V_{VIN} = 65 V, T_A = 25°C		11.0	15.0	
$I_{Q\text{-}ACTIVE\text{-}PFM}$	VIN DC supply current, active	PFM mode		205		
$I_{Q\text{-}ACTIVE\text{-}COT}$	VIN DC supply current, active	COT mode, R_{RT} = 107 kΩ		300		
POWER SWITCHES						
R_{DSON1}	High-side MOSFET $R_{DS(on)}$	I_{SW} = –10 mA		2		Ω
R_{DSON2}	Low-side MOSFET $R_{DS(on)}$	I_{SW} = 10 mA		1		
CURRENT LIMITING						
I_{LIM1}	High-side peak current current threshold	ILIM shorted to GND	220	240	264	mA
I_{LIM2}		R_{ILIM} = 24.9 kΩ	155	180	205	
I_{LIM3}		R_{ILIM} = 56.2 kΩ	100	120	145	
I_{LIM4}		R_{ILIM} = 100 kΩ	48	60	75	
REGULATION COMPARATOR						
V_{VOUT50}	VOUT 5V DC setpoint	LM5165X	4.9	5.0	5.1	V
V_{VOUT33}	VOUT 3.3V DC setpoint	LM5165Y	3.23	3.30	3.37	

(1) All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \bullet \theta_{JA})$ where θ_{JA} (in °C/W) is the package thermal impedance provided in the *Thermal Information* section.

Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to +125°C junction temperature range. V_{IN} = 12 V (unless otherwise noted).(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VOUT}	VOUT pin input current	V_{VOUT} = 5 V, LM5165X-Q1		6.7		µA
		V_{VOUT} = 3.3 V, LM5165Y-Q1		3.9		
V_{REF1}	Lower FB regulation threshold (PFM, COT)	Adjustable output version	1.205	1.223	1.241	V
V_{REF2}	Upper FB regulation threshold (PFM)		1.220	1.233	1.246	
$FB_{HYS-PFM}$	FB comparator PFM hysteresis	PFM mode		10		mV
$FB_{HYS-COT}$	FB comparator dropout hysteresis	COT mode		4		
I_{FB}	FB pin input bias current	V_{FB} = 1 V			100	nA
$FB_{LINE-REG}$	FB threshold variation over line	V_{VIN} = 3 V to 65 V		0.001		%/V
$VOUT_{LINE-REG}$	VOUT threshold variation over line	LM5165X-Q1, V_{VIN} = 6 V to 65 V LM5165Y-Q1, V_{VIN} = 4.5 V to 65 V		0.001		
POWER GOOD						
UVT_{RISING}	PGOOD comparator	FB voltage rising, relative to V_{REF1}		94%		
$UVT_{FALLING}$		FB voltage falling, relative to V_{REF1}		87%		
R_{PGOOD}	PGOOD on-resistance	V_{FB} = 1 V		80	200	Ω
$V_{INMIN-PGOOD}$	Minimum VIN for valid PGOOD	VIN falling, I_{PGOOD} = 0.1 mA, V_{PGOOD} < 0.5 V		1.20	1.65	V
I_{PGOOD}	PGOOD off-state leakage current	V_{FB} = 1.2 V, V_{PGOOD} = 5.5 V		10	100	nA
ENABLE / UVLO						
V_{IN-ON}	Turn-on threshold	VIN voltage rising	2.60	2.75	2.95	V
V_{IN-OFF}	Turn-off threshold	VIN voltage falling	2.35	2.45	2.60	V
V_{EN-ON}	Enable turn-on threshold	EN voltage rising	1.163	1.212	1.262	V
V_{EN-OFF}	Enable turn-off threshold	EN voltage falling	1.109	1.144	1.178	V
V_{EN-HYS}	Enable hysteresis			68		mV
V_{EN-SD}	EN shutdown threshold	EN voltage falling	0.3	0.6		V
R_{HYS}	HYS on-resistance	V_{EN} = 1 V		80	200	Ω
I_{HYS}	HYS off-state leakage current	V_{EN} = 1.5 V, V_{HYS} = 5.5 V		10	100	nA
SOFT-START						
I_{SS}	Soft-start charging current	V_{SS} = 1 V		10		µA
T_{SS-INT}	Soft-start rise time	SS floating		900		µs
THERMAL SHUTDOWN						
T_{J-SD}	Thermal shutdown threshold			170		°C
$T_{J-SD-HYS}$	Thermal shutdown hysteresis			10		

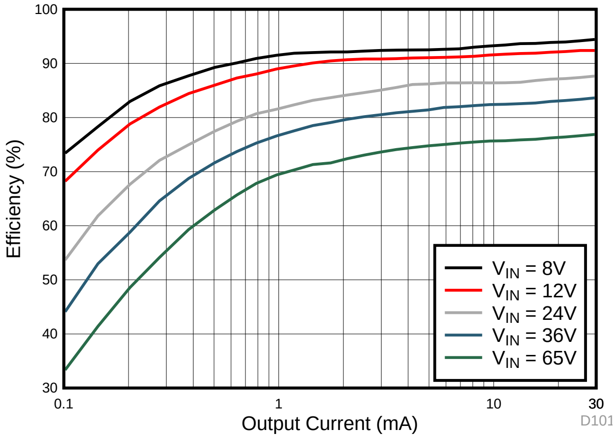
6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{ON-MIN}	Minimum controllable PWM on-time			180		ns
T_{ON1}	PWM on-time	16 kΩ from RT to GND		250		ns
T_{ON2}	PWM on-time	75 kΩ from RT to GND		1000		ns

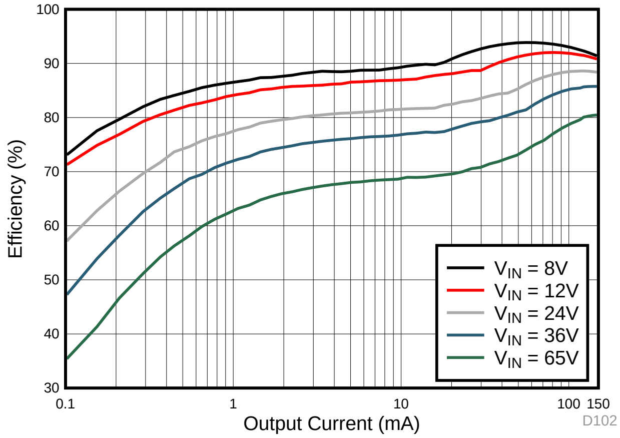
6.7 Typical Characteristics

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to the *Typical Applications* section for circuit designs.



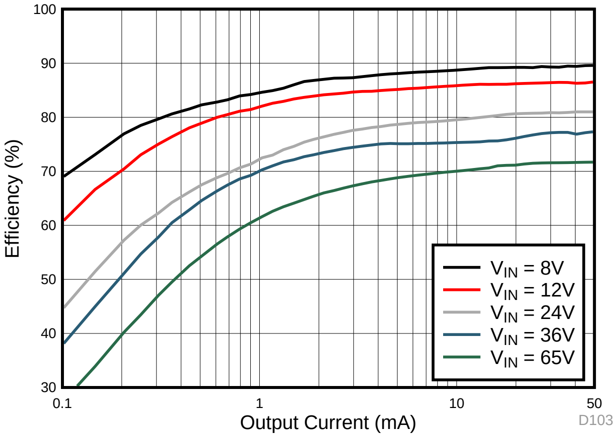
5-V, 25-mA Design
L_F = 470 µH
C_{OUT} = 47 µF
$F_{SW(nom)}$ = 100 kHz
R_{ILIM} ≥ 100 kΩ

Figure 1. Converter Efficiency: 5 V, 25 mA, PFM



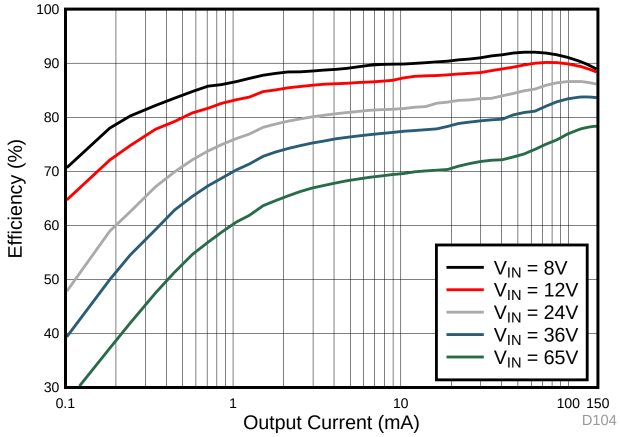
See schematic, Figure 37
L_F = 220 µH
C_{OUT} = 22 µF
$F_{SW(nom)}$ = 230 kHz
R_{RT} = 133 kΩ

Figure 2. Converter Efficiency: 5 V, 150 mA, COT



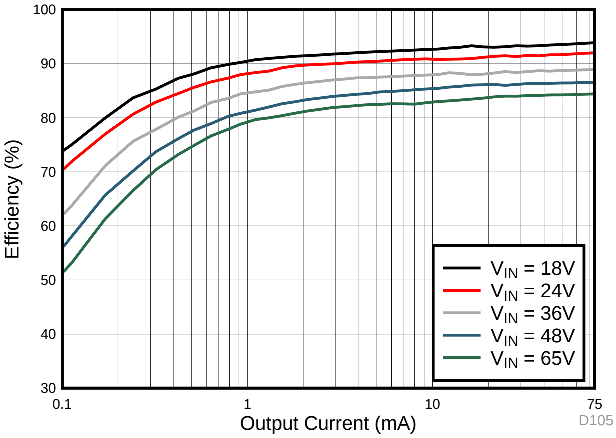
See schematic, Figure 50
L_F = 47 µH
C_{OUT} = 10 µF
$F_{SW(nom)}$ = 350 kHz
R_{ILIM} = 56.2 kΩ

Figure 3. Converter Efficiency: 3.3 V, 50 mA, PFM



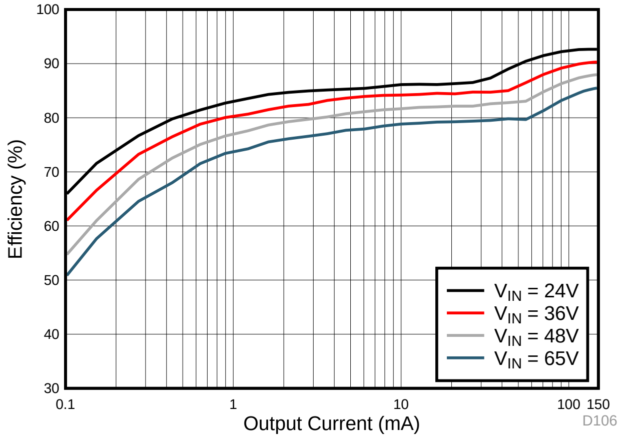
See schematic, Figure 62
L_F = 150 µH
C_{OUT} = 22 µF
$F_{SW(nom)}$ = 160 kHz
R_{RT} = 121 kΩ

Figure 4. Converter Efficiency: 3.3 V, 150 mA, COT



See schematic, Figure 57
L_F = 47 µH
C_{OUT} = 10 µF
$F_{SW(nom)}$ = 500 kHz
R_{ILIM} = 24.9 kΩ

Figure 5. Converter Efficiency: 12 V, 75 mA, PFM



See schematic, Figure 65
L_F = 150 µH
C_{OUT} = 10 µF
$F_{SW(nom)}$ = 600 kHz
R_{RT} = 143 kΩ

Figure 6. Converter Efficiency: 15 V, 150 mA, COT

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to the *Typical Applications* section for circuit designs.

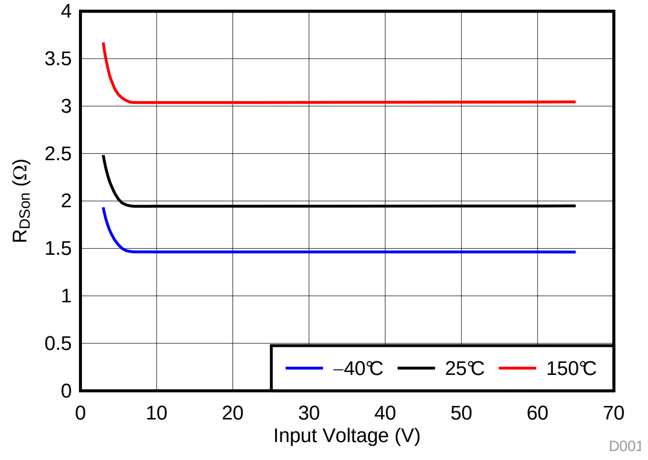


Figure 7. High-Side MOSFET On-state Resistance vs Input Voltage

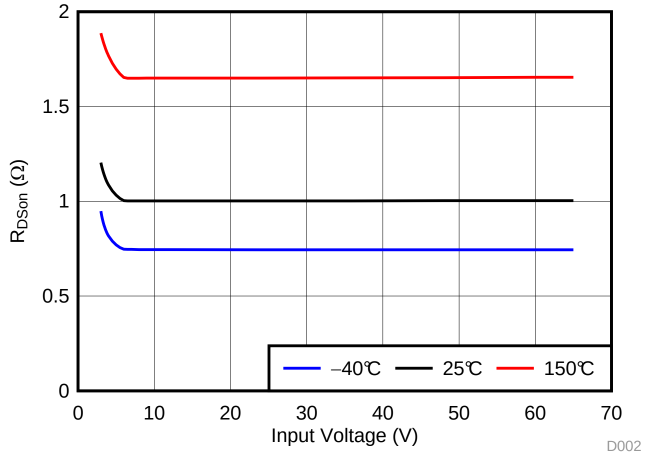


Figure 8. Low-Side MOSFET On-state Resistance vs Input Voltage

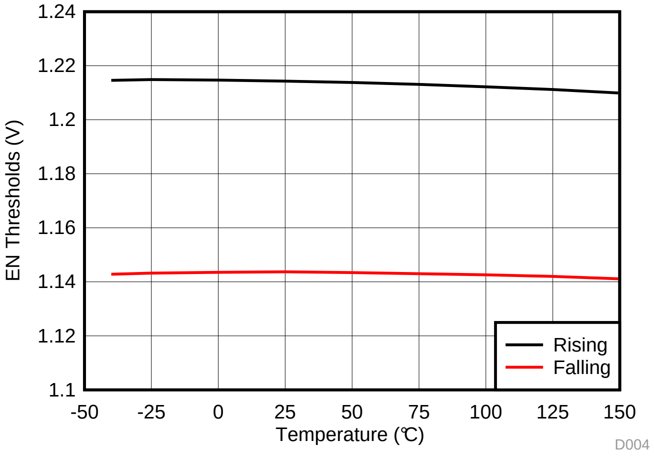


Figure 9. Enable Threshold Voltage vs Temperature

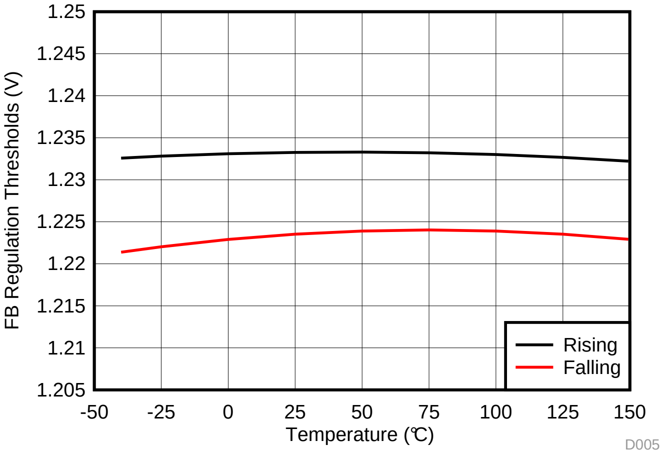
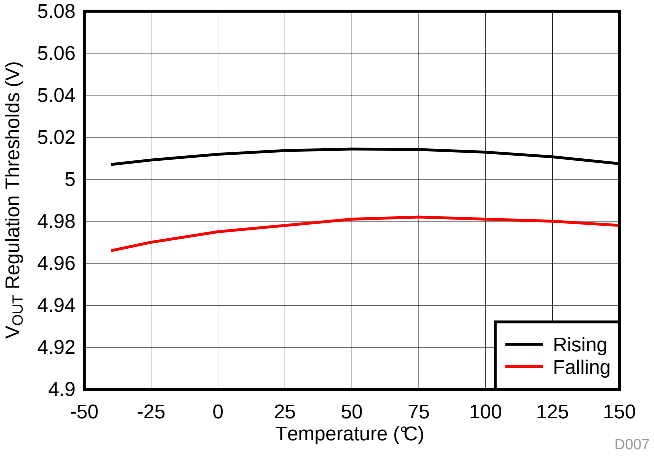
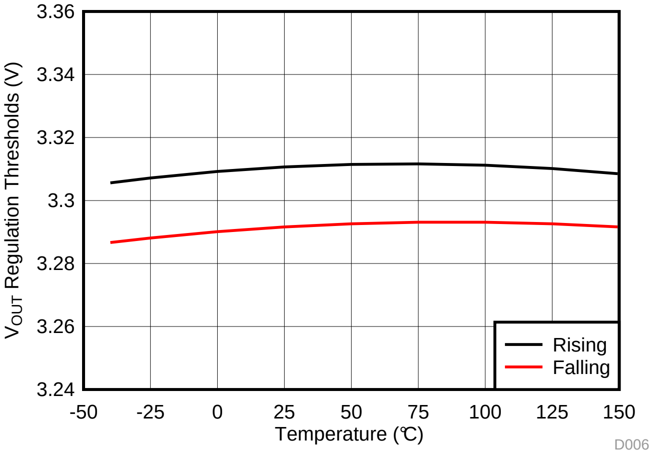


Figure 10. Feedback Comparator Voltage vs Temperature



LM5165X

Figure 11. VOUT Regulation Thresholds vs Temperature



LM5165Y

Figure 12. VOUT Regulation Thresholds vs Temperature

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to the *Typical Applications* section for circuit designs.

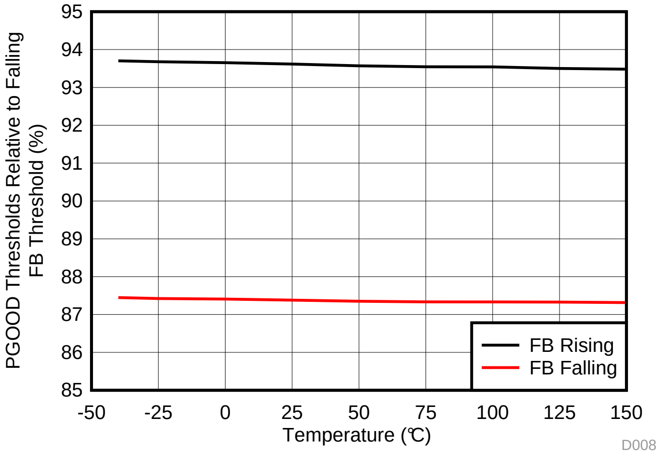


Figure 13. PGOOD Thresholds vs Temperature

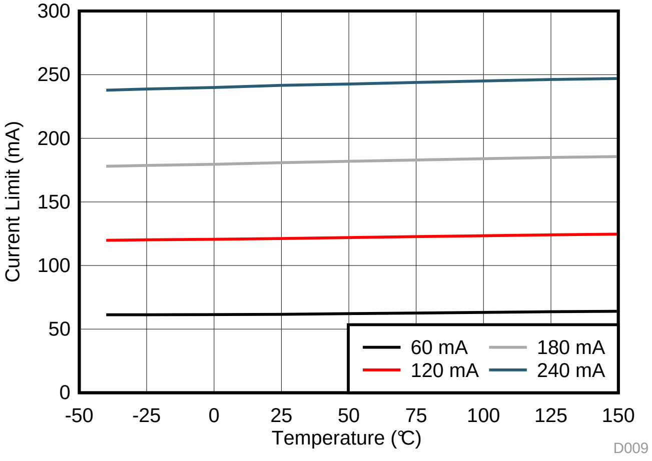


Figure 14. Peak Current Limits vs Temperature

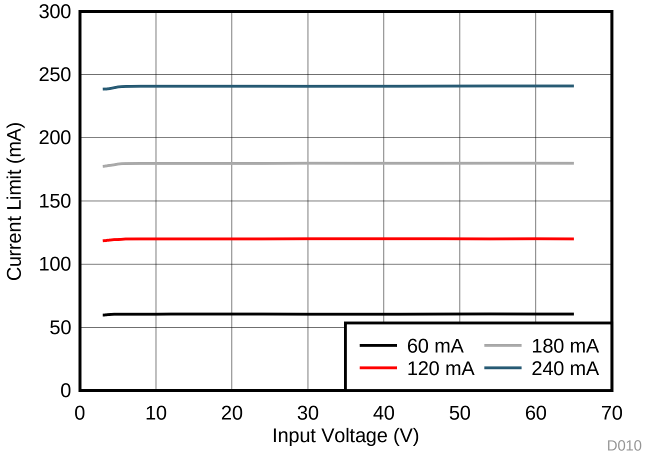


Figure 15. Peak Current Limits vs Input Voltage

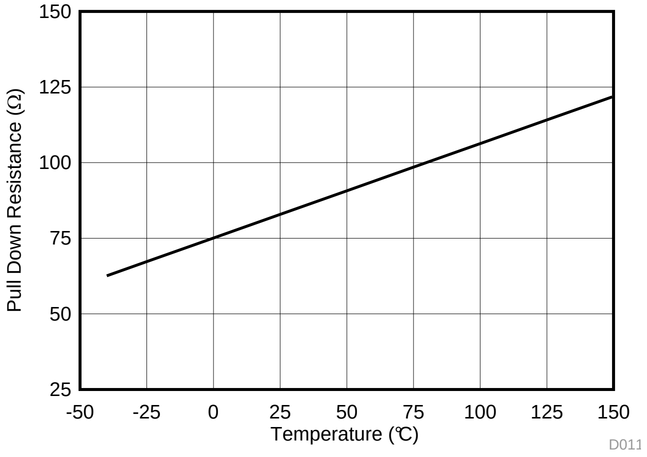


Figure 16. PGOOD and HYS Pulldown $R_{DS(on)}$ vs Temperature

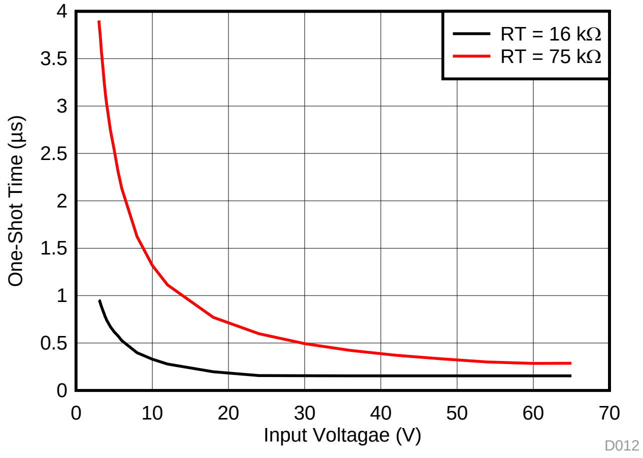


Figure 17. COT One-shot Timer T_{ON} vs Input Voltage

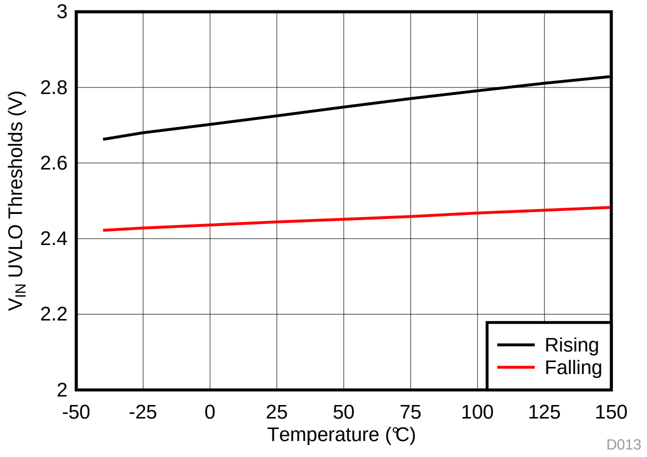


Figure 18. Internal V_{IN} UVLO Voltage vs Temperature

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to the *Typical Applications* section for circuit designs.

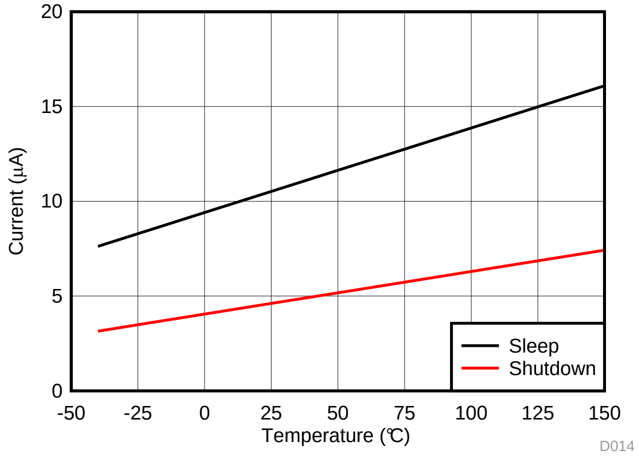


Figure 19. VIN Sleep and Shutdown Supply Current vs Temperature

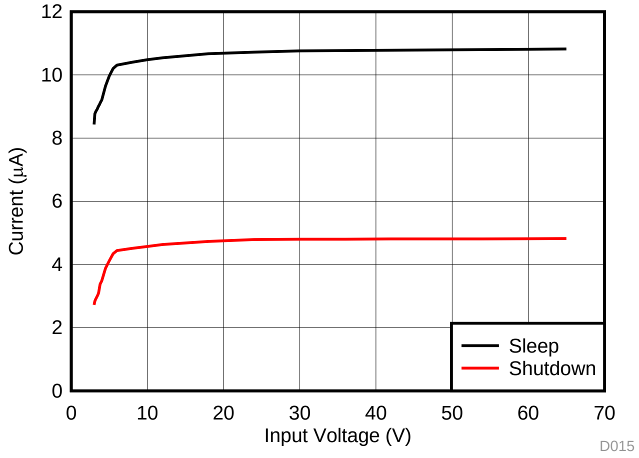
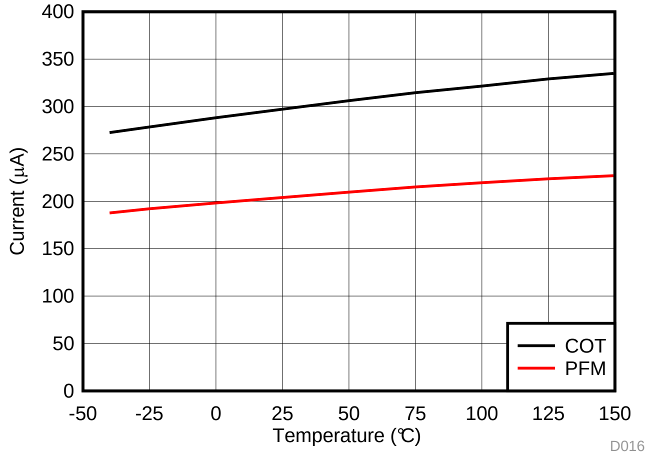
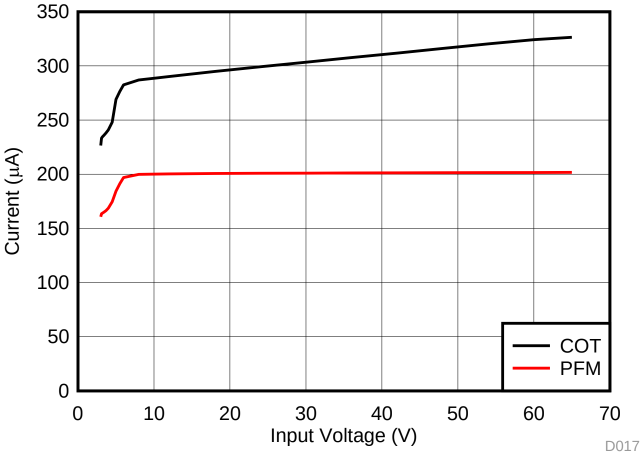


Figure 20. VIN Sleep and Shutdown Supply Current vs Input Voltage



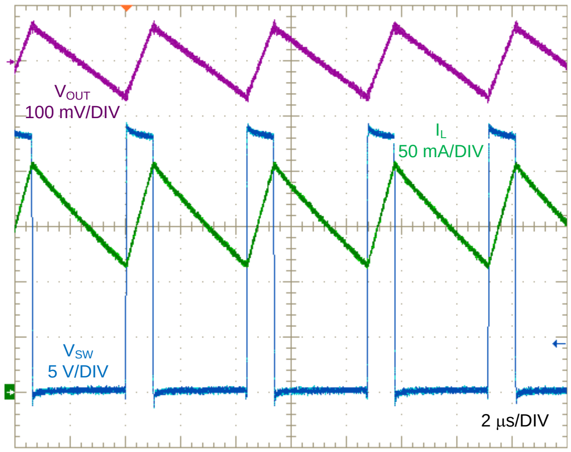
R_{RT} = 75 kΩ

Figure 21. VIN Active Mode Supply Current vs Temperature



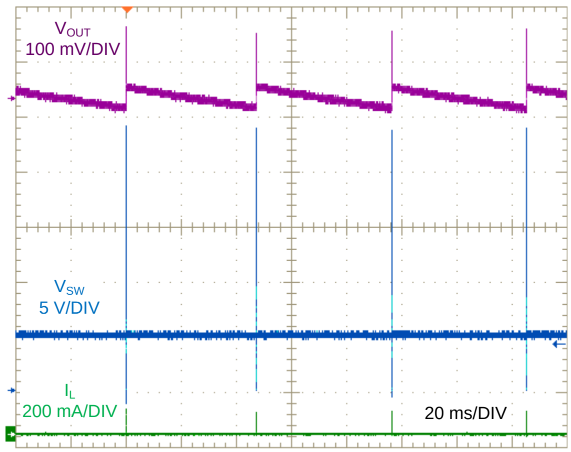
R_{RT} = 75 kΩ

Figure 22. VIN Active Mode Supply Current vs Input Voltage



5-V, 150-mA Design

Figure 23. Full Load Switching Waveforms, COT

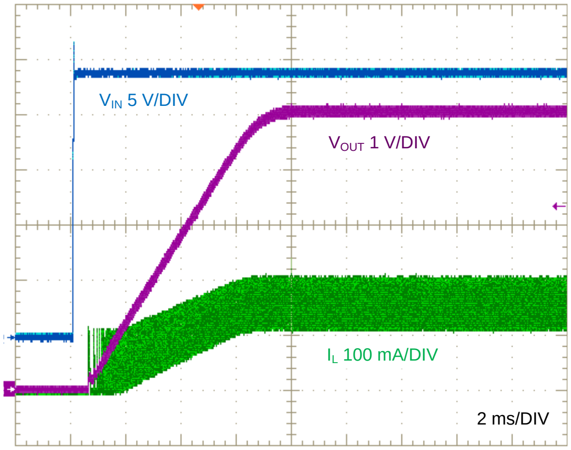


5-V, 150-mA Design

Figure 24. No Load Switching Waveforms, COT

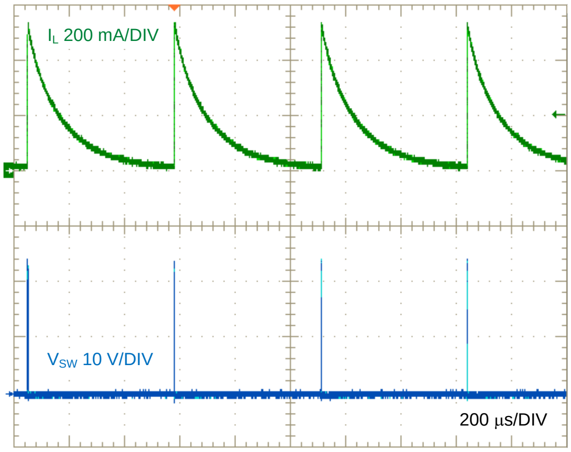
Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to the *Typical Applications* section for circuit designs.



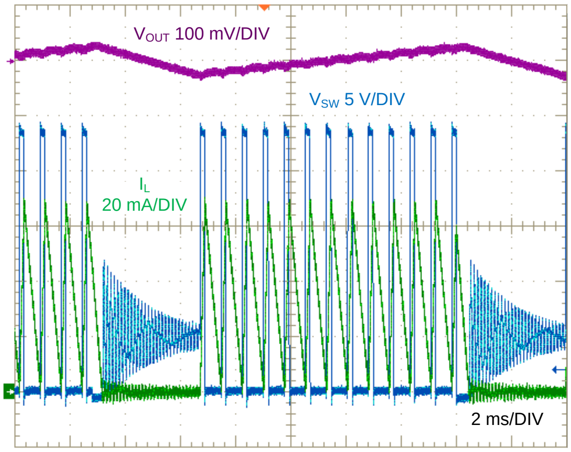
5-V, 150-mA Design

Figure 25. Full Load Startup, COT



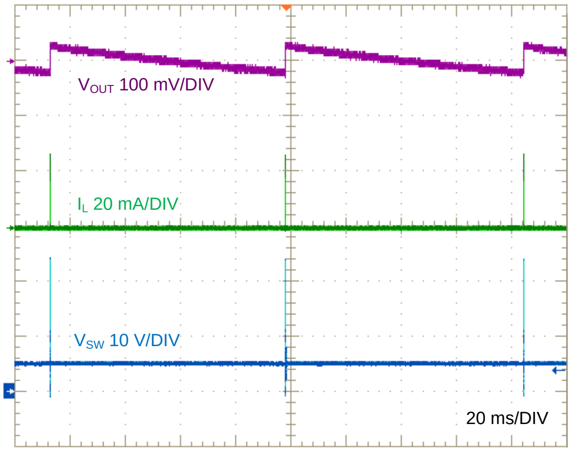
5-V, 150-mA Design

Figure 26. Short Circuit, COT



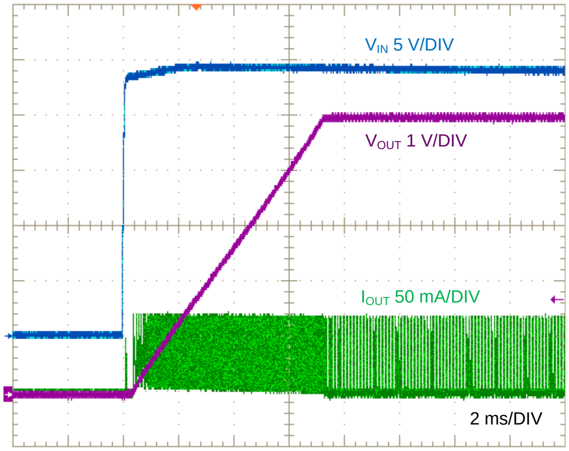
5-V, 25-mA Design

Figure 27. Full Load Switching Waveforms, PFM



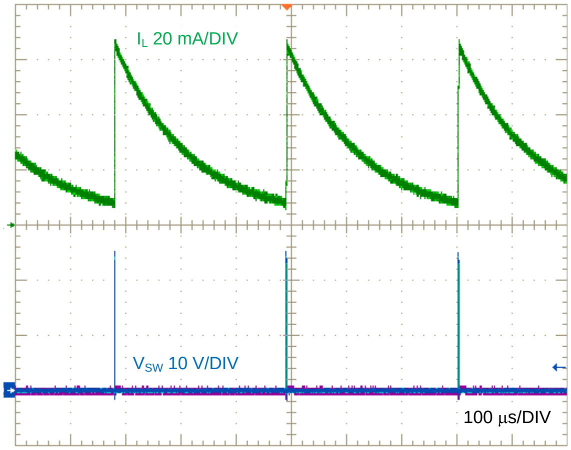
5-V, 25-mA Design

Figure 28. No Load Switching Waveforms, PFM



5-V, 25-mA Design

Figure 29. Full Load Startup, PFM



5-V, 25-mA Design

Figure 30. Short Circuit, PFM

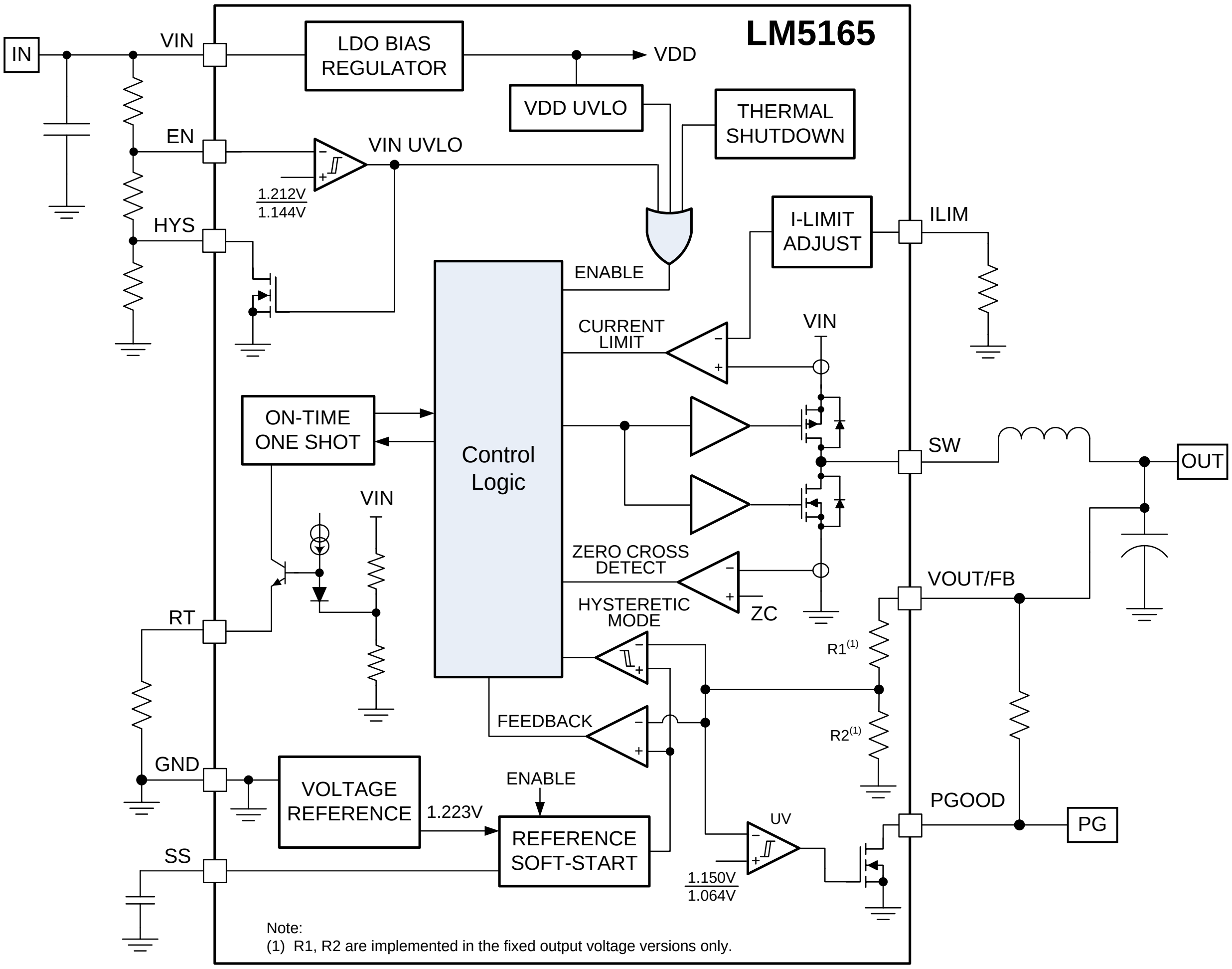
7 Detailed Description

7.1 Overview

The LM5165-Q1 converter is an easy-to-use synchronous buck DC/DC regulator that operates from a 3-V to 65-V supply voltage. The device is intended for step-down conversions from 3.3-V, 5-V, 12-V, 24-V, and 48-V unregulated, semi-regulated and fully-regulated supply rails. With integrated high-side and low-side power MOSFETs, the LM5165-Q1 delivers up to 150-mA DC load current with high efficiency and ultra-low input quiescent current in a very small solution size. Designed for simple implementation, a choice of operating modes offers flexibility to optimize its usage according to the target application. In constant on-time (COT) mode of operation, ideal for low-noise, high current, fast load transient requirements, the device operates with predictive on-time switching pulse. A quasi-fixed switching frequency over the input voltage range is achieved by using an input voltage feedforward to set the on-time. Alternatively, pulse frequency modulation (PFM) mode, complemented by an adjustable peak current limit, achieves exceptional light-load efficiency performance. Control loop compensation is not required with either operating mode, reducing design time and external component count.

The LM5165-Q1 incorporates other features for comprehensive system requirements, including an open-drain Power Good circuit for power-rail sequencing and fault reporting, internally-fixed or externally-adjustable soft-start, monotonic startup into prebiased loads, precision enable with customizable hysteresis for programmable line undervoltage lockout (UVLO), adjustable cycle-by-cycle current limit for optimal inductor sizing, and thermal shutdown with automatic recovery. These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple *PCB Layout*, requiring only a few external components.

7.2 Functional Block Diagram



Note:
(1) R1, R2 are implemented in the fixed output voltage versions only.

7.3 Feature Description

7.3.1 Integrated Power MOSFETs

The LM5165-Q1 is a step-down buck converter with integrated high-side PMOS buck switch and low-side NMOS synchronous switch. During the high-side MOSFET on-time, the SW voltage V_{SW} swings up to approximately V_{IN}, and the inductor current increases with slope $(V_{IN} – V_{OUT})/L_F$. When the high-side MOSFET is turned off by the control logic, the low-side MOSFET turns on after an adaptive deadtime. Inductor current flows through the low-side MOSFET with slope $–V_{OUT}/L_F$. Duty cycle D is defined as T_{ON}/T_{SW}, where T_{ON} is the high-side MOSFET conduction time and T_{SW} is the switching period.

7.3.2 Selectable PFM or COT Mode Converter Operation

Figure 31 and Figure 32 show converter schematics for PFM and COT modes of operation.

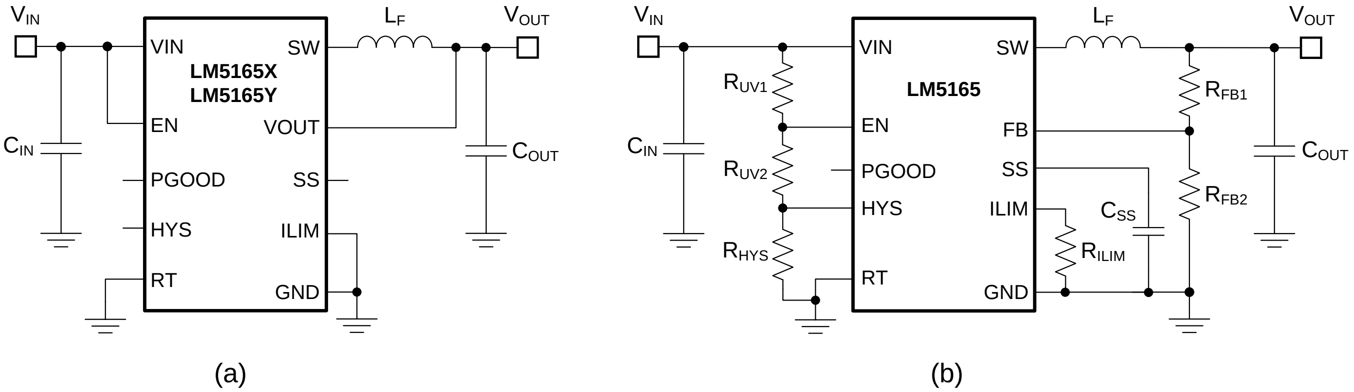


Figure 31. PFM Mode Converter Schematics: (a) Fixed Output Voltage of 5 V or 3.3 V, (b) Adjustable Output Voltage with Programmable Soft Start, Current Limit and UVLO

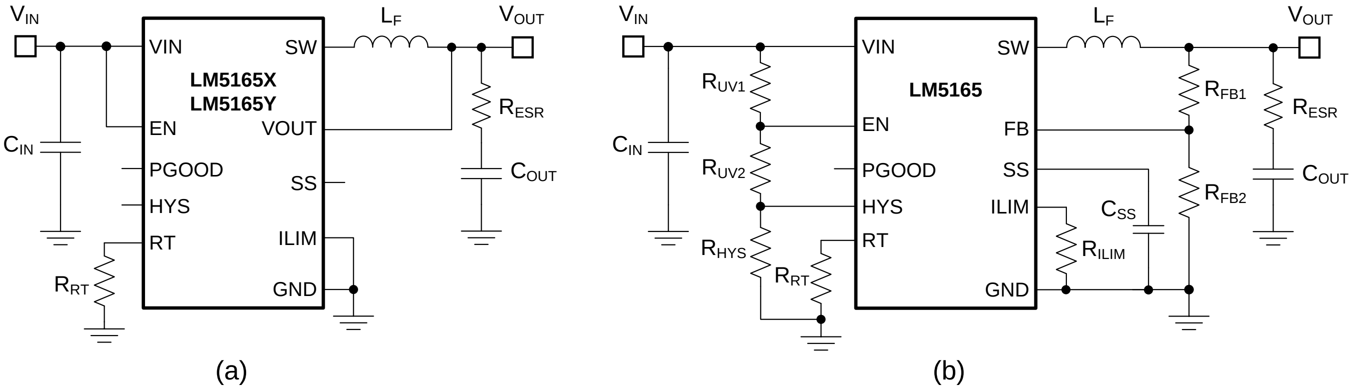


Figure 32. COT Mode Converter Schematics: (a) Fixed Output Voltage of 5 V or 3.3 V, (b) Adjustable Output Voltage with Programmable Soft Start, Current Limit and UVLO

The LM5165-Q1 operates in PFM mode when RT is shorted to GND. Configured as such, the LM5165-Q1 behaves as a hysteretic voltage regulator operating in boundary conduction mode, controlling the output voltage within upper and lower hysteresis levels according to the PFM feedback comparator hysteresis of 10 mV. Figure 33 is a representation of the relevant output voltage and inductor current waveforms. The LM5165-Q1 provides the required switching pulses to recharge the output capacitor, followed by a sleep period where most of the internal circuits are shut off. The load current is supported by the output capacitor during this time, and the LM5165-Q1 current consumption approaches the sleep quiescent current of 10.5 µA. The sleep period duration depends on load current and output capacitance.

Feature Description (continued)

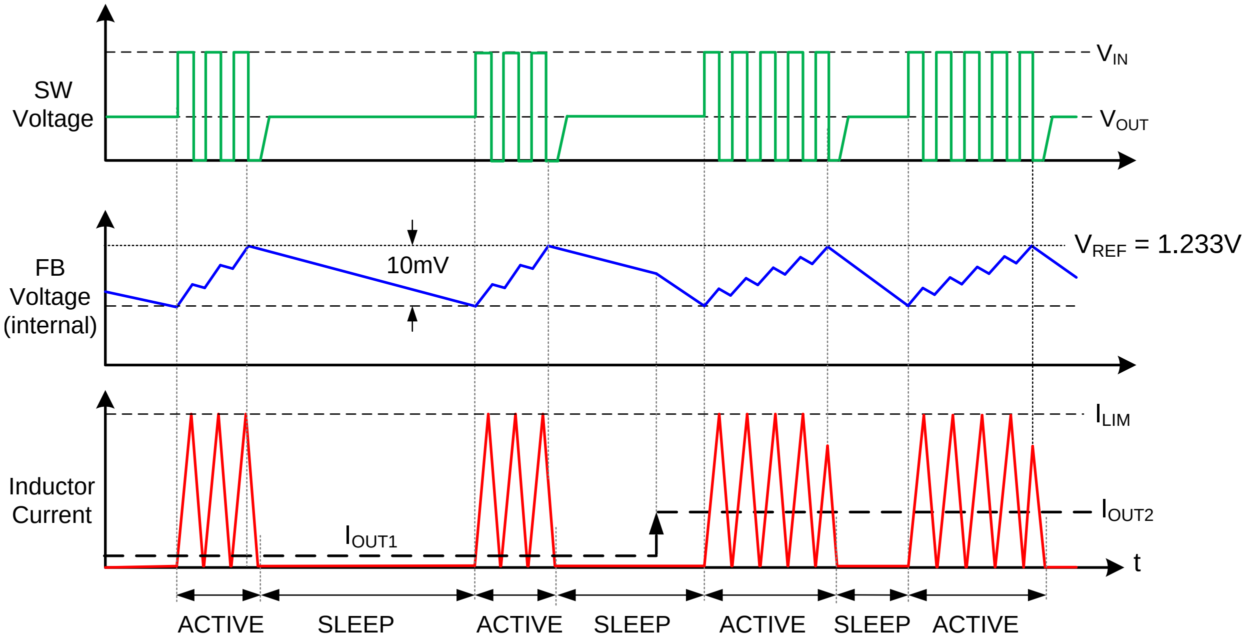


Figure 33. PFM Mode SW Node Voltage, Feedback Voltage and Inductor Current Waveforms

When operating in PFM mode at given input and output voltages, the chosen filter inductance dictates the PFM pulse frequency as

$$F_{SW(PFM)} = \frac{V_{OUT}}{L_F \cdot I_{PK(PFM)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{1}$$

where $I_{PK(PFM)}$ corresponds to one of the four programmable levels for peak limit of inductor current. See the *Adjustable Current Limit* section for more detail.

Configured in COT mode, the LM5165-Q1 based converter turns on the high-side MOSFET with on-time inversely proportional to V_{IN} to operate with essentially fixed switching frequency when in continuous conduction mode (CCM). Diode emulation mode (DEM) prevents negative inductor current, and pulse skipping maintains highest efficiency at light load currents by decreasing the effective switching frequency. The COT-controlled LM5165-Q1 waveforms in CCM and DEM are represented in Figure 34. The PWM on-time is set by resistor R_{RT} connected from RT to GND as shown in Figure 32. The control loop maintains a constant output voltage by adjusting the PWM off-time.

Feature Description (continued)

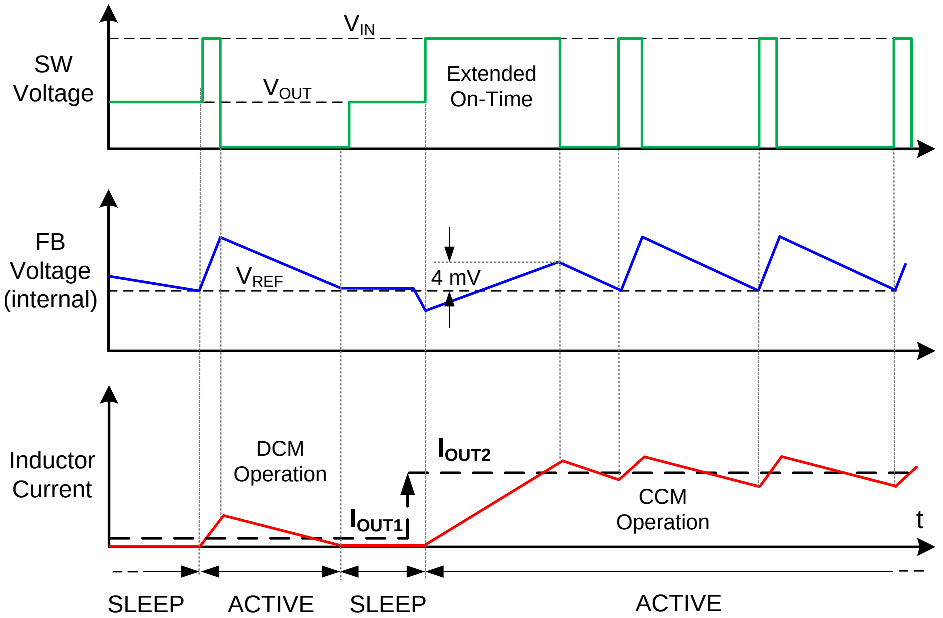


Figure 34. COT Mode SW Node Voltage, Feedback Voltage and Inductor Current Waveforms

The required on-time adjust resistance for a particular frequency is given in Equation 2 and tabulated in Table 1. The maximum programmable on-time is 15 µs.

$$R_{RT}\left[k\Omega\right] = \frac{V_{OUT}\left[V\right]}{F_{SW}\left[kHz\right]} \cdot \frac{10^4}{1.6} \tag{2}$$

Table 1. On-Time Adjust Resistance (E96 EIA Values) for Various Switching Frequencies and Output Voltages

F_{SW} (kHz)	R_{RT} (kΩ)			
	V_{OUT} = 1.8 V	V_{OUT} = 3.3 V	V_{OUT} = 5 V	V_{OUT} = 12 V
100	113	205	316	750
200	56.2	105	154	374
300	37.3	68.1	105	249
400	28	51.1	78.7	187
500	23.2	41.2	61.9	150
600	20	34	52.3	124

The choice of control mode and switching frequency requires a compromise between conversion efficiency, quiescent current, and passive component size. Lower switching frequency implies reduced switching losses (including gate charge losses, transition losses, etc.) and higher overall efficiency. Higher switching frequency, on the other hand, implies a smaller LC output filter and hence a more compact design. Lower inductance also helps transient response as the large-signal slew rate of inductor current increases. The ideal switching frequency in a given application is a tradeoff and thus is determined on a case-by-case basis. It relates to the input voltage, output voltage, most frequent load current level(s), external component choices, and circuit size requirement. At light loads, the PFM converter has a relatively longer sleep time interval and thus operates with lower input quiescent current and higher efficiency.

7.3.3 COT Mode Light-Load Operation

Diode emulation mode (DEM) operation occurs when the low-side MOSFET switches off as inductor valley current reaches zero. Here, the load current is less than half of the peak-to-peak inductor current ripple in CCM. Turning off the low-side MOSFET at zero current reduces switching loss, and preventing negative current conduction reduces conduction loss. Power conversion efficiency is thus higher in a DEM converter than an equivalent forced-PWM CCM converter. With DEM operation, the duration that both power MOSFETs remain off progressively increases as load current decreases.

7.3.4 Low Dropout Operation and 100% Duty Cycle Mode

If R_{DSON1} and R_{DSON2} are the high-side and low-side MOSFET on-state resistances, respectively, and R_{DCR} is the inductor DC resistance, the duty cycle in COT (CCM) or PFM mode is given by Equation 3.

$$D = \frac{V_{OUT} + \left(R_{DSON2} + R_{DCR}\right) \cdot I_{OUT}}{V_{IN} - \left(R_{DSON1} - R_{DSON2}\right) \cdot I_{OUT}} \approx \frac{V_{OUT}}{V_{IN}} \quad (3)$$

The LM5165-Q1 offers a low input voltage to output voltage dropout by engaging the high-side MOSFET at 100% duty cycle. In COT mode, a frequency foldback feature effectively extends maximum duty cycle to 100% during low dropout conditions or load-on transients. Based on the 4-mV FB comparator dropout hysteresis, the duty cycle extends as needed at low input voltage conditions, corresponding to lower switching frequency. The PWM on-time extends based on the requirement that the FB voltage exceeds the dropout hysteresis during a given on-time. 100% duty cycle operation is eventually reached as the input voltage decreases towards the output setpoint. The output voltage stays in regulation at a lower supply voltage, thus achieving an extremely low dropout voltage.

Note that PFM mode operation provides an inherently natural transition to 100% duty cycle if needed for low dropout applications.

Use Equation 4 to calculate the minimum input voltage to maintain output regulation.

$$V_{IN(min)} = V_{OUT} + I_{OUT} \cdot \left(R_{DSON1} + R_{DCR}\right) \quad (4)$$

7.3.5 Adjustable Output Voltage (FB)

Three voltage feedback options are available: the fixed 3.3-V and 5-V versions include internal feedback resistors that sense the output directly through the VOUT pin; the adjustable voltage option senses the output through an external resistor divider connected from the output to the FB pin.

The LM5165-Q1 voltage regulation loop regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage, V_{REF1}. A resistor divider programs the ratio from output voltage V_{OUT} to FB. For a target V_{OUT} setpoint, calculate R_{FB2} based on the selected R_{FB1} using Equation 5.

$$R_{FB2} = \frac{1.223V}{V_{OUT} - 1.223V} \cdot R_{FB1} \quad (5)$$

Selecting R_{FB1} of 100 kΩ is recommended for most applications. A larger R_{FB1} consumes less DC current, mandatory if light-load efficiency is critical. High feedback resistances generally require more careful feedback path PCB layout. It is important to route the feedback trace away from the noisy area of the PCB. For more layout recommendations, please refer to the *PCB Layout* section.

7.3.6 Adjustable Current Limit

The LM5165-Q1 manages overcurrent conditions by cycle-by-cycle current limiting of the peak inductor current. The current sensed in the high-side MOSFET is compared every switching cycle to the current limit threshold set by the ILIM pin. Current is sensed after a leading-edge blanking time following the high-side MOSFET turn-on transition. The propagation delay of current limit comparator is 100 ns.

Four programmable peak current levels are available: 60 mA, 120 mA, 180 mA and 240 mA, corresponding to resistors of 100 kΩ, 56.2 kΩ, 24.9 kΩ and 0 Ω connected at the ILIM pin, respectively. In turn, 25mA, 50mA, 75mA and 100mA output current levels in boundary conduction mode PFM operation are possible, respectively.

Note that in PFM mode, the inductor current ramps from zero to the chosen peak threshold every switching cycle. Consequently, the maximum output current is equal to half the peak inductor current. Meanwhile, the corresponding output current capability in COT mode is higher as the ripple current is determined by the input and output voltage and the chosen inductance.

7.3.7 Precision Enable (EN) and Hysteresis (HYS)

The precision EN input supports adjustable input undervoltage lockout (UVLO) with hysteresis programmed independently via the HYS pin for application specific power-up and power-down requirements. EN connects to a comparator-based input referenced to a 1.212-V bandgap voltage with 68-mV hysteresis. An external logic signal can be used to drive the EN input to toggle the output on and off and for system sequencing or protection. The simplest way to enable the LM5165's operation is to connect EN directly to VIN. This allows self-startup of the LM5165-Q1 when V_{IN} is within its valid operating range. However, many applications benefit from using a resistor divider R_{UV1} and R_{UV2} as shown in Figure 35 to establish a precision UVLO level. In tandem with the EN setting, use HYS to increase the voltage hysteresis as needed.

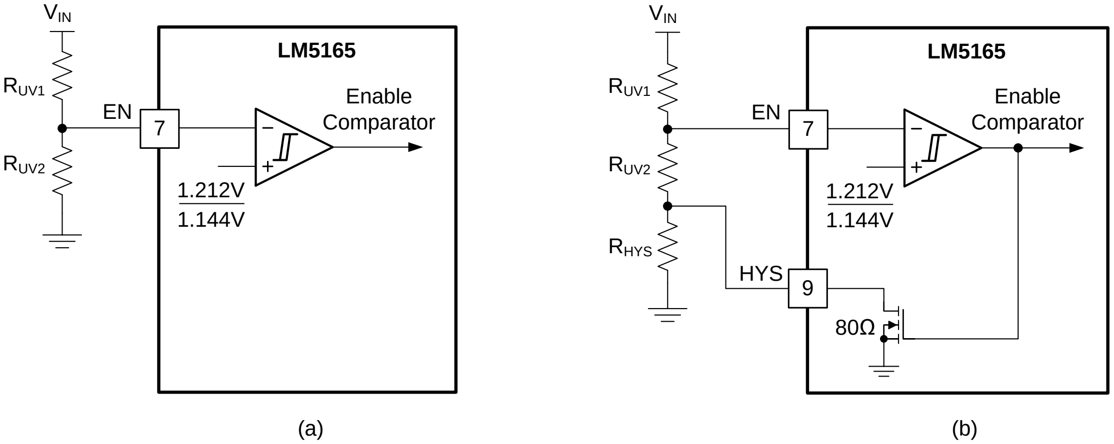


Figure 35. Programmable Input Voltage UVLO with (a) Fixed Hysteresis, (b) Adjustable Hysteresis

Use Equation 6 and Equation 7 to calculate the input UVLO voltages turn-on and turn-off voltages, respectively.

$$V_{IN(on)} = 1.212V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) \tag{6}$$

$$V_{IN(off)} = 1.144V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2} + R_{HYS}}\right) \tag{7}$$

There is also a low I_Q shutdown mode when EN is pulled below a base-emitter voltage drop (approximately 0.6 V at room temperature). If EN is below this hard shutdown threshold, the internal LDO regulator powers off and the internal bias supply rail collapses, shutting down the bias currents of the LM5165-Q1. The LM5165-Q1 operates in standby mode when the EN voltage is between the hard shutdown and precision enable thresholds.

7.3.8 Power Good (PGOOD)

The LM5165-Q1 provides a PGOOD flag pin to indicate when the output voltage is within the regulation level. Use the PGOOD signal for startup sequencing of downstream converters, as shown in Figure 36, or for fault protection and output monitoring. PGOOD is an open-drain output that requires a pull-up resistor to a DC supply not greater than 12 V. Typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pull-up rail.

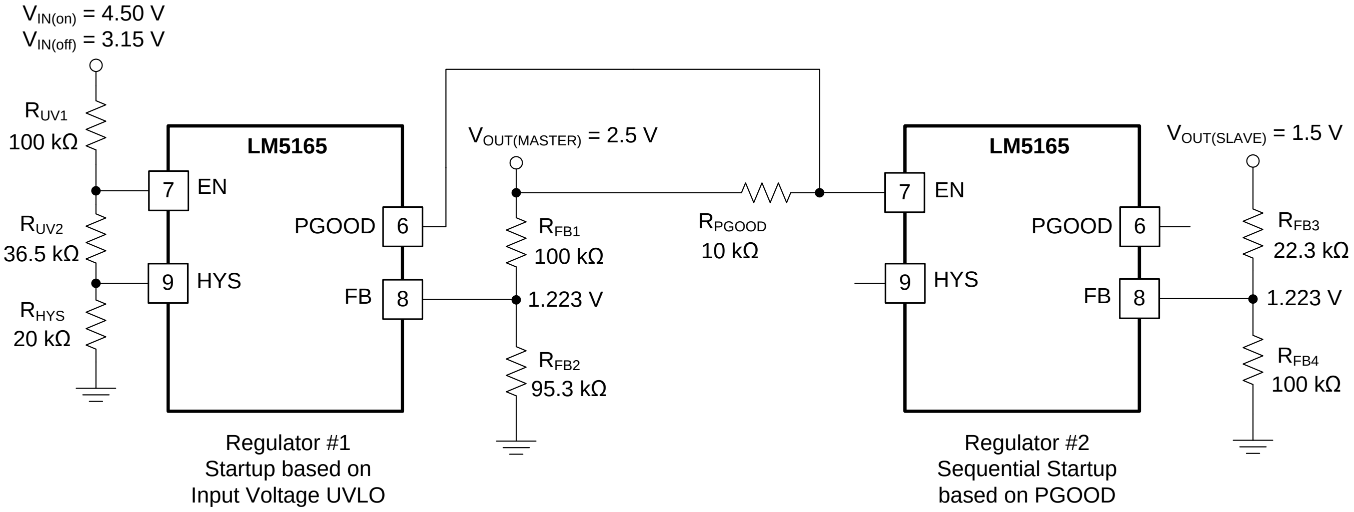


Figure 36. Master-Slave Sequencing Implementation using PGOOD and EN

When the FB voltage exceeds 94% of the internal reference V_{REF1}, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pull-up. If the FB voltage falls below 87% of V_{REF1}, the internal PGOOD switch turns on, and PGOOD is pulled low to indicate that the output voltage is out of regulation. The rising edge of PGOOD has a built-in deglitch delay of 5 µs.

7.3.9 Configurable Soft Start (SS)

The LM5165-Q1 has a flexible and easy-to-use soft start control pin, SS. The soft-start feature prevents inrush current impacting the LM5165-Q1 and the input supply when power is first applied. Soft start is achieved by slowly ramping up the target regulation voltage when the device is first enabled or powered up. Selectable/adjustable startup timing options include minimum delay (no soft-start), 900-µs internally fixed soft start, and an externally programmable soft start.

The simplest way to use the LM5165-Q1 is to leave the SS pin open. The LM5165-Q1 employs the internal soft-start control ramp and starts up to the regulated output voltage in 900 µs. In applications with a large amount of output capacitance, higher V_{OUT}, or other special requirements, extend the soft-start time by connecting an external capacitor C_{SS} from SS to GND. Longer soft-start time further reduces the supply current needed to charge the output capacitors and supply any output loading. An internal current source I_{SS} of 10 µA charges C_{SS} and generates a ramp to control the ramp rate of the output voltage. Use Equation 8 to calculate the C_{SS} capacitance for a desired soft start time t_{SS}.

$$C_{SS}\left[\text{nF}\right] = 8.1 \cdot t_{SS}\left[\text{ms}\right] \tag{8}$$

C_{SS} is discharged by an internal FET when V_{OUT} is shutdown by EN, UVLO or thermal shutdown.

It is desirable in some applications for the output voltage to reach its nominal setpoint in the shortest possible time. Connecting a 100-kΩ resistor from SS to GND disables the soft-start circuit, and the LM5165-Q1 operates in current limit during startup to rapidly charge the output capacitance.

As negative inductor current is prevented, the LM5165-Q1 is capable of startup into prebiased output conditions. With a prebiased output voltage, the LM5165-Q1 waits until the soft-start ramp allows regulation above the prebiased voltage and then follows the soft-start ramp to the regulation setpoint.

7.3.10 Thermal Shutdown

Thermal shutdown is an integrated self-protection to limit junction temperature and prevent damage related to over-heating. Thermal shutdown turns off the device when the junction temperature exceeds 170°C to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the LM5165-Q1 restarts when the junction temperature falls to 160°C.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides ON and OFF control for the LM5165-Q1. When V_{EN} is below approximately 0.6 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 4.6 µA at V_{IN} = 12 V. The LM5165-Q1 also employs internal bias rail undervoltage protection. If the internal bias supply voltage is below its UV threshold, the regulator remains off.

7.4.2 Standby Mode

The internal bias rail LDO has a lower enable threshold than the regulator itself. When V_{EN} is above 0.6 V and below the precision enable threshold (1.212 V typically), the internal LDO is on and regulating. The precision enable circuitry is turned on once the internal V_{CC} is above its UV threshold. The switching action and voltage regulation are not enabled until V_{EN} rises above the precision enable threshold.

7.4.3 Active Mode in COT

The LM5165-Q1 is in active mode when V_{EN} is above the precision enable threshold and the internal bias rail is above its UV threshold. In COT active mode, the LM5165-Q1 is in one of three modes depending on the load current:

1. CCM with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple;
2. Pulse skipping and diode emulation mode (DEM) when the load current is less than half of the peak-to-peak inductor current ripple in CCM operation. Refer to the *COT Mode Light-Load Operation* section for more detail;
3. Frequency foldback mode to maintain output regulation at low dropout and for improved load-on transient response. Refer to the *Low Dropout Operation and 100% Duty Cycle Mode* section for more detail.

7.4.4 Active Mode in PFM

Similarly, the LM5165-Q1 is in PFM active mode when V_{EN} and the internal bias rail are above the relevant thresholds, FB has fallen below the lower hysteresis level (V_{REF1}), and boundary conduction mode is recharging the output capacitor to the upper hysteresis level (V_{REF2}). There is a 4-µs wake-up delay from sleep to active states.

7.4.5 Sleep Mode in PFM

The LM5165-Q1 is in PFM sleep mode when V_{EN} and the internal bias rail are above the relevant threshold levels, V_{FB} has exceeded the upper hysteresis level (V_{REF2}), and the output capacitor is sourcing the load current. In PFM sleep mode, the LM5165-Q1 operates with very low quiescent current.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5165-Q1 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing of a LM5165-Q1-based converter, a comprehensive LM5165-Q1 *quick-start design tool* is available for download to assist the designer with component selection for a given application. WEBENCH® online software is also available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following sections discuss the design procedure for both COT and PFM modes using specific circuit design examples.

As mentioned previously, the LM5165-Q1 also integrates several optional features to meet system design requirements, including precision enable, UVLO, programmable soft start, programmable switching frequency in COT mode, adjustable current limit, and PGOOD indicator. Each application incorporates these features as needed for a more comprehensive design. The application circuits detailed below show LM5165-Q1 configuration options suitable for several application use cases. Please see the *LM5165EVM-HD-C50X* and *LM5165EVM-HD-P50A* EVM user's guides for more detail.

8.2 Typical Applications

8.2.1 Design 1: Wide V_{IN}, Low I_Q COT Converter Rated at 5 V, 150 mA

The schematic diagram of a 5-V, 150-mA COT converter is given in Figure 37.

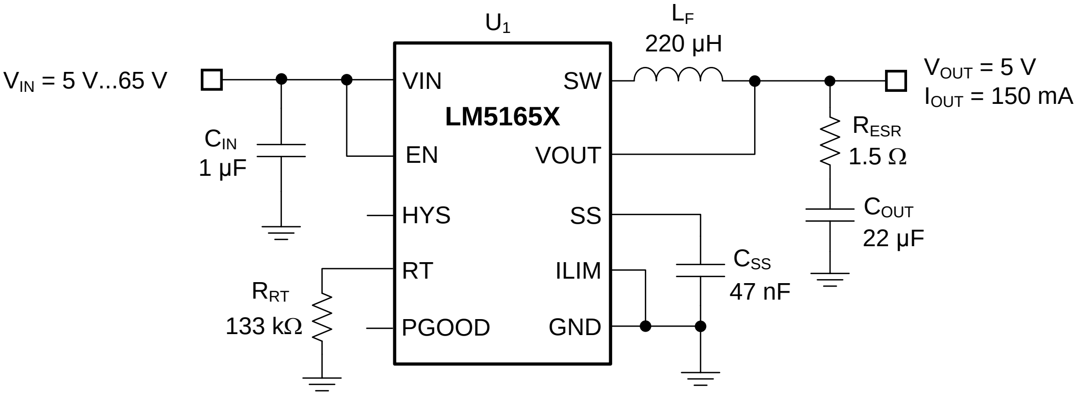


Figure 37. Schematic for Design 1 with $V_{IN(nom)}$ = 12 V, V_{OUT} = 5 V, $I_{OUT(max)}$ = 150 mA, $F_{SW(nom)}$ = 230 kHz

8.2.1.1 Design Requirements

The target full-load efficiency is 91% based on a nominal input voltage of 12 V and an output voltage of 5 V. The required input voltage range is 5 V to 65 V. The LM5165X-Q1 is chosen to deliver a fixed 5-V output voltage. The switching frequency is set by resistor R_{RT} at 230 kHz. The output voltage soft-start time is 6 ms. The required components are listed in Table 2.

Typical Applications (continued)

Table 2. List of Components for Design 1(1)

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	1 µF, 100 V, X7R, 1206 ceramic	TDK	C3216X7R2A105K160AA
C_{OUT}	1	22 µF, 10 V, X7R, 1206 ceramic	Murata	GRM31CR71A226KE15L
L_F	1	220 µH ±20%, 0.29 A, 0.92 Ω typ DCR, 5.8 x 5.8 x 2.8 mm	Würth Electronik	WE-TPC 5828 744053221
		220 µH ±30%, 0.3 A, 1.25 Ω max DCR, 5.8 x 5.8 x 3.0 mm	Bourns	SRR5028-221Y
R_{ESR}	1	1.5 Ω, 5%, 0402	Std	Std
R_{RT}	1	133 kΩ, 1%, 0402	Std	Std
C_{SS}	1	47 nF, 10 V, X7R, 0402 ceramic	Std	Std
U_1	1	LM5165X-Q1 Synchronous Buck Converter, VSON-10, 5V Fixed	TI	LM5165XQDRCRQ1

(1) See *Third-Party Products Disclaimer*.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Switching Frequency – R_T

As mentioned, the switching frequency of a COT-configured LM5165-Q1 is set by the on-time programming resistor at the RT pin. As shown by Equation 2, a standard 1% resistor of 133 kΩ gives a switching frequency of 230 kHz.

Note that at very low duty cycles, the minimum controllable on-time of the high-side MOSFET, $T_{ON(min)}$, of 180 ns may affect choice of switching frequency. In CCM, $T_{ON(min)}$ limits the voltage conversion step-down ratio for a given switching frequency. The minimum controllable duty cycle is given by

$$D_{MIN} = T_{ON(min)} \cdot F_{SW} \tag{9}$$

Given a fixed $T_{ON(min)}$, it follows that higher switching frequency implies a larger minimum controllable duty cycle. Ultimately, the choice of switching frequency for a given output voltage affects the available input voltage range, solution size and efficiency. The maximum supply voltage for a given $T_{ON(min)}$ before switching frequency reduction occurs is given by Equation 10.

$$V_{IN(max)} = \frac{V_{OUT}}{T_{ON(min)} \cdot F_{SW}} \tag{10}$$

8.2.1.2.2 Filter Inductor – L_F

The inductor ripple current (assuming CCM operation) and peak inductor current are given respectively by Equation 11 and Equation 12.

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \cdot L_F} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{11}$$

$$I_{L(peak)} = I_{OUT(max)} + \frac{\Delta I_L}{2} \tag{12}$$

For most applications, choose an inductance such that the inductor ripple current, ΔI_L, is between 30% and 50% of the rated load current at nominal input voltage. Calculate the inductance using Equation 13.

$$L_F = \frac{V_{OUT}}{F_{SW} \cdot \Delta I_{L(nom)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(nom)}}\right) \tag{13}$$

Choosing a 220-µH inductor in this design results in 55 mA peak-to-peak ripple current at nominal input voltage of 12 V, equivalent to 37% of the 150-mA rated load current. The peak inductor current at maximum input voltage of 65 V is 195 mA, sufficiently below the LM5165-Q1 peak current limit of 240 mA.

Check the inductor datasheet to ensure that the inductor's saturation current is well above the current limit setting of a particular design. Ferrite designs have low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. However, ferrite core materials exhibit a hard saturation characteristic – the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current, higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that inductor saturation current generally deceases as the core temperature increases.

8.2.1.2.3 Output Capacitors – C_{OUT}

Select the output capacitor to limit the capacitive voltage ripple at the converter output. This is the sinusoidal ripple voltage that arises from the triangular ripple current flowing in the capacitor. Select an output capacitance using Equation 14 to limit the voltage ripple component to 0.5% of the output voltage.

$$C_{OUT} \geq \frac{\Delta I_{L(nom)} \cdot 100}{F_{SW} \cdot V_{OUT}} \tag{14}$$

Substituting $\Delta I_{L(nom)}$ of 55 mA gives C_{OUT} greater than 5 µF. Mindful of the voltage coefficient of ceramic capacitors, select a 22-µF, 10-V capacitor with X7R dielectric in 1206 footprint.

8.2.1.2.4 Series Ripple Resistor – R_{ESR}

Select a series resistor such that sufficient ripple in phase with the SW node voltage appears at the feedback node, FB. Use Equation 15 to calculate the required ripple resistance, designated R_{ESR}.

$$R_{ESR} \geq \frac{20mV \cdot V_{OUT}}{V_{REF} \cdot \Delta I_{L(nom)}} \tag{15}$$

With V_{OUT} of 5 V, V_{REF} of 1.223 V, and $\Delta I_{L(nom)}$ of 55 mA at the nominal input voltage of 12 V, the required R_{ESR} is 1.5 Ω. Calculate the total output voltage ripple in CCM using Equation 16.

$$\Delta V_{OUT} = \Delta I_L \cdot \sqrt{R_{ESR}{}^2 + \left(\frac{1}{8 \cdot F_{SW} \cdot C_{OUT}}\right)^2} \tag{16}$$

8.2.1.2.5 Input Capacitor – C_{IN}

An input capacitor is necessary to limit the input ripple voltage while providing switching-frequency AC current to the buck power stage. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the VIN and GND pins of the LM5165-Q1. The input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak ripple voltage amplitude is given by Equation 17.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot C_{IN}} + D \cdot I_{OUT} \cdot R_{ESR} \tag{17}$$

The input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}, is given by Equation 18.

$$C_{IN} \geq \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot (\Delta V_{IN} - D \cdot I_{OUT} \cdot R_{ESR})} \tag{18}$$

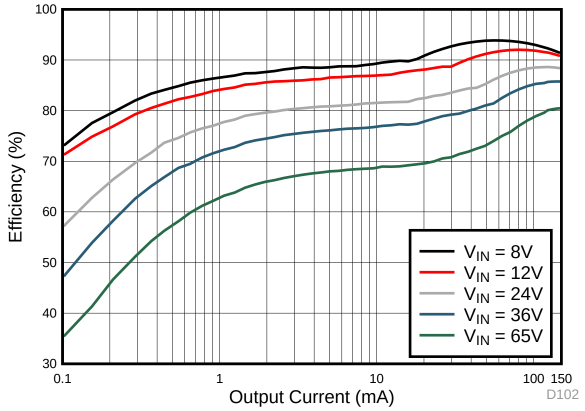
The recommended high-frequency capacitance is 1 µF or higher and should be a high-quality ceramic type X5R or X7R with sufficient voltage rating. Based on the voltage coefficient of ceramic capacitors, choose a voltage rating of twice the maximum input voltage. Additionally, some bulk capacitance is required if the LM5165-Q1 circuit is not located within approximately 5 cm from the input voltage source. This capacitor provides damping to the resonance associated with parasitic inductance of the supply lines and high-Q ceramics.

8.2.1.2.6 Soft-Start Capacitor – C_{SS}

Connect an external soft-start capacitor for a specific soft-start time. In this example, select a soft-start capacitance of 47 nF based on Equation 8 to achieve a soft-start time of 6 ms.

8.2.1.3 Application Performance Curves

Unless otherwise stated, application performance curves were taken at T_A = 25 °C.



V_{OUT} = 5 V

Figure 38. Efficiency

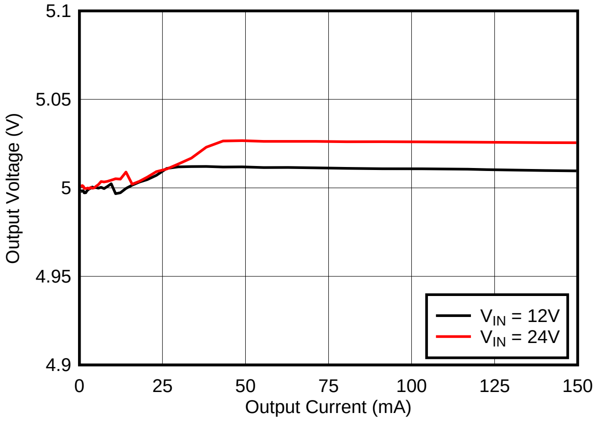
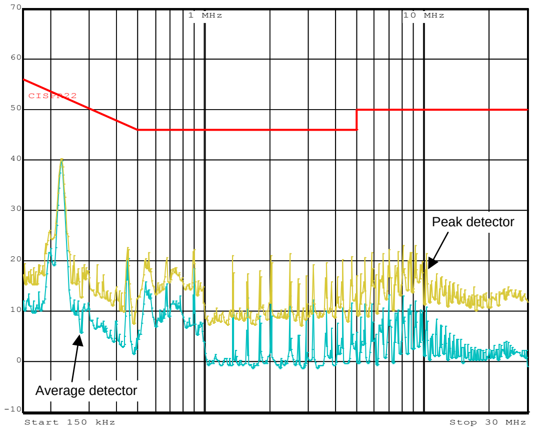


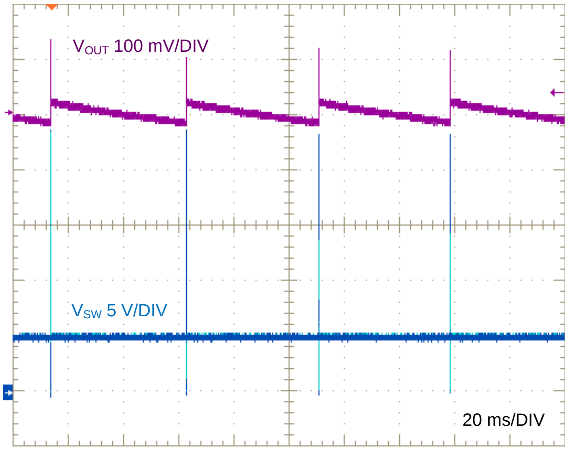
Figure 39. Load Regulation



V_{IN} = 13.5 V
I_{OUT} = 100 mA

L_{IN} = 22 µH
$C_{IN(EXT)}$ = 10 µF

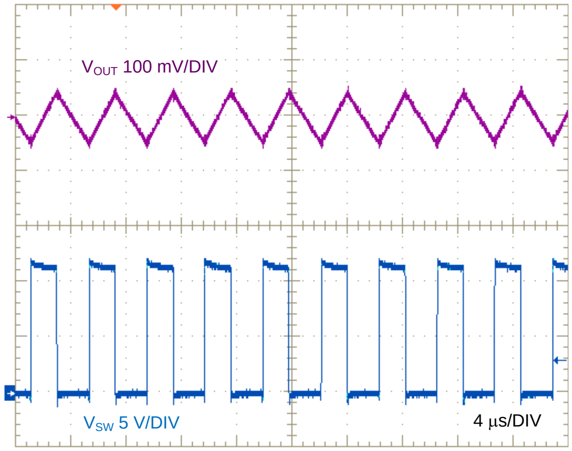
Figure 40. EMI Plot – CISPR 22 Filtered Emissions



V_{IN} = 12 V

I_{OUT} = 0 mA

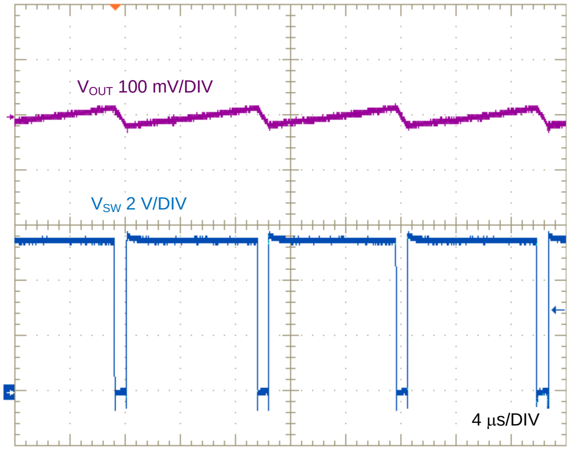
Figure 41. SW Node and Output Ripple Voltage, No Load



V_{IN} = 12 V

I_{OUT} = 150 mA

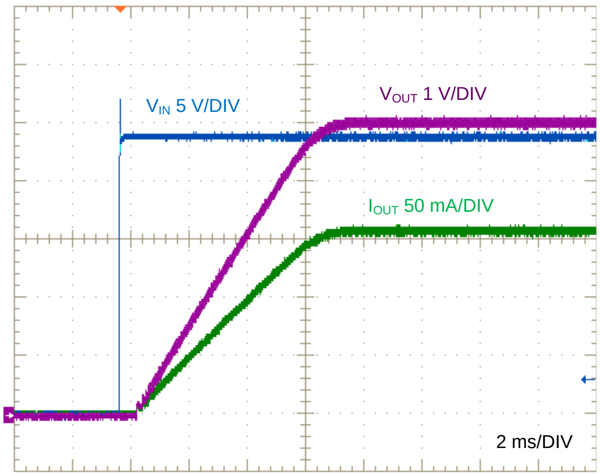
Figure 42. SW Node and Output Ripple Voltage, Full Load



V_{IN} = 5.7 V

I_{OUT} = 150 mA

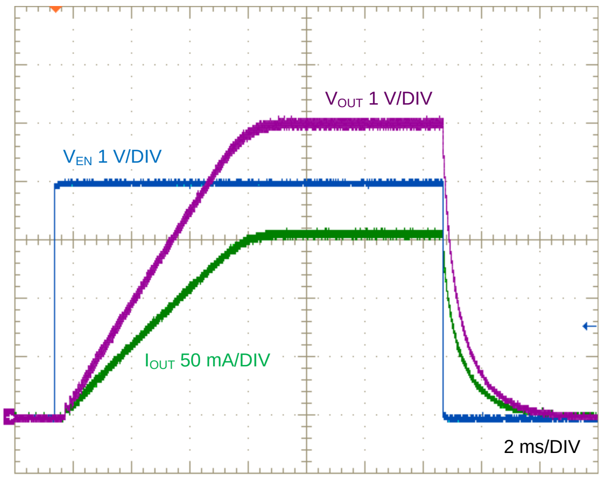
Figure 43. SW Node and Output Ripple Voltage Showing Frequency Foldback Near Dropout



V_{IN} stepped to 24 V

30-Ω Load

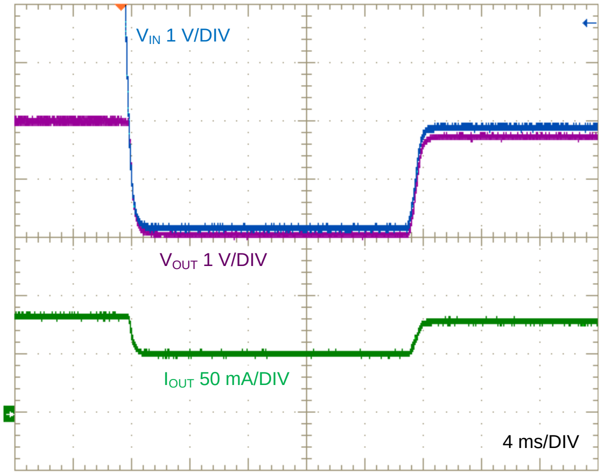
Figure 44. Startup, Full Load



V_{IN} = 24 V

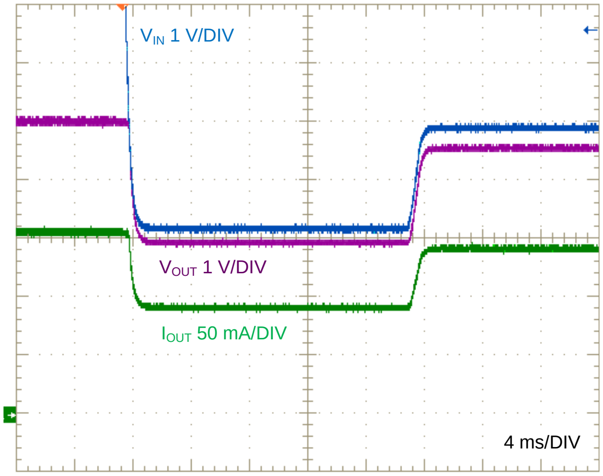
30-Ω Load

Figure 45. Enable ON and OFF



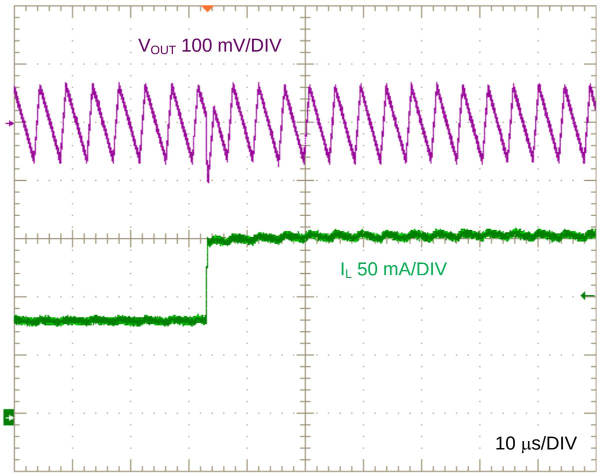
V_{IN} brownout to 3.2 V

Figure 46. Dropout Performance, 75-mA Resistive Load



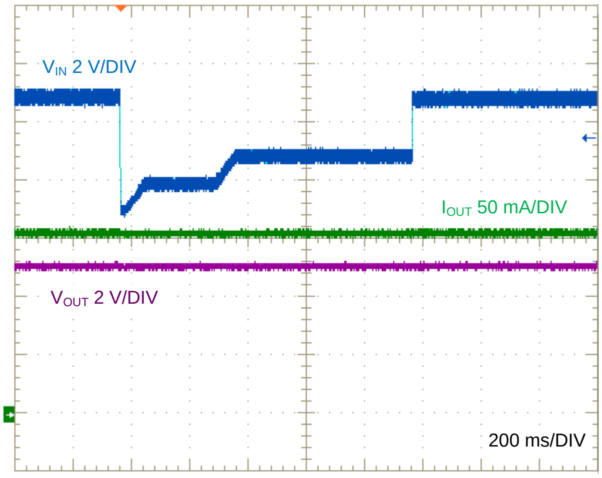
V_{IN} brownout to 3.2 V

Figure 47. Dropout Performance, 150-mA Resistive Load



V_{IN} = 24 V

Figure 48. Load Transient, 50 mA to 150 mA, 1 A/µs



I_{OUT} = 150 mA

Figure 49. Input Transient (Automotive Cold Crank Profile)

8.2.2 Design 2: Small Solution Size PFM Converter Rated at 3.3 V, 50 mA

The schematic diagram of a 3.3-V, 50-mA PFM converter with minimum component count is given in Figure 50.

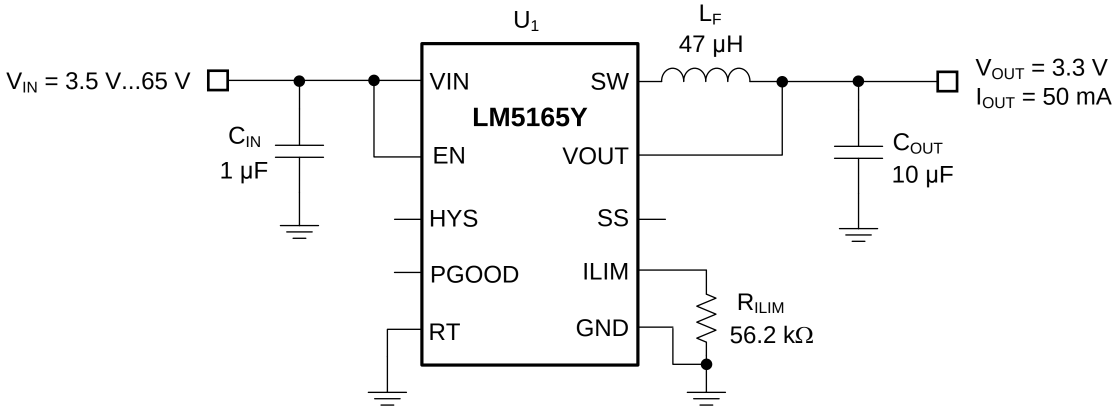


Figure 50. Schematic for Design 2 with $V_{IN(nom)}$ = 12 V, V_{OUT} = 3.3 V, $I_{OUT(max)}$ = 50 mA, $F_{SW(nom)}$ = 350 kHz

8.2.2.1 Design Requirements

The target full-load efficiency of this design is 88% based on a nominal input voltage of 12 V and an output voltage of 3.3 V. The required total input voltage range is 3.5 V to 65 V. The LM5165-Q1 has an internally-set soft-start time of 900 µs and an adjustable peak current limit threshold. The BOM is listed in Table 3.

Table 3. List of Components for Design 2(1)

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	1 µF, 100 V, X7S, 0805 ceramic	TDK	C2012X7S2A474M125AE
C_{OUT}	1	10 µF, 6.3 V, X7R, 0805 ceramic	Taiyo Yuden	JMK212AB7106KG-T
			Murata	GRM21BR70J106KE76K
L_F	1	47 µH ±20%, 0.56 A, 650 mΩ max DCR, 3.9 x 3.9 x 1.7 mm	Coilcraft	LPS4018-473MRC
		47 µH ±20%, 0.7 A, 620 mΩ typ DCR, 4.0 x 4.0 x 1.8 mm	Würth	74404042470
		47 µH ±20%, 0.57 A, 650 mΩ typ DCR, 4.0 x 4.0 x 1.8 mm	Taiyo Yuden	NR4018T470M
R_{ILIM}	1	56.2 kΩ, 1%, 0402	Std	Std
U_1	1	LM5165Y-Q1 Synchronous Buck Converter, VSON-10, 3.3 V Fixed	TI	LM5165YQDRCRQ1

(1) See *Third-Party Products Disclaimer*.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Peak Current Limit Setting – R_{ILIM}

Install a 56.2 kΩ resistor from ILIM to GND to select a 120-mA peak current limit threshold setting to meet the rated output current of 50 mA.

8.2.2.2.2 Switching Frequency – L_F

Tie RT to GND to select PFM mode of operation. The inductor, input voltage, output voltage and peak current determine the pulse switching frequency of a PFM-configured LM5165-Q1. For a given input voltage, output voltage and peak current, the inductance of L_F sets the switching frequency when the output is in regulation. Use Equation 19 to select an inductance of 47 µH based on the target PFM converter switching frequency of 350 kHz at 12-V input.

$$L_F = \frac{V_{OUT}}{F_{SW(PFM)} \cdot I_{PK(PFM)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{19}$$

$I_{PK(PFM)}$ in this example is the peak current limit setting of 120 mA plus an additional 10% margin added to include the effect of the 100-ns peak current comparator delay. An additional constraint on the inductance is the 180-ns minimum on-time of the high-side MOSFET. Therefore, in order to keep the inductor current well controlled, choose an inductance that is larger than $L_{F(min)}$ using Equation 20 where $V_{IN(max)}$ is the maximum input supply voltage for the application, $t_{ON(min)}$ is 180 ns, and $I_{L(max)}$ is the maximum allowed peak inductor current.

$$L_{F(min)} = \frac{V_{IN(max)} \cdot t_{ON(min)}}{I_{L(max)}} \tag{20}$$

Choose an inductor with saturation current rating above the peak current limit setting, and allow for derating of the saturation current at the highest expected operating temperature.

8.2.2.2.3 Output Capacitor – C_{OUT}

The output capacitor, C_{OUT}, filters the inductor’s ripple current and stores energy to meet the load current requirement when the LM5165-Q1 is in sleep mode. The output ripple has a base component of amplitude $V_{OUT}/123$ related to the 10-mV typical feedback comparator hysteresis in PFM. The wakeup time from sleep to active mode adds a ripple voltage component that is a function of the output current. Approximate the total output ripple by Equation 21.

$$\Delta V_{OUT} = \frac{I_{OUT} \cdot 4\mu s}{C_{OUT}} + \frac{V_{OUT}}{123} \tag{21}$$

Also, the output capacitance must be large enough to accept the energy stored in the inductor without a large deviation in output voltage. Setting this voltage change equal to 0.5% of the output voltage results in

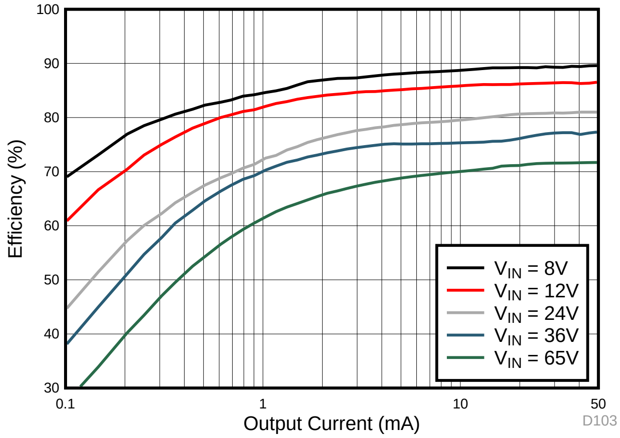
$$C_{OUT} \geq 100 \cdot L_F \cdot \left(\frac{I_{PK(PFM)}}{V_{OUT}} \right)^2 \tag{22}$$

In general, select the capacitance of C_{OUT} to limit the output voltage ripple at full load current, ensuring that it is rated for worst-case RMS ripple current given by $I_{RMS} = I_{PK(PFM)}/2$. In this design example, choose a 10-µF, 6.3-V ceramic output capacitor with X7R dielectric and 0805 footprint.

8.2.2.2.4 Input Capacitor – C_{IN}

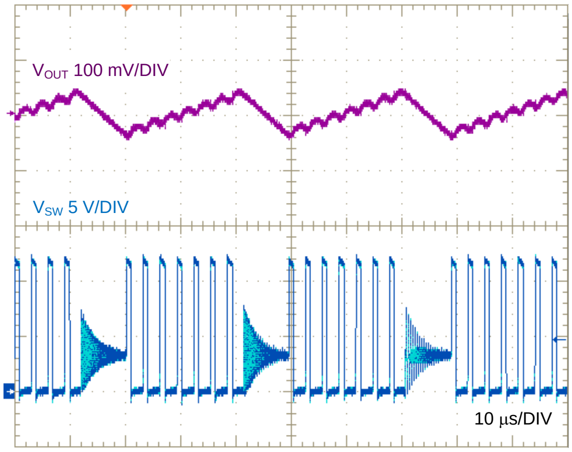
The input capacitor, C_{IN}, filters the high-side MOSFET's triangular current waveform, see Figure 72. To prevent large ripple voltage, use a low ESR ceramic input capacitor sized for the worst-case RMS ripple current given by $I_{RMS} = I_{OUT}/2$. In this design example, choose a 1-µF, 100-V ceramic input capacitor with X7S dielectric and 0805 footprint.

8.2.2.3 Application Performance Curves



V_{OUT} = 3.3 V

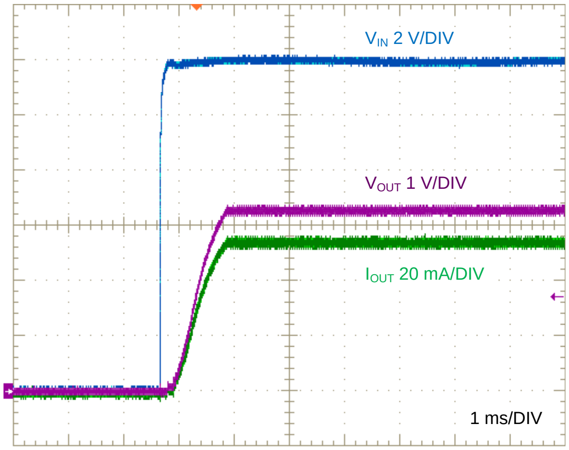
Figure 51. Efficiency



V_{IN} = 12 V

I_{OUT} = 50 mA

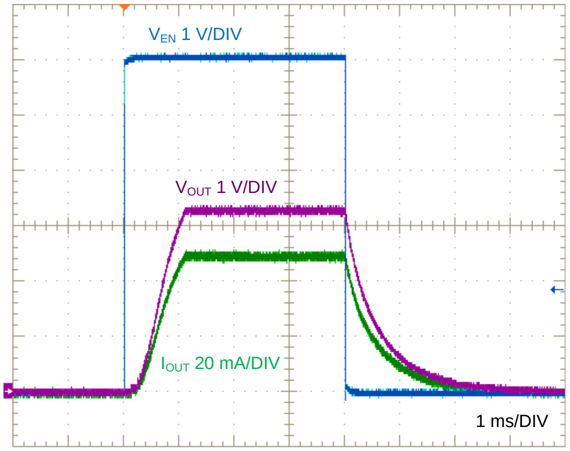
Figure 52. SW Node and Output Ripple Voltage, Full Load



V_{IN} stepped to 12 V

66-Ω Load

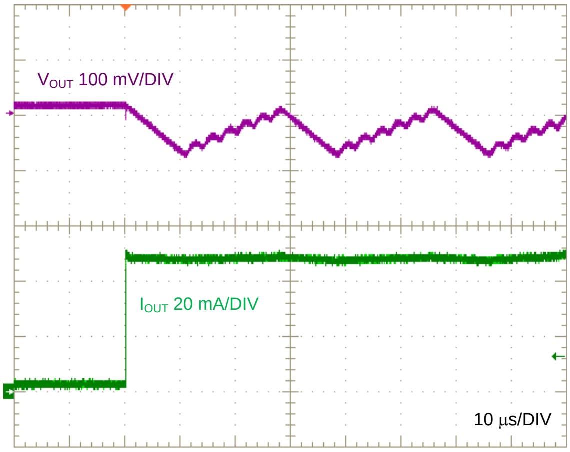
Figure 53. Startup, Full Load



V_{IN} = 12 V

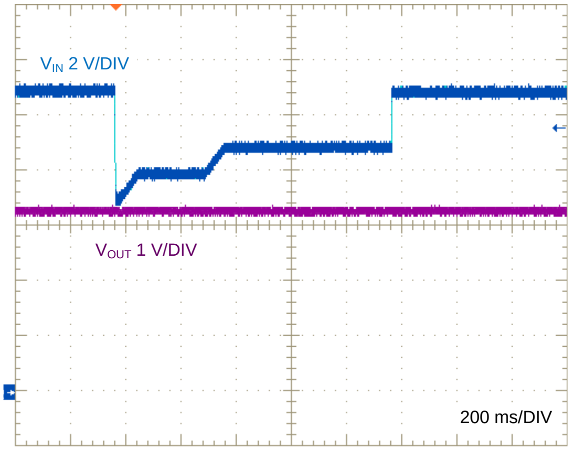
66-Ω Load

Figure 54. Enable ON and OFF



V_{IN} = 12 V

Figure 55. Load Transient, 0 mA to 50 mA, 1 A/µs



I_{OUT} = 50 mA

Figure 56. Input Voltage Transient (Automotive Cold Crank Profile)

8.2.3 Design 3: High Density 12-V, 75-mA PFM Converter

The schematic diagram of 12-V, 75-mA PFM converter is given in Figure 57.

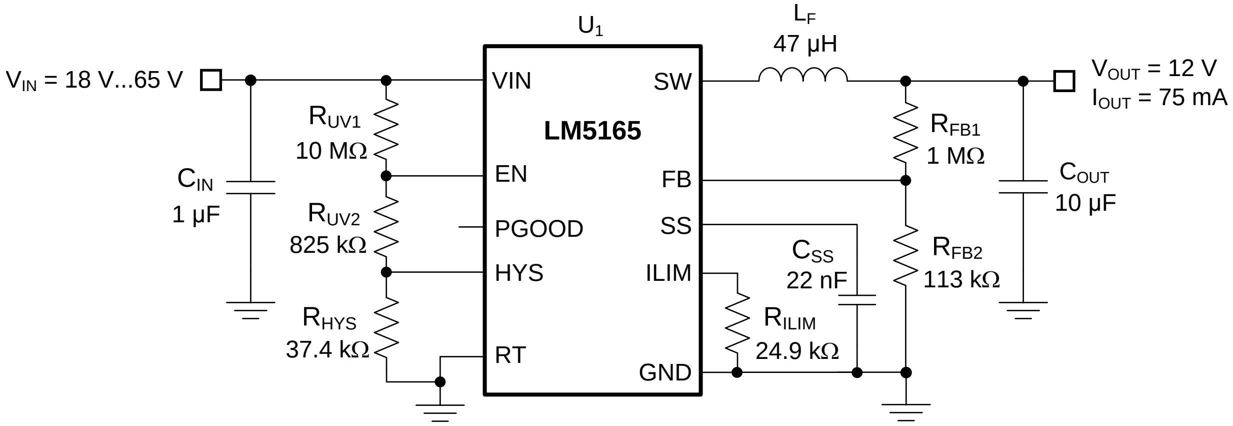


Figure 57. Schematic for Design 3 with $V_{IN(nom)}$ = 24 V, V_{OUT} = 12 V, $I_{OUT(max)}$ = 75 mA, $F_{SW(nom)}$ = 500 kHz

8.2.3.1 Design Requirements

The full-load efficiency specification is 92% based on a nominal input voltage of 24 V and an output voltage of 12 V. The total input voltage range is 18 V to 65 V, with UVLO turn on and turn off at 16 V and 14.5 V, respectively. The output voltage setpoint is established by feedback resistors, R_{FB1} and R_{FB2}. The switching frequency is set by inductor L_F at 500 kHz at nominal input voltage. The required components are listed in Table 4.

Table 4. List of Components for Design 3(1)

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	1 µF, 100 V, X7S, 0805 ceramic	Murata	GRJ21BC72A105KE11L
		1 µF, 100 V, X7S, 0805 ceramic, AEC-Q200	TDK	CGA4J3X7S2A105K125AE
C_{OUT}	1	10 µF, 16 V, X7R, 0805 ceramic	Taiyo Yuden	EMK212BB7106MG-T
		10 µF, 16 V, X7R, 0805 ceramic, AEC-Q200	TDK	CGA4J1X7S1C106K125AC
L_F	1	47 µH ±20%, 0.56 A, 650 mΩ max DCR, 3.9 x 3.9 x 1.7 mm AEC-Q200	Coilcraft	LPS4018-473MRC
R_{ILIM}	1	24.9 kΩ, 1%, 0402	Std	Std
R_{FB1}	1	1 MΩ, 1%, 0402	Std	Std
R_{FB2}	1	113 kΩ, 1%, 0402	Std	Std
R_{UV1}	1	10 MΩ, 1%, 0603	Std	Std
R_{UV2}	1	825 kΩ, 1%, 0402	Std	Std
R_{HYS}	1	37.4 kΩ, 1%, 0402	Std	Std
C_{SS}	1	22 nF, 10 V, X7R, 0402	Std	Std
U_1	1	LM5165-Q1 Synchronous Buck Converter, VSON-10, 3mm x 3 mm	TI	LM5165QDRCRQ1

(1) See *Third-Party Products Disclaimer*.

8.2.3.2 Detailed Design Procedure

The component selection procedure for this PFM design is quite similar to that of Design 2, see Figure 50.

8.2.3.2.1 Peak Current Limit Setting – R_{ILIM}

Install a 24.9 kΩ resistor from ILIM to GND to select the 180-mA peak current limit setting for a rated output current of 75 mA.

8.2.3.2.2 Switching Frequency – L_F

Tie RT to GND to select PFM mode of operation. Set the switching frequency by the filter inductance, L_F. Calculate an inductance of 47 µH based on the target PFM converter switching frequency of 500 kHz at 24-V input using Equation 19. Use a peak current limit setting, $I_{PK(PFM)}$, of 180 mA plus an additional 50% margin in this high-frequency design to include the effect of the 100-ns current limit comparator delay. Choose an inductor with saturation current rating well above the peak current limit setting, and allow for derating of the saturation current at the highest expected operating temperature.

8.2.3.2.3 Input and Output Capacitors – C_{IN}, C_{OUT}

Choose a 1-µF, 100-V ceramic input capacitor with 0805 footprint. Such a capacitor is typically available in X5R or X7S dielectric. Based on Equation 22, select a 10-µF, 16-V ceramic output capacitor with X7R dielectric and 0805 footprint.

8.2.3.2.4 Feedback Resistors – R_{FB1}, R_{FB2}

The output voltage of the LM5165-Q1 is externally adjustable using a resistor divider network. The divider network comprises the upper feedback resistor R_{FB1} and lower feedback resistor R_{FB2}. Select R_{FB1} of 1 MΩ to minimize quiescent current and improve light-load efficiency in this application. With the desired output voltage setpoint of 12 V and V_{FB} = 1.223 V, calculate the resistance of R_{FB2} using Equation 5 as 113.5 kΩ. Choose the closest available standard value of 113 kΩ for R_{FB2}. Please refer to the *Adjustable Output Voltage (FB)* section for more detail.

8.2.3.2.5 Undervoltage Lockout Setpoint – R_{UV1}, R_{UV2}, R_{HYS}

Adjust the undervoltage lockout (UVLO) using an externally-connected resistor divider network of R_{UV1}, R_{UV2} and R_{HYS}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. The EN rising threshold for the LM5165-Q1 is 1.212 V.

Rearranging Equation 6 and Equation 7, the expressions to calculate R_{UV2} and R_{HYS} are as follows.

$$R_{UV2} = \frac{V_{EN(on)}}{V_{IN(on)} - V_{EN(on)}} \cdot R_{UV1} \tag{23}$$

$$R_{HYS} = \frac{V_{EN(off)}}{V_{IN(off)} - V_{EN(off)}} \cdot R_{UV1} - R_{UV2} \tag{24}$$

Choose R_{UV1} as 10 MΩ to minimize input quiescent current. Given the desired input voltage UVLO thresholds of 16 V and 14.5V, calculate the resistance of R_{UV2} and R_{HYS} as 825 kΩ and 37.4 kΩ, respectively. Please refer to the *Precision Enable (EN) and Hysteresis (HYS)* section for more detail.

8.2.3.2.6 Soft Start – C_{SS}

Install a 22-nF capacitor from SS to GND for a soft-start time of 3 ms.

8.2.3.3 Application Performance Curves

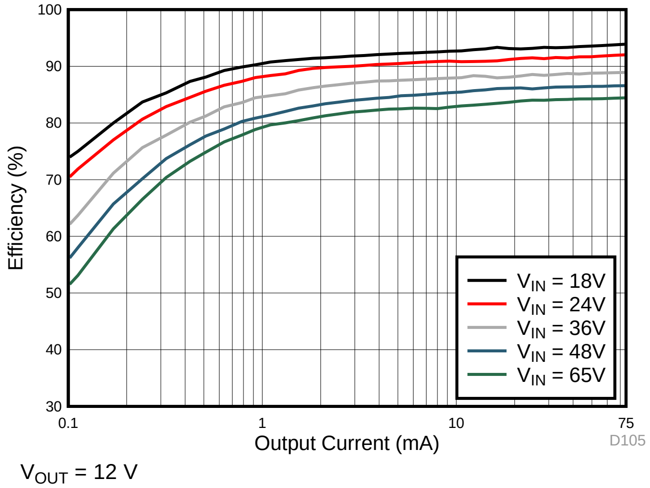


Figure 58. Efficiency

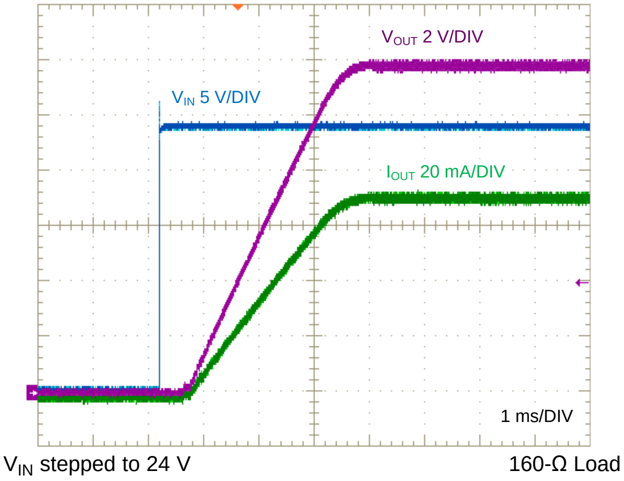


Figure 59. Startup, Full Load

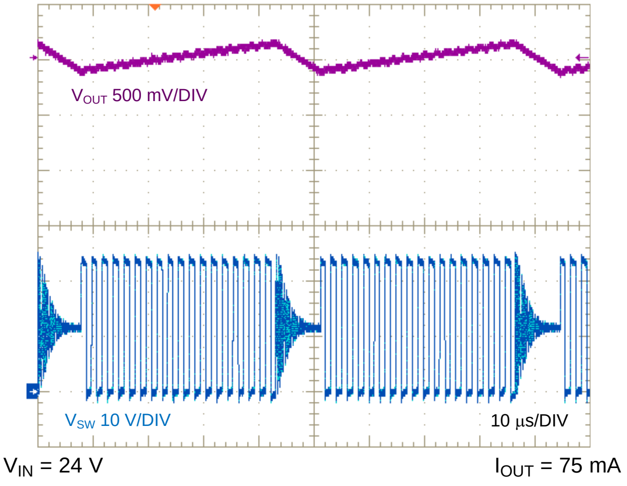


Figure 60. SW Node and Output Ripple Voltage, Full Load

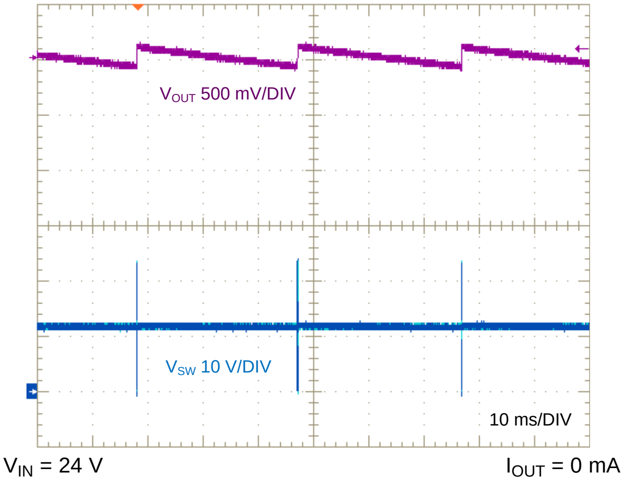


Figure 61. SW Node and Output Ripple Voltage, No Load

8.2.4 Design 4: 3.3-V, 150-mA COT Converter with High Efficiency

The schematic diagram of a 3.3-V, 150-mA COT converter is given in Figure 62.

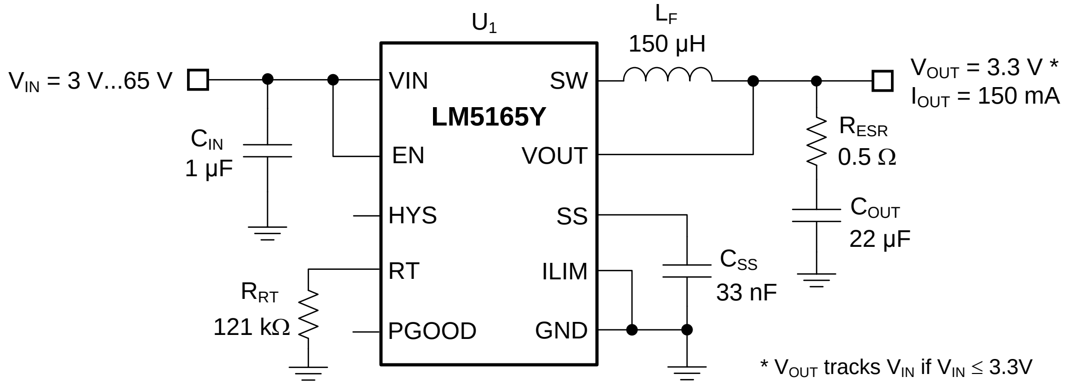


Figure 62. Schematic for Design 4 with $V_{IN(nom)}$ = 24 V, V_{OUT} = 3.3 V, $I_{OUT(max)}$ = 150 mA, $F_{SW(nom)}$ = 160 kHz

8.2.4.1 Design Requirements

The target full-load efficiency is 91% based on a nominal input voltage of 24 V and an output voltage of 3.3 V. The required input voltage range is 3 V to 65 V. The LM5165Y-Q1 is chosen to deliver a fixed 3.3-V output voltage. The switching frequency is set by resistor R_{RT} at approximately 160 kHz. The output voltage soft-start time is 4 ms. The required components are listed in Table 5. The component selection procedure for this COT design is quite similar to that of Design 1, see Figure 37.

Table 5. List of Components for Design 4[(1)]

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	1 µF, 100 V, X7R, 1206 ceramic	Murata	GRM31CR72A105KA01L
C_{OUT}	1	22 µF, 6.3 V, X7S, 0805 ceramic	Murata	GRM21BR660J226ME39K
L_F	1	150 µH ±20%, 0.29 A, 0.86 Ω typ DCR, 4.8 x 4.8 x 2.9 mm	Coilcraft	LPS5030-154MLC
R_{ESR}	1	0.5 Ω, 5%, 0402	Std	Std
R_{RT}	1	121 kΩ, 1%, 0402	Std	Std
C_{SS}	1	33 nF, 10 V, X7R, 0402 ceramic	Std	Std
U_1	1	LM5165Y-Q1 Synchronous Buck Converter, VSON-10, 3.3V Fixed	TI	LM5165YQDRCRQ1

(1) See *Third-Party Products Disclaimer*.

8.2.4.2 Application Performance Curves

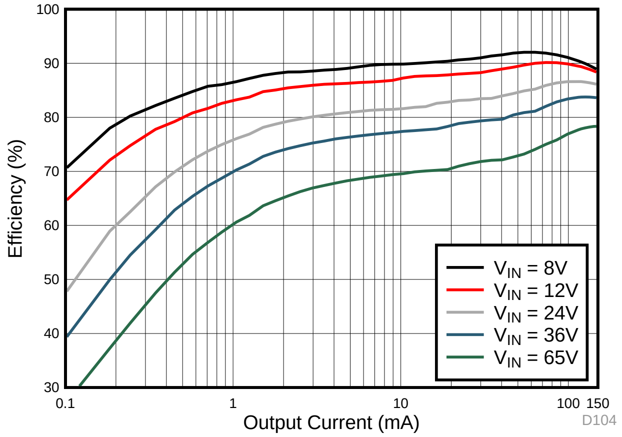


Figure 63. Efficiency

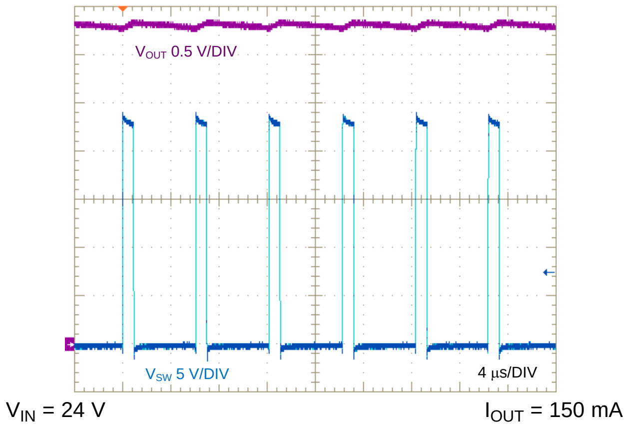


Figure 64. SW Node and Output Ripple Voltages, Full Load

8.2.5 Design 5: 15-V, 150-mA, 600-kHz COT Converter

The schematic diagram of a 15-V, 150-mA COT converter is given in Figure 65.

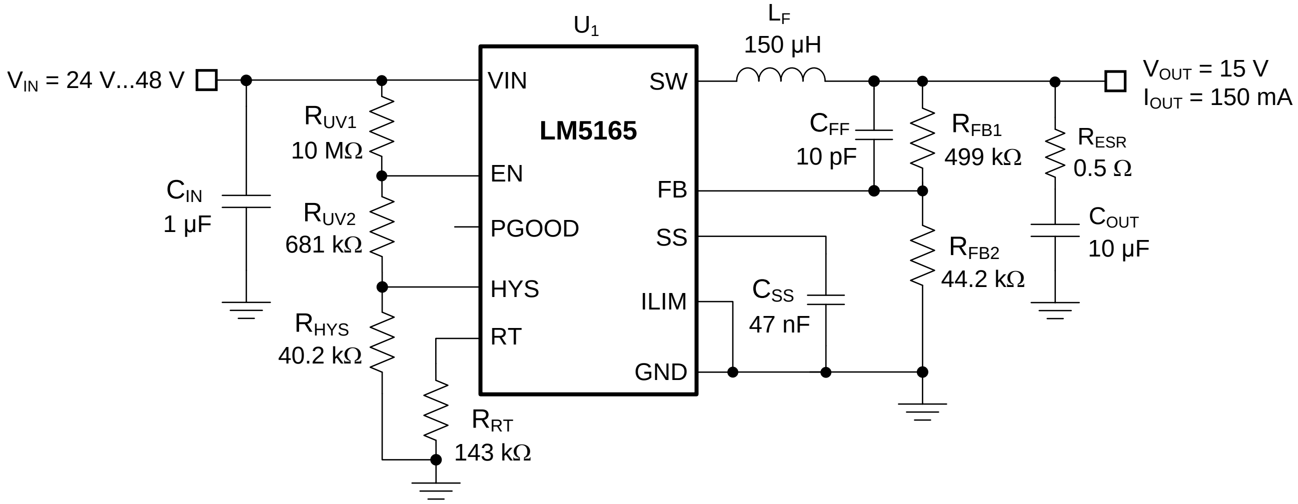


Figure 65. Schematic for Design 5 with $V_{IN(nom)}$ = 36 V, V_{OUT} = 15 V, $I_{OUT(max)}$ = 150 mA, $F_{SW(nom)}$ = 600 kHz

8.2.5.1 Design Requirements

The target full-load efficiency is 92% based on a nominal input voltage of 36 V and an output voltage of 15 V. The input voltage operating range is 24 V to 48 V, but transients as high as 65 V are possible in the application. UVLO turn on and turn off are set at 19 V and 17 V, respectively. The LM5165-Q1 switching frequency is set at approximately 600 kHz by resistor R_{RT} of 143 kΩ. The output voltage soft-start time is 6 ms. The required components are listed in Table 6. The component selection procedure for this COT design is quite similar to that of Design 1, see Figure 37.

Table 6. List of Components for Design 5[1]

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	1 µF, 100 V, X7R, 1206 ceramic	AVX	12061C105KAT2A
C_{OUT}	1	10 µF, 25 V, X7R, 1206 ceramic	Taiyo Yuden	TMK316B7106KL-TD
L_F	1	150 µH ±20%, 0.29 A, 0.86 Ω typ DCR, 4.8 x 4.8 x 2.9 mm	Coilcraft	LPS5030-154MLC
R_{ESR}	1	2.2 Ω, 5%, 0402	Std	Std
R_{RT}	1	143 kΩ, 1%, 0402	Std	Std
R_{FB1}	1	499 kΩ, 1%, 0402	Std	Std
R_{FB2}	1	44.2 kΩ, 1%, 0402	Std	Std
R_{UV1}	1	10 MΩ, 1%, 0603	Std	Std
R_{UV2}	1	681 kΩ, 1%, 0402	Std	Std
R_{HYS}	1	40.2 kΩ, 1%, 0402	Std	Std
C_{FF}	1	10 pF, 10 V, X7R, 0402 ceramic	Std	Std
C_{SS}	1	47 nF, 10 V, X7R, 0402 ceramic	Std	Std
U_1	1	LM5165-Q1 Synchronous Buck Converter, VSON-10, 3 mm x 3 mm	TI	LM5165QDRCRQ1

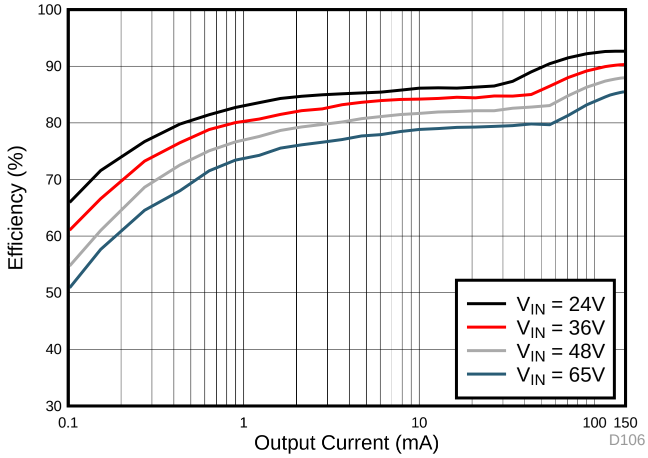
(1) See *Third-Party Products Disclaimer*.

8.2.5.2 Detailed Design Procedure

8.2.5.2.1 COT Output Ripple Voltage Reduction

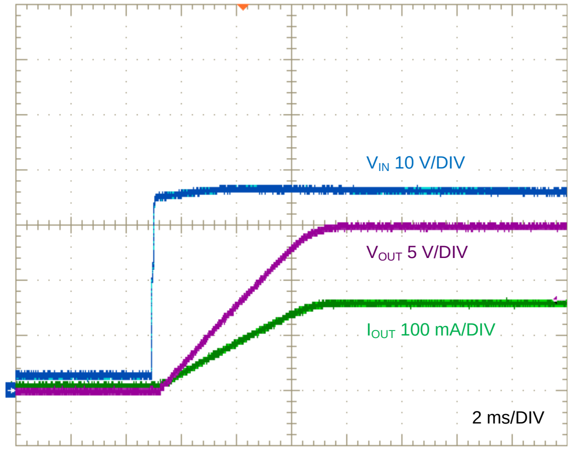
Depending on the required ripple resistance when operating in COT mode, the resultant output voltage ripple may be deemed too high for a given application. One option is to place a feed-forward capacitor C_{FF} in parallel with the upper feedback resistor R_{FB1}. Capacitor C_{FF} increases the high-frequency gain from V_{OUT} to V_{FB} close to unity such that the output voltage ripple couples directly to the FB node.

8.2.5.3 Application Performance Curves



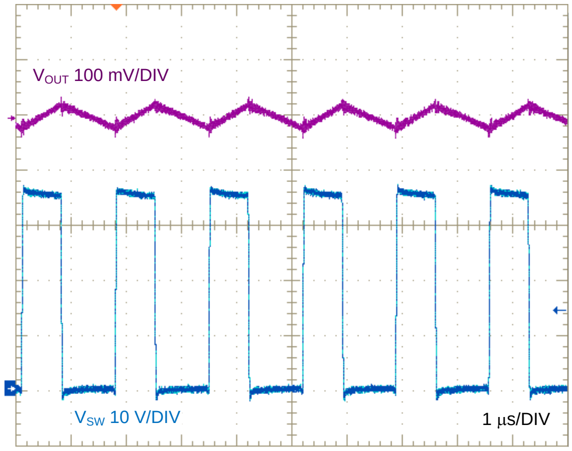
V_{OUT} = 15 V

Figure 66. Efficiency



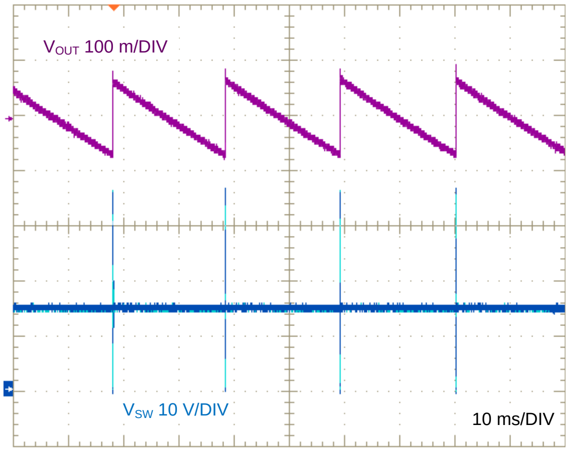
V_{IN} stepped to 36 V I_{OUT} = 150 mA

Figure 67. Startup, Full Load



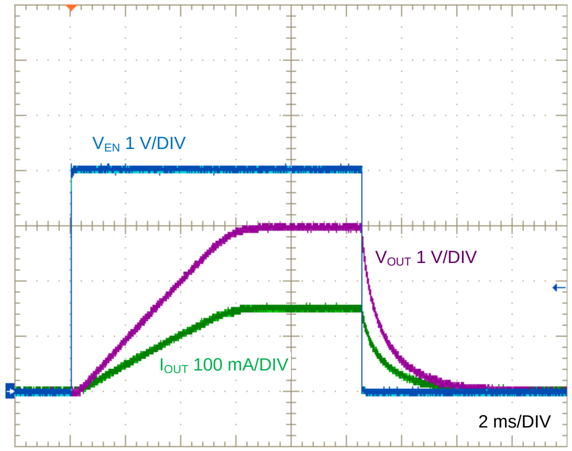
V_{IN} = 36 V I_{OUT} = 150 mA

Figure 68. SW Node and Output Ripple Voltage, Full Load



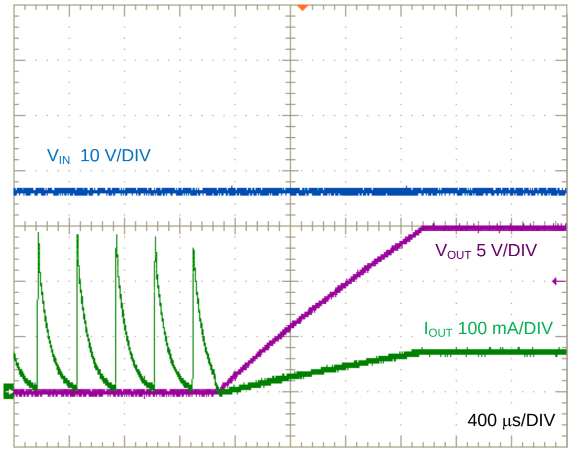
V_{IN} = 36 V I_{OUT} = 0 mA

Figure 69. SW Node and Output Ripple Voltage, No Load



V_{IN} = 36 V

Figure 70. Enable ON and OFF



V_{IN} = 36 V

Figure 71. Short Circuit Recovery

9 Power Supply Recommendations

The LM5165-Q1 is designed to operate from an input voltage supply range between 3 V and 65 V. This input supply should be able to provide the maximum input current and maintain a voltage above 3 V. Ensure that the resistance of the input supply rail is low enough that an input current transient does not cause a high enough drop at the LM5165-Q1 supply rail to cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LM5165-Q1 converter, additional bulk capacitance may be required in addition to the ceramic input capacitance. A 4.7-µF electrolytic capacitor is a typical choice for this function, whereby the capacitor ESR provides a level of damping against input filter resonances. A typical ESR of 0.5 Ω provides enough damping for most input circuit configurations.

10 PCB Layout

The performance of any switching converter depends as much upon PCB layout as it does the component selection. The following guidelines are provided to assist with designing a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

10.1 Layout Guidelines

PCB layout is a critical for good power supply design. There are several paths that conduct high slew-rate currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise and EMI or degrade the power supply's performance.

1. Bypass the VIN pin to GND with a low ESR ceramic capacitor of X5R or X7R dielectric. Place C_{IN} as close as possible to the LM5165-Q1 VIN and GND pins. Ground return paths for both the input and output capacitors should consist of localized top-side planes that connect to the GND pin and exposed PAD.
2. Minimize the loop area formed by the input capacitor connections and the VIN and GND pins.
3. Locate the power inductor close to the SW pin. Minimize the area of the SW trace/plane to prevent excessive capacitive coupling.
4. Tie the GND pin directly to the power pad under the device and to a heat-sinking PCB ground plane.
5. Use a ground plane in one of the middle layers as a noise shielding and heat dissipation path.
6. Have a single-point ground connection to the plane. Route the ground connections for the feedback, soft-start, and enable components to the ground plane. This prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior.
7. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
8. Minimize trace length to the FB pin. Locate both feedback resistors close to the FB pin. Place C_{FF} (if used) directly in parallel with R_{FB1}. Route the V_{OUT} sense path away from noisy nodes and preferably on a layer at the other side of a shielding layer.
9. Locate the components at RT and SS as close as possible to the device. Route with minimal trace lengths.
10. Provide adequate heat-sinking for the LM5165-Q1 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed PAD to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes.

10.1.1 Compact PCB Layout for EMI Reduction

Radiated EMI generated by high di/dt components relates to pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimize radiated EMI is to identify the pulsing current path and minimize the area of that path.

The critical switching loop of the power stage in terms of EMI is denoted in Figure 72. The topological architecture of a buck converter means that a particularly high di/dt current effective path exists in the loop comprising the input capacitor and the LM5165-Q1's integrated MOSFETs, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing the effective loop area.

Layout Guidelines (continued)

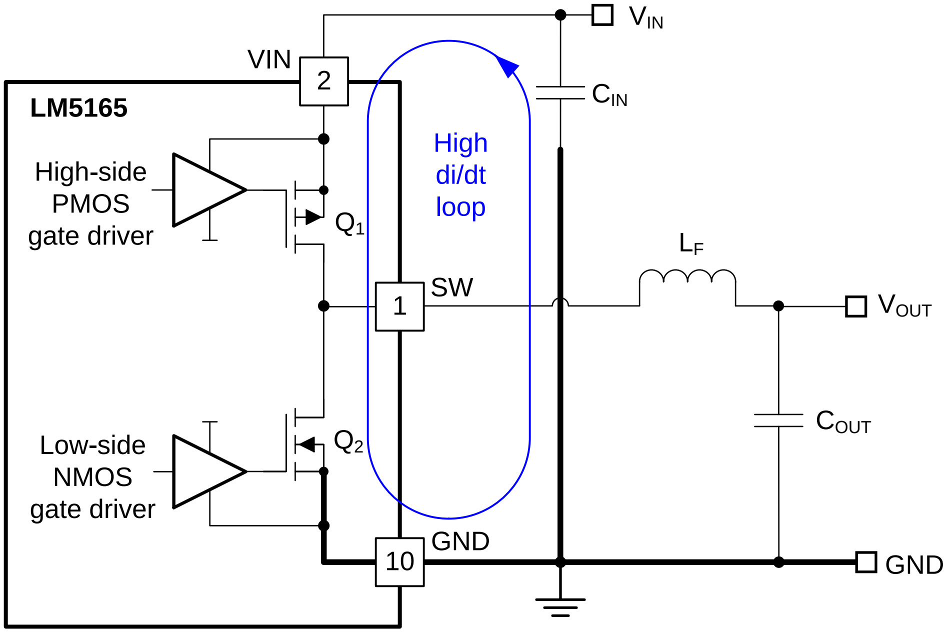


Figure 72. Synchronous Buck Converter with Power Stage Critical Switching Loop

The input capacitor provides the primary path for the high di/dt components of the high-side MOSFET's current. Placing a ceramic capacitor as close as possible to the VIN and GND pins is the key to EMI reduction. Keep the trace connecting SW to the inductor as short as possible and just wide enough to carry the load current without excessive heating. Use short, thick traces or copper pours (shapes) for current conduction path to minimize parasitic resistance. Place the output capacitor close to the V_{OUT} side of the inductor, and connect the capacitor's return terminal to the LM5165-Q1's GND pin and exposed PAD.

10.1.2 Feedback Resistor Layout

For the adjustable output voltage version of the LM5165-Q1, reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. This reduces the trace length of FB signal and noise coupling. The FB pin is the input to the feedback comparator and, as such, is a high impedance node sensitive to noise. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if a short path is not available.

Route the voltage sense trace from the load to the feedback resistor divider away from the SW node path, the inductor and V_{IN} path to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high feedback resistances, greater than 100 kΩ, are used to set the output voltage. Also, route the voltage sense trace on a different layer from the inductor, SW node and V_{IN} path, such that there is a ground plane that separates the feedback trace from the inductor and SW node copper polygon. This provides further shielding for the voltage feedback path from switching noise sources.

10.2 Layout Example

Figure 73 shows an example layout for the PCB top layer of a single-sided design. The bottom layer is essentially a full ground plane except for short connecting traces for SW, EN and PGOOD.

Layout Example (continued)

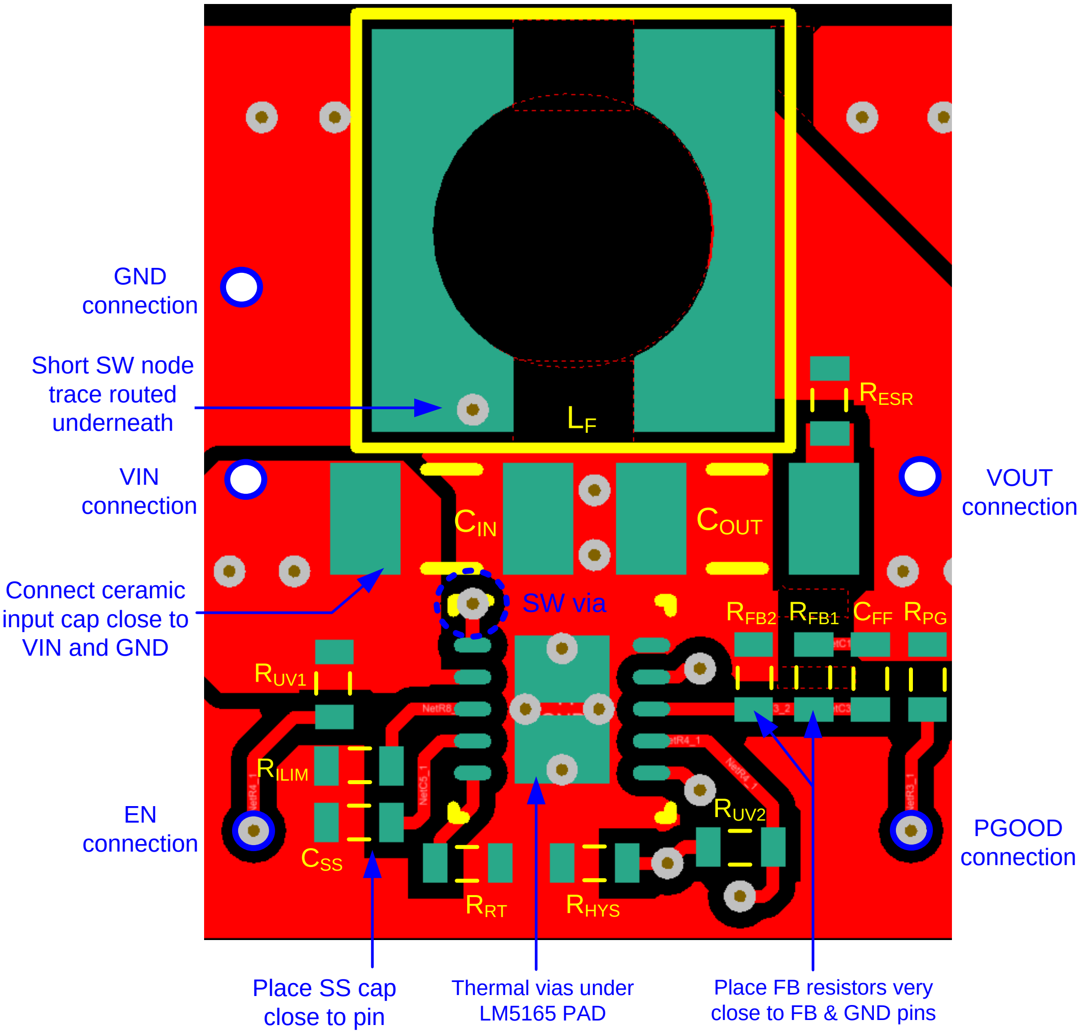


Figure 73. PCB Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

- LM5165-Q1 *Quick-start Design Tool*
- TIDesigns Reference Design Library
- WEBENCH® Designer

11.2 Documentation Support

11.2.1 Related Documentation

- *LM5165-HD-P50A EVM User's Guide*, SNVU474
- *LM5165-HD-C50X EVM User's Guide*, SNVU511
- *AN-2162: Simple Success with Conducted EMI from DC-DC Converters*, SNVA489
- *Automotive Cranking Simulator User's Guide*, SLVU984
- *Using New Thermal Metrics* Application Report, SBVA025
- *Semiconductor and IC Package Thermal Metrics*, SPRA953

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5165QDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5165Q	Samples
LM5165QDRCTQ1	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5165Q	Samples
LM5165XQDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5165XQ	Samples
LM5165XQDRCTQ1	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5165XQ	Samples
LM5165YQDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5165YQ	Samples
LM5165YQDRCTQ1	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5165YQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM5165-Q1 :

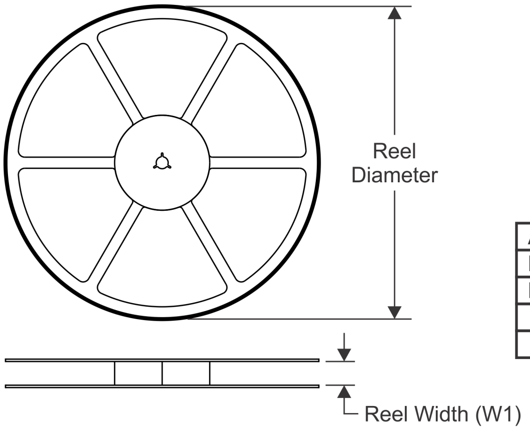
- Catalog: LM5165

NOTE: Qualified Version Definitions:

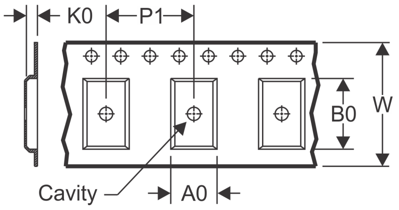
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

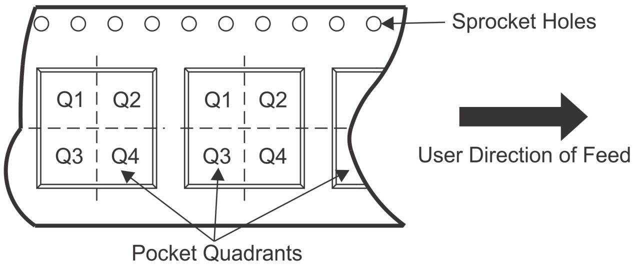


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

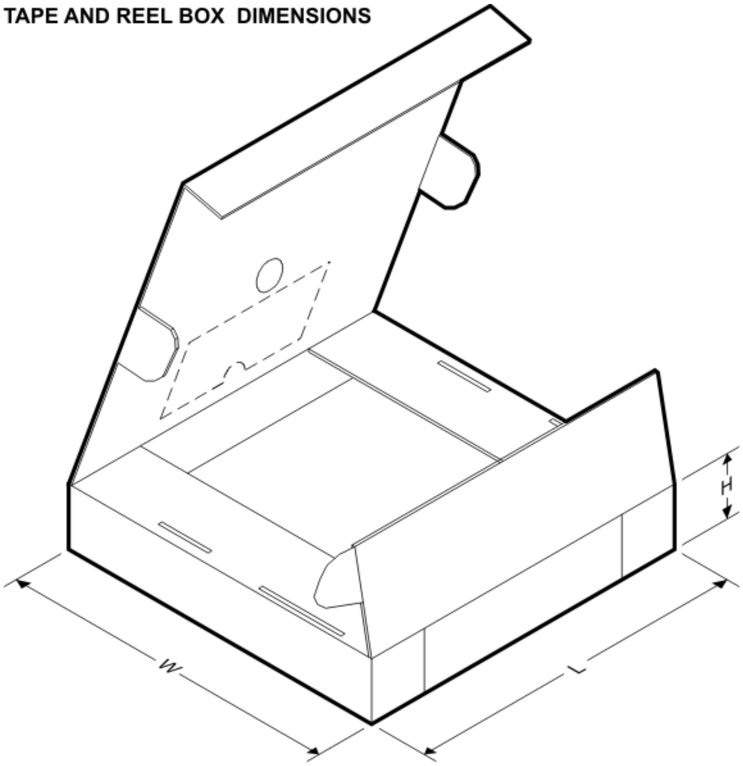
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5165QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM5165QDRCTQ1	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM5165XQDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM5165XQDRCTQ1	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM5165YQDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM5165YQDRCTQ1	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

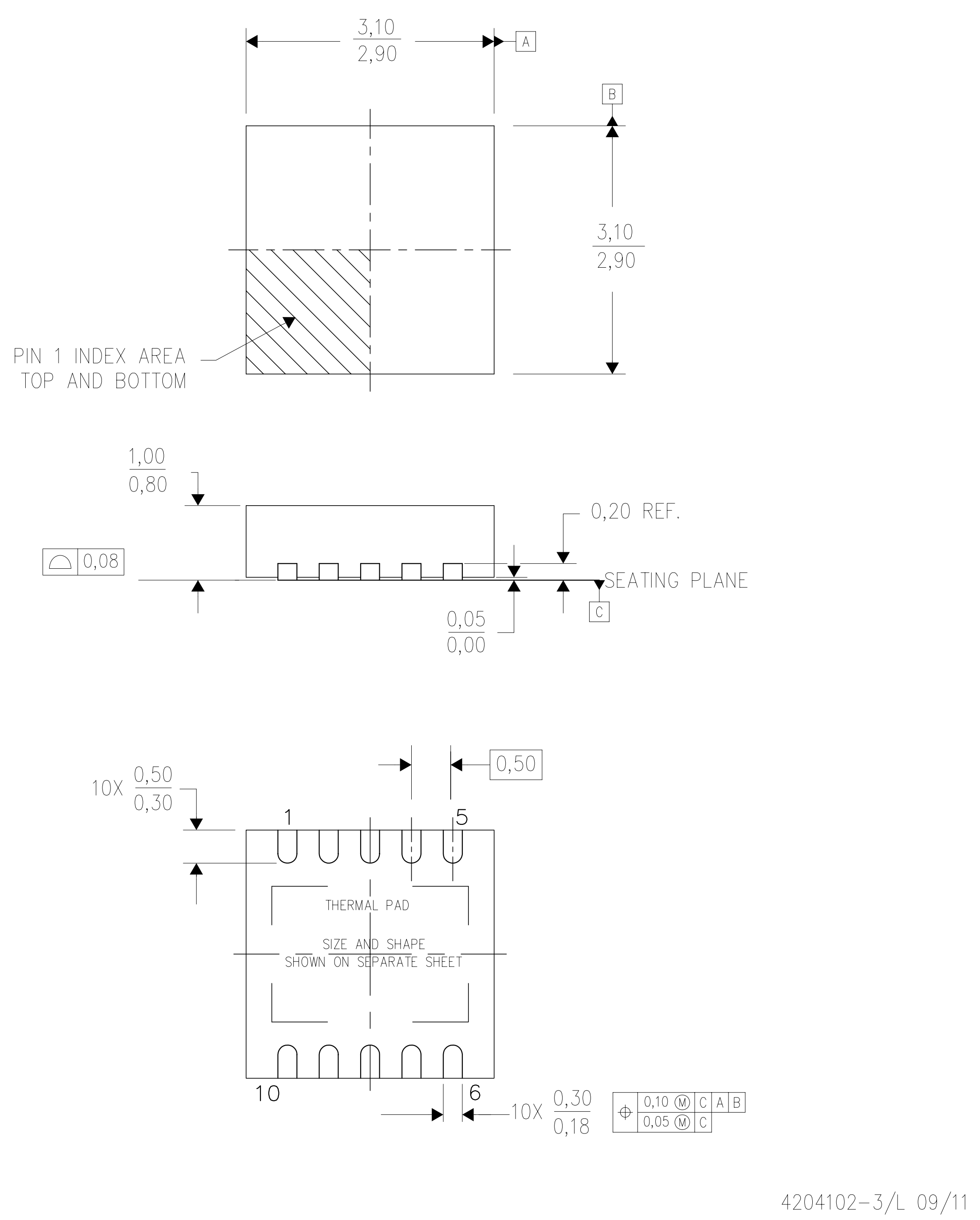
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5165QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
LM5165QDRCTQ1	VSON	DRC	10	250	210.0	185.0	35.0
LM5165XQDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
LM5165XQDRCTQ1	VSON	DRC	10	250	210.0	185.0	35.0
LM5165YQDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
LM5165YQDRCTQ1	VSON	DRC	10	250	210.0	185.0	35.0

DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

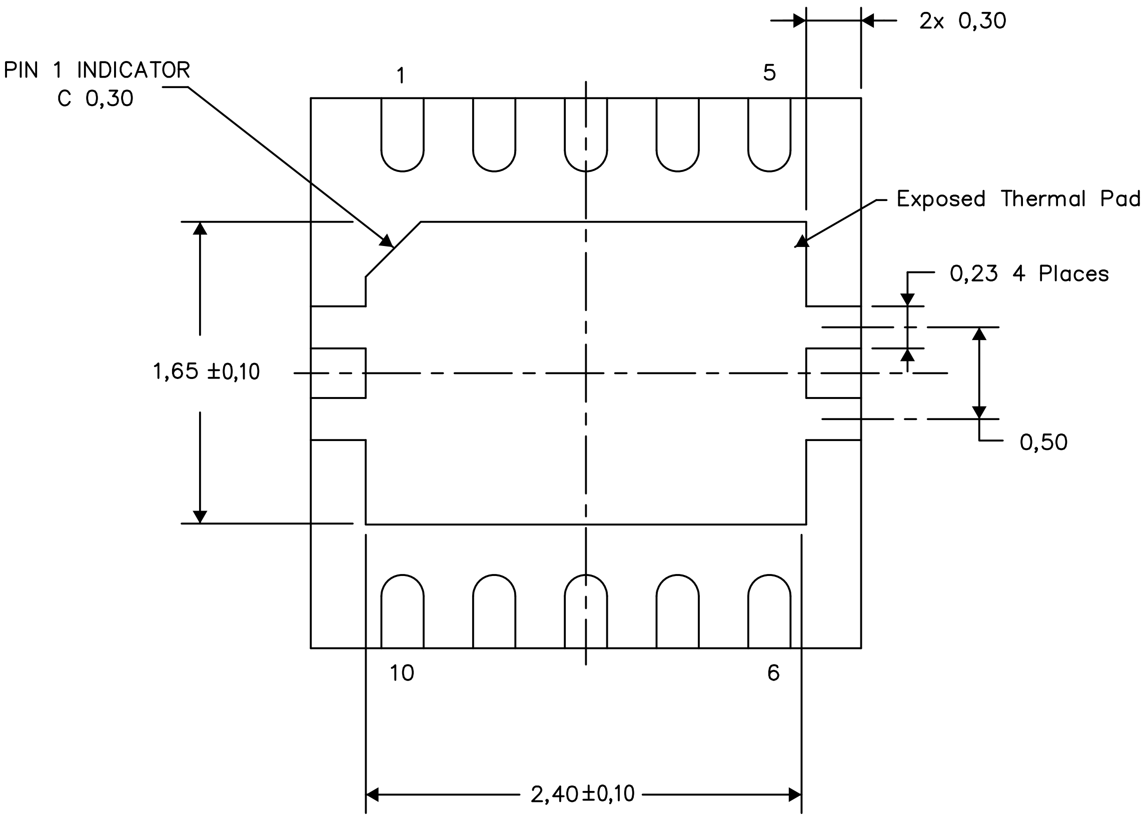
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



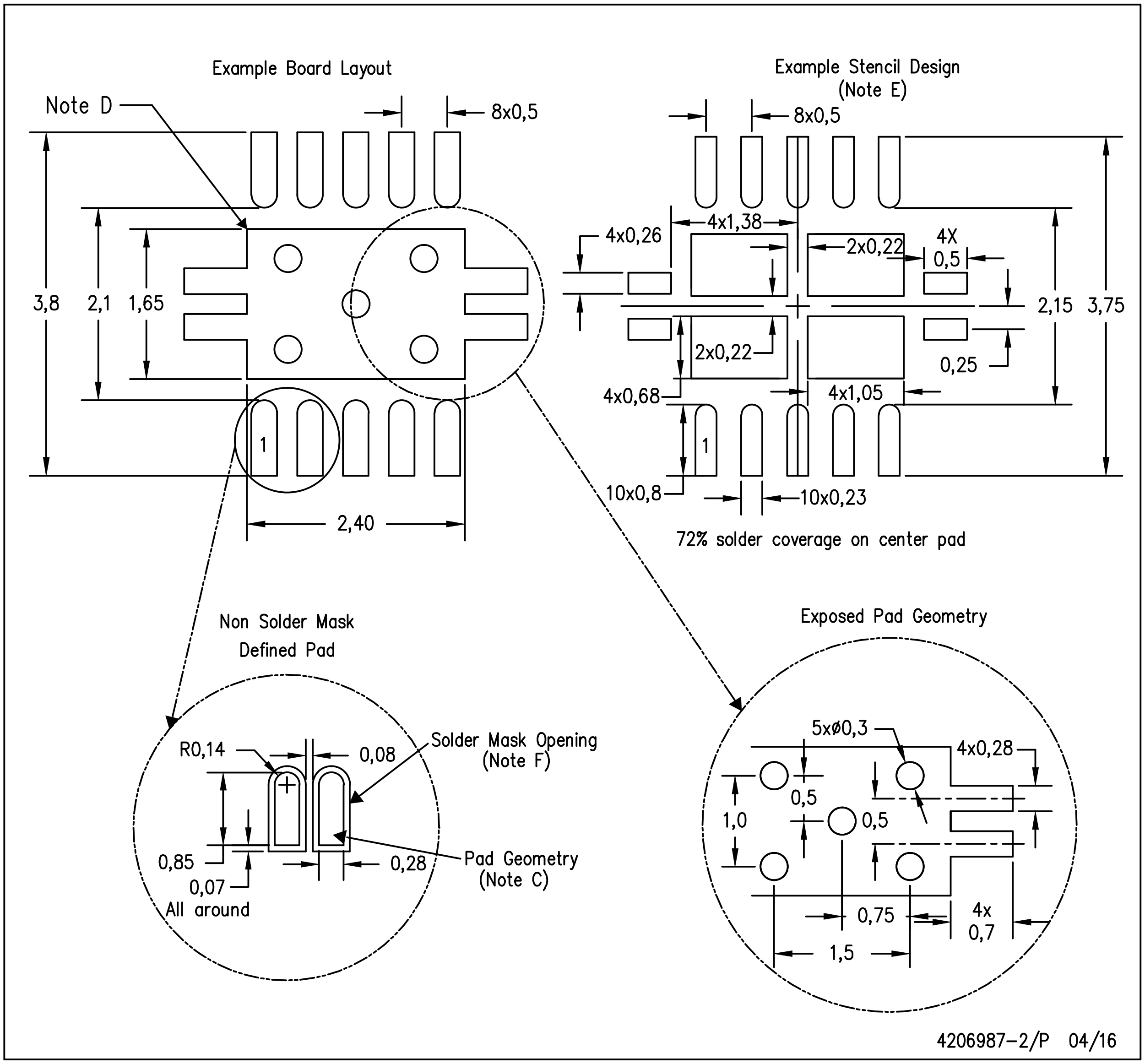
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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