

MSP430FG662x, MSP430FG642x Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Low Supply Voltage Range:
3.6 V Down to 1.8 V
- Ultra-Low Power Consumption
 - Active Mode (AM):
All System Clocks Active:
250 μ A/MHz at 8 MHz, 3.0 V, Flash Program Execution (Typical)
 - Standby Mode (LPM3):
Watchdog With Crystal, and Supply Supervisor Operational, Full RAM Retention, Fast Wakeup:
3.2 μ A at 2.2 V, 3.4 μ A at 3.0 V (Typical)
 - Shutdown RTC Mode (LPM3.5):
Shutdown Mode, Active Real-Time Clock With Crystal:
0.9 μ A at 3.0 V (Typical)
 - Shutdown Mode (LPM4.5):
0.2 μ A at 3.0 V (Typical)
- Wake up From Standby Mode in 3 μ s (Typical)
- 16-Bit RISC Architecture, Extended Memory, up to 20-MHz System Clock
- Flexible Power-Management System
 - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
 - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
 - FLL Control Loop for Frequency Stabilization
 - Low-Power Low-Frequency Internal Clock Source (VLO)
 - Low-Frequency Trimmed Internal Reference Source (REFO)
 - 32-kHz Crystals (XT1)
 - High-Frequency Crystals up to 32 MHz (XT2)
- Four 16-Bit Timers With 3, 5, or 7 Capture/Compare Registers
- Two Universal Serial Communication Interfaces
 - USCI_A0 and USCI_A1 Each Support
 - Enhanced UART With Automatic Baud-Rate Detection
 - IrDA Encoder and Decoder
 - Synchronous SPI
 - USCI_B0 and USCI_B1 Each Support
 - I²C
 - Synchronous SPI
- Full-Speed Universal Serial Bus (USB)
 - Integrated USB-PHY
 - Integrated 3.3-V and 1.8-V USB Power System
 - Integrated USB-PLL
 - Eight Input and Eight Output Endpoints
- Continuous-Time Sigma-Delta 16-Bit Analog-to-Digital Converter (ADC) With Internal Reference With 10 External Analog Inputs, 6 Single-Ended and 4 Selectable as Differential or Single-Ended
- Dual Low-Power Operational Amplifiers
- Quad Low-Impedance Ground Switches
- Dual 12-Bit Digital-to-Analog Converters (DACs) With Synchronization
- Voltage Comparator
- Integrated LCD Driver With Contrast Control for up to 160 Segments
- Hardware Multiplier Supports 32-Bit Operations
- Serial Onboard Programming, No External Programming Voltage Needed
- Six-Channel Internal DMA
- Real-Time Clock (RTC) Module With Supply Voltage Backup Switch
- [Table 3-1](#) Summarizes Family Members
- For Complete Module Descriptions, See the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#))

1.2 Applications

- Analog Sensor Systems
- Digital Sensor Systems
- Hand-Held Meters
- Medical Diagnostic Meters
- Hand-Held Industrial Testers
- Measurement Equipment



1.3 Description

The TI MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in 3 μs (typical).

The MSP430FG6626 and MSP430FG6625 are microcontrollers with a high-performance 16-bit analog-to-digital converter (ADC), dual 12-bit digital-to-analog converters (DACs), dual operational amplifiers, a comparator, two universal serial communication interfaces (USCIs), USB 2.0, a hardware multiplier, DMA, four 16-bit timers, a real-time clock (RTC) module with alarm capabilities, an LCD driver, and up to 73 I/O pins.

The MSP430FG6426 and MSP430FG6425 are microcontrollers with a high-performance 16-bit ADC, dual 12-bit DACs, dual low-power operational amplifiers, a comparator, two USCIs, a 3.3-V LDO, a hardware multiplier, DMA, four 16-bit timers, an RTC module with alarm capabilities, an LCD driver, and up to 73 I/O pins.

Typical applications for these devices include analog and digital sensor systems, hand-held meters, such as medical diagnostic meters, measurement equipment, and hand-held industrial testers.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE ⁽²⁾ |
|------------------|-----------|--------------------------|
| MSP430FG6626IPZ | PZ (100) | 14 mm x 14 mm |
| MSP430FG6626IZQW | ZQW (113) | 7 mm x 7 mm |

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in [Section 9](#), or see the TI website at www.ti.com.

(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 9](#).

1.4 Functional Block Diagrams

Figure 1-1 shows the functional block diagram for the MSP430FG6626 and MSP430FG6625 devices.

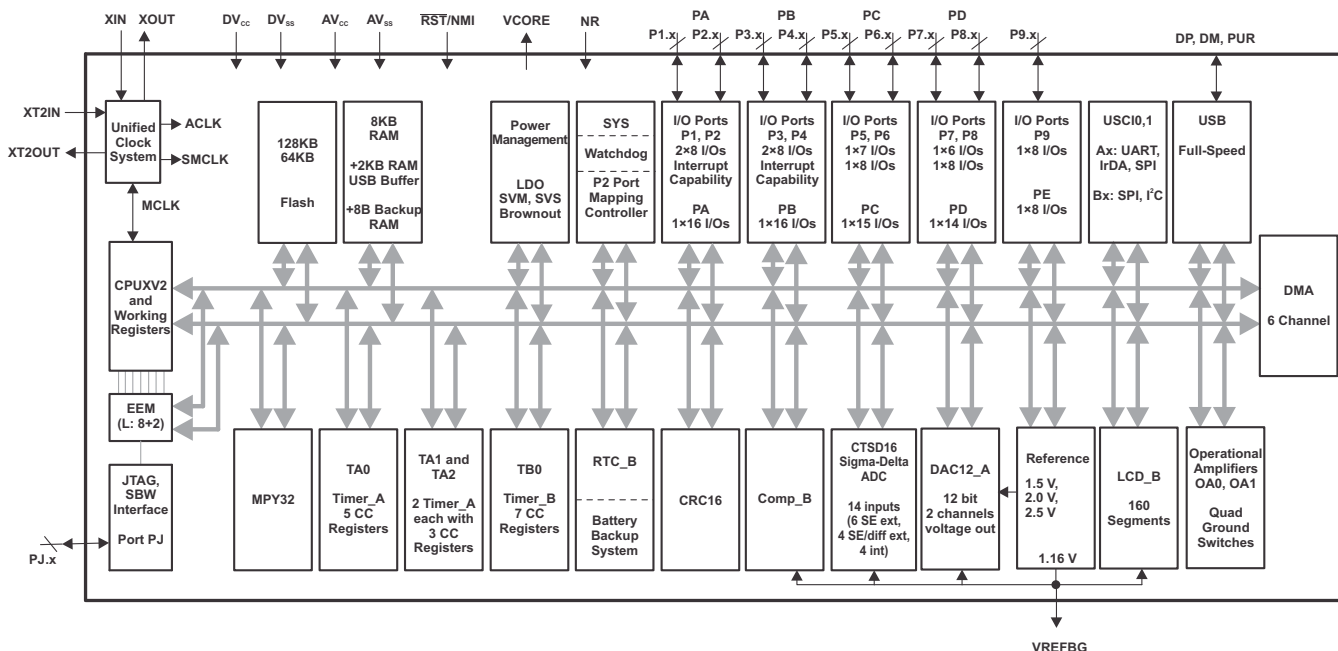


Figure 1-1. Functional Block Diagram – MSP430FG6626, MSP430FG6625

Figure 1-2 shows the functional block diagram for the MSP430FG6426 and MSP430FG6425 devices.

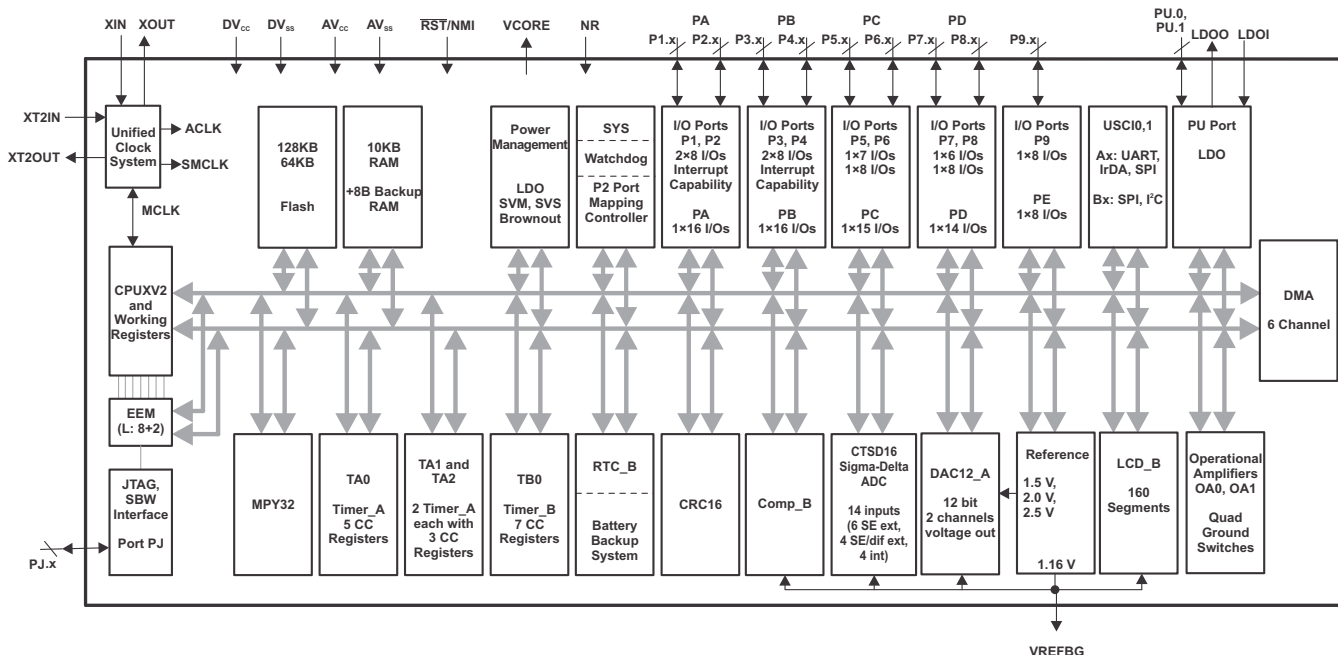


Figure 1-2. Functional Block Diagram – MSP430FG6426, MSP430FG6425

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2 Revision History

| DATE | REVISION | NOTES |
|----------|----------|-----------------|
| May 2015 | * | Initial Release |

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison⁽¹⁾⁽²⁾

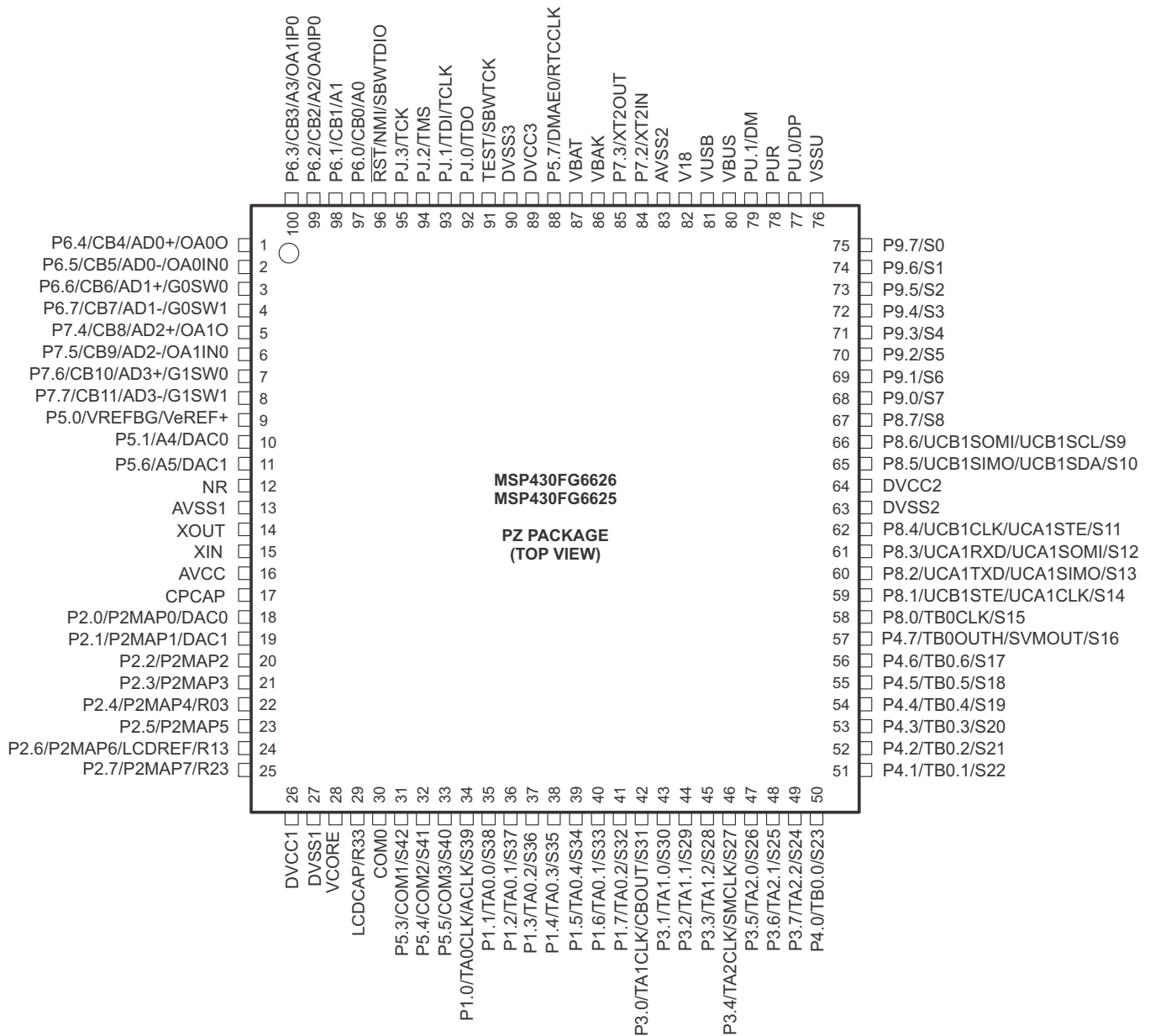
| DEVICE | FLASH (KB) | SRAM (KB) ⁽³⁾ | Timer_A ⁽⁴⁾ | Timer_B ⁽⁵⁾ | USCI | | CTSD16 (Ch) ⁽⁶⁾ | DAC12_A (Ch) | OA | Comp_B (Ch) | USB | I/O | PACKAGE |
|--------------|------------|--------------------------|------------------------|------------------------|----------------------------|----------------------------------|----------------------------|--------------|----|-------------|-----|-----|-------------------|
| | | | | | CHANNEL A: UART, IrDA, SPI | CHANNEL B: SPI, I ² C | | | | | | | |
| MSP430FG6626 | 128 | 8 + 2 | 5, 3, 3 | 7 | 2 | 2 | 10 ext, 5 int | 2 | 2 | 12 | 1 | 73 | 100 PZ 113 ZQW |
| MSP430FG6625 | 64 | 8 + 2 | 5, 3, 3 | 7 | 2 | 2 | 10 ext, 5 int | 2 | 2 | 12 | 1 | 73 | 100 PZ 113 ZQW |
| MSP430FG6426 | 128 | 10 | 5, 3, 3 | 7 | 2 | 2 | 10 ext, 5 int | 2 | 2 | 12 | 0 | 73 | 100 PZ 113 ZQW |
| MSP430FG6425 | 64 | 10 | 5, 3, 3 | 7 | 2 | 2 | 10 ext, 5 int | 2 | 2 | 12 | 0 | 73 | 100 PZ 113 ZQW |

- (1) For the most current package and ordering information, see the *Package Option Addendum* in Section 9, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
- (3) The additional 2KB of USB SRAM that is listed can be used as general-purpose SRAM when USB is not in use.
- (4) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (5) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (6) ADC inputs consist of a mix of single ended and differential. Refer to the pinning for available input pairs and types.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

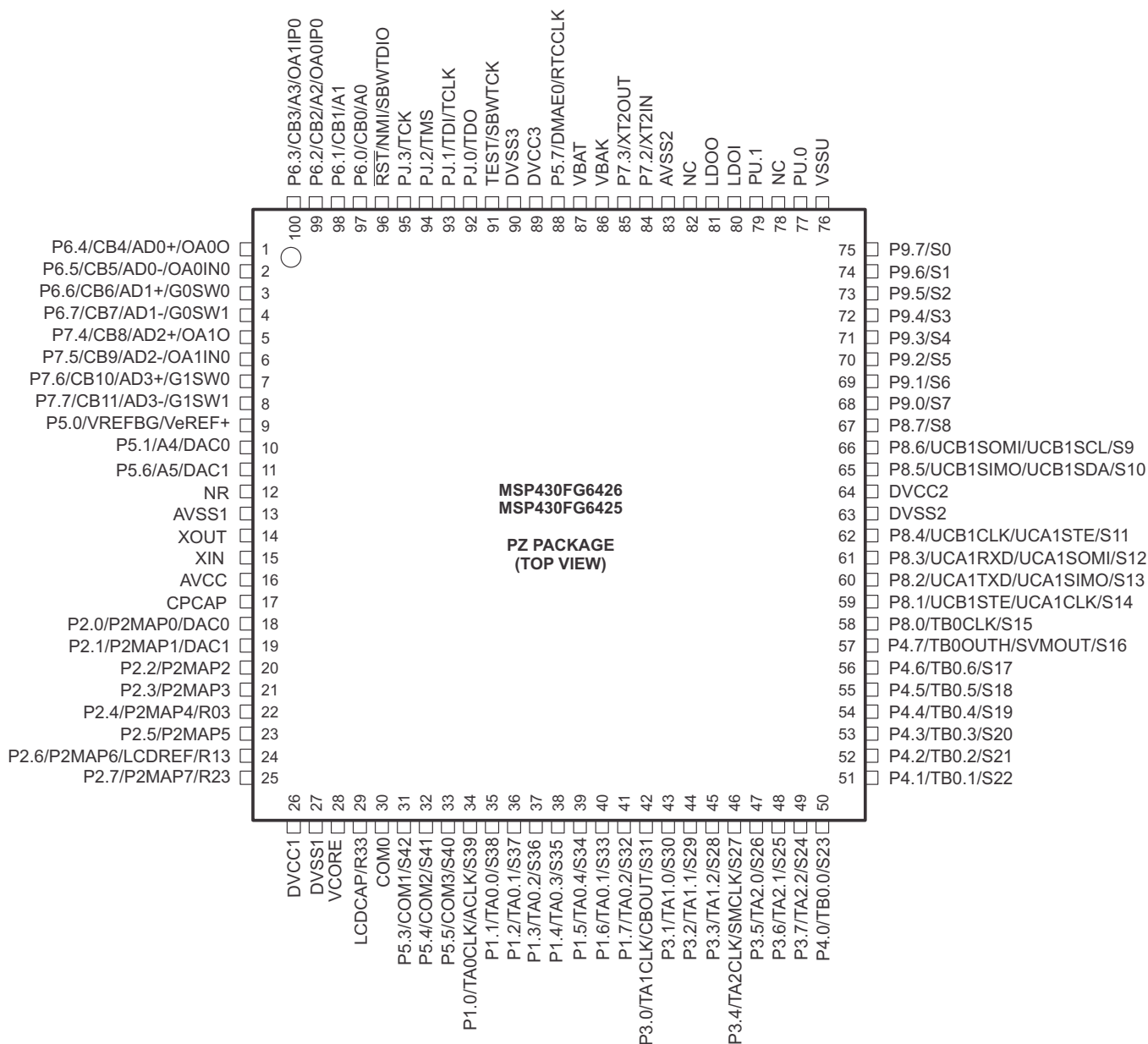
Figure 4-1 shows the pin assignments for the MSP430FG6626 and MSP430FG6625 devices in the 100-pin PZ package.



CAUTION: LDCAP/R33 must be connected to DV_{SS} if not used.

Figure 4-1. 100-Pin PZ Package (Top View), MSP430FG6626IPZ, MSP430FG6625IPZ

Figure 4-2 shows the pin assignments for the MSP430FG6426 and MSP430FG6425 devices in the 100-pin PZ package.



CAUTION: LDCAP/R33 must be connected to DV_{SS} if not used.

Figure 4-2. 100-Pin PZ Package (Top View), MSP430FG6426IPZ, MSP430FG6425IPZ

Figure 4-3 shows the pin assignments for the 113-pin ZQW package.



NOTE: For terminal assignments, see [Table 4-2](#).

**Figure 4-3. 113-Pin ZQW Package (Top View), MSP430FG6626IZQW, MSP430FG6625IZQW,
MSP430FG6426IZQW, MSP430FG6425IZQW**

4.2 Pin Attributes

Table 4-1 describes the attributes of the pins.

Table 4-1. Pin Attributes

| PIN NO. | | SIGNAL NAME ⁽¹⁾ ⁽²⁾ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE ⁽⁵⁾ | RESET STATE AFTER BOR ⁽⁶⁾ ⁽⁷⁾ |
|---------|-----|---|----------------------------|----------------------------|-----------------------------|---|
| PZ | ZQW | | | | | |
| 1 | A1 | P6.4 | I/O | LVC MOS | DVCC | OFF |
| | | CB4 | I | Analog | DVCC | N/A |
| | | AD0+ | I | Analog | DVCC | N/A |
| | | OA0O | O | Analog | DVCC | N/A |
| 2 | B2 | P6.5 | I/O | LVC MOS | DVCC | OFF |
| | | CB5 | I | Analog | DVCC | N/A |
| | | AD0- | I | Analog | DVCC | N/A |
| | | OA0IN0 | I | Analog | DVCC | N/A |
| 3 | B1 | P6.6 | I/O | LVC MOS | DVCC | OFF |
| | | CB6 | I | Analog | DVCC | N/A |
| | | AD1+ | I | Analog | DVCC | N/A |
| | | G0SW0 | I | Analog | DVCC | N/A |
| 4 | C3 | P6.7 | I/O | LVC MOS | DVCC | OFF |
| | | CB7 | I | Analog | DVCC | N/A |
| | | AD1- | I | Analog | DVCC | N/A |
| | | G0SW1 | I | Analog | DVCC | N/A |
| 5 | C2 | P7.4 | I/O | LVC MOS | DVCC | OFF |
| | | CB8 | I | Analog | DVCC | N/A |
| | | AD2+ | I | Analog | DVCC | N/A |
| | | OA1O | O | Analog | DVCC | N/A |
| 6 | C1 | P7.5 | I/O | LVC MOS | DVCC | OFF |
| | | CB9 | I | Analog | DVCC | N/A |
| | | AD2- | I | Analog | DVCC | N/A |
| | | OA1IN0 | I | Analog | DVCC | N/A |
| 7 | D4 | P7.6 | I/O | LVC MOS | DVCC | OFF |
| | | CB10 | I | Analog | DVCC | N/A |
| | | AD3+ | I | Analog | DVCC | N/A |
| | | G1SW0 | I | Analog | DVCC | N/A |
| 8 | D2 | P7.7 | I/O | LVC MOS | DVCC | OFF |
| | | CB11 | I | Analog | DVCC | N/A |
| | | AD3- | I | Analog | DVCC | N/A |
| | | G1SW1 | I | Analog | DVCC | N/A |

(1) For each multiplexed pin, the signal that is listed first in this table is the reset default.

(2) To determine the pin mux encodings for each pin, refer to [Section 6.12.23, Input/Output Schematics](#).

(3) Signal Types: I = Input, O = Output, I/O = Input or Output, P = power

(4) Buffer Types: LVC MOS, HVCMOS, Analog, or Power (see [Table 4-3](#) for details).

(5) The power source shown in this table is the I/O power source, which may differ from the module power source.

(6) Reset States:

OFF = High-impedance input with pullup or pulldown disabled (if available)

HiZ = High-impedance (neither input nor output)

PD = High-impedance input with pulldown enabled

PU = High-impedance input with pullup enabled

DRIVE0 = Drive output low

DRIVE1 = Drive output high

N/A = Not applicable

(7) For Debug pins: Emu = with emulator attached at reset, No Emu = without emulator attached at reset

Table 4-1. Pin Attributes (continued)

| PIN NO. | | SIGNAL NAME ⁽¹⁾ ⁽²⁾ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE ⁽⁵⁾ | RESET STATE AFTER BOR ⁽⁶⁾ ⁽⁷⁾ |
|---------|--------|---|----------------------------|----------------------------|-----------------------------|---|
| PZ | ZQW | | | | | |
| 9 | D1 | P5.0 | I/O | LVC MOS | DVCC | OFF |
| | | VREFBG | O | Analog | DVCC | N/A |
| | | VeREF+ | I | Analog | N/A | N/A |
| 10 | E4 | P5.1 | I/O | LVC MOS | DVCC | OFF |
| | | A4 | I | Analog | DVCC | N/A |
| | | DAC0 | O | Analog | DVCC | N/A |
| 11 | E2 | P5.6 | I/O | LVC MOS | DVCC | OFF |
| | | A5 | I | Analog | DVCC | N/A |
| | | DAC1 | O | Analog | DVCC | N/A |
| 12 | E1 | NR | I | Analog | N/A | N/A |
| 13 | F2 | AVSS1 | P | Power | N/A | N/A |
| 14 | F1 | XOUT | O | Analog | N/A | N/A |
| 15 | G1 | XIN | I | Analog | N/A | N/A |
| 16 | H1, G2 | DVCC | P | Power | N/A | N/A |
| 17 | G4 | CPCAP | I/O | Analog | DVCC | N/A |
| 18 | H2 | P2.0 | I/O | LVC MOS | DVCC | OFF |
| | | P2MAP0 | I/O | LVC MOS | DVCC | N/A |
| | | DAC0 | O | Analog | DVCC | N/A |
| 19 | J1 | P2.1 | I/O | LVC MOS | DVCC | OFF |
| | | P2MAP1 | I/O | LVC MOS | DVCC | N/A |
| | | DAC1 | O | Analog | DVCC | N/A |
| 20 | H4 | P2.2 | I/O | LVC MOS | DVCC | OFF |
| | | P2MAP2 | I/O | LVC MOS | DVCC | N/A |
| 21 | J2 | P2.3 | I/O | LVC MOS | DVCC | OFF |
| | | P2MAP3 | I/O | LVC MOS | DVCC | N/A |
| 22 | K1 | P2.4 | I/O | LVC MOS | DVCC | OFF |
| | | P2MAP4 | I/O | LVC MOS | DVCC | N/A |
| | | R03 | I/O | Analog | DVCC | N/A |
| 23 | K2 | P2.5 | I/O | LVC MOS | DVCC | OFF |
| | | P2MAP5 | I/O | LVC MOS | DVCC | N/A |
| 24 | L2 | P2.6 | I/O | LVC MOS | DVCC | OFF |
| | | P2MAP6 | I/O | LVC MOS | DVCC | N/A |
| | | LCDREF | I | Analog | N/A | N/A |
| | | R13 | I/O | Analog | DVCC | N/A |
| 25 | L3 | P2.7 | I/O | LVC MOS | DVCC | OFF |
| | | P2MAP7 | I/O | LVC MOS | DVCC | N/A |
| | | R23 | I/O | Analog | DVCC | N/A |
| 26 | L1 | DVCC1 | P | Power | N/A | N/A |
| 27 | M1 | DVSS1 | P | Power | N/A | N/A |
| 28 | M2 | VCORE | P | Power | DVCC | N/A |
| 29 | M3 | LDCAP | I/O | Analog | DVCC | N/A |
| | | R33 | I/O | Analog | DVCC | N/A |
| 30 | J4 | COM0 | O | Analog | DVCC | N/A |
| 31 | L4 | P5.3 | I/O | LVC MOS | DVCC | OFF |
| | | COM1 | O | Analog | DVCC | N/A |
| | | S42 | O | Analog | DVCC | N/A |

Table 4-1. Pin Attributes (continued)

| PIN NO. | | SIGNAL NAME ⁽¹⁾ ⁽²⁾ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE ⁽⁵⁾ | RESET STATE AFTER BOR ⁽⁶⁾ ⁽⁷⁾ |
|---------|-----|---|----------------------------|----------------------------|-----------------------------|---|
| PZ | ZQW | | | | | |
| 32 | M4 | P5.4 | I/O | LVC MOS | DVCC | OFF |
| | | COM2 | O | LVC MOS | DVCC | N/A |
| | | S41 | O | Analog | DVCC | N/A |
| 33 | J5 | P5.5 | I/O | LVC MOS | DVCC | OFF |
| | | COM3 | I/O | LVC MOS | DVCC | N/A |
| | | S40 | O | Analog | DVCC | N/A |
| 34 | L5 | P1.0 | I/O | LVC MOS | DVCC | OFF |
| | | TA0CLK | I | LVC MOS | DVCC | N/A |
| | | ACLK | O | LVC MOS | DVCC | N/A |
| | | S39 | O | Analog | DVCC | N/A |
| 35 | M5 | P1.1 | I/O | LVC MOS | DVCC | OFF |
| | | TA0.0 | I/O | LVC MOS | DVCC | N/A |
| | | BSLTX | O | LVC MOS | DVCC | N/A |
| | | S38 | O | Analog | DVCC | N/A |
| 36 | J6 | P1.2 | I/O | LVC MOS | DVCC | OFF |
| | | TA0.1 | I/O | LVC MOS | DVCC | N/A |
| | | BSLRX | I | LVC MOS | DVCC | N/A |
| | | S37 | O | Analog | DVCC | N/A |
| 37 | H6 | P1.3 | I/O | LVC MOS | DVCC | OFF |
| | | TA0.2 | I/O | LVC MOS | DVCC | N/A |
| | | S36 | O | Analog | DVCC | N/A |
| 38 | M6 | P1.4 | I/O | LVC MOS | DVCC | OFF |
| | | TA0.3 | I/O | LVC MOS | DVCC | N/A |
| | | S35 | O | Analog | DVCC | N/A |
| 39 | L6 | P1.5 | I/O | LVC MOS | DVCC | OFF |
| | | TA0.4 | I/O | LVC MOS | DVCC | N/A |
| | | S34 | O | Analog | DVCC | N/A |
| 40 | J7 | P1.6 | I/O | LVC MOS | DVCC | OFF |
| | | TA0.1 | I/O | LVC MOS | DVCC | N/A |
| | | S33 | O | Analog | DVCC | N/A |
| 41 | M7 | P1.7 | I/O | LVC MOS | DVCC | OFF |
| | | TA0.2 | I/O | LVC MOS | DVCC | N/A |
| | | S32 | O | Analog | DVCC | N/A |
| 42 | L7 | P3.0 | I/O | LVC MOS | DVCC | OFF |
| | | TA1CLK | I | LVC MOS | DVCC | N/A |
| | | CBOUT | O | LVC MOS | DVCC | N/A |
| | | S31 | O | Analog | DVCC | N/A |
| 43 | H7 | P3.1 | I/O | LVC MOS | DVCC | OFF |
| | | TA1.0 | I/O | LVC MOS | DVCC | N/A |
| | | S30 | O | Analog | DVCC | N/A |
| 44 | M8 | P3.2 | I/O | LVC MOS | DVCC | OFF |
| | | TA1.1 | I/O | LVC MOS | DVCC | N/A |
| | | S29 | O | Analog | DVCC | N/A |
| 45 | L8 | P3.3 | I/O | LVC MOS | DVCC | OFF |
| | | TA1.2 | I/O | LVC MOS | DVCC | N/A |
| | | S28 | O | Analog | DVCC | N/A |

Table 4-1. Pin Attributes (continued)

| PIN NO. | | SIGNAL NAME ⁽¹⁾ ⁽²⁾ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE ⁽⁵⁾ | RESET STATE AFTER BOR ⁽⁶⁾ ⁽⁷⁾ |
|---------|-----|---|----------------------------|----------------------------|-----------------------------|---|
| PZ | ZQW | | | | | |
| 46 | J8 | P3.4 | I/O | LVC MOS | DVCC | OFF |
| | | TA2CLK | I | LVC MOS | DVCC | N/A |
| | | SMCLK | O | LVC MOS | DVCC | N/A |
| | | S27 | O | Analog | DVCC | N/A |
| 47 | M9 | P3.5 | I/O | LVC MOS | DVCC | OFF |
| | | TA2.0 | I/O | LVC MOS | DVCC | N/A |
| | | S26 | O | Analog | DVCC | N/A |
| 48 | L9 | P3.6 | I/O | LVC MOS | DVCC | OFF |
| | | TA2.1 | I/O | LVC MOS | DVCC | N/A |
| | | S25 | O | Analog | DVCC | N/A |
| 49 | M10 | P3.7 | I/O | LVC MOS | DVCC | OFF |
| | | TA2.2 | I/O | LVC MOS | DVCC | N/A |
| | | S24 | O | Analog | DVCC | N/A |
| 50 | J9 | P4.0 | I/O | LVC MOS | DVCC | OFF |
| | | TB0.0 | I/O | LVC MOS | DVCC | N/A |
| | | S23 | O | Analog | DVCC | N/A |
| 51 | M11 | P4.1 | I/O | LVC MOS | DVCC | OFF |
| | | TB0.1 | I/O | LVC MOS | DVCC | N/A |
| | | S22 | O | Analog | DVCC | N/A |
| 52 | L10 | P4.2 | I/O | LVC MOS | DVCC | OFF |
| | | TB0.2 | I/O | LVC MOS | DVCC | N/A |
| | | S21 | O | Analog | DVCC | N/A |
| 53 | M12 | P4.3 | I/O | LVC MOS | DVCC | OFF |
| | | TB0.3 | I/O | LVC MOS | DVCC | N/A |
| | | S20 | O | Analog | DVCC | N/A |
| 54 | L12 | P4.4 | I/O | LVC MOS | DVCC | OFF |
| | | TB0.4 | I/O | LVC MOS | DVCC | N/A |
| | | S19 | O | Analog | DVCC | N/A |
| 55 | L11 | P4.5 | I/O | LVC MOS | DVCC | OFF |
| | | TB0.5 | I/O | LVC MOS | DVCC | N/A |
| | | S18 | O | Analog | DVCC | N/A |
| 56 | K11 | P4.6 | I/O | LVC MOS | DVCC | OFF |
| | | TB0.6 | I/O | LVC MOS | DVCC | N/A |
| | | S17 | O | Analog | DVCC | N/A |
| 57 | K12 | P4.7 | I/O | LVC MOS | DVCC | OFF |
| | | TB0OUTH | I | LVC MOS | DVCC | N/A |
| | | SVMOUT | O | LVC MOS | DVCC | N/A |
| | | S16 | O | Analog | DVCC | N/A |
| 58 | J11 | P8.0 | I/O | LVC MOS | DVCC | OFF |
| | | TB0CLK | I | LVC MOS | DVCC | N/A |
| | | S15 | O | Analog | DVCC | N/A |
| 59 | J12 | P8.1 | I/O | LVC MOS | DVCC | OFF |
| | | UCB1STE | I/O | LVC MOS | DVCC | N/A |
| | | UCA1CLK | I/O | LVC MOS | DVCC | N/A |
| | | S14 | O | Analog | DVCC | N/A |

Table 4-1. Pin Attributes (continued)

| PIN NO. | | SIGNAL NAME ⁽¹⁾ ⁽²⁾ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE ⁽⁵⁾ | RESET STATE AFTER BOR ⁽⁶⁾ ⁽⁷⁾ |
|---------|----------|---|----------------------------|----------------------------|-----------------------------|---|
| PZ | ZQW | | | | | |
| 60 | H11 | P8.2 | I/O | LVC MOS | DVCC | OFF |
| | | UCA1TXD | O | LVC MOS | DVCC | N/A |
| | | UCA1SIMO | I/O | LVC MOS | DVCC | N/A |
| | | S13 | O | Analog | DVCC | N/A |
| 61 | H12 | P8.3 | I/O | LVC MOS | DVCC | OFF |
| | | UCA1RXD | I | LVC MOS | DVCC | N/A |
| | | UCA1SOMI | I/O | LVC MOS | DVCC | N/A |
| | | S12 | O | Analog | DVCC | N/A |
| 62 | G11 | P8.4 | I/O | LVC MOS | DVCC | OFF |
| | | UCB1CLK | I/O | LVC MOS | DVCC | N/A |
| | | UCA1STE | I/O | LVC MOS | DVCC | N/A |
| | | S11 | O | Analog | DVCC | N/A |
| 63 | G12 | DVSS2 | P | Power | N/A | N/A |
| 64 | F12 | DVCC2 | P | Power | N/A | N/A |
| 65 | F11 | P8.5 | I/O | LVC MOS | DVCC | OFF |
| | | UCB1SIMO | I/O | LVC MOS | DVCC | N/A |
| | | UCB1SDA | I/O | LVC MOS | DVCC | N/A |
| | | S10 | O | Analog | DVCC | N/A |
| 66 | G9 | P8.6 | I/O | LVC MOS | DVCC | OFF |
| | | UCB1SOMI | I/O | LVC MOS | DVCC | N/A |
| | | UCB1SCL | I/O | LVC MOS | DVCC | N/A |
| | | S9 | O | Analog | DVCC | N/A |
| 67 | E12 | P8.7 | I/O | LVC MOS | DVCC | OFF |
| | | S8 | O | Analog | DVCC | N/A |
| 68 | E11 | P9.0 | I/O | LVC MOS | DVCC | OFF |
| | | S7 | O | Analog | DVCC | N/A |
| 69 | F9 | P9.1 | I/O | LVC MOS | DVCC | OFF |
| | | S6 | O | Analog | DVCC | N/A |
| 70 | D12 | P9.2 | I/O | LVC MOS | DVCC | OFF |
| | | S5 | O | Analog | DVCC | N/A |
| 71 | D11 | P9.3 | I/O | LVC MOS | DVCC | OFF |
| | | S4 | O | Analog | DVCC | N/A |
| 72 | E9 | P9.4 | I/O | LVC MOS | DVCC | OFF |
| | | S3 | O | Analog | DVCC | N/A |
| 73 | C12 | P9.5 | I/O | LVC MOS | DVCC | OFF |
| | | S2 | O | Analog | DVCC | N/A |
| 74 | C11 | P9.6 | I/O | LVC MOS | DVCC | OFF |
| | | S1 | O | Analog | DVCC | N/A |
| 75 | D9 | P9.7 | I/O | LVC MOS | DVCC | OFF |
| | | S0 | O | Analog | DVCC | N/A |
| 76 | B11, B12 | VSSU | P | Power | N/A | N/A |
| 77 | A12 | PU.0 | I/O | HVCMOS | VBUS | HiZ |
| | | DP | I/O | HVCMOS | VBUS | N/A |
| 78 | B10 | PUR (FG662x only) | I/O | HVCMOS/open-drain | VBUS | HiZ |
| | | NC (FG642x only) | I/O | N/A | N/A | N/A |

Table 4-1. Pin Attributes (continued)

| PIN NO. | | SIGNAL NAME ⁽¹⁾ ⁽²⁾ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE ⁽⁵⁾ | RESET STATE AFTER BOR ⁽⁶⁾ ⁽⁷⁾ |
|---------|-----|---|----------------------------|----------------------------|-----------------------------|---|
| PZ | ZQW | | | | | |
| 79 | A11 | PU.1 | I/O | HVCMOS | VBUS | HiZ |
| | | DM | I/O | HVCMOS | VBUS | N/A |
| 80 | A10 | VBUS | I | Power | N/A | N/A |
| | | LDOI | I | Analog | External | N/A |
| 81 | A9 | VUSB | O | Power | N/A | N/A |
| | | LDOO | O | Analog | VBUS | N/A |
| 82 | B9 | V18 (FG662x only) | O | Power | N/A | N/A |
| | | NC (FG642x only) | – | N/A | N/A | N/A |
| 83 | A8 | AVSS2 | P | Power | N/A | N/A |
| 84 | B8 | P7.2 | I/O | LVC MOS | DVCC | OFF |
| | | XT2IN | I | Analog | DVCC | N/A |
| 85 | B7 | P7.3 | I/O | LVC MOS | DVCC | OFF |
| | | XT2OUT | O | Analog | DVCC | N/A |
| 86 | A7 | VBAK | I/O | Analog | N/A | N/A |
| 87 | D8 | VBAT | P | Power | N/A | N/A |
| 88 | D7 | P5.7 | I/O | LVC MOS | DVCC | OFF |
| | | DMAE0 | I | LVC MOS | DVCC | N/A |
| | | RTCCLK | O | LVC MOS | DVCC | N/A |
| 89 | A6 | DVCC3 | P | Power | N/A | N/A |
| 90 | A5 | DVSS3 | P | Power | N/A | N/A |
| 91 | B6 | TEST | I | LVC MOS | DVCC | No Emu: PD Emu: PD |
| | | SBWTCK | I | LVC MOS | DVCC | N/A |
| 92 | B5 | PJ.0 | I/O | LVC MOS | DVCC | OFF |
| | | TDO | O | LVC MOS | DVCC | No Emu: OFF Emu: DRIVE0 |
| 93 | A4 | PJ.1 | I/O | LVC MOS | DVCC | OFF |
| | | TDI | I | LVC MOS | DVCC | No Emu: OFF Emu: PU |
| | | TCLK | I | LVC MOS | DVCC | No Emu: OFF Emu: OFF |
| 94 | E7 | PJ.2 | I/O | LVC MOS | DVCC | OFF |
| | | TMS | I | LVC MOS | DVCC | No Emu: OFF Emu: PU |
| 95 | D6 | PJ.3 | I/O | LVC MOS | DVCC | OFF |
| | | TCK | I | LVC MOS | DVCC | No Emu: OFF Emu: PU |
| 96 | A3 | $\overline{\text{RST}}$ | I/O | LVC MOS | DVCC | PU |
| | | NMI | I | LVC MOS | DVCC | N/A |
| | | SBWTDIO | I/O | LVC MOS | DVCC | PU |
| 97 | B4 | P6.0 | I/O | LVC MOS | DVCC | OFF |
| | | CB0 | I | Analog | DVCC | N/A |
| | | A0 | I | Analog | DVCC | N/A |
| 98 | B3 | P6.1 | I/O | LVC MOS | DVCC | OFF |
| | | CB1 | I | Analog | DVCC | N/A |
| | | A1 | I | Analog | DVCC | N/A |

Table 4-1. Pin Attributes (continued)

| PIN NO. | | SIGNAL NAME ⁽¹⁾ ⁽²⁾ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE ⁽⁵⁾ | RESET STATE AFTER BOR ⁽⁶⁾ ⁽⁷⁾ |
|---------|---|---|----------------------------|----------------------------|-----------------------------|---|
| PZ | ZQW | | | | | |
| 99 | A2 | P6.2 | I/O | LVC MOS | DVCC | OFF |
| | | CB2 | I | Analog | DVCC | N/A |
| | | A2 | I | Analog | DVCC | N/A |
| | | OA0IP0 | I | Analog | DVCC | N/A |
| 100 | D5 | P6.3 | I/O | LVC MOS | DVCC | OFF |
| | | CB3 | I | Analog | DVCC | N/A |
| | | A3 | I | Analog | DVCC | N/A |
| | | OA1IP0 | I | Analog | DVCC | N/A |
| N/A | E5, E6, E8, F4, F5, F8, G5, G8, H5, H8, H9 | Reserved | - | - | - | - |

4.3 Signal Descriptions

Table 4-2 describes the signals for all device variants and package options.

Table 4-2. Signal Descriptions

| FUNCTION | SIGNAL NAME | PIN NO. | | PIN TYPE ⁽¹⁾ | DESCRIPTION |
|-------------|-------------|---------|-----|-------------------------|---|
| | | PZ | ZQW | | |
| ADC | A0 | 97 | B4 | I | ADC analog single ended input A0 |
| | A1 | 98 | B3 | I | ADC analog single ended input A1 |
| | A2 | 99 | A2 | I | ADC analog single ended input A2 |
| | A3 | 100 | D5 | I | ADC analog single ended input A3 |
| | A4 | 10 | E4 | I | ADC analog single ended input A4 |
| | A5 | 11 | E2 | I | ADC analog single ended input A5 |
| | AD0+ | 1 | A1 | I | ADC positive analog differential input AD0+ |
| | AD0- | 2 | B2 | I | ADC negative analog differential input AD0- |
| | AD1+ | 3 | B1 | I | ADC positive analog differential input AD1+ |
| | AD1- | 4 | C3 | I | ADC negative analog differential input AD1- |
| | AD2+ | 5 | C2 | I | ADC positive analog differential input AD2+ |
| | AD2- | 6 | C1 | I | ADC negative analog differential input AD2- |
| | AD3+ | 7 | D4 | I | ADC positive analog differential input AD3+ |
| | AD3- | 8 | D2 | I | ADC negative analog differential input AD3- |
| | VeREF+ | 9 | D1 | I | Input for an external reference voltage to the ADC and DAC |
| BSL | BSLRX | 36 | J6 | I | BSL receive input |
| | BSLTX | 35 | M5 | O | BSL transmit output |
| Backup | VBAK | 86 | A7 | I/O | Capacitor for backup subsystem. Do not load this pin externally. For capacitor values, see C _{BAK} in Recommended Operating Conditions . |
| | VBAT | 87 | D8 | P | Backup or secondary supply voltage. If backup voltage is not supplied, connect to DVCC externally. |
| Charge Pump | CPCAP | 17 | G4 | I/O | Capacitor for op amp and CTSD16 rail-to-rail charge pump |
| Clock | ACLK | 34 | L5 | O | ACLK output (divided by 1, 2, 4, 8, 16, or 32) |
| | RTCCLK | 88 | D7 | O | RTCCLK output |
| | SMCLK | 46 | J8 | O | SMCLK output |
| | XIN | 15 | G1 | I | Input terminal for crystal oscillator XT1 |
| | XOUT | 14 | F1 | O | Output terminal of crystal oscillator XT1 |
| | XT2IN | 84 | B8 | I | Input terminal for crystal oscillator XT2 |
| | XT2OUT | 85 | B7 | O | Output terminal of crystal oscillator XT2 |
| Comparator | CB0 | 97 | B4 | I | Comparator_B input CB0 |
| | CB1 | 98 | B3 | I | Comparator_B input CB1 |
| | CB2 | 99 | A2 | I | Comparator_B input CB2 |
| | CB3 | 100 | D5 | I | Comparator_B input CB3 |
| | CB4 | 1 | A1 | I | Comparator_B input CB4 |
| | CB5 | 2 | B2 | I | Comparator_B input CB5 |
| | CB6 | 3 | B1 | I | Comparator_B input CB6 |
| | CB7 | 4 | C3 | I | Comparator_B input CB7 |
| | CB8 | 5 | C2 | I | Comparator_B input CB8 |
| | CB9 | 6 | C1 | I | Comparator_B input CB9 |
| | CB10 | 7 | D4 | I | Comparator_B input CB10 |
| | CB11 | 8 | D2 | I | Comparator_B input CB11 |
| | | CBOUT | 42 | L7 | O |

(1) I = input, O = output, I/O = input or output, P = power

Table 4-2. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | | PIN TYPE ⁽¹⁾ | DESCRIPTION |
|----------|-------------|----------|----------|-------------------------|---|
| | | PZ | ZQW | | |
| DAC | DAC0 | 10 18 | E4 H2 | O | DAC output channel 0 |
| | DAC1 | 11 19 | E2 J1 | O | DAC output channel 1 |
| DMA | DMAE0 | 88 | D7 | I | DMA external trigger input |
| Debug | SBWTCK | 91 | B6 | I | Spy-Bi-Wire input clock |
| | TCK | 95 | D6 | I | Test clock |
| | TCLK | 93 | A4 | I | Test clock input |
| | TDI | 93 | A4 | I | Test data input |
| | TDO | 92 | B5 | O | Test data output |
| | TEST | 91 | B6 | I | Test mode pin; selects digital I/O on JTAG pins |
| | TMS | 94 | E7 | I | Test mode select |
| | SBWTDIO | 96 | A3 | I/O | Spy-Bi-Wire data input/output |
| GPIO | P1.0 | 34 | L5 | I/O | General-purpose digital I/O with port interrupt |
| | P1.1 | 35 | M5 | I/O | General-purpose digital I/O with port interrupt |
| | P1.2 | 36 | J6 | I/O | General-purpose digital I/O with port interrupt |
| | P1.3 | 37 | H6 | I/O | General-purpose digital I/O with port interrupt |
| | P1.4 | 38 | M6 | I/O | General-purpose digital I/O with port interrupt |
| | P1.5 | 39 | L6 | I/O | General-purpose digital I/O with port interrupt |
| | P1.6 | 40 | J7 | I/O | General-purpose digital I/O with port interrupt |
| | P1.7 | 41 | M7 | I/O | General-purpose digital I/O with port interrupt |
| | P2.0 | 18 | H2 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.1 | 19 | J1 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.2 | 20 | H4 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.3 | 21 | J2 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.4 | 22 | K1 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.5 | 23 | K2 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.6 | 24 | L2 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.7 | 25 | L3 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P3.0 | 42 | L7 | I/O | General-purpose digital I/O with port interrupt |
| | P3.1 | 43 | H7 | I/O | General-purpose digital I/O with port interrupt |
| | P3.2 | 44 | M8 | I/O | General-purpose digital I/O with port interrupt |
| | P3.3 | 45 | L8 | I/O | General-purpose digital I/O with port interrupt |
| | P3.4 | 46 | J8 | I/O | General-purpose digital I/O with port interrupt |
| | P3.5 | 47 | M9 | I/O | General-purpose digital I/O with port interrupt |
| | P3.6 | 48 | L9 | I/O | General-purpose digital I/O with port interrupt |
| | P3.7 | 49 | M10 | I/O | General-purpose digital I/O with port interrupt |

Table 4-2. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | | PIN TYPE ⁽¹⁾ | DESCRIPTION |
|----------|-------------|---------|-----|-----------------------------|---|
| | | PZ | ZQW | | |
| GPIO | P4.0 | 50 | J9 | I/O | General-purpose digital I/O with port interrupt |
| | P4.1 | 51 | M11 | I/O | General-purpose digital I/O with port interrupt |
| | P4.2 | 52 | L10 | I/O | General-purpose digital I/O with port interrupt |
| | P4.3 | 53 | M12 | I/O | General-purpose digital I/O with port interrupt |
| | P4.4 | 54 | L12 | I/O | General-purpose digital I/O with port interrupt |
| | P4.5 | 55 | L11 | I/O | General-purpose digital I/O with port interrupt |
| | P4.6 | 56 | K11 | I/O | General-purpose digital I/O with port interrupt |
| | P4.7 | 57 | K12 | I/O | General-purpose digital I/O with port interrupt |
| | P5.0 | 9 | D1 | I/O | General-purpose digital I/O |
| | P5.1 | 10 | E4 | I/O | General-purpose digital I/O |
| | P5.3 | 31 | L4 | I/O | General-purpose digital I/O |
| | P5.4 | 32 | M4 | I/O | General-purpose digital I/O |
| | P5.5 | 33 | J5 | I/O | General-purpose digital I/O |
| | P5.6 | 11 | E2 | I/O | General-purpose digital I/O |
| | P5.7 | 88 | D7 | I/O | General-purpose digital I/O |
| | P6.0 | 97 | B4 | I/O | General-purpose digital I/O |
| | P6.1 | 98 | B3 | I/O | General-purpose digital I/O |
| | P6.2 | 99 | A2 | I/O | General-purpose digital I/O |
| | P6.3 | 100 | D5 | I/O | General-purpose digital I/O |
| | P6.4 | 1 | A1 | I/O | General-purpose digital I/O |
| | P6.5 | 2 | B2 | I/O | General-purpose digital I/O |
| | P6.6 | 3 | B1 | I/O | General-purpose digital I/O |
| | P6.7 | 4 | C3 | I/O | General-purpose digital I/O |
| | P7.2 | 84 | B8 | I/O | General-purpose digital I/O |
| | P7.3 | 85 | B7 | I/O | General-purpose digital I/O |
| | P7.4 | 5 | C2 | I/O | General-purpose digital I/O |
| | P7.5 | 6 | C1 | I/O | General-purpose digital I/O |
| | P7.6 | 7 | D4 | I/O | General-purpose digital I/O |
| | P7.7 | 8 | D2 | I/O | General-purpose digital I/O |
| | P8.0 | 58 | J11 | I/O | General-purpose digital I/O |
| | P8.1 | 59 | J12 | I/O | General-purpose digital I/O |
| | P8.2 | 60 | H11 | I/O | General-purpose digital I/O |
| | P8.3 | 61 | H12 | I/O | General-purpose digital I/O |
| | P8.4 | 62 | G11 | I/O | General-purpose digital I/O |
| | P8.5 | 65 | F11 | I/O | General-purpose digital I/O |
| | P8.6 | 66 | G9 | I/O | General-purpose digital I/O |
| | P8.7 | 67 | E12 | I/O | General-purpose digital I/O |
| | P9.0 | 68 | E11 | I/O | General-purpose digital I/O |
| | P9.1 | 69 | F9 | I/O | General-purpose digital I/O |
| | P9.2 | 70 | D12 | I/O | General-purpose digital I/O |
| P9.3 | 71 | D11 | I/O | General-purpose digital I/O | |
| P9.4 | 72 | E9 | I/O | General-purpose digital I/O | |
| P9.5 | 73 | C12 | I/O | General-purpose digital I/O | |
| P9.6 | 74 | C11 | I/O | General-purpose digital I/O | |
| P9.7 | 75 | D9 | I/O | General-purpose digital I/O | |

Table 4-2. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | | PIN TYPE ⁽¹⁾ | DESCRIPTION |
|------------------|-------------|---------|-----|-------------------------|--|
| | | PZ | ZQW | | |
| GPIO | PJ.0 | 92 | B5 | I/O | General-purpose digital I/O |
| | PJ.1 | 93 | A4 | I/O | General-purpose digital I/O |
| | PJ.2 | 94 | E7 | I/O | General-purpose digital I/O |
| | PJ.3 | 95 | D6 | I/O | General-purpose digital I/O |
| | PU.0 | 77 | A12 | I/O | General-purpose digital I/O - controlled by USB control register (FG662x devices) or PU control register |
| | PU.1 | 79 | A11 | I/O | General-purpose digital I/O - controlled by USB control register (FG662x devices) or PU control register |
| Ground Switch | G0SW0 | 3 | B1 | I | Analog switch to AVSS. Internally connected to ADC positive analog differential input AD1+. |
| | G0SW1 | 4 | C3 | I | Analog switch to AVSS. Internally connected to ADC negative analog differential input AD1-. |
| | G1SW0 | 7 | D4 | I | Analog switch to AVSS. Internally connected to ADC positive analog differential input AD3+. |
| | G1SW1 | 8 | D2 | I | Analog switch to AVSS. Internally connected to ADC negative analog differential input AD3-. |
| I ² C | UCB1SCL | 66 | G9 | I/O | USCI_B1 I ² C clock |
| | UCB1SDA | 65 | F11 | I/O | USCI_B1 I ² C data |
| LCD | COM0 | 30 | J4 | O | LCD common output COM0 for LCD backplane |
| | COM1 | 31 | L4 | O | LCD common output COM1 for LCD backplane |
| | COM2 | 32 | M4 | O | LCD common output COM2 for LCD backplane |
| | COM3 | 33 | J5 | I/O | LCD common output COM3 for LCD backplane |
| | LDCAP | 29 | M3 | I/O | LCD capacitor connection CAUTION: LDCAP/R33 must be connected to DV _{SS} if not used. |
| | LCDREF | 24 | L2 | I | External reference voltage input for regulated LCD voltage |
| | R03 | 22 | K1 | I/O | Input/output port of lowest analog LCD voltage (V5) |
| | R13 | 24 | L2 | I/O | Input/output port of third most positive analog LCD voltage (V3 or V4) |
| | R23 | 25 | L3 | I/O | Input/output port of second most positive analog LCD voltage (V2) |
| | R33 | 29 | M3 | I/O | Input/output port of most positive analog LCD voltage (V1) CAUTION: LDCAP/R33 must be connected to DV _{SS} if not used. |
| | S0 | 75 | D9 | O | LCD segment output S0 |
| | S1 | 74 | C11 | O | LCD segment output S1 |
| | S2 | 73 | C12 | O | LCD segment output S2 |
| | S3 | 72 | E9 | O | LCD segment output S3 |
| | S4 | 71 | D11 | O | LCD segment output S4 |
| | S5 | 70 | D12 | O | LCD segment output S5 |
| | S6 | 69 | F9 | O | LCD segment output S6 |
| | S7 | 68 | E11 | O | LCD segment output S7 |
| | S8 | 67 | E12 | O | LCD segment output S8 |
| | S9 | 66 | G9 | O | LCD segment output S9 |
| | S10 | 65 | F11 | O | LCD segment output S10 |
| | S11 | 62 | G11 | O | LCD segment output S11 |
| | S12 | 61 | H12 | O | LCD segment output S12 |
| | S13 | 60 | H11 | O | LCD segment output S13 |
| | S14 | 59 | J12 | O | LCD segment output S14 |
| | S15 | 58 | J11 | O | LCD segment output S15 |
| S16 | 57 | K12 | O | LCD segment output S16 | |
| S17 | 56 | K11 | O | LCD segment output S17 | |
| S18 | 55 | L11 | O | LCD segment output S18 | |

Table 4-2. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | | PIN TYPE ⁽¹⁾ | DESCRIPTION |
|-----------------|-------------|---------|-----|-------------------------|--|
| | | PZ | ZQW | | |
| LCD | S19 | 54 | L12 | O | LCD segment output S19 |
| | S20 | 53 | M12 | O | LCD segment output S20 |
| | S21 | 52 | L10 | O | LCD segment output S21 |
| | S22 | 51 | M11 | O | LCD segment output S22 |
| | S23 | 50 | J9 | O | LCD segment output S23 |
| | S24 | 49 | M10 | O | LCD segment output S24 |
| | S25 | 48 | L9 | O | LCD segment output S25 |
| | S26 | 47 | M9 | O | LCD segment output S26 |
| | S27 | 46 | J8 | O | LCD segment output S27 |
| | S28 | 45 | L8 | O | LCD segment output S28 |
| | S29 | 44 | M8 | O | LCD segment output S29 |
| | S30 | 43 | H7 | O | LCD segment output S30 |
| | S31 | 42 | L7 | O | LCD segment output S31 |
| | S32 | 41 | M7 | O | LCD segment output S32 |
| | S33 | 40 | J7 | O | LCD segment output S33 |
| | S34 | 39 | L6 | O | LCD segment output S34 |
| | S35 | 38 | M6 | O | LCD segment output S35 |
| | S36 | 37 | H6 | O | LCD segment output S36 |
| | S37 | 36 | J6 | O | LCD segment output S37 |
| | S38 | 35 | M5 | O | LCD segment output S38 |
| | S39 | 34 | L5 | O | LCD segment output S39 |
| | S40 | 33 | J5 | O | LCD segment output S40 |
| | S41 | 32 | M4 | O | LCD segment output S41 |
| | S42 | 31 | L4 | O | LCD segment output S42 |
| Mappable | P2MAP0 | 18 | H2 | I/O | Default mapping: USCI_B0 SPI slave transmit enable; USCI_A0 clock input/output Mapping Options: See Table 6-8 |
| | P2MAP1 | 19 | J1 | I/O | Default mapping: USCI_B0 SPI slave in/master out; USCI_B0 I ² C data Mapping Options: See Table 6-8 |
| | P2MAP2 | 20 | H4 | I/O | Default mapping: USCI_B0 SPI slave out/master in; USCI_B0 I ² C clock Mapping Options: See Table 6-8 |
| | P2MAP3 | 21 | J2 | I/O | Default mapping: USCI_B0 clock input/output; USCI_A0 SPI slave transmit enable Mapping Options: See Table 6-8 |
| | P2MAP4 | 22 | K1 | I/O | Default mapping: USCI_A0 UART transmit data; USCI_A0 SPI slave in/master out Mapping Options: See Table 6-8 |
| | P2MAP5 | 23 | K2 | I/O | Default mapping: USCI_A0 UART receive data; USCI_A0 slave out/master in Mapping Options: See Table 6-8 |
| | P2MAP6 | 24 | L2 | I/O | Default mapping: no secondary function Mapping Options: See Table 6-8 |
| | P2MAP7 | 25 | L3 | I/O | Default mapping: no secondary function Mapping Options: See Table 6-8 |
| Noise Reduction | NR | 12 | E1 | I | Noise reduction. Connect pin to analog ground. |

Table 4-2. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | | PIN TYPE ⁽¹⁾ | DESCRIPTION |
|----------|----------------------|----------|---|-------------------------|---|
| | | PZ | ZQW | | |
| Op Amp | OA1IN0 | 6 | C1 | I | OA1 negative input internally connected to ADC negative analog differential input AD2- |
| | OA0IN0 | 2 | B2 | I | OA0 negative input internally connected to ADC negative analog differential input AD0- |
| | OA0IP0 | 99 | A2 | I | OA0 positive input internally connected to ADC analog input A2 |
| | OA0O | 1 | A1 | O | OA0 output internally connected to ADC positive analog differential input AD0+ |
| | OA1IP0 | 100 | D5 | I | OA1 positive input internally connected to ADC analog input A3 |
| | OA1O | 5 | C2 | O | OA1 output internally connected to ADC positive analog differential input AD2+ |
| Power | AVSS1 | 13 | F2 | P | Analog ground supply |
| | AVSS2 | 83 | A8 | P | Analog ground supply |
| | DVCC | 16 | H1, G2 | P | Digital power supply |
| | DVCC1 | 26 | L1 | P | Digital power supply |
| | DVCC2 | 64 | F12 | P | Digital power supply |
| | DVCC3 | 89 | A6 | P | Digital power supply |
| | DVSS1 | 27 | M1 | P | Digital ground supply |
| | DVSS2 | 63 | G12 | P | Digital ground supply |
| | DVSS3 | 90 | A5 | P | Digital ground supply |
| | LDOI | 80 | A10 | I | LDO input (not available on FG662x devices) |
| | LDOO | 81 | A9 | O | LDO output (not available on FG662x devices) |
| | VCORE ⁽²⁾ | 28 | M2 | O | Regulated core power supply (internal use only, no external current loading) |
| REF | VREFBG | 9 | D1 | O | Output of reference voltage to the ADC and DAC |
| Reserved | NC | 78 82 | B10 B9 | I/O | Not connected (not available on FG662x devices) |
| | Reserved | – | E5, E6, E8, F4, F5, F8, G5, G8, H5, H8, H9 | – | Reserved. Internally connected to DVSS. TI recommends external connection to ground (DVSS). |
| SPI | UCA1CLK | 59 | J12 | I/O | USCI_A1 clock input/output |
| | UCA1SIMO | 60 | H11 | I/O | USCI_A1 SPI slave in/master out |
| | UCA1SOMI | 61 | H12 | I/O | USCI_A1 SPI slave out/master in |
| | UCA1STE | 62 | G11 | I/O | USCI_A1 SPI slave transmit enable |
| | UCB1CLK | 62 | G11 | I/O | USCI_B1 clock input/output |
| | UCB1SIMO | 65 | F11 | I/O | USCI_B1 SPI slave in/master out |
| | UCB1SOMI | 66 | G9 | I/O | USCI_B1 SPI slave out/master in |
| | UCB1STE | 59 | J12 | I/O | USCI_B1 SPI slave transmit enable |
| System | NMI | 96 | A3 | I | Nonmaskable interrupt input |
| | RST | 96 | A3 | I/O | Reset input (active low) ⁽³⁾ |
| | SVMOUT | 57 | K12 | O | SVM output |

(2) VCORE is for internal use only. No external current loading is possible. VCORE must be connected to the recommended capacitor value, C_{VCORE}.

(3) When this pin is configured as reset, the internal pullup resistor is enabled by default.

Table 4-2. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | | PIN TYPE ⁽¹⁾ | DESCRIPTION |
|----------------------|-------------|---------|------------|---|--|
| | | PZ | ZQW | | |
| Timer_A | TA0.0 | 35 | M5 | I/O | Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output |
| | TA0.1 | 36 | J6 | I/O | Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output |
| | | 40 | J7 | I/O | Timer TA0 CCR1 capture: CCI1B input, compare: Out1 output |
| | TA0.2 | 37 | H6 | I/O | Timer TA0 CCR2 capture: CCI2A input, compare: Out2 output |
| | | 41 | M7 | I/O | Timer TA0 CCR2 capture: CCI2B input, compare: Out2 output |
| | TA0.3 | 38 | M6 | I/O | Timer TA0 CCR3 capture: CCI3A input compare: Out3 output |
| | TA0.4 | 39 | L6 | I/O | Timer TA0 CCR4 capture: CCI4A input, compare: Out4 output |
| | TA0CLK | 34 | L5 | I | Timer TA0 clock signal TACLK input |
| | TA1.0 | 43 | H7 | I/O | Timer TA1 capture CCR0: CCI0A input, compare: Out0 output |
| | TA1.1 | 44 | M8 | I/O | Timer TA1 capture CCR1: CCI1A input, compare: Out1 output |
| | TA1.2 | 45 | L8 | I/O | Timer TA1 capture CCR2: CCI2A input, compare: Out2 output |
| | TA1CLK | 42 | L7 | I | Timer TA1 clock input |
| | TA2.0 | 47 | M9 | I/O | Timer TA2 capture CCR0: CCI0A input, compare: Out0 output |
| | TA2.1 | 48 | L9 | I/O | Timer TA2 capture CCR1: CCI1A input, compare: Out1 output |
| TA2.2 | 49 | M10 | I/O | Timer TA2 capture CCR2: CCI2A input, compare: Out2 output | |
| TA2CLK | 46 | J8 | I | Timer TA2 clock input | |
| Timer_B | TB0.0 | 50 | J9 | I/O | Timer TB0 capture CCR0: CCI0A input, compare: Out0 output |
| | TB0.1 | 51 | M11 | I/O | Timer TB0 capture CCR1: CCI1A input, compare: Out1 output |
| | TB0.2 | 52 | L10 | I/O | Timer TB0 capture CCR2: CCI2A input, compare: Out2 output |
| | TB0.3 | 53 | M12 | I/O | Timer TB0 capture CCR3: CCI3A input, compare: Out3 output |
| | TB0.4 | 54 | L12 | I/O | Timer TB0 capture CCR4: CCI4A input, compare: Out4 output |
| | TB0.5 | 55 | L11 | I/O | Timer TB0 capture CCR5: CCI5A input, compare: Out5 output |
| | TB0.6 | 56 | K11 | I/O | Timer TB0 capture CCR6: CCI6A input, compare: Out6 output |
| | TB0CLK | 58 | J11 | I | Timer TB0 clock input |
| | TB0OUTH | 57 | K12 | I | Timer TB0: Switch all PWM outputs high impedance |
| UART | UCA1CLK | 59 | J12 | I/O | USCI_A1 clock input/output |
| | UCA1RXD | 61 | H12 | I | USCI_A1 UART receive data |
| | UCA1TXD | 60 | H11 | O | USCI_A1 UART transmit data |
| USB (FG662x only) | DM | 79 | A11 | I/O | USB data terminal DM (not available on FG6426 and FG6425 devices) |
| | DP | 77 | A12 | I/O | USB data terminal DP (not available on FG6426 and FG6425 devices) |
| | PUR | 78 | B10 | I/O | USB pullup resistor pin (open drain). The voltage level at the PUR pin is used to invoke the default USB BSL. Recommended 1-MΩ resistor to ground. See Section 6.6 for more information. Not available on FG6426 and FG6425 devices. |
| | V18 | 82 | B9 | O | USB regulated power (internal use only, no external current loading) (not available on FG6426 and FG6425 devices) |
| | VBUS | 80 | A10 | I | USB LDO input (connect to USB power source) (not available on FG6426 and FG6425 devices) |
| | VSSU | 76 | B11 B12 | P | USB PHY ground supply |
| | VUSB | 81 | A9 | O | USB LDO output (not available on FG6426 and FG6425 devices) |

4.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see [Section 6.12.23](#).

Table 4-3. Buffer Type

| BUFFER TYPE (STANDARD) | NOMINAL VOLTAGE | HYSTERESIS | PU OR PD | NOMINAL PU OR PD STRENGTH (μ A) | OUTPUT DRIVE STRENGTH (mA) | OTHER CHARACTERISTICS |
|--------------------------------------|-----------------|------------------|--------------|---|--|---|
| Analog ⁽¹⁾ | 3.0 V | N | N/A | N/A | N/A | See analog modules in Section 5, Specifications for details |
| HVCMOS | 5.0 V | Y | N/A | N/A | See Section 5.5.5.1, Typical Characteristics – Outputs | |
| LVC MOS | 3.0 V | Y ⁽²⁾ | Programmable | See Section 5.5.5, General-Purpose I/Os | See Section 5.5.5.1, Typical Characteristics – Outputs | |
| Power (DVCC) ⁽³⁾ | 3.0 V | N | N/A | N/A | N/A | SVS enables hysteresis on DVCC |
| Power (AVCC) ⁽³⁾ | 3.0 V | N | N/A | N/A | N/A | |
| Power (DVSS and AVSS) ⁽³⁾ | 0 V | N | N/A | N/A | N/A | |

(1) This is a switch, not a buffer.

(2) Only for input pins

(3) This is supply input, not a buffer.

4.5 Connection of Unused Pins

Table 4-4 lists the correct termination of all unused pins.

Table 4-4. Connection of Unused Pins⁽¹⁾

| PIN | POTENTIAL | COMMENT |
|--|-------------------------------------|---|
| AVCC | DV _{CC} | |
| AVSS | DV _{SS} | |
| CPCAP | Open | For devices where the charge pump is not used (no rail-to-rail OA and no rail-to-rail CTSD16). |
| LCDCAP | DV _{SS} | |
| LDO1 | DV _{SS} | For devices with LDO-PWR module when not being used in the application. |
| LDO0 | Open | For devices with LDO-PWR module when not being used in the application. |
| NC | Open | |
| PJ.0/TDO PJ.1/TDI PJ.2/TMS PJ.3/TCK | Open | The JTAG pins are shared with general-purpose I/O function (PJ.x). If not being used, these must be switched to port function, output direction (PJDIR.n = 1). When used as JTAG pins, these pins must remain open. |
| PU.0/DP PU.1/DM | Open | For USB devices only when USB module is not being used in the application |
| PUR ⁽²⁾ | DV _{SS} | For USB devices only when USB module is not being used in the application |
| Px.y | Open | Switched to port function, output direction (PxDIR.n = 1). Px.y represents port x and bit y of port x (for example, P1.0, P1.1, P2.2, PJ.0, PJ.1) |
| RST/NMI | DV _{CC} or V _{CC} | 47-kΩ pullup or internal pullup selected with 10-nF (2.2 nF) pulldown ⁽³⁾ |
| Reserved | DV _{SS} | |
| TEST | Open | This pin always has an internal pulldown enabled. |
| V18 | Open | For USB devices only when USB module is not being used in the application |
| VBAK | Open | For devices where no separate battery backup supply is used in the system. Set bit BAKDIS = 1. |
| VBAT | DV _{CC} | For devices where no separate battery backup supply is used in the system. Set bit BAKDIS = 1. |
| VBUS, VSSU | DV _{SS} | For USB devices only when USB module is not being used in the application |
| VUSB | Open | For USB devices only when USB module is not being used in the application |
| XIN | DV _{SS} | For dedicated XIN pins only. XIN pins with shared GPIO functions must be programmed to GPIO and follow Px.y recommendations. |
| XOUT | Open | For dedicated XOUT pins only. XOUT pins with shared GPIO functions must be programmed to GPIO and follow Px.y recommendations. |
| XT2IN | DV _{SS} | For dedicated XT2IN pins only. XT2IN pins with shared GPIO functions must be programmed to GPIO and follow Px.y recommendations. |
| XT2OUT | Open | For dedicated XT2OUT pins only. XT2OUT pins with shared GPIO functions must be programmed to GPIO and follow Px.y recommendations. |

- (1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.y unused pin connection guidelines.
- (2) The default USB BSL evaluates the state of the PUR pin after a BOR reset. If it is pulled high externally, then the BSL is invoked. Therefore, unless invoking the BSL, it is important to keep PUR pulled low after a BOR reset, even if BSL or USB is never used. TI recommends a 1-MΩ resistor to ground.
- (3) The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools such as FET interfaces or GANG programmers.

5 Specifications

5.1 Absolute Maximum Ratings ⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|--|------|----------------|------|
| Voltage applied at V_{CC} to V_{SS} | -0.3 | 4.1 | V |
| Voltage applied to any pin (excluding V _{CORE} , V _{BUS} , V18, LDO1) ⁽²⁾ | -0.3 | $V_{CC} + 0.3$ | V |
| Diode current at any device pin | | ±2 | mA |
| Storage temperature, T_{stg} ⁽³⁾ | -55 | 150 | °C |
| Maximum junction temperature, T_J | | 95 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS} . V_{CORE} is for internal device use only. No external DC loading or voltage should be applied.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

| | VALUE | UNIT |
|-------------------------------------|--|-------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±1000 |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±250 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT | |
|-----------------------------|--|---|------|-----|------|----|
| V_{CC} | Supply voltage during program execution and flash programming ($AV_{CC} = DV_{CC1} = DV_{CC2} = DV_{CC3} = DV_{CC} = V_{CC}$) ^{(1) (2) (3)} | PMMCOREV = 0 | 1.8 | 3.6 | V | |
| | | PMMCOREV = 0, 1 | 2.0 | 3.6 | | |
| | | PMMCOREV = 0, 1, 2 | 2.2 | 3.6 | | |
| | | PMMCOREV = 0, 1, 2, 3 | 2.4 | 3.6 | | |
| $V_{CC,USB}$ ⁽²⁾ | Supply voltage during USB operation, USB PLL disabled ($USB_EN = 1, UPLLEN = 0$) | PMMCOREV = 0 | 1.8 | 3.6 | V | |
| | | PMMCOREV = 0, 1 | 2.0 | 3.6 | | |
| | | PMMCOREV = 0, 1, 2 | 2.2 | 3.6 | | |
| | | PMMCOREV = 0, 1, 2, 3 | 2.4 | 3.6 | | |
| | Supply voltage during USB operation, USB PLL enabled ⁽⁴⁾ ($USB_EN = 1, UPLLEN = 1$) | PMMCOREV = 2 | 2.2 | 3.6 | | |
| | | PMMCOREV = 2, 3 | 2.4 | 3.6 | | |
| V_{SS} | Supply voltage ($AV_{SS1} = AV_{SS2} = AV_{SS3} = DV_{SS1} = DV_{SS2} = DV_{SS3} = V_{SS}$) | | 0 | | V | |
| $V_{BAT,RTC}$ | Backup-supply voltage with RTC operational | $T_A = 0^\circ\text{C}$ to 85°C | 1.55 | 3.6 | V | |
| | | $T_A = -40^\circ\text{C}$ to 85°C | 1.70 | 3.6 | | |
| $V_{BAT,MEM}$ | Backup-supply voltage with backup memory retained. | $T_A = -40^\circ\text{C}$ to 85°C | 1.20 | 3.6 | V | |
| T_A | Operating free-air temperature | I version | -40 | 85 | °C | |
| T_J | Operating junction temperature | I version | -40 | 85 | °C | |
| C_{BAK} | Capacitance at pin V _{BAK} | | 1 | 4.7 | 10 | nF |
| C_{VCORE} | Capacitor at V _{CORE} ⁽⁵⁾ | | | 470 | | nF |

- (1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
- (2) Some modules may have reduced recommended ranges of operation.
- (3) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the threshold parameters in [Table 5-19](#) for the exact values and further details.
- (4) USB operation with USB PLL enabled requires $PMMCOREV \geq 2$ for proper operation.
- (5) A capacitor tolerance of ±20% is required.

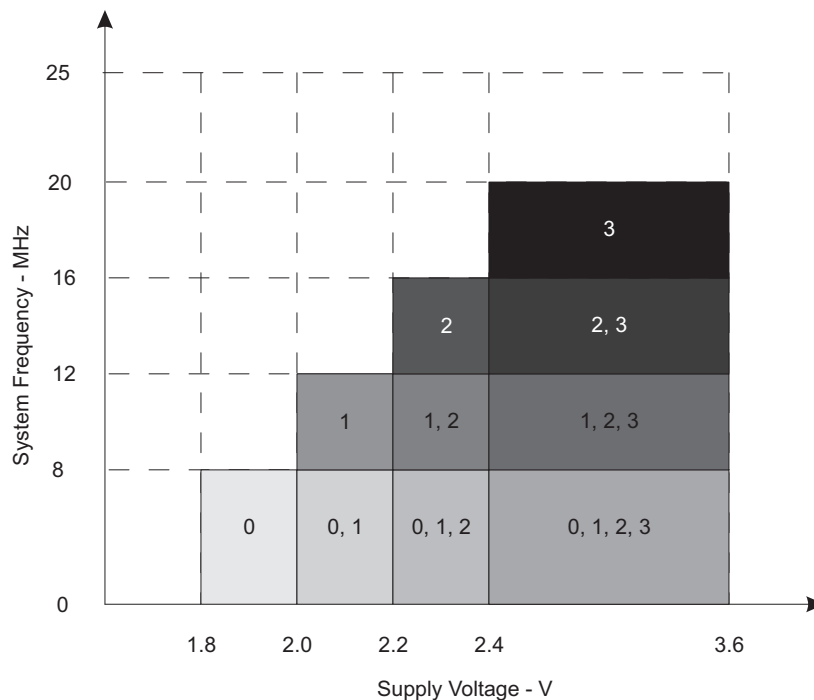
Recommended Operating Conditions (continued)

Typical values are specified at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT | |
|----------------------|---|--|-----|-----|--------|-----|
| C_{DVCC}/C_{VCORE} | Capacitor ratio of DVCC to VCORE | 10 | | | | |
| f_{SYSTEM} | Processor frequency (maximum MCLK frequency) ⁽⁶⁾ ⁽⁷⁾ (see Figure 5-1) | PMMCOREV = 0, $1.8\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ (default condition) | | 0 | 8.0 | MHz |
| | | PMMCOREV = 1, $2\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ | | 0 | 12.0 | |
| | | PMMCOREV = 2, $2.2\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ | | 0 | 16.0 | |
| | | PMMCOREV = 3, $2.4\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ | | 0 | 20.0 | |
| f_{SYSTEM_USB} | Minimum processor frequency for USB operation | 1.5 | | | MHz | |
| USB_wait | Wait state cycles during USB operation | 16 | | | cycles | |

(6) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.

(7) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 5-1. Frequency vs Supply Voltage

Table 5-1. Active Mode Supply Current Into V_{CC} Excluding External Current

 over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾ ⁽²⁾ ⁽³⁾

| PARAMETER | EXECUTION MEMORY | V_{CC} | PMMCOREV | FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$) | | | | | | | | UNIT |
|-----------------|------------------|----------|----------|--|------|-------|-----|--------|-----|--------|-----|------|
| | | | | 1 MHz | | 8 MHz | | 12 MHz | | 20 MHz | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM, Flash}$ | Flash | 3 V | 0 | 0.31 | 0.36 | 2.0 | 2.4 | | | | | mA |
| | | | 1 | 0.35 | | 2.3 | | 3.4 | 4.0 | | | |
| | | | 2 | 0.37 | | 2.5 | | 3.8 | | | | |
| | | | 3 | 0.4 | | 2.7 | | 4.0 | 6.6 | | | |
| $I_{AM, RAM}$ | RAM | 3 V | 0 | 0.2 | 0.23 | 1.1 | 1.2 | | | | | mA |
| | | | 1 | 0.22 | | 1.3 | | 1.9 | 2.1 | | | |
| | | | 2 | 0.24 | | 1.5 | | 2.2 | | | | |
| | | | 3 | 0.26 | | 1.6 | | 2.4 | 3.9 | | | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

(3) Characterized with program executing typical data processing. FG6626 and FG6625 USB disabled ($V_{USBEN} = 0$, $SLDOEN = 0$). FG6426 and FG6425 LDO disabled ($LDOEN = 0$).

$f_{ACLK} = 32786$ Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.

$XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0$.

Table 5-2. Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | V _{CC} | PMMCOREV | -40°C | | 25°C | | 60°C | | 85°C | | UNIT |
|---|-----------------|----------|-------|-----|------|-----|------|-----|------|------|------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| I _{LPM0,1MHz} Low-power mode 0 ^{(3) (4)} | 2.2 V | 0 | 72 | | 77 | 87 | 81 | | 87 | 98 | μA |
| | 3 V | 3 | 86 | | 92 | 105 | 97 | | 104 | 117 | |
| I _{LPM2} Low-power mode 2 ^{(5) (4)} | 2.2 V | 0 | 6.9 | | 7.5 | 9.9 | 8.5 | | 12 | 17 | μA |
| | 3 V | 3 | 7.9 | | 8.5 | 11 | 9.7 | | 14 | 20 | |
| I _{LPM3,XT1LF} Low-power mode 3, crystal mode ^{(6) (4)} | 2.2 V | 0 | 2.8 | | 3.2 | 3.7 | 4.2 | | 7.6 | 13.5 | μA |
| | | 1 | 3.1 | | 3.6 | | 4.6 | | 8.2 | | |
| | | 2 | 3.5 | | 4.0 | | 5.1 | | 8.8 | | |
| | 3 V | 0 | 3.0 | | 3.4 | 4.0 | 4.4 | | 7.9 | 14 | |
| | | 1 | 3.3 | | 3.8 | | 4.9 | | 8.5 | | |
| | | 2 | 3.7 | | 4.2 | | 5.3 | | 9.0 | | |
| I _{LPM3,VLO,WDT} Low-power mode 3, VLO mode, Watchdog enabled ^{(7) (4)} | 3 V | 3 | 3.7 | | 4.2 | 4.8 | 5.3 | | 9.1 | 16 | |
| | | 0 | 1.2 | | 1.5 | 2.1 | 2.4 | | 5.8 | 12.5 | |
| | | 1 | 1.4 | | 1.6 | | 2.6 | | 6.1 | | |
| | | 2 | 1.6 | | 1.8 | | 2.8 | | 6.5 | | |
| I _{LPM4} Low-power mode 4 ^{(8) (4)} | 3 V | 3 | 1.6 | | 1.8 | 2.6 | 2.9 | | 6.5 | 14 | |
| | | 0 | 0.6 | | 0.9 | 1.8 | 1.9 | | 5.4 | 11.5 | |
| | | 1 | 0.7 | | 1.0 | | 2.0 | | 5.6 | | |
| | | 2 | 0.8 | | 1.1 | | 2.2 | | 5.9 | | |
| I _{LPM3.5,RTC,VCC} Low-power mode 3.5 (LPM3.5) current with active RTC into primary supply pin DV _{CC} ⁽⁹⁾ | 3 V | 3 | 0.8 | | 1.1 | 2.1 | 2.2 | | 6.0 | 13 | |
| | | 0 | | | | | | | 0.7 | 1.7 | |
| I _{LPM3.5,RTC,VBAT} Low-power mode 3.5 (LPM3.5) current with active RTC into backup supply pin VBAT ⁽¹⁰⁾ | 3 V | 3 | | | | | | | 0.9 | 1.2 | |
| | | 0 | | | | | | | | | |
| I _{LPM3.5,RTC,TOT} Total low-power mode 3.5 (LPM3.5) current with active RTC ⁽¹¹⁾ | 3 V | | 0.8 | | 0.9 | | 1.0 | | 1.6 | 2.9 | μA |

- (1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
- (3) Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).
- (4) Current for brownout included. Low side supervisor and monitors disabled (SVS_L, SVM_L). High side supervisor and monitor disabled (SVS_H, SVM_H). RAM retention enabled.
- (5) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled. FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).
- (6) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).
- (7) Current for watchdog timer clocked by VLO included. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).
- (8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).
- (9) V_{VBAT} = V_{CC} - 0.2 V, f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, PMMREGOFF = 1, RTC in backup domain active
- (10) V_{VBAT} = V_{CC} - 0.2 V, f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, PMMREGOFF = 1, RTC in backup domain active, no current drawn on VBAK
- (11) f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, PMMREGOFF = 1, RTC in backup domain active, no current drawn on VBAK

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | V_{CC} | PMMCOREV | -40°C | | 25°C | | 60°C | | 85°C | | UNIT |
|--|----------|----------|-------|-----|------|-----|------|-----|------|-----|---------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM4.5}$ Low-power mode 4.5 (LPM4.5) ⁽¹²⁾ | 3 V | | 0.12 | | 0.2 | 0.6 | 0.32 | | 0.8 | 1.9 | μ A |

(12) Internal regulator disabled. No data retention.

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5); $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

Table 5-3. Low-Power Mode With LCD Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | V_{CC} | PMMCOREV | Temperature (T_A) | | | | | | | | UNIT |
|---|----------|----------|-----------------------|-----|------|-----|------|------|------|------|---------|
| | | | -40°C | | 25°C | | 60°C | | 85°C | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3, LCD, ext. bias}$ Low-power mode 3 (LPM3) current, LCD 4-mux mode, external biasing ^{(3) (4)} | 3 V | 0 | 3.7 | | 4.3 | 4.9 | 5.5 | | 9.0 | 15.0 | μ A |
| | | 1 | 4.1 | | 4.7 | | 5.9 | | 9.6 | | |
| | | 2 | 4.5 | | 5.1 | | 6.3 | | 10.2 | | |
| | | 3 | 4.5 | 5.2 | 5.8 | 6.5 | 10.4 | 18.0 | | | |
| $I_{LPM3, LCD, int. bias}$ Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump disabled ^{(3) (5)} | 3 V | 0 | 4.2 | | 4.8 | 5.4 | 6.0 | | 9.6 | 17.0 | μ A |
| | | 1 | 4.7 | | 5.4 | | 6.6 | | 10.4 | | |
| | | 2 | 5.1 | | 5.8 | | 7.1 | | 11.0 | | |
| | | 3 | 5.0 | 5.7 | 6.4 | 7.0 | 11.0 | 19.0 | | | |
| $I_{LPM3, LCD, CP}$ Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump enabled ^{(3) (6)} | 2.2 V | 0 | | | 6.4 | | | | | | μ A |
| | | 1 | | | 6.77 | | | | | | |
| | | 2 | | | 7.13 | | | | | | |
| | | 3 | | | 7.6 | | | | | | |
| | 3 V | 0 | | | 6.53 | | | | | | μ A |
| | | 1 | | | 7.0 | | | | | | |
| | | 2 | | | 7.43 | | | | | | |
| | | 3 | | | 7.6 | | | | | | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.

(3) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); $f_{ACLK} = 32768$ Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO} = 0$ MHz

Current for brownout included. Low-side supervisor (SVSL) and low-side monitor (SVM_L) disabled. High-side supervisor (SVSH) and high-side monitor (SVM_H) disabled. RAM retention enabled.

(4) LCDMx = 11 (4-mux mode), LCDREXT = 1, LCDEXTBIAS = 1 (external biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD} = 32768$ Hz/32/4 = 256 Hz)

Current through external resistors not included (voltage levels are supplied by test equipment).

Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

(5) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD} = 32768$ Hz/32/4 = 256 Hz)

Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

(6) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 ($V_{LCD} = 3$ V, typ.), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD} = 32768$ Hz/32/4 = 256 Hz)

Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

5.4 Thermal Characteristics

| PARAMETER | | VALUE | UNIT |
|--------------------|--|-----------|------|
| θ_{JA} | Junction-to-ambient thermal resistance, still air ⁽¹⁾ | QFP (PZ) | 122 |
| | | BGA (ZQW) | 108 |
| $\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance ⁽²⁾ | QFP (PZ) | 83 |
| | | BGA (ZQW) | 72 |
| θ_{JB} | Junction-to-board thermal resistance ⁽³⁾ | QFP (PZ) | 98 |
| | | BGA (ZQW) | 76 |

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

5.5 Timing and Switching Characteristics

5.5.1 Power Supply Sequencing

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in [Section 5.1](#), *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and flash.

Table 5-4. Brownout and Device Reset Power Ramp Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|---------------------------------|------|------|------|------|
| $V_{(DVCC_BOR_IT-)}$ | BOR _H on voltage, DV _{CC} falling level | $ dDV_{CC}/dt < 3 \text{ V/s}$ | | | 1.47 | V |
| $V_{(DVCC_BOR_IT+)}$ | BOR _H off voltage, DV _{CC} rising level | $ dDV_{CC}/dt < 3 \text{ V/s}$ | 0.80 | 1.30 | 1.55 | V |
| $V_{(DVCC_BOR_hys)}$ | BOR _H hysteresis | | 60 | | 250 | mV |

5.5.2 Reset Timing

Table 5-5. Reset Input

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TYP | UNIT |
|-------------|--|-----|------|
| t_{RESET} | Pulse duration required at RST/NMI pin to accept a reset | 2 | μs |

5.5.3 Clock Specifications

Table 5-6. Crystal Oscillator, XT1, Low-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|-----------------|-----|--------|-------|------------|
| $\Delta I_{DVCC,LF}$ Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1 | 3 V | | 0.075 | | μ A |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 2 | | | 0.170 | | |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3 | | | 0.290 | | |
| $f_{XT1,LF0}$ XT1 oscillator crystal frequency, LF mode | XTS = 0, XT1BYPASS = 0 | | | 32768 | | Hz |
| $f_{XT1,LF,SW}$ XT1 oscillator logic-level square-wave input frequency, LF mode | XTS = 0, XT1BYPASS = 1 ⁽²⁾ ⁽³⁾ | | 10 | 32.768 | 50 | kHz |
| OA_{LF} Oscillation allowance for LF crystals ⁽⁴⁾ | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, $f_{XT1,LF} = 32768$ Hz, $C_{L,eff} = 6$ pF | | | 210 | | k Ω |
| | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, $f_{XT1,LF} = 32768$ Hz, $C_{L,eff} = 12$ pF | | | 300 | | |
| $C_{L,eff}$ Integrated effective load capacitance, LF mode ⁽⁵⁾ | XTS = 0, XCAP _x = 0 ⁽⁶⁾ | | | 1 | | pF |
| | XTS = 0, XCAP _x = 1 | | | 5.5 | | |
| | XTS = 0, XCAP _x = 2 | | | 8.5 | | |
| | XTS = 0, XCAP _x = 3 | | | 12.0 | | |
| Duty cycle, LF mode | XTS = 0, Measured at ACLK, $f_{XT1,LF} = 32768$ Hz | | 30% | | 70% | |
| $f_{Fault,LF}$ Oscillator fault frequency, LF mode ⁽⁷⁾ | XTS = 0 ⁽⁸⁾ | | 10 | | 10000 | Hz |
| $t_{START,LF}$ Start-up time, LF mode | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, $C_{L,eff} = 6$ pF | 3 V | | 1000 | | ms |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, $C_{L,eff} = 12$ pF | | | 500 | | |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE_x settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - For XT1DRIVE_x = 0, $C_{L,eff} \leq 6$ pF.
 - For XT1DRIVE_x = 1, 6 pF $\leq C_{L,eff} \leq 9$ pF.
 - For XT1DRIVE_x = 2, 6 pF $\leq C_{L,eff} \leq 10$ pF.
 - For XT1DRIVE_x = 3, $C_{L,eff} \geq 6$ pF.
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, TI recommends verifying the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-7. Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|---|--|-----------------|-----|-----|-----|------|
| I _{DVCC,XT2} | XT2 oscillator crystal current consumption | f _{OSC} = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 0, T _A = 25°C | 3 V | | 200 | | μA |
| | | f _{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 1, T _A = 25°C | | | 260 | | |
| | | f _{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 2, T _A = 25°C | | | 325 | | |
| | | f _{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 3, T _A = 25°C | | | 450 | | |
| f _{XT2,HF0} | XT2 oscillator crystal frequency, mode 0 | XT2DRIVE _x = 0, XT2BYPASS = 0 ⁽³⁾ | | 4 | | 8 | MHz |
| f _{XT2,HF1} | XT2 oscillator crystal frequency, mode 1 | XT2DRIVE _x = 1, XT2BYPASS = 0 ⁽³⁾ | | 8 | | 16 | MHz |
| f _{XT2,HF2} | XT2 oscillator crystal frequency, mode 2 | XT2DRIVE _x = 2, XT2BYPASS = 0 ⁽³⁾ | | 16 | | 24 | MHz |
| f _{XT2,HF3} | XT2 oscillator crystal frequency, mode 3 | XT2DRIVE _x = 3, XT2BYPASS = 0 ⁽³⁾ | | 24 | | 32 | MHz |
| f _{XT2,HF,SW} | XT2 oscillator logic-level square-wave input frequency | XT2BYPASS = 1 ^{(4) (3)} | | 0.7 | | 32 | MHz |
| O _{AHF} | Oscillation allowance for HF crystals ⁽⁵⁾ | XT2DRIVE _x = 0, XT2BYPASS = 0, f _{XT2,HF0} = 6 MHz, C _{L,eff} = 15 pF | | | 450 | | Ω |
| | | XT2DRIVE _x = 1, XT2BYPASS = 0, f _{XT2,HF1} = 12 MHz, C _{L,eff} = 15 pF | | | 320 | | |
| | | XT2DRIVE _x = 2, XT2BYPASS = 0, f _{XT2,HF2} = 20 MHz, C _{L,eff} = 15 pF | | | 200 | | |
| | | XT2DRIVE _x = 3, XT2BYPASS = 0, f _{XT2,HF3} = 32 MHz, C _{L,eff} = 15 pF | | | 200 | | |
| t _{START,HF} | Start-up time | f _{OSC} = 6 MHz XT2BYPASS = 0, XT2DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 15 pF | 3 V | | 0.5 | | ms |
| | | f _{OSC} = 20 MHz XT2BYPASS = 0, XT2DRIVE _x = 3, T _A = 25°C, C _{L,eff} = 15 pF | | | 0.3 | | |
| C _{L,eff} | Integrated effective load capacitance, HF mode ^{(6) (1)} | | | | 1 | | pF |
| | Duty cycle | Measured at ACLK, f _{XT2,HF2} = 20 MHz | | 40% | 50% | 60% | |
| f _{Fault,HF} | Oscillator fault frequency ⁽⁷⁾ | XT2BYPASS = 1 ⁽⁸⁾ | | 30 | | 300 | kHz |

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.

- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down.

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).

Because the PCB adds additional capacitance, TI recommends verifying the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-8. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| f _{VLO} | VLO frequency | Measured at ACLK | 1.8 V to 3.6 V | 6 | 9.4 | 14 | kHz |
| df _{VLO} /dT | VLO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 1.8 V to 3.6 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} | VLO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 1.8 V to 3.6 V | | 4 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |

(1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-9. Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------------------|-------------------------------------|---------------------------------|-----------------|-----|-------|-------|------|
| I _{REFO} | REFO oscillator current consumption | T _A = 25°C | 1.8 V to 3.6 V | | 3 | | μA |
| f _{REFO} | REFO frequency calibrated | Measured at ACLK | 1.8 V to 3.6 V | | 32768 | | Hz |
| | REFO absolute tolerance calibrated | Full temperature range | 1.8 V to 3.6 V | | | ±3.5% | |
| | | T _A = 25°C | 3 V | | | ±1.5% | |
| df _{REFO} /dT | REFO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 1.8 V to 3.6 V | | 0.01 | | %/°C |
| df _{REFO} /dV _{CC} | REFO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 1.8 V to 3.6 V | | 1.0 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |
| t _{START} | REFO start-up time | 40%/60% duty cycle | 1.8 V to 3.6 V | | 25 | | μs |

(1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-10. DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--------------------|--|--|------|------|-------|---|
| $f_{DCO(0,0)}$ | DCO frequency (0, 0) ⁽¹⁾ | DCORSELx = 0, DCOx = 0, MODx = 0 | 0.07 | 0.20 | MHz | |
| $f_{DCO(0,31)}$ | DCO frequency (0, 31) ⁽¹⁾ | DCORSELx = 0, DCOx = 31, MODx = 0 | 0.70 | 1.70 | MHz | |
| $f_{DCO(1,0)}$ | DCO frequency (1, 0) ⁽¹⁾ | DCORSELx = 1, DCOx = 0, MODx = 0 | 0.15 | 0.36 | MHz | |
| $f_{DCO(1,31)}$ | DCO frequency (1, 31) ⁽¹⁾ | DCORSELx = 1, DCOx = 31, MODx = 0 | 1.47 | 3.45 | MHz | |
| $f_{DCO(2,0)}$ | DCO frequency (2, 0) ⁽¹⁾ | DCORSELx = 2, DCOx = 0, MODx = 0 | 0.32 | 0.75 | MHz | |
| $f_{DCO(2,31)}$ | DCO frequency (2, 31) ⁽¹⁾ | DCORSELx = 2, DCOx = 31, MODx = 0 | 3.17 | 7.38 | MHz | |
| $f_{DCO(3,0)}$ | DCO frequency (3, 0) ⁽¹⁾ | DCORSELx = 3, DCOx = 0, MODx = 0 | 0.64 | 1.51 | MHz | |
| $f_{DCO(3,31)}$ | DCO frequency (3, 31) ⁽¹⁾ | DCORSELx = 3, DCOx = 31, MODx = 0 | 6.07 | 14.0 | MHz | |
| $f_{DCO(4,0)}$ | DCO frequency (4, 0) ⁽¹⁾ | DCORSELx = 4, DCOx = 0, MODx = 0 | 1.3 | 3.2 | MHz | |
| $f_{DCO(4,31)}$ | DCO frequency (4, 31) ⁽¹⁾ | DCORSELx = 4, DCOx = 31, MODx = 0 | 12.3 | 28.2 | MHz | |
| $f_{DCO(5,0)}$ | DCO frequency (5, 0) ⁽¹⁾ | DCORSELx = 5, DCOx = 0, MODx = 0 | 2.5 | 6.0 | MHz | |
| $f_{DCO(5,31)}$ | DCO frequency (5, 31) ⁽¹⁾ | DCORSELx = 5, DCOx = 31, MODx = 0 | 23.7 | 54.1 | MHz | |
| $f_{DCO(6,0)}$ | DCO frequency (6, 0) ⁽¹⁾ | DCORSELx = 6, DCOx = 0, MODx = 0 | 4.6 | 10.7 | MHz | |
| $f_{DCO(6,31)}$ | DCO frequency (6, 31) ⁽¹⁾ | DCORSELx = 6, DCOx = 31, MODx = 0 | 39.0 | 88.0 | MHz | |
| $f_{DCO(7,0)}$ | DCO frequency (7, 0) ⁽¹⁾ | DCORSELx = 7, DCOx = 0, MODx = 0 | 8.5 | 19.6 | MHz | |
| $f_{DCO(7,31)}$ | DCO frequency (7, 31) ⁽¹⁾ | DCORSELx = 7, DCOx = 31, MODx = 0 | 60 | 135 | MHz | |
| $S_{DCORSEL}$ | Frequency step between range DCORSEL and DCORSEL + 1 | $S_{RSEL} = f_{DCO(DCORSEL+1,DCO)} / f_{DCO(DCORSEL,DCO)}$ | 1.2 | 2.3 | ratio | |
| S_{DCO} | Frequency step between tap DCO and DCO + 1 | $S_{DCO} = f_{DCO(DCORSEL,DCO+1)} / f_{DCO(DCORSEL,DCO)}$ | 1.02 | 1.12 | ratio | |
| | Duty cycle | Measured at SMCLK | 40 | 50 | 60 | % |
| df_{DCO}/dT | DCO frequency temperature drift | $f_{DCO} = 1$ MHz, | | 0.1 | %/°C | |
| df_{DCO}/dV_{CC} | DCO frequency voltage drift | $f_{DCO} = 1$ MHz | | 1.9 | %/V | |

- (1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO} , should be set to reside within the range of $f_{DCO(n,0),MAX} \leq f_{DCO} \leq f_{DCO(n,31),MIN}$, where $f_{DCO(n,0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.

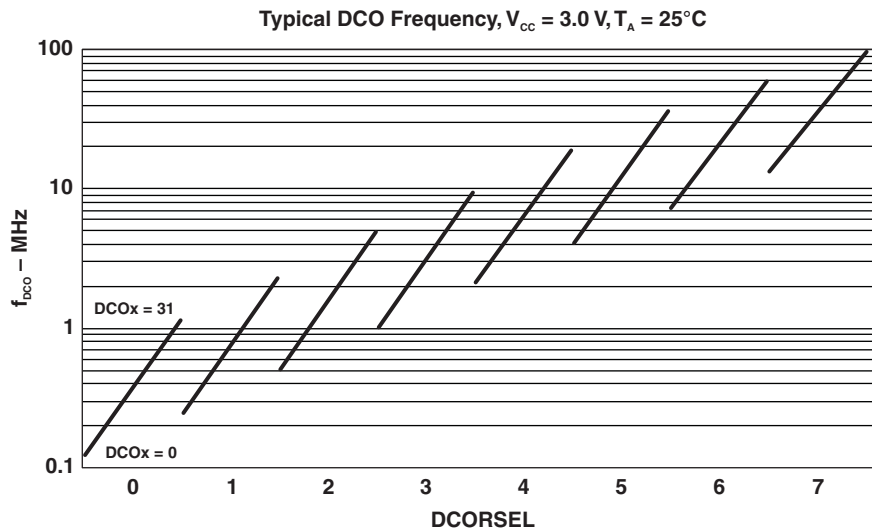


Figure 5-2. Typical DCO Frequency

5.5.4 Wake-Up Characteristics

Table 5-11. Wake-Up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------------|--|---|-----------------------------------|-----|-----|-----|------|
| t _{WAKE-UP-FAST} | Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽¹⁾ | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1 | f _{MCLK} ≥ 4 MHz | 3 | 6.5 | μs | |
| | | | 1 MHz < f _{MCLK} < 4 MHz | 4 | 8.0 | | |
| t _{WAKE-UP-SLOW} | Wake-up time from LPM2, LPM3 or LPM4 to active mode ⁽²⁾ | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0 | | 150 | 165 | μs | |
| t _{WAKE-UP-LPM5} | Wake-up time from LPM3.5 or LPM4.5 to active mode ⁽³⁾ | | | 2 | 3 | ms | |
| t _{WAKE-UP-RESET} | Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode ⁽³⁾ | | | 2 | 3 | ms | |

- (1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). Fastest wake-up times are possible with SVS_L and SVM_L in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)).
- (2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). In this case, the SVS_L and SVM_L are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)).
- (3) This value represents the time from the wake-up event to the reset vector execution.

5.5.5 General-Purpose I/Os

Table 5-12. Schmitt-Trigger Inputs – General-Purpose I/O⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|-----------------|------|-----|------|------|
| V _{IT+} Positive-going input threshold voltage | | 1.8 V | 0.80 | | 1.40 | V |
| | | 3 V | 1.50 | | 2.10 | |
| V _{IT-} Negative-going input threshold voltage | | 1.8 V | 0.45 | | 1.00 | V |
| | | 3 V | 0.75 | | 1.65 | |
| V _{hys} Input voltage hysteresis (V _{IT+} – V _{IT-}) | | 1.8 V | 0.3 | | 0.8 | V |
| | | 3 V | 0.4 | | 1.0 | |
| R _{Pull} Pullup/pulldown resistor | For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC} | | 20 | 35 | 50 | kΩ |
| C _I Input capacitance | V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

Table 5-13. Inputs – Ports P1, P2, P3, and P4⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---|---|-----------------|-----|-----|------|
| t _(int) External interrupt timing ⁽²⁾ | Port P1, P2, P3, P4: P1.x to P4.x, External trigger pulse duration to set interrupt flag | 2.2 V, 3 V | 20 | | ns |

- (1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
 (2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

Table 5-14. Leakage Current – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---|-----------------|---------------------------------|-----|-----|------|
| I _{lkg(Px.x)} High-impedance leakage current | | ⁽¹⁾⁽²⁾ 1.8 V, 3 V | | ±50 | nA |

- (1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
 (2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Table 5-15. Outputs – General-Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---|--|-----------------|------------------------|------------------------|------|
| V _{OH} High-level output voltage | I _(OHmax) = –3 mA ⁽¹⁾ | 1.8 V | V _{CC} – 0.25 | V _{CC} | V |
| | I _(OHmax) = –10 mA ⁽²⁾ | | V _{CC} – 0.60 | V _{CC} | |
| | I _(OHmax) = –5 mA ⁽¹⁾ | 3 V | V _{CC} – 0.25 | V _{CC} | |
| | I _(OHmax) = –15 mA ⁽²⁾ | | V _{CC} – 0.60 | V _{CC} | |
| V _{OL} Low-level output voltage | I _(OLmax) = 3 mA ⁽¹⁾ | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| | I _(OLmax) = 10 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | I _(OLmax) = 5 mA ⁽¹⁾ | 3 V | V _{SS} | V _{SS} + 0.25 | |
| | I _(OLmax) = 15 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |

- (1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
 (2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

Table 5-16. Outputs – General-Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|---------------------------|---|-----------------|------------------------|------------------------|------|
| V _{OH} | High-level output voltage | I _(OHmax) = –1 mA ⁽²⁾ | 1.8 V | V _{CC} – 0.25 | V _{CC} | V |
| | | I _(OHmax) = –3 mA ⁽³⁾ | | V _{CC} – 0.60 | V _{CC} | |
| | | I _(OHmax) = –2 mA ⁽²⁾ | 3 V | V _{CC} – 0.25 | V _{CC} | |
| | | I _(OHmax) = –6 mA ⁽³⁾ | | V _{CC} – 0.60 | V _{CC} | |
| V _{OL} | Low-level output voltage | I _(OLmax) = 1 mA ⁽²⁾ | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| | | I _(OLmax) = 3 mA ⁽³⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | | I _(OLmax) = 2 mA ⁽²⁾ | 3 V | V _{SS} | V _{SS} + 0.25 | |
| | | I _(OLmax) = 6 mA ⁽³⁾ | | V _{SS} | V _{SS} + 0.60 | |

(1) Selecting reduced drive strength may reduce EMI.

(2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

(3) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

Table 5-17. Output Frequency – Ports P1, P2 and P3

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------------|-----------------------------------|---|--|-----|------|
| f _{Px,y} | Port output frequency (with load) | P3.4/TA2CLK/SMCLK/S27 C _L = 20 pF, R _L = 1 kΩ ⁽¹⁾ or 3.2 kΩ ^{(2) (3)} | V _{CC} = 1.8 V PMMCOREVx = 0 | 8 | MHz |
| | | | V _{CC} = 3 V PMMCOREVx = 3 | 20 | |
| f _{Port_CLK} | Clock output frequency | P1.0/TA0CLK/ACLK/S39 P3.4/TA2CLK/SMCLK/S27 P2.0/P2MAP0 (P2MAP0 = PM_MCLK) C _L = 20 pF ⁽³⁾ | V _{CC} = 1.8 V PMMCOREVx = 0 | 8 | MHz |
| | | | V _{CC} = 3 V PMMCOREVx = 3 | 20 | |

(1) Full drive strength of port: A resistive divider with 2 × 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.

(2) Reduced drive strength of port: A resistive divider with 2 × 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.

(3) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.5.5.1 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

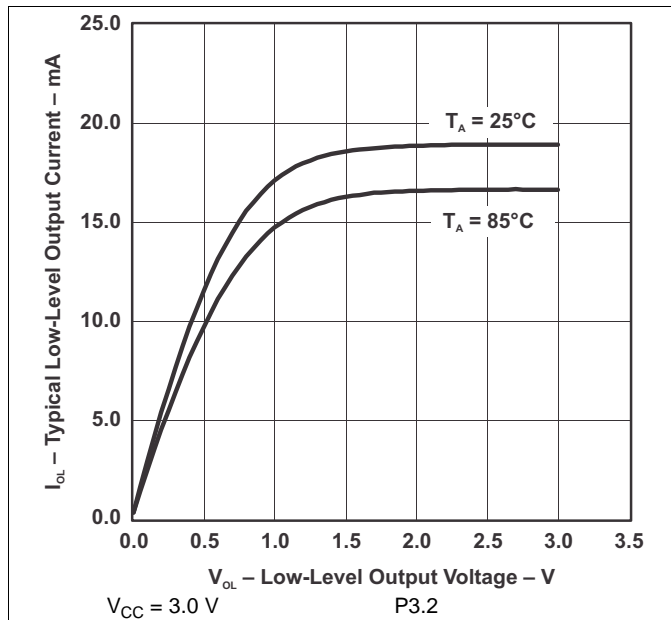


Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage

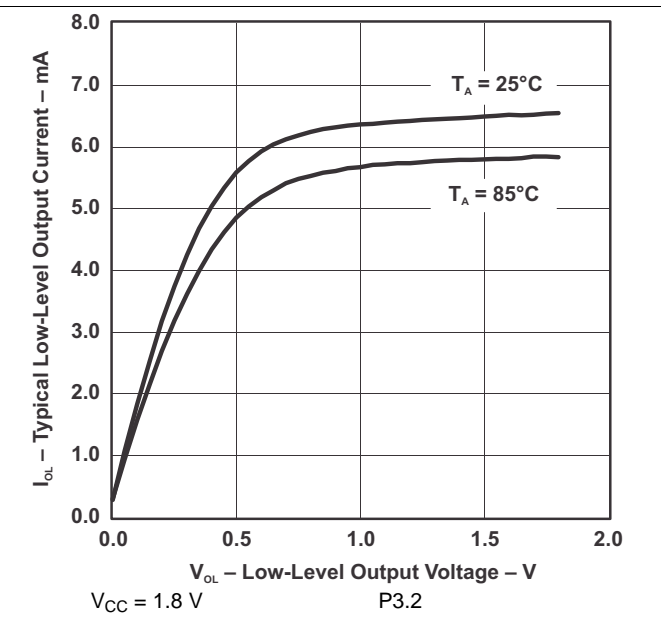


Figure 5-4. Typical Low-Level Output Current vs Low-Level Output Voltage

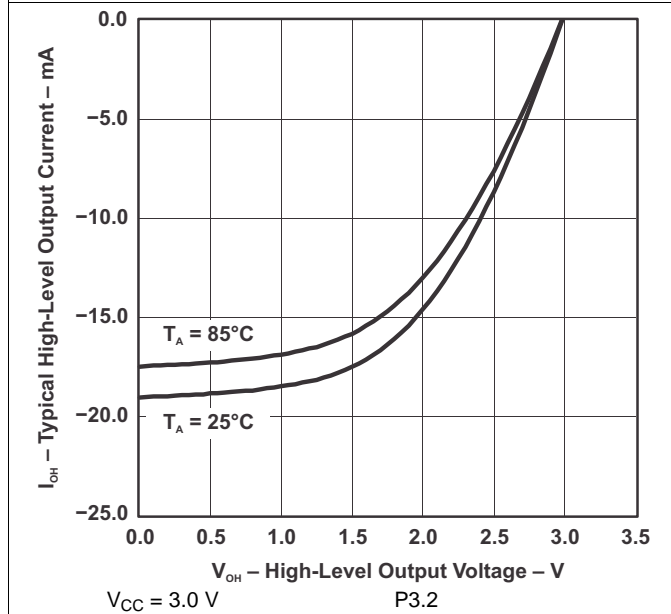


Figure 5-5. Typical High-Level Output Current Vs High-Level Output Voltage

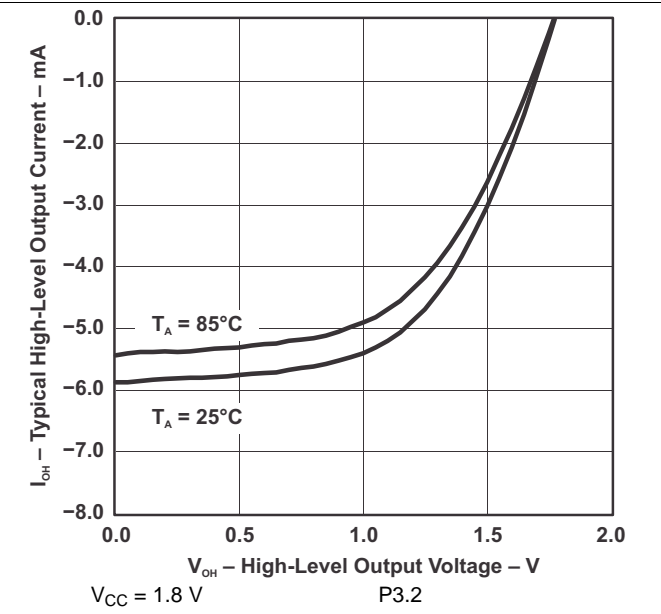


Figure 5-6. Typical High-Level Output Current Vs High-Level Output Voltage

5.5.5.2 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

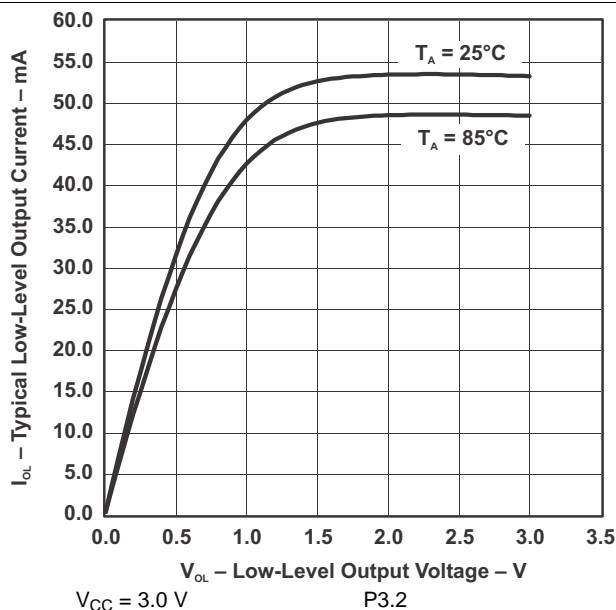


Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage

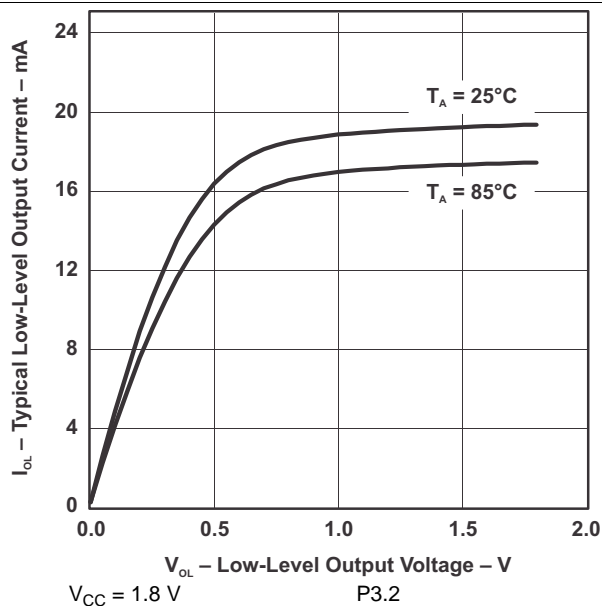


Figure 5-8. Typical Low-Level Output Current vs Low-Level Output Voltage

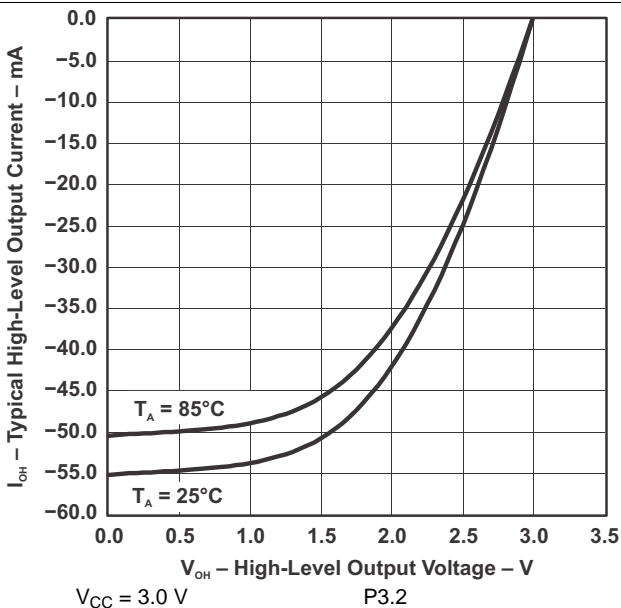


Figure 5-9. Typical High-Level Output Current vs High-level Output Voltage

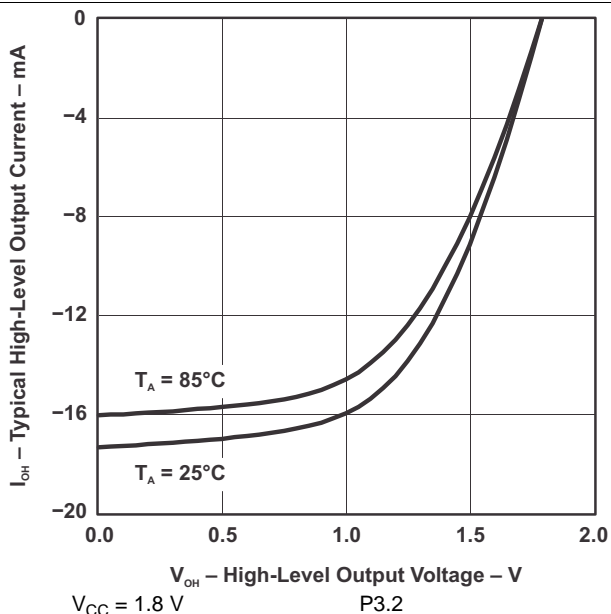


Figure 5-10. Typical High-Level Output Current vs High-level Output Voltage

5.5.6 PMM

Table 5-18. PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|--|-----|------|-----|------|
| $V_{CORE3(AM)}$ | Core voltage, active mode, PMMCOREV = 3 | $2.4\text{ V} \leq DV_{CC} \leq 3.6\text{ V}$, $0\text{ mA} \leq I(V_{CORE}) \leq 21\text{ mA}$ | | 1.90 | | V |
| $V_{CORE2(AM)}$ | Core voltage, active mode, PMMCOREV = 2 | $2.2\text{ V} \leq DV_{CC} \leq 3.6\text{ V}$, $0\text{ mA} \leq I(V_{CORE}) \leq 21\text{ mA}$ | | 1.80 | | V |
| $V_{CORE1(AM)}$ | Core voltage, active mode, PMMCOREV = 1 | $2\text{ V} \leq DV_{CC} \leq 3.6\text{ V}$, $0\text{ mA} \leq I(V_{CORE}) \leq 17\text{ mA}$ | | 1.60 | | V |
| $V_{CORE0(AM)}$ | Core voltage, active mode, PMMCOREV = 0 | $1.8\text{ V} \leq DV_{CC} \leq 3.6\text{ V}$, $0\text{ mA} \leq I(V_{CORE}) \leq 13\text{ mA}$ | | 1.40 | | V |
| $V_{CORE3(LPM)}$ | Core voltage, low-current mode, PMMCOREV = 3 | $2.4\text{ V} \leq DV_{CC} \leq 3.6\text{ V}$, $0\text{ }\mu\text{A} \leq I(V_{CORE}) \leq 30\text{ }\mu\text{A}$ | | 1.94 | | V |
| $V_{CORE2(LPM)}$ | Core voltage, low-current mode, PMMCOREV = 2 | $2.2\text{ V} \leq DV_{CC} \leq 3.6\text{ V}$, $0\text{ }\mu\text{A} \leq I(V_{CORE}) \leq 30\text{ }\mu\text{A}$ | | 1.84 | | V |
| $V_{CORE1(LPM)}$ | Core voltage, low-current mode, PMMCOREV = 1 | $2\text{ V} \leq DV_{CC} \leq 3.6\text{ V}$, $0\text{ }\mu\text{A} \leq I(V_{CORE}) \leq 30\text{ }\mu\text{A}$ | | 1.64 | | V |
| $V_{CORE0(LPM)}$ | Core voltage, low-current mode, PMMCOREV = 0 | $1.8\text{ V} \leq DV_{CC} \leq 3.6\text{ V}$, $0\text{ }\mu\text{A} \leq I(V_{CORE}) \leq 30\text{ }\mu\text{A}$ | | 1.44 | | V |

Table 5-19. PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|---|---|------|------|------|---------------|
| $I_{(SVSH)}$ | SVS current consumption | SVSHE = 0, $DV_{CC} = 3.6\text{ V}$ | | 0 | | nA |
| | | SVSHE = 1, $DV_{CC} = 3.6\text{ V}$, SVSHFP = 0 | | 200 | | |
| | | SVSHE = 1, $DV_{CC} = 3.6\text{ V}$, SVSHFP = 1 | | 2.0 | | μA |
| $V_{(SVSH_IT-)}$ | SVS _H on voltage level ⁽¹⁾ | SVSHE = 1, SVSHRVL = 0 | 1.59 | 1.64 | 1.69 | V |
| | | SVSHE = 1, SVSHRVL = 1 | 1.79 | 1.84 | 1.91 | |
| | | SVSHE = 1, SVSHRVL = 2 | 1.98 | 2.04 | 2.11 | |
| | | SVSHE = 1, SVSHRVL = 3 | 2.10 | 2.16 | 2.23 | |
| $V_{(SVSH_IT+)}$ | SVS _H off voltage level ⁽¹⁾ | SVSHE = 1, SVSMHRRL = 0 | 1.62 | 1.74 | 1.81 | V |
| | | SVSHE = 1, SVSMHRRL = 1 | 1.88 | 1.94 | 2.01 | |
| | | SVSHE = 1, SVSMHRRL = 2 | 2.07 | 2.14 | 2.21 | |
| | | SVSHE = 1, SVSMHRRL = 3 | 2.20 | 2.26 | 2.33 | |
| | | SVSHE = 1, SVSMHRRL = 4 | 2.32 | 2.40 | 2.48 | |
| | | SVSHE = 1, SVSMHRRL = 5 | 2.56 | 2.70 | 2.84 | |
| | | SVSHE = 1, SVSMHRRL = 6 | 2.85 | 3.00 | 3.15 | |
| | | SVSHE = 1, SVSMHRRL = 7 | 2.85 | 3.00 | 3.15 | |
| $t_{pd(SVSH)}$ | SVS _H propagation delay | SVSHE = 1, $dV_{DVCC}/dt = 10\text{ mV}/\mu\text{s}$, SVSHFP = 1 | | 2.5 | | μs |
| | | SVSHE = 1, $dV_{DVCC}/dt = 1\text{ mV}/\mu\text{s}$, SVSHFP = 0 | | 20 | | |
| $t_{(SVSH)}$ | SVS _H on or off delay time | SVSHE = 0→1, SVSHFP = 1 | | 12.5 | | μs |
| | | SVSHE = 0→1, SVSHFP = 0 | | 100 | | |
| dV_{DVCC}/dt | DV_{CC} rise time | | 0 | | 1000 | V/s |

(1) The SVS_H settings available depend on the V_{CORE} (PMMCOREV) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)) on recommended settings and usage.

Table 5-20. PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---|--|------|------|------|------|
| $I_{(SVMH)}$ | SVM _H current consumption | SVMHE = 0, DV _{CC} = 3.6 V | | 0 | | nA |
| | | SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 0 | | 200 | | |
| | | SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 1 | | 2.0 | | μA |
| $V_{(SVMH)}$ | SVM _H on or off voltage level ⁽¹⁾ | SVMHE = 1, SVSMHRRRL = 0 | 1.65 | 1.74 | 1.86 | V |
| | | SVMHE = 1, SVSMHRRRL = 1 | 1.85 | 1.94 | 2.02 | |
| | | SVMHE = 1, SVSMHRRRL = 2 | 2.02 | 2.14 | 2.22 | |
| | | SVMHE = 1, SVSMHRRRL = 3 | 2.18 | 2.26 | 2.35 | |
| | | SVMHE = 1, SVSMHRRRL = 4 | 2.32 | 2.40 | 2.48 | |
| | | SVMHE = 1, SVSMHRRRL = 5 | 2.56 | 2.70 | 2.84 | |
| | | SVMHE = 1, SVSMHRRRL = 6 | 2.85 | 3.00 | 3.15 | |
| | | SVMHE = 1, SVSMHRRRL = 7 | 2.85 | 3.00 | 3.15 | |
| $t_{pd(SVMH)}$ | SVM _H propagation delay | SVMHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1 | | 2.5 | | μs |
| | | SVMHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0 | | 20 | | |
| $t_{(SVMH)}$ | SVM _H on or off delay time | SVMHE = 0→1, SVSMFPP = 1 | | 12.5 | | μs |
| | | SVMHE = 0→1, SVMHFP = 0 | | 100 | | |

(1) The SVM_H settings available depend on the V_{CORE} (PMMCOREV) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)) on recommended settings and usage.

Table 5-21. PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---------------------------------------|---|-----|------|-----|------|
| $I_{(SVSL)}$ | SVS _L current consumption | SVSLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFPP = 0 | | 200 | | |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFPP = 1 | | 2.0 | | μA |
| $t_{pd(SVSL)}$ | SVS _L propagation delay | SVSLE = 1, dV _{CORE} /dt = 10 mV/μs, SVSLFPP = 1 | | 2.5 | | μs |
| | | SVSLE = 1, dV _{CORE} /dt = 1 mV/μs, SVSLFPP = 0 | | 20 | | |
| $t_{(SVSL)}$ | SVS _L on or off delay time | SVSLE = 0→1, SVSLFPP = 1 | | 12.5 | | μs |
| | | SVSLE = 0→1, SVSLFPP = 0 | | 100 | | |

Table 5-22. PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---------------------------------------|---|-----|------|-----|------|
| $I_{(SVML)}$ | SVM _L current consumption | SVMLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFPP = 0 | | 200 | | |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFPP = 1 | | 2.0 | | μA |
| $t_{pd(SVML)}$ | SVM _L propagation delay | SVMLE = 1, dV _{CORE} /dt = 10 mV/μs, SVMLFPP = 1 | | 2.5 | | μs |
| | | SVMLE = 1, dV _{CORE} /dt = 1 mV/μs, SVMLFPP = 0 | | 20 | | |
| $t_{(SVML)}$ | SVM _L on or off delay time | SVMLE = 0→1, SVMLFPP = 1 | | 12.5 | | μs |
| | | SVMLE = 0→1, SVMLFPP = 0 | | 100 | | |

5.5.7 Timers

Table 5-23. Timer_A, Timers TA0, TA1, and TA2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---------------------|-------------------------------|--|-----------------|-----|-----|------|
| f _{TA} | Timer_A input clock frequency | Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ±10% | 1.8 V, 3 V | | 20 | MHz |
| t _{TA,cap} | Timer_A capture timing | All capture inputs, Minimum pulse duration required for capture | 1.8 V, 3 V | 20 | | ns |

Table 5-24. Timer_B, Timer TB0

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---------------------|-------------------------------|--|-----------------|-----|-----|------|
| f _{TB} | Timer_B input clock frequency | Internal: SMCLK, ACLK External: TBCLK Duty cycle = 50% ±10% | 1.8 V, 3 V | | 20 | MHz |
| t _{TB,cap} | Timer_B capture timing | All capture inputs, Minimum pulse duration required for capture | 1.8 V, 3 V | 20 | | ns |

5.5.8 Battery Backup

Table 5-25. Battery Backup

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|----------------------|--|---|-----------------|-----|------------------------|------------------------|------|------|
| I _{VBAT} | Current into VBAT terminal in case no primary battery is connected. | VBAT = 1.7 V, DVCC not connected, RTC running | 0 V | | T _A = -40°C | 0.43 | μA | |
| | | | | | T _A = 25°C | 0.52 | | |
| | | | | | T _A = 60°C | 0.58 | | |
| | | | | | T _A = 85°C | 0.66 | | |
| | | VBAT = 2.2 V, DVCC not connected, RTC running | | | T _A = -40°C | 0.50 | | |
| | | | | | T _A = 25°C | 0.59 | | |
| | | | | | T _A = 60°C | 0.64 | | |
| | | | | | T _A = 85°C | 0.72 | | |
| | | VBAT = 3 V, DVCC not connected, RTC running | | | T _A = -40°C | 0.68 | | |
| | | | | | T _A = 25°C | 0.75 | | |
| | | | | | T _A = 60°C | 0.79 | | |
| | | | | | T _A = 85°C | 0.86 | | |
| V _{SWITCH} | Switch-over level (V _{CC} to VBAT) | C _{VCC} = 4.7 μF | 0 V | | General | V _{SVSH_IT} - | V | |
| | | | | | SVSHRL = 0 | 1.59 | | 1.69 |
| | | | | | SVSHRL = 1 | 1.79 | | 1.91 |
| | | | | | SVSHRL = 2 | 1.98 | | 2.11 |
| | | | | | SVSHRL = 3 | 2.10 | | 2.23 |
| R _{ON_VBAT} | On-resistance of switch between VBAT and VBAK | V _{BAT} = 1.8 V | 0 V | | 0.35 | 1 | kΩ | |
| V _{BAT3} | VBAT to ADC: V _{BAT} divided, V _{BAT3} = V _{BAT} /3 | | 1.8 V | | 0.6 | ±5% | V | |
| | | | 3 V | | 1.0 | ±5% | | |
| | | | 3.6 V | | 1.2 | ±5% | | |
| V _{CHVx} | Charger end voltage | CHVx = 2 | | | 2.65 | 2.7 | 2.9 | V |

Battery Backup (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|--------------------------|-----------------|-----------------|-----|-----|------|------|
| R _{CHARGE} | Charge limiting resistor | CHCx = 1 | | | | 5.2 | kΩ |
| | | CHCx = 2 | | | | 10.2 | |
| | | CHCx = 3 | | | | 20 | |

5.5.9 USCI

Table 5-26. USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---------------------|--|--|-----------------|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ±10% | | | f _{SYSTEM} | MHz |
| f _{BITCLK} | BITCLK clock frequency (equals baud rate in MBaud) | | | | 1 | MHz |
| t _r | UART receive deglitch time ⁽¹⁾ | | 2.2 V | 50 | 600 | ns |
| | | | 3 V | 50 | 600 | |

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-27. USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾
(see [Figure 5-11](#) and [Figure 5-12](#))

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------------|--|---|-----------------|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | SMCLK, ACLK, Duty cycle = 50% ±10% | | | f _{SYSTEM} | MHz |
| t _{SU,MI} | SOMI input data setup time | PMMCOREV = 0 | 1.8 V | 55 | | ns |
| | | | 3 V | 38 | | |
| | | | 2.4 V | 30 | | |
| t _{HD,MI} | SOMI input data hold time | PMMCOREV = 3 | 3 V | 25 | | ns |
| | | | 1.8 V | 0 | | |
| | | | 3 V | 0 | | |
| t _{VALID,MO} | SIMO output data valid time ⁽²⁾ | UCLK edge to SIMO valid, C _L = 20 pF, PMMCOREV = 0 | 1.8 V | | 20 | ns |
| | | | 3 V | | 18 | |
| | | | 2.4 V | | 16 | |
| t _{HD,MO} | SIMO output data hold time ⁽³⁾ | UCLK edge to SIMO valid, C _L = 20 pF, PMMCOREV = 3 | 3 V | | 15 | ns |
| | | | 1.8 V | -10 | | |
| | | | 3 V | -8 | | |
| t _{HD,MO} | SIMO output data hold time ⁽³⁾ | C _L = 20 pF, PMMCOREV = 0 | 2.4 V | -10 | | ns |
| | | | 3 V | -8 | | |

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO}(USCI) + t_{SU,SI}(Slave), t_{SU,MI}(USCI) + t_{VALID,SO}(Slave))$.
For the slave parameters $t_{SU,SI}(Slave)$ and $t_{VALID,SO}(Slave)$, see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-11](#) and [Figure 5-12](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 5-11](#) and [Figure 5-12](#).

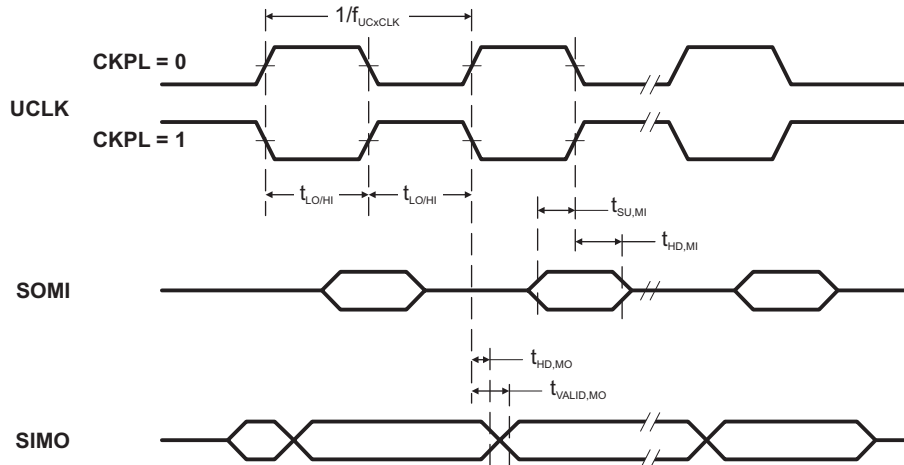


Figure 5-11. SPI Master Mode, CKPH = 0

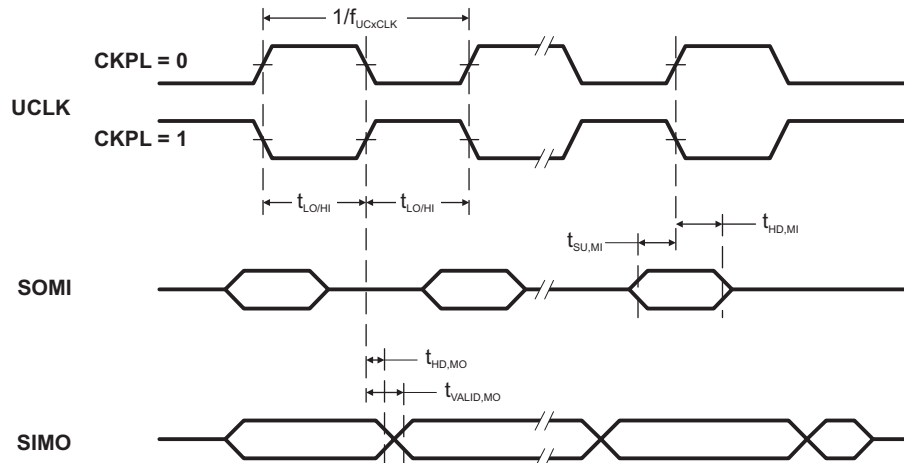


Figure 5-12. SPI Master Mode, CKPH = 1

Table 5-28. USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾
(see [Figure 5-13](#) and [Figure 5-14](#))

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------------|---|---|-----------------|-----|-----|------|
| t _{STE,LEAD} | STE lead time, STE low to clock | PMMCOREV = 0 | 1.8 V | 11 | ns | |
| | | | 3 V | 8 | | |
| | | PMMCOREV = 3 | 2.4 V | 7 | | |
| | | | 3 V | 6 | | |
| t _{STE,LAG} | STE lag time, Last clock to STE high | PMMCOREV = 0 | 1.8 V | 3 | ns | |
| | | | 3 V | 3 | | |
| | | PMMCOREV = 3 | 2.4 V | 3 | | |
| | | | 3 V | 3 | | |
| t _{STE,ACC} | STE access time, STE low to SOMI data out | PMMCOREV = 0 | 1.8 V | 66 | ns | |
| | | | 3 V | 50 | | |
| | | PMMCOREV = 3 | 2.4 V | 36 | | |
| | | | 3 V | 30 | | |
| t _{STE,DIS} | STE disable time, STE high to SOMI high impedance | PMMCOREV = 0 | 1.8 V | 30 | ns | |
| | | | 3 V | 30 | | |
| | | PMMCOREV = 3 | 2.4 V | 30 | | |
| | | | 3 V | 30 | | |
| t _{SU,SI} | SIMO input data setup time | PMMCOREV = 0 | 1.8 V | 5 | ns | |
| | | | 3 V | 5 | | |
| | | PMMCOREV = 3 | 2.4 V | 2 | | |
| | | | 3 V | 2 | | |
| t _{HD,SI} | SIMO input data hold time | PMMCOREV = 0 | 1.8 V | 5 | ns | |
| | | | 3 V | 5 | | |
| | | PMMCOREV = 3 | 2.4 V | 5 | | |
| | | | 3 V | 5 | | |
| t _{VALID,SO} | SOMI output data valid time ⁽²⁾ | UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 0 | 1.8 V | 76 | ns | |
| | | | 3 V | 60 | | |
| | | UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 3 | 2.4 V | 44 | | |
| | | | 3 V | 40 | | |
| t _{HD,SO} | SOMI output data hold time ⁽³⁾ | C _L = 20 pF, PMMCOREV = 0 | 1.8 V | 12 | ns | |
| | | | 3 V | 12 | | |
| | | C _L = 20 pF, PMMCOREV = 3 | 2.4 V | 12 | | |
| | | | 3 V | 12 | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.

For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-13](#) and [Figure 5-14](#).

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-13](#) and [Figure 5-14](#).

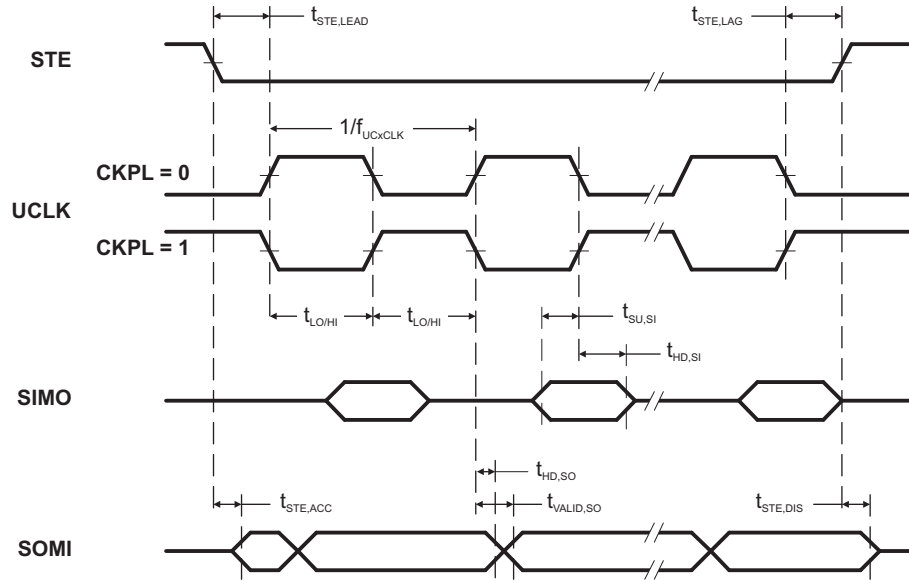


Figure 5-13. SPI Slave Mode, CKPH = 0

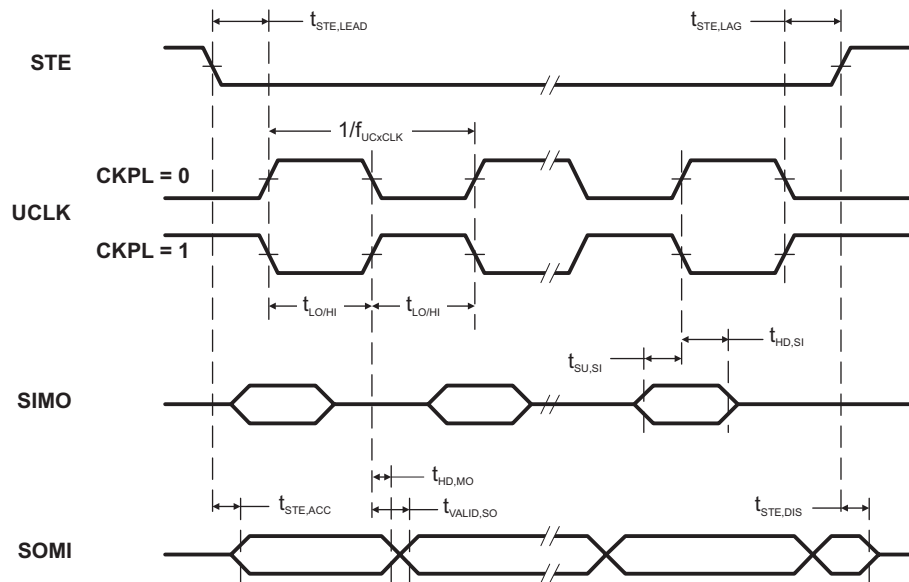


Figure 5-14. SPI Slave Mode, CKPH = 1

Table 5-29. USCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-15](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---------------------|---|--|--------------|---------------------|------|
| f _{USCI} | USCI input clock frequency | Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ±10% | | f _{SYSTEM} | MHz |
| f _{SCL} | SCL clock frequency | | 2.2 V, 3 V | 0 400 | kHz |
| t _{HD,STA} | Hold time (repeated) START | f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz | 2.2 V, 3 V | 4.0 0.6 | μs |
| t _{SU,STA} | Setup time for a repeated START | f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz | 2.2 V, 3 V | 4.7 0.6 | μs |
| t _{HD,DAT} | Data hold time | | 2.2 V, 3 V | 0 | ns |
| t _{SU,DAT} | Data setup time | | 2.2 V, 3 V | 250 | ns |
| t _{SU,STO} | Setup time for STOP | f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz | 2.2 V, 3 V | 4.0 0.6 | μs |
| t _{SP} | Pulse duration of spikes suppressed by input filter | | 2.2 V 3 V | 50 600 50 600 | ns |

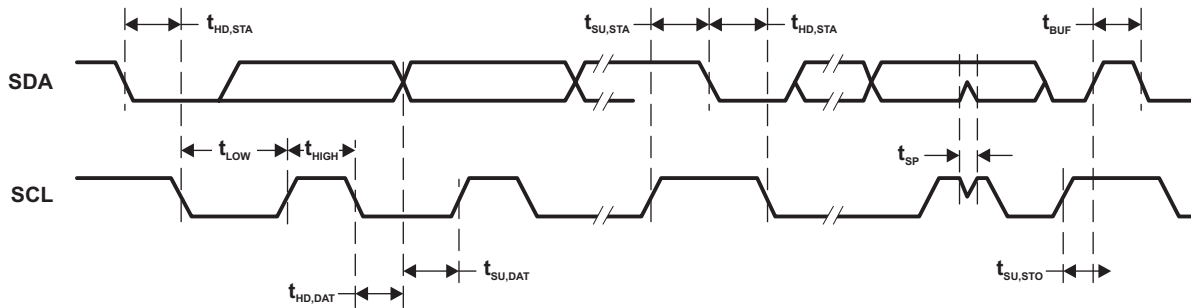


Figure 5-15. I²C Mode Timing

5.5.10 LCD Controller

Table 5-30. LCD_B, Recommended Operating Conditions

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT | |
|----------------------------|--|---|-----|-----------|--|---------------|
| $V_{CC,LCD_B,CP\ en,3,6}$ | Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.6\text{ V}$ | LCDPEN = 1, $0000 < VLCDx \leq 1111$ (charge pump enabled, $V_{LCD} \leq 3.6\text{ V}$) | | 2.2 | 3.6 | V |
| $V_{CC,LCD_B,CP\ en,3,3}$ | Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.3\text{ V}$ | LCDPEN = 1, $0000 < VLCDx \leq 1100$ (charge pump enabled, $V_{LCD} \leq 3.3\text{ V}$) | | 2.0 | 3.6 | V |
| $V_{CC,LCD_B,int.\ bias}$ | Supply voltage range, internal biasing, charge pump disabled | LCDPEN = 0, VLCDEXT = 0 | | 2.4 | 3.6 | V |
| $V_{CC,LCD_B,ext.\ bias}$ | Supply voltage range, external biasing, charge pump disabled | LCDPEN = 0, VLCDEXT = 0 | | 2.4 | 3.6 | V |
| $V_{CC,LCD_B,VLCDEXT}$ | Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled | LCDPEN = 0, VLCDEXT = 1 | | 2.0 | 3.6 | V |
| $V_{LCDCAP/R33}$ | External LCD voltage at LCDCAP/R33, internal or external biasing, charge pump disabled | LCDPEN = 0, VLCDEXT = 1 | | 2.4 | 3.6 | V |
| C_{LCDCAP} | Capacitor on LCDCAP when charge pump enabled | LCDPEN = 1, VLCDx > 0000 (charge pump enabled) | | 4.7 | 10 | μF |
| f_{Frame} | LCD frame frequency range | $f_{LCD} = 2 \times \text{MUX} \times f_{FRAME}$ (mux = 1 (static), 2, 3, 4) | | 0 | 100 | Hz |
| $f_{ACLK,in}$ | ACLK input frequency range | 30 | 32 | 40 | | kHz |
| C_{Panel} | Panel capacitance | 100-Hz frame frequency | | | 10000 | pF |
| V_{R33} | Analog input voltage at R33 | LCDPEN = 0, VLCDEXT = 1 | | 2.4 | $V_{CC} + 0.2$ | V |
| $V_{R23,1/3bias}$ | Analog input voltage at R23 | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | | V_{R13} | $V_{R03} + 2/3 \times (V_{R33} - V_{R03})$ | V_{R33} |
| $V_{R13,1/3bias}$ | Analog input voltage at R13 with 1/3 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | | V_{R03} | $V_{R03} + 1/3 \times (V_{R33} - V_{R03})$ | V_{R23} |
| $V_{R13,1/2bias}$ | Analog input voltage at R13 with 1/2 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1 | | V_{R03} | $V_{R03} + 1/2 \times (V_{R33} - V_{R03})$ | V_{R33} |
| V_{R03} | Analog input voltage at R03 | R0EXT = 1 | | V_{SS} | | V |
| $V_{LCD}-V_{R03}$ | Voltage difference between V_{LCD} and R03 | LCDPEN = 0, R0EXT = 1 | | 2.4 | $V_{CC} + 0.2$ | V |
| $V_{LCDREF/R13}$ | External LCD reference voltage applied at LCDREF/R13 | VLCDREFx = 01 | | 0.8 | 1.2 | 1.5 |

Table 5-31. LCD_B, Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------------|--|--|-----------------|-----|-----------------|-----|------|
| V _{LCD} | LCD voltage | VLCDx = 0000, VLCDxEXT = 0 | 2.4 V to 3.6 V | | V _{CC} | | V |
| | | LCDCPEN = 1, VLCDx = 0001 | 2 V to 3.6 V | | 2.60 | | |
| | | LCDCPEN = 1, VLCDx = 0010 | 2 V to 3.6 V | | 2.66 | | |
| | | LCDCPEN = 1, VLCDx = 0011 | 2 V to 3.6 V | | 2.72 | | |
| | | LCDCPEN = 1, VLCDx = 0100 | 2 V to 3.6 V | | 2.79 | | |
| | | LCDCPEN = 1, VLCDx = 0101 | 2 V to 3.6 V | | 2.85 | | |
| | | LCDCPEN = 1, VLCDx = 0110 | 2 V to 3.6 V | | 2.92 | | |
| | | LCDCPEN = 1, VLCDx = 0111 | 2 V to 3.6 V | | 2.98 | | |
| | | LCDCPEN = 1, VLCDx = 1000 | 2 V to 3.6 V | | 3.05 | | |
| | | LCDCPEN = 1, VLCDx = 1001 | 2 V to 3.6 V | | 3.10 | | |
| | | LCDCPEN = 1, VLCDx = 1010 | 2 V to 3.6 V | | 3.17 | | |
| | | LCDCPEN = 1, VLCDx = 1011 | 2 V to 3.6 V | | 3.24 | | |
| | | LCDCPEN = 1, VLCDx = 1100 | 2 V to 3.6 V | | 3.30 | | |
| | | LCDCPEN = 1, VLCDx = 1101 | 2.2 V to 3.6 V | | 3.36 | | |
| | | LCDCPEN = 1, VLCDx = 1110 | 2.2 V to 3.6 V | | 3.42 | | |
| LCDCPEN = 1, VLCDx = 1111 | 2.2 V to 3.6 V | | 3.48 | 3.6 | | | |
| I _{CC,Peak,CP} | Peak supply currents due to charge pump activities | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | | 400 | | μA |
| t _{LCD,CP,on} | Time to charge C _{LCD} when discharged | C _{LCD} = 4.7 μF, LCDCPEN = 0→1, VLCDx = 1111 | 2.2 V | | 100 | 500 | ms |
| I _{CP,Load} | Maximum charge pump load current | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | 50 | | | μA |
| R _{LCD,Seg} | LCD driver output impedance, segment lines | LCDCPEN = 1, VLCDx = 1000, I _{LOAD} = ±10 μA | 2.2 V | | | 10 | kΩ |
| R _{LCD,COM} | LCD driver output impedance, common lines | LCDCPEN = 1, VLCDx = 1000, I _{LOAD} = ±10 μA | 2.2 V | | | 10 | kΩ |

5.5.11 CTSD16

NOTE

The delta-sigma analog-to-digital converter uses the CTSD16. The CTSD16 is preceded by a unity-gain buffer stage following the channel muxing as shown in [Figure 6-1](#). Refer to [Table 5-46](#) for the electrical characteristics of the PGA buffer stages.

Table 5-32. CTSD16, Power Supply and Recommended Operating Conditions

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|---|--|----------------------|-----|--------------------|-----|------|
| V _{CC} | Supply voltage range | AVSS = DVSS = 0 V | | 2.2 | | 3.6 | V |
| I _{CTSD16} | Analog plus digital supply current per converter (reference current not included) | CTSD16OSRx = 256, CTSD16RRI = 0 | GAIN: 1, 2, 4, 8, 16 | 3 V | 190 ⁽¹⁾ | | μA |
| | | | GAIN: 1, 16 | 3 V | 300 ⁽¹⁾ | | |
| I _{CTSD16CLK} | CTSD16 clock current consumption | This is requested when CTSD16 is converting, or CTSD16RRIBURST = 0, or when OA is in rail-to-rail input mode (OARRI = 1), or when OA charge pump is on. The current should only be counted once even if both OA and CTSD16 are requesting the clock. | 3 V | | 205 | 240 | μA |

(1) Refer to [Table 5-33](#) to calculate total current from CTSD16 for different use cases.

[Table 5-33](#) explains how to compute the total current, I_{TOTAL}, when the CTSD, along with associated modules, are used. Refer to [Table 5-47](#) for a similar table for the OA. A "yes" means it must be included in computing I_{TOTAL}. Here is an example current calculation for CTS16D in rail-to-rail input mode (CTSD16RRI = 1) using the internal reference (CTSD16REFS = 1) and OA0 and OA1 enabled in rail-to-rail input modes, OARRI = 1.

As an example, assume that the application uses the CTS16D in rail-to-rail input mode (CTSD16RRI = 1) with the internal reference (CTSD16REFS = 1) and OA0 and OA1 are enabled in rail-to-rail input modes, OARRI = 1. The total current, I_{TOTAL}, would be computed as follows:

$$I_{TOTAL} = I_{CTSD16} + I_{CTSD16CLK} + I_{CP} + I_{REFBG} + 2 \times I_{OA}$$

Table 5-33. CTSD16, Current Calculation

| USE CASE NAME | USE CASE DETAILS | I _{CTSD16} | I _{CTSD16CLK} ⁽¹⁾ | I _{CP} ⁽²⁾ | I _{REFBG} ⁽³⁾ | I _{REF} ⁽⁴⁾ |
|----------------------------|------------------|---------------------|---------------------------------------|--------------------------------|---|---------------------------------|
| CTSD16 | | yes | yes | no | yes if CTSD16REFS = 1 no if CTSD16REFS = 0 | yes |
| CTSD16 rail-to-rail inputs | CTSD16RRI = 1 | yes | yes | yes | yes if CTSD16REFS = 1 no if CTSD16REFS = 0 | yes |

(1) Count this only once no matter how many modules use it. OA can also use this when rail-to-rail input is selected.

(2) Count this only once no matter how many modules use it. OA also uses this. This current is listed in the [Table 5-46](#) table.

(3) Count this only once no matter how many modules use it. DAC can use this as well as internal reference when it is available externally, REFOUT=1. This current is listed in the [Table 5-39](#) table.

(4) Count this only once no matter how many modules use it. This current is listed in the [Table 5-46](#) table. If I_{REFBG} is used that includes I_{REF} current.

Table 5-34. CTSD16, External Voltage Reference

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|---------------------|-----------------|-----------------|-----|-----|-----|------|
| V _{VeREF+} | Input voltage range | CTSD16REFS = 0 | 3 V | 1.0 | 1.2 | 1.5 | V |
| I _{VeREF+} | Input current | CTSD16REFS = 0 | 3 V | | | 50 | nA |

Table 5-35. CTSD16, Input Range⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|---------------------|---|--|-----------------|---|-----|---|------|----|
| V _{ID,FSR} | Differential full-scale input voltage range | V _{ID} = V _{I,A+} - V _{I,A-} | | -V _R /Gain | | +V _R /Gain | V | |
| V _{I,FSR} | Single-ended full-scale input voltage range | V _{ID} = V _{I,A+} - V _R <i>negative input is tied to V_R</i> | | V _R - V _R /Gain | | V _R + V _R /Gain | V | |
| V _{ID} | Differential input voltage range for specified performance ⁽²⁾ | CTSD16REFS = 1 | | | | CTSD16GAINx = 1 | ±928 | mV |
| | | | | | | CTSD16GAINx = 2 | ±464 | |
| | | | | | | CTSD16GAINx = 4 | ±232 | |
| | | | | | | CTSD16GAINx = 8 | ±116 | |
| | | | | | | CTSD16GAINx = 16 | ±58 | |
| V _I | Single-ended input voltage range for specified performance | | | V _R - (0.8 × V _R /Gain) | | V _R + (0.8 × V _R /Gain) | V | |
| Z _I | Input impedance (pin Ax or ADx+ or ADx- to AVSS) | CTSD16GAINx = 1, 16 | 3 V | | 20 | | MΩ | |
| Z _{ID} | Differential input impedance (pin ADx+ to pin ADx-) | CTSD16GAINx = 1, 16 | 3 V | | 35 | | MΩ | |
| V _I | Absolute input voltage range | | | AVSS | | V _{CC} | V | |
| V _{IC} | Common-mode input voltage range | | | AVSS | | V _{CC} | V | |

(1) All parameters pertain to each CTSD16 input.

 (2) The full-scale range is defined by V_{FSR+} = +V_R/GAIN and V_{FSR-} = -V_R/GAIN; FSR = V_{FSR+} - V_{FSR-} = 2xV_R/GAIN. If V_R is sourced externally, the analog input range should not exceed 80% of V_{FSR+} or V_{FSR-}; that is, V_{ID} = 0.8 V_{FSR-} to 0.8 V_{FSR+}. If V_R is sourced internally, the given V_{ID} ranges apply.

Table 5-36. CTSD16, Performance

CTSD16OSRx = 256, CTSD164REFS = 1

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|----------------|--|--|-----------------|--|-------|-----|------|----|
| f _M | modulator clock | | | | 1.024 | | MHz | |
| SINAD | Signal-to-noise + distortion ratio for differential inputs | CTSD16GAINx = 1, input ADx+ and ADx- (differential) | 3 V | f _{IN} = 50 Hz ⁽¹⁾ | | 84 | 87 | dB |
| | | CTSD16GAINx = 2, input ADx+ and ADx- (differential) | | | | 86 | | |
| | | CTSD16GAINx = 4, input ADx+ and ADx- (differential) | | | | 85 | | |
| | | CTSD16GAINx = 8, input ADx+ and ADx- (differential) | | | | 82 | | |
| | | CTSD16GAINx = 16, input ADx+ and ADx- (differential) | | | | 77 | | |

(1) The following voltages were applied to the CTSD16 inputs:

$$V_{I,A+}(t) = 0 \text{ V} + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$$

$$V_{I,A-}(t) = 0 \text{ V} - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$$

 resulting in a differential voltage of V_{ID} = V_{IN,A+}(t) - V_{IN,A-}(t) = V_{PP} × sin(2π × f_{IN} × t) with V_{PP} being selected as the maximum value allowed for a given range (according to CTSD16 input range).

CTSD16, Performance (continued)

CTSD16OSRx = 256, CTSD164REFS = 1

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------------|---|---|-----------------|-----|------|------|------------|
| SINAD | Signal-to-noise + distortion ratio for single-ended input | CTSD16GAINx = 1, input Ax (single-ended) | 3 V | | 83 | | dB |
| | | CTSD16GAINx = 2, input Ax (single-ended) | | | 82 | | |
| | | CTSD16GAINx = 4, input Ax (single-ended) | | | 78 | | |
| | | CTSD16GAINx = 8, input Ax (single-ended) | | | 72 | | |
| | | CTSD16GAINx = 16, input Ax (single-ended) | | | 66 | | |
| G | Nominal gain | CTSD16GAINx = 1 | 3 V | | 1 | | |
| | | CTSD16GAINx = 2 | | | 2 | | |
| | | CTSD16GAINx = 4 | | | 4 | | |
| | | CTSD16GAINx = 8 | | | 8 | | |
| | | CTSD16GAINx = 16 | | | 16 | | |
| E _G | Gain error | CTSD16GAINx: 1,8,16 with external reference (1.2 V) | 3 V | -1% | | +1% | |
| ΔE _G /ΔT | Gain error temperature coefficient, internal reference | CTSD16GAINx: 1,8,16. | 3 V | | 3 | 50 | ppm/°C |
| ΔE _G /ΔT | Gain error temperature coefficient, external reference | CTSD16GAIN: 1,8,16 with external reference (1.2 V) | 3 V | | 4 | 15 | ppm/°C |
| ΔE _G /ΔV _{CC} | Gain error vs VCC | CTSD16GAINx: 1,8,16. | | | 0.02 | | %/V |
| E _{OS} | Offset error | CTSD16GAINx = 1 | 3 V | | | ±4.1 | mV |
| | | CTSD16GAINx = 16 | | | | ±3.4 | |
| ΔEOS/ΔT | Offset error temperature coefficient | CTSD16GAINx = 1, 16 | 3 V | | ±1 | ±10 | ppm/FSR/°C |
| ΔEOS/ΔV _{CC} | Offset error vs VCC | CTSD16GAINx = 1, 16 | 3 V | | 11 | | μV/V |
| CMRR, 50 Hz | Common-mode rejection ratio at 50 Hz | CTSD16GAINx = 1, V _{ID} = 928 mV, f _{IN} = 50 Hz | 3 V | | 78 | | dB |
| | | CTSD16GAINx = 16, V _{ID} = 58 mV, f _{IN} = 50 Hz | | | 80 | | |
| AC PSRR | AC power supply rejection ratio | CTSD16GAINx: 1, V _{CC} = 3 V ±50 mV × sin(2π × f _{VCC} × t), f _{VCC} = 50 Hz, Inputs grounded (no analog signal applied) | | | 95 | | dB |
| | | CTSD16GAINx: 8, V _{CC} = 3 V ±50 mV × sin(2π × f _{VCC} × t), f _{VCC} = 50 Hz, Inputs grounded (no analog signal applied) | | | 105 | | |
| | | CTSD16GAINx: 16, V _{CC} = 3 V ±50 mV × sin(2π × f _{VCC} × t), f _{VCC} = 50 Hz, Inputs grounded (no analog signal applied) | | | 105 | | |
| DC PSRR | DC power supply rejection ratio | CTSD16GAINx: (1, 8, 16), V _{CC} = 2.2 V to 3.6 V, (PSRR [dB] = -20 log(dV _{out} /dV _{cc}) with dV _{out} observed as change in the digital conversion result; assumed to be dominated by reference) | | | 90 | | dB |

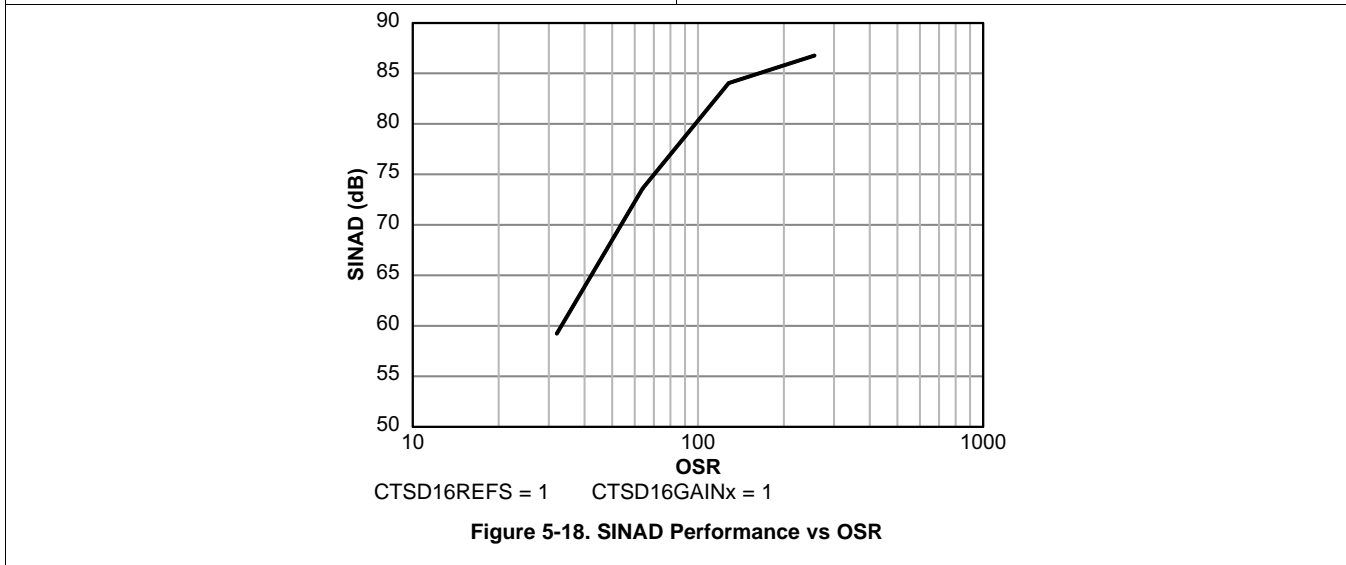
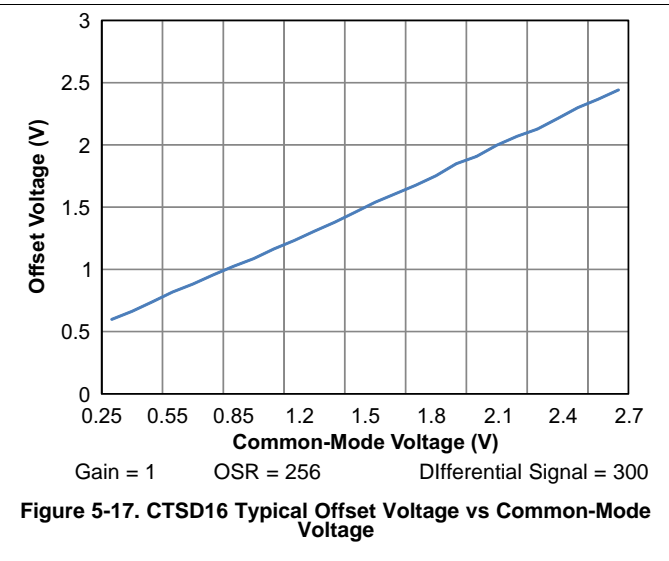
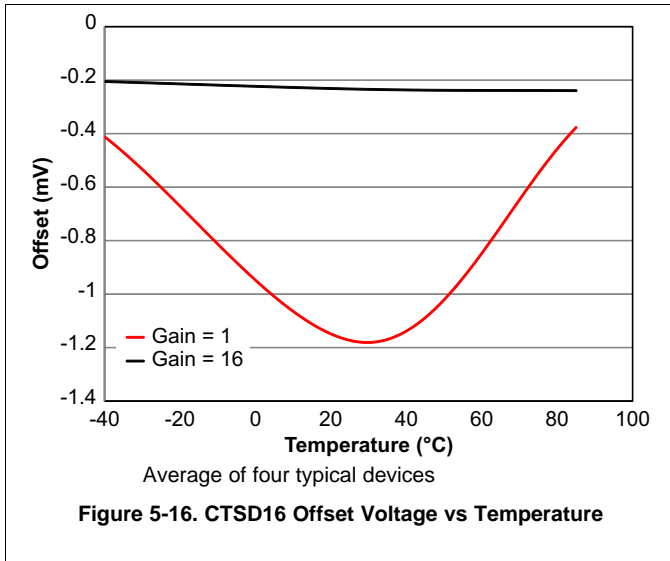


Table 5-37. Built-in V_{CC} Sense

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------|---------------------------------|----------------------------------|----------------------|----------------------------------|------|
| V _{CC,sense} | AV _{CC} divider | CTSD16ON = 1, CTSD16INCH = 0111 | 0.95 × (AV _{CC} / 2) | AV _{CC} / 2 | 1.05 × (AV _{CC} / 2) | V |

Table 5-38. Temperature Sensor

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|--|---|-----|-----|-----|------|
| V _{sensor} | Temperature sensor output voltage ^{(1) (2)} | CTSD16ON = 1, CTSD16INCH = 110, V _{CC} = 3 V, T _A = 30°C | | 800 | | mV |
| I _{sensor} | Temperature sensor quiescent current consumption | CTSD16ON = 1, CTSD16INCH = 110, T _A = 85°C | | 2 | | uA |

- (1) The temperature sensor offset can be as much as ±30°C. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
- (2) The device descriptor structure contains calibration values for 30°C ±3°C and 85°C ±3°C for each of the available reference voltage levels. The sensor voltage can be computed as V_{SENSE} = TC_{SENSOR} * (Temperature, °C) + V_{SENSOR}, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.

5.5.12 REF

Table 5-39. REF and REFBG, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---|--|-------|------|-----------|-----------------------|
| I_{REFBG} | Operating supply current into AVCC terminal ⁽¹⁾ | $V_{CC} = 3.0\text{ V}$, REFON = 1 and REFOUT = 1 | | 110 | 130 | μA |
| V_{REFBG} | Bandgap output voltage calibrated | $V_{CC} = 3.0\text{ V}$, $V_{eREF+} \leq 1.5\text{ V}$ if used | 1.146 | 1.16 | 1.174 | V |
| I_{REF} | Operating supply current into AVCC terminal ⁽¹⁾ | $V_{CC} = 3.0\text{ V}$, REFON=1 | | 15 | 20 | μA |
| V_{REF} | Positive built-in reference voltage output | REFVSEL = {2} for 2.5 V, REFON = 1 | | 2.5 | $\pm 1\%$ | V |
| | | REFVSEL = {1} for 2.0 V, REFON = 1 | | 2.0 | $\pm 1\%$ | |
| | | REFVSEL = {0} for 1.5 V, REFON = 1 | | 1.5 | $\pm 1\%$ | |
| $AV_{CC(min)}$ | AVCC minimum voltage, Positive built-in reference active | DAC12SREFx=0, REFVSEL = {0} for 1.5 V | | 2.2 | | V |
| | | DAC12SREFx=0, REFVSEL = {1} for 2 V | | 2.3 | | |
| | | DAC12SREFx=0, REFVSEL = {2} for 2.5 V | | 2.8 | | |
| PSRR_DC | Power supply rejection ratio (DC) | $V_{CC} = 2.2\text{ V}$ to 3.6 V , $T_A = 25^\circ\text{C}$ | | 50 | | $\mu\text{V/V}$ |
| PSRR_AC | Power supply rejection ratio (AC) | $V_{CC} = 2.2\text{ V}$ to 3.6 V , $T_A = 25^\circ\text{C}$, $f = 1\text{ kHz}$, $\Delta V_{pp} = 100\text{ mV}$ | | 1.5 | | mV/V |
| TC_{REF+} | Bandgap reference temperature coefficient ⁽²⁾ | $I_{VREF+} = 0\text{ A}$ | | 15 | 50 | ppm/ $^\circ\text{C}$ |
| t_{SETTLE} | Settling time of V_{REFBG} reference voltage ⁽³⁾ | $AV_{CC} = AV_{CC(min)}$ through $AV_{CC(max)}$, REFON = 0 \rightarrow 1 | | | 120 | μs |
| C_{VREFBG} | Capacitance at VREFBG terminal | See ⁽⁴⁾ | | | 1 | nF |
| I_{LOAD} | VREFBG maximum load current | REFOUT = REFON = 1 | | | 1 | mA |
| $I_{L(VREFBG)}$ | Load-current regulation, VREFBG terminal ⁽⁵⁾ | $I_{(VREF+)} = +1\text{ mA}$ or -1 mA , $AV_{CC} = AV_{CC(min)}$, REFON = REFOUT = 1 | | | 3.5 | mV/mA |

(1) The internal reference current is supplied from terminal AVCC. Consumption is independent of the CTSD16ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

(2) Calculated using the box method: $(\text{MAX}(-40^\circ\text{C} \text{ to } 85^\circ\text{C}) - \text{MIN}(-40^\circ\text{C} \text{ to } 85^\circ\text{C})) / \text{MIN}(-40^\circ\text{C} \text{ to } 85^\circ\text{C}) / (85^\circ\text{C} - (-40^\circ\text{C}))$.

(3) The condition is that the error in a conversion started after t_{REFON} is less than ± 0.5 LSB.

(4) There is no capacitance required on VREFBG if the reference voltage is not used externally. However, TI recommends a capacitance close to the maximum value to reduce any reference voltage noise.

(5) Contribution only due to the reference and buffer including package. This does not include resistance due to PCB traces or other external factors.

5.5.13 DAC

Table 5-40. 12-Bit DAC, Supply Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|-----------------|-----|-----|------|------|
| AV _{CC} Analog supply voltage | AV _{CC} = DV _{CC} , AV _{SS} = DV _{SS} = 0 V | | 2.2 | | 3.6 | V |
| I _{DD} Supply current, single DAC channel ^{(1) (2)} | DAC12AMP _x = 2, DAC12IR = 0, DAC12OG = 1, DAC12_xDAT = 0800h, VeREF+ = VREFBG = 1.16 V | 3 V | | 65 | 110 | μA |
| | DAC12AMP _x = 2, DAC12IR = 1, DAC12_xDAT = 0800h, VeREF+ = AV _{CC} | 2.2 V to 3.6 V | | 125 | 165 | |
| | DAC12AMP _x = 5, DAC12IR = 1, DAC12_xDAT = 0800h, VeREF+ = AV _{CC} | | | 250 | 350 | |
| | DAC12AMP _x = 7, DAC12IR = 1, DAC12_xDAT = 0800h, VeREF+ = AV _{CC} | | | 750 | 1100 | |
| PSRR Power supply rejection ratio ^{(3) (4)} | DAC12_xDAT = 800h, VeREF+ = 1.16 V or 1.5 V, ΔAV _{CC} = 100 mV | 2.2 V to 3.6 V | | 70 | | dB |
| | DAC12_xDAT = 800h, VeREF+ = 1.16 V or 2.5 V, ΔAV _{CC} = 100 mV | 3 V | | 70 | | |

- (1) No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
- (2) Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications [Table 5-43](#).
- (3) PSRR = 20 log (ΔAV_{CC} / ΔV_{DAC12_xOUT})
- (4) The internal reference is not used.

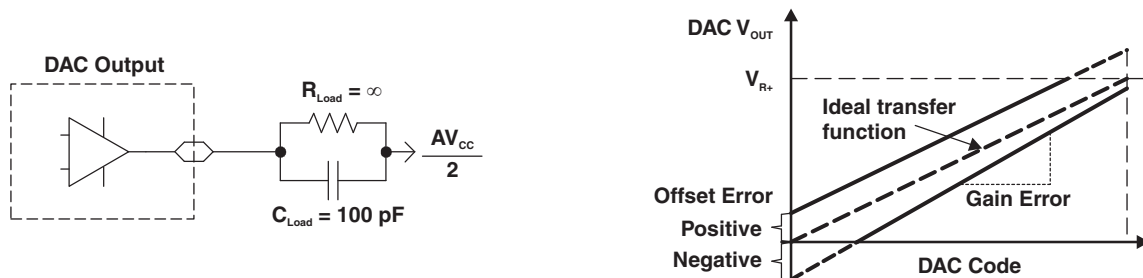


Figure 5-19. Linearity Test Load Conditions and Gain/Offset Definition

Table 5-41. 12-Bit DAC, Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-19](#))

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|-------------------------|---|---|---|------------|-----|---------------|------|------|
| | Resolution | 12-bit monotonic | | 12 | | | bits | |
| INL | Integral nonlinearity ⁽¹⁾ | V _{eREF+} = 1.16 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V, 3 V | ±2 | | ±4 | LSB | |
| | | V _{eREF+} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V, 3 V | ±2 | | ±4 | | |
| DNL | Differential nonlinearity ⁽¹⁾ | V _{eREF+} = 1.16 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V, 3 V | ±0.4 | | ±1 | LSB | |
| | | V _{eREF+} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V, 3 V | ±0.4 | | ±1 | | |
| E _O | Offset voltage | Without calibration ^{(1) (2)} | V _{eREF+} = 1.16 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V, 3 V | | | mV | |
| | | | V _{eREF+} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V, 3 V | | | | |
| | | With calibration ^{(1) (2)} | V _{eREF+} = 1.16 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V, 3 V | | | | ±1.5 |
| | | | V _{eREF+} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1 | 2.2 V, 3 V | | | | ±1.5 |
| d _{E(O)/dT} | Offset error temperature coefficient ⁽¹⁾ | With calibration | 2.2 V, 3 V | ±10 | | µV/°C | | |
| E _G | Gain error | V _{eREF+} = 1.16 V | 2.2 V, 3 V | | | ±2.5 | %FSR | |
| | | V _{eREF+} = 2.5 V | 2.2 V, 3 V | | | ±2.5 | | |
| d _{E(G)/dT} | Gain temperature coefficient ⁽¹⁾ | | 2.2 V, 3 V | 10 | | ppm of FSR/°C | | |
| t _{Offset_Cal} | Time for offset calibration ⁽³⁾ | DAC12AMPx = 2 | 2.2 V, 3 V | | | 165 | ms | |
| | | DAC12AMPx = 3, 5 | | | | 66 | | |
| | | DAC12AMPx = 4, 6, 7 | | | | 16.5 | | |

(1) Parameters calculated from the best-fit curve from 0x0F to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation: $y = a + bx$. $V_{DAC12_xOUT} = E_O + (1 + E_G) \times (V_{eREF+}/4095) \times DAC12_xDAT$, DAC12IR = 1.

(2) The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON

(3) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. TI recommends configuring the DAC12 module before initiating calibration. Port activity during calibration may affect accuracy and is not recommended.

Table 5-42. 12-Bit DAC, Output Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|--|-----------------|-------------------------|-----|------------------|------|
| V _O | No load, V _{eREF+} = AV _{CC} , DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7 | 2.2 V, 3.6 V | 0 | | 0.005 | V |
| | No load, V _{eREF+} = AV _{CC} , DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7 | | AV _{CC} - 0.05 | | AV _{CC} | |
| | R _{Load} = 3 kΩ, V _{eREF+} = AV _{CC} , DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7 | | 0 | | 0.1 | |
| | R _{Load} = 3 kΩ, V _{eREF+} = AV _{CC} , DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7 | | AV _{CC} - 0.13 | | AV _{CC} | |
| C _{L(DAC12)} | Maximum DAC12 load capacitance | 2.2 V, 3.6 V | | | 100 | pF |
| I _{L(DAC12)} | DAC12AMPx = 2, DAC12_xDAT = 0FFFh, V _{O/P(DAC12)} > AV _{CC} - 0.3 | 2.2 V, 3.6 V | -1 | | | mA |
| | DAC12AMPx = 2, DAC12_xDAT = 0h, V _{O/P(DAC12)} < 0.3 V | | | | 1 | |
| R _{O/P(DAC12)} | R _{Load} = 3 kΩ, V _{O/P(DAC12)} < 0.3 V, DAC12AMPx = 2, DAC12_xDAT = 0h | 2.2 V, 3.6 V | | 150 | 250 | Ω |
| | R _{Load} = 3 kΩ, V _{O/P(DAC12)} > AV _{CC} - 0.3 V, DAC12_xDAT = 0FFFh | | | 150 | 250 | |
| | R _{Load} = 3 kΩ, 0.3 V ≤ V _{O/P(DAC12)} ≤ AV _{CC} - 0.3 V | | | | | |

(1) Data is valid after the offset calibration of the output amplifier.

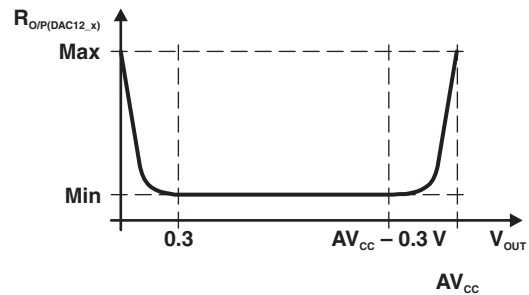
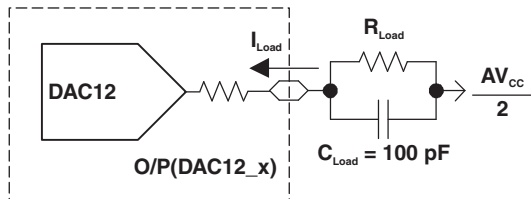


Figure 5-20. DAC12_x Output Resistance Tests

Table 5-43. 12-Bit DAC, Reference Input Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|--|-----------------|----------------------|----------------------|------------------------|------|
| V _{eREF+} | Reference input voltage range | DAC12IR = 0 ⁽¹⁾ (2) | 2.2 V to 3.6 V | AV _{CC} / 3 | AV _{CC} / 3 | AV _{CC} + 0.2 | V |
| | | DAC12IR = 1 ⁽³⁾ (4) | | | | | |
| R _{i(VREFBG)} , R _{i(VeREF+)} | Reference input resistance ⁽⁵⁾ | DAC12_0 IR = DAC12_1 IR = 0 | 2.2 V, 3 V | 20 | 52 | 52 | MΩ |
| R _{i(VREF+)} , R _{i(VeREF+)} | | DAC12_0 IR = 1, DAC12_1 IR = 0 | | | | | |
| | | DAC12_0 IR = 0, DAC12_1 IR = 1 | | | | | |
| | | DAC12_0 IR = DAC12_1 IR = 1, DAC12_0 SREFx = DAC12_1 SREFx ⁽⁶⁾ | | | | | |

- (1) For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
- (2) The maximum voltage applied at reference input voltage terminal VeREF+ = [AV_{CC} - V_{E(O)}] / [3 × (1 + E_G)].
- (3) For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
- (4) The maximum voltage applied at reference input voltage terminal VeREF+ = [AV_{CC} - V_{E(O)}] / (1 + E_G).
- (5) This impedance depends on tradeoff in power savings. Current devices have 48 kΩ for each channel when divide is enabled. Can be increased if performance can be maintained.
- (6) When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

Table 5-44. 12-Bit DAC, Dynamic Specifications

V_{REF} = V_{CC}, DAC12IR = 1 (see Figure 5-21 and Figure 5-22), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|-----------------------------|--|-----------------|------|------|------|------|
| t _{ON} | DAC12 on time | DAC12_xDAT = 800h, Error _{V(O)} < ±0.5 LSB ⁽¹⁾ (see Figure 5-21) | 2.2 V, 3 V | 60 | 120 | 15 | 30 |
| | | DAC12AMPx = 0 → {2, 3, 4} | | | | | |
| | | DAC12AMPx = 0 → {5, 6} | | | | | |
| t _{S(FS)} | Settling time, full scale | DAC12_xDAT = 80h → F7Fh → 80h | 2.2 V, 3 V | 100 | 200 | 40 | 80 |
| | | DAC12AMPx = 2 | | | | | |
| | | DAC12AMPx = 3, 5 | | | | | |
| t _{S(C-C)} | Settling time, code to code | DAC12_xDAT = 3F8h → 408h → 3F8h, BF8h → C08h → BF8h | 2.2 V, 3 V | 5 | 2 | 1 | μs |
| | | DAC12AMPx = 2 | | | | | |
| | | DAC12AMPx = 3, 5 | | | | | |
| SR | Slew rate | DAC12_xDAT = 80h → F7Fh → 80h ⁽²⁾ | 2.2 V, 3 V | 0.05 | 0.35 | 0.35 | 1.10 |
| | | DAC12AMPx = 2 | | | | | |
| | | DAC12AMPx = 3, 5 | | | | | |
| Glitch energy | Glitch energy | DAC12_xDAT = 800h → 7FFh → 800h | 2.2 V, 3 V | 1.50 | 5.20 | 35 | nV-s |
| | | DAC12AMPx = 4, 6, 7 | | | | | |

- (1) R_{Load} and C_{Load} connected to AV_{SS} (not AV_{CC}/2) in Figure 5-21.
- (2) Slew rate applies to output voltage steps ≥ 200 mV.

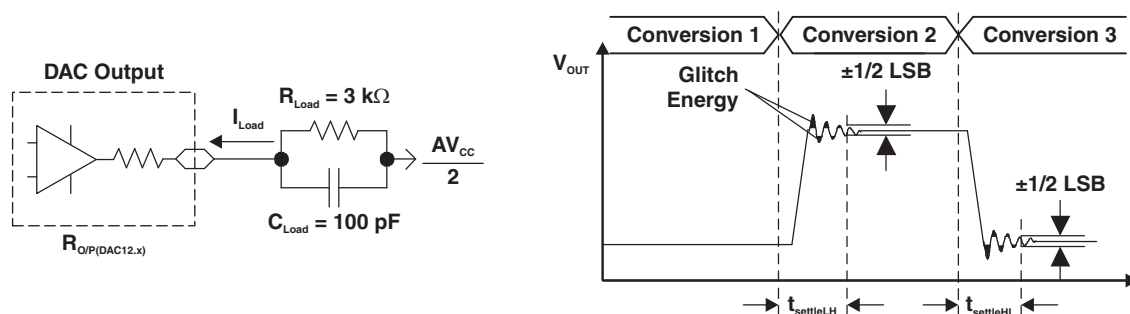


Figure 5-21. Settling Time and Glitch Energy Testing

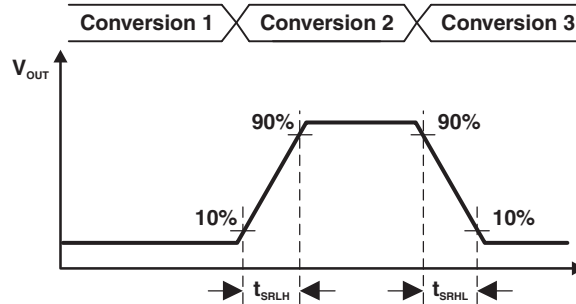


Figure 5-22. Slew Rate Testing

Table 5-45. 12-Bit DAC, Dynamic Specifications (Continued)

over recommended ranges of supply voltage and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|--|--|------------|-----|-----|-----|------|
| BW_{-3dB} 3-dB bandwidth, $V_{DC} = 1.5\text{ V}$, $V_{AC} = 0.1\text{ V}_{PP}$ (see Figure 5-23) | DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h | 2.2 V, 3 V | 40 | | | kHz |
| | DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h | | 180 | | | |
| | DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h | | 550 | | | |
| Channel-to-channel crosstalk ⁽¹⁾ (see Figure 5-24) | DAC12_0DAT = 800h, No load, DAC12_1DAT = 80h \leftrightarrow F7Fh, $R_{Load} = 3\text{ k}\Omega$, $f_{DAC12_1OUT} = 10\text{ kHz}$ at 50/50 duty cycle | 2.2 V, 3 V | | -80 | | dB |
| | DAC12_0DAT = 80h \leftrightarrow F7Fh, $R_{Load} = 3\text{ k}\Omega$, DAC12_1DAT = 800h, No load, $f_{DAC12_0OUT} = 10\text{ kHz}$ at 50/50 duty cycle | | | -80 | | |

(1) $R_{Load} = 3\text{ k}\Omega$, $C_{Load} = 100\text{ pF}$

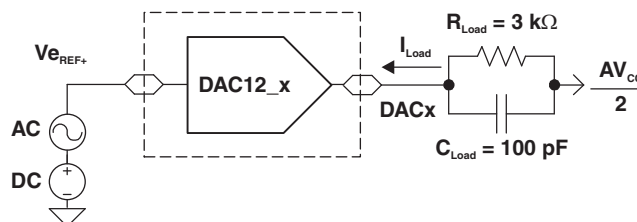


Figure 5-23. Test Conditions for 3-dB Bandwidth Specification

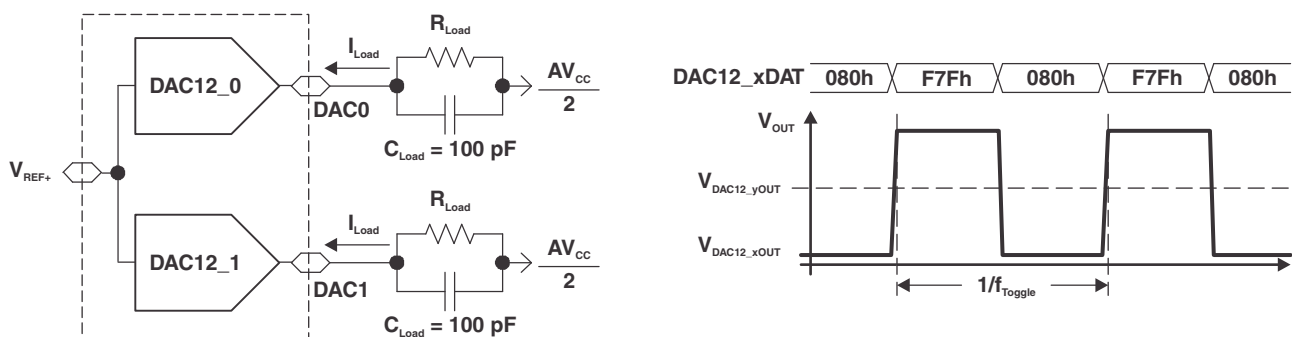


Figure 5-24. Crosstalk Test Conditions

5.5.14 Operational Amplifier

Table 5-46. Operational Amplifier, OA0, OA1, PGA Buffers

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|--|--|-----------------|-----|--------------------|-----------------------|--------|
| V _{CC} | Analog supply voltage | AV _{CC} = DV _{CC} , AV _{SS} = DV _{SS} = 0 V | | 2.2 | | 3.6 | V |
| C _{CP} CAP | External charge pump capacitor to AV _{SS} . | Required when charge pump is enabled | | 20 | 22 | 24 | nF |
| I _{CP} PEAK | Charge pump peak current | OARRI = 0h to 1h, I _{CP} LOAD = 0 μA | | | 1.6 | | mA |
| I _{CP} | Charge pump average current | OARRI = 1h, I _{CP} LOAD = 100 μA | | | 570 ⁽¹⁾ | 710 ⁽¹⁾ | μA |
| t _{CP} EN fast | Charge pump enable time fast | OARRI = 0h to 1h, I _{CP} LOAD = 0 μA, AFE biases previously enabled and settled which can be done with REFON=1 or other modules requesting REFON. | | | 50 | | μs |
| t _{CP} EN slow | Charge pump enable time slow | OARRI = 0h to 1h, I _{CP} LOAD = 0 μA, Includes AFE bias settling | | | 75 | | μs |
| I _{OA} | Supply current, per opamp | I _O = 0 mA, OARRI = 0h (charge pump disabled) | | | 105 ⁽¹⁾ | 130 ⁽¹⁾ | μA |
| V _{OS} | Input offset voltage | Noninverting, unity gain | | | ±2 | | mV |
| dV _{OS} /dT | Input offset voltage temperature drift | Noninverting, unity gain | | | ±1 | | μV/°C |
| dV _{OS} /dV | Input offset voltage voltage drift | Noninverting, unity gain | | | ±3 | | μV/V |
| C _{in} | Input capacitance | Differential | | | 4 | | pF |
| | | Common mode | | | 6 | | pF |
| PSRR _{DC} | Power supply rejection ratio, DC | Noninverting, unity gain, V _{INP} = positive input of OA = 1 V | | | 50 | | μV/V |
| V _{CM} | Common mode voltage range ⁽²⁾ | OARRI = 0h, Noninverting, unity gain | | 0.1 | | V _{CC} - 1.0 | V |
| | | OARRI = 1h, Noninverting, unity gain | | 0.1 | | V _{CC} - 0.1 | V |
| CMRR _{DC} | Common mode rejection ratio, DC | Over common-mode voltage range | | | 110 | | dB |
| e _n | Input voltage noise density | f = 100 Hz, OARRI = 0h or 1h | 3.0 V | | 90 | | nV/√Hz |
| | | f = 50 kHz, OARRI = 0h or 1h | 3.0 V | | 25 | | |
| A _{OL} | Open-loop voltage gain, DC | | | | 95 | | dB |
| GBW | Gain-bandwidth product | C _L = 100 pF, OAM = 1h | | | 800 | | kHz |
| SR | Slew rate | Noninverting, unity gain, C _L = 100 pF, OAM = 1h | | | 0.4 | | V/μs |
| t _{SETTLE} | Settling time | Noninverting, unity gain, 2.0-V step, 0.1%, OAM = 1h | 3.0 V | | 5.3 | | μs |
| V _O | Voltage output swing from rail | -250 μA ≤ I _O ≤ 250 μA, Noninverting, unity gain (OAM = 1h) | | | 5 | 55 | mV |

(1) Refer to Table 5-47 to calculate total current from OA for different use cases.

(2) The common-mode input range is measured with the OA in a unity-gain source-follower configuration. The input signal is swept from 0 V to V_{CC}, and the output of the OA is monitored. The minimum and maximum values represent when the input and output differ more than 10 mV, not including the offset, V_{OS}.

Operational Amplifier, OA0, OA1, PGA Buffers (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------------------------|--|-----------------|-----|-----|-----|------|
| t _{EN_FAST} Enable time fast | Noninverting, unity gain, OAM = 0h transition to 1h, AFE biases previously enabled and settled which can be done with REFON=1 or other modules requesting REFON ⁽³⁾ | | | 3 | 7 | μs |
| t _{EN_SLOW} Enable time slow | Noninverting, unity gain, OARRI = 0h transition to 1h, OAM = 0h transition to 1h, Includes AFE bias and charge pump settling ⁽³⁾ | | | 190 | 225 | μs |
| t _{DIS} Disable time | | | | 0.4 | | μs |

(3) The AFE bias is used by several modules including the OA charge pump, OA, and CTSD16. Any of these modules will request the AFE bias when enabled. The AFE bias is generated by the REF module, so enabling the REF module also enables the AFE bias.

Table 5-47 explains how to compute the total current, I_{TOTAL}, when the OA and associated modules are used. Refer to Table 5-33 for a similar table for the CTSD16. A "yes" means it must be included in computing I_{TOTAL}.

As an example, assume that the application uses the CTS16D in rail-to-rail input mode (CTSD16RRI = 1) with the internal reference (CTSD16REFS = 1) and OA0 and OA1 are enabled in rail-to-rail input modes, OARRI = 1. The total current, I_{TOTAL}, would be computed as follows:

$$I_{TOTAL} = I_{CTSD16} + I_{CTSD16CLK} + I_{CP} + I_{REFBG} + 2 \times I_{OA}$$

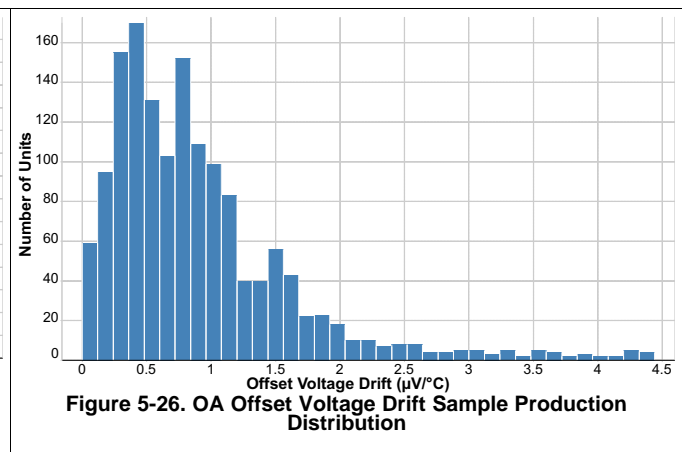
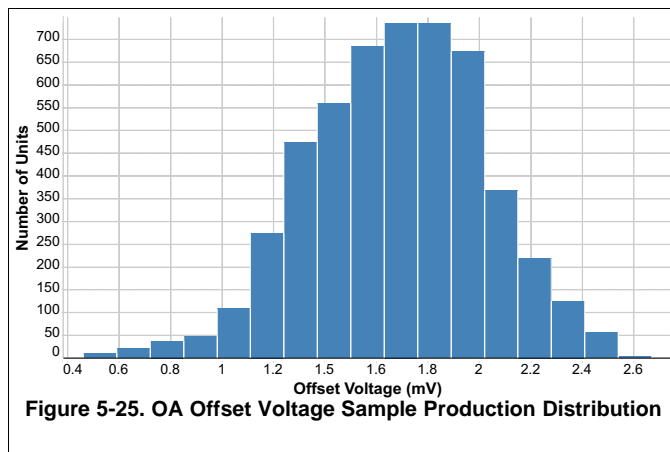


Table 5-47. OA, Current Calculation

| USE CASE NAME | USE CASE DETAILS | I _{OA} | I _{CTSD16CLK} ⁽¹⁾ | I _{CP} ⁽²⁾ | I _{REF} ⁽³⁾ |
|-----------------------------------|---|-----------------|---------------------------------------|--------------------------------|---------------------------------|
| OA | OARRI = 0 | yes | no | no | yes |
| OA with rail-to-rail input | OARRI = 1 | yes | yes | yes | yes |
| Rail-to-rail input up, module off | (CTSD16SC = 0) AND (CTSD16RRI = 1) AND (CTSD16RRIBURST = 0) OR ((OARRI = 1 (for any OA)) AND (OAM = 0)) | no | yes | yes | yes |

(1) Count this current only once no matter how many modules use it. CTSD16 and the charge pump also use this. This current is listed in Table 5-32.

(2) Count this current only once no matter how many modules use it. CTSD16 also uses this when rail-to-rail inputs are selected.

(3) Count this current only once no matter how many modules use it. This current is listed in Table 5-46. If I_{REFBG} is used, that includes the I_{REF} current.

5.5.15 Switches

Table 5-48. Ground Switches (GSW0A, GSW0B, GSW1A, GSW1B)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----|-------|------|------|
| V _{CC} Supply voltage | | 2.2 | | 3.6 | V |
| I _{LKG} Input leakage ⁽¹⁾ | T _A = 0°C to 60°C | | ±0.25 | | nA |
| | T _A = -40°C to 85°C | | | ±50 | |
| I _{IN} Input current switch to AVSS | | 0 | | 100 | µA |
| R _{ON} Switch ON resistance with switch closed | I _{IN} = 100 µA, T _A = -40°C to 85°C | | 9.5 | 18.5 | Ω |
| R _{OFF} Switch OFF resistance with switch open | T _A = -40°C to 85°C, Input signal frequency < 100 Hz | 100 | | | MΩ |
| t _{ON/OFF} Enable or disable time | T _A = -40°C to 85°C | | 0.25 | | µs |

(1) Ground switches are shared with general-purpose I/Os. This leakage includes all leakage seen at the device pin, not only leakage caused by the switch itself.

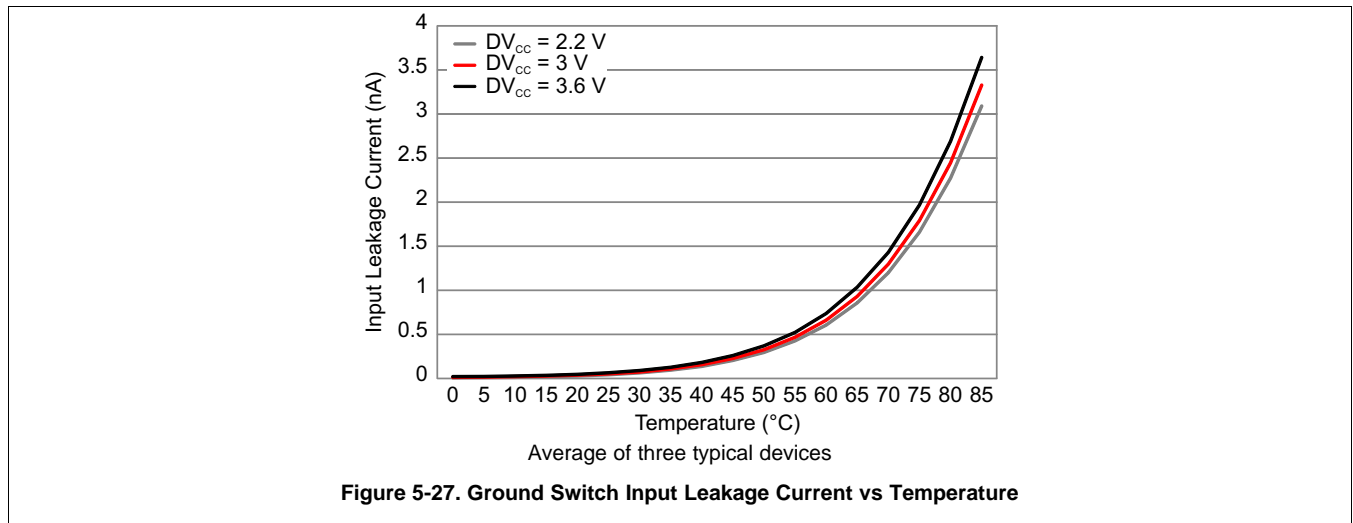


Figure 5-27. Ground Switch Input Leakage Current vs Temperature

Table 5-49. Operational Amplifier Switches

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|--|--|-----|-------|-----|------|
| V _{CC} | Supply voltage | | 2.2 | | 3.6 | V |
| I _{LKG} | Input leakage ⁽¹⁾ | T _A = 0°C to 60°C | | ±0.25 | | nA |
| | | T _A = -40°C to 85°C | | | ±50 | |
| I _{IN} | Input current through switch | | 0 | | 100 | µA |
| R _{ON} | Switch ON resistance with switch closed ⁽²⁾ | I _{IN} = 100 µA, T _A = -40°C to 85°C | | 1 | | kΩ |
| R _{OFF} | Switch OFF resistance with switch open | T _A = -40°C to 85°C, Input signal frequency < 100 Hz | 100 | | | MΩ |
| t _{ON/OFF} | Enable or disable time | T _A = -40°C to 85°C | | 0.45 | | µs |

- (1) This leakage includes all leakage seen at the device pin, not only leakage caused by the switch itself. It assumes a total of five switches present and a shared digital I/O.
 (2) The resistance varies with input voltage range. This resistance represents the peak resistance at the worst case input range (see Figure 5-29).

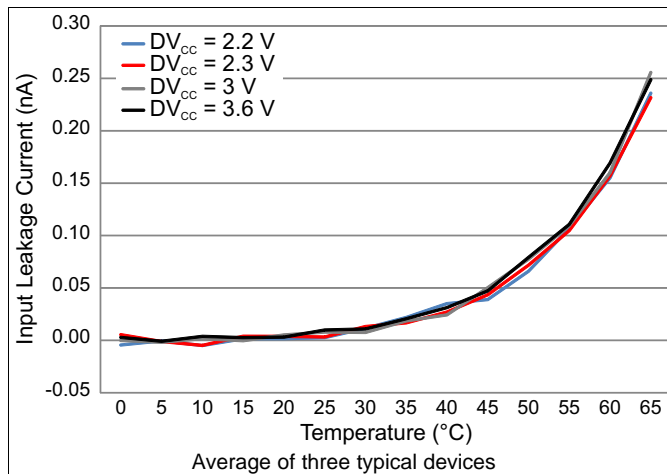


Figure 5-28. OA Switch Input Leakage Current vs Temperature

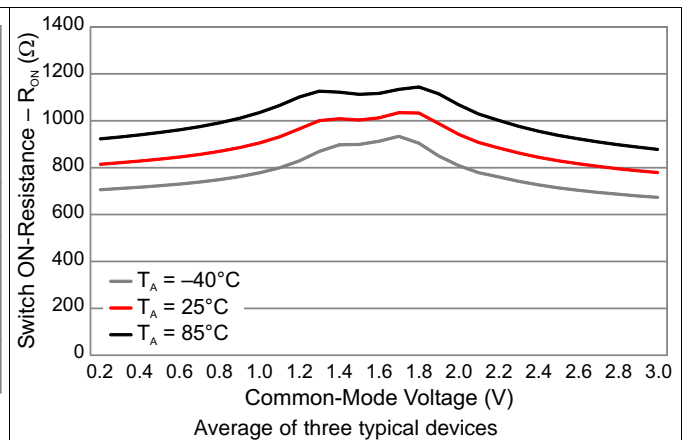


Figure 5-29. OA Switch R_{ON} vs Common-Mode Voltage

5.5.16 Comparator

Table 5-50. Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|------------------------|---|---|------------|--------------------------------|------------------------------|--------------------------------|----|
| V _{CC} | Supply voltage | | 1.8 | | 3.6 | V | |
| I _{AVCC_COMP} | Comparator operating supply current into AVCC, Excludes reference resistor ladder | CBPWRMD = 00, CBON = 1, CBRSx = 00 | 1.8 V | | 40 | μA | |
| | | | 2.2 V | 30 | 50 | | |
| | | | 3 V | 40 | 65 | | |
| | | CBPWRMD = 01, CBON = 1, CBRSx = 00 | 2.2 V, 3 V | 10 | 30 | | |
| | | CBPWRMD = 10, CBON = 1, CBRSx = 00 | 2.2 V, 3 V | 0.5 | 1.3 | | |
| I _{AVCC_REF} | Quiescent current of resistor ladder into AVCC, Includes REF module current | CBREFACC = 1, CBREFLx = 01, CBRSx = 10, REFON = 0, CBON = 0 | 2.2 V, 3 V | 10 | 22 | μA | |
| V _{IC} | Common mode input range | | 0 | | V _{CC} - 1 | V | |
| V _{OFFSET} | Input offset voltage | CBPWRMD = 00 | | -20 | 20 | mV | |
| | | CBPWRMD = 01, 10 | | -10 | 10 | | |
| C _{IN} | Input capacitance | | | 5 | | pF | |
| R _{SIN} | Series input resistance | ON (switch closed) | | 3 | 4 | kΩ | |
| | | OFF (switch open) | | 50 | | MΩ | |
| t _{PD} | Propagation delay, response time | CBPWRMD = 00, CBF = 0 | | | 450 | ns | |
| | | CBPWRMD = 01, CBF = 0 | | | 600 | | |
| | | CBPWRMD = 10, CBF = 0 | | | 50 | μs | |
| t _{PD,filter} | Propagation delay with filter active | CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 00 | | 0.35 | 0.6 | 1.5 | μs |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 01 | | 0.6 | 1.0 | 1.8 | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 10 | | 1.0 | 1.8 | 3.4 | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 11 | | 1.8 | 3.4 | 6.5 | |
| t _{EN_CMP} | Comparator enable time | CBON = 0 to CBON = 1, | | 1 | 2 | μs | |
| t _{EN_REF} | Resistor reference enable time | CBON = 0 to CBON = 1 | | 1.0 | 1.5 | μs | |
| TC _{CB_REF} | Temperature coefficient of V _{CB_REF} | | | | 50 | ppm/°C | |
| V _{CB_REF} | Reference voltage for a given tap | V _{IN} = reference into resistor ladder, n = 0 to 31 | | V _{IN} × (n+0.5) / 32 | V _{IN} × (n+1) / 32 | V _{IN} × (n+1.5) / 32 | V |

5.5.17 USB

Table 5-51. Ports PU.0 and PU.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------|---------------------------|--|-----|------|
| V_{OH} | High-level output voltage | $V_{USB} = 3.3\text{ V} \pm 10\%$, $I_{OH} = -25\text{ mA}$ | | V |
| V_{OL} | Low-level output voltage | $V_{USB} = 3.3\text{ V} \pm 10\%$, $I_{OL} = 25\text{ mA}$ | | V |
| V_{IH} | High-level input voltage | $V_{USB} = 3.3\text{ V} \pm 10\%$ | | V |
| V_{IL} | Low-level input voltage | $V_{USB} = 3.3\text{ V} \pm 10\%$ | | V |

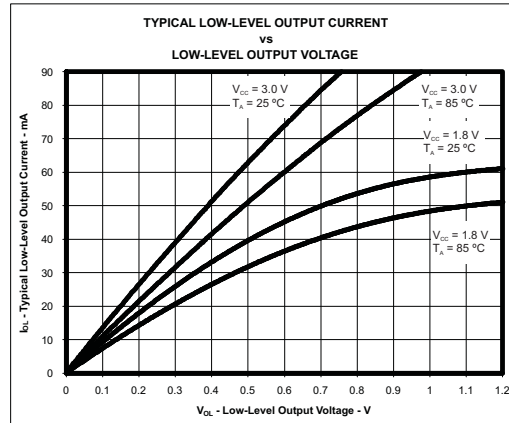


Figure 5-30. Ports PU.0, PU.1 Typical Low-Level Output Characteristics

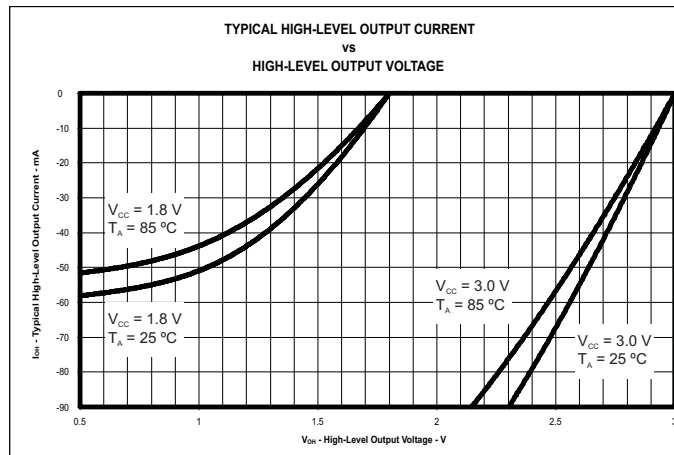


Figure 5-31. Ports PU.0, PU.1 Typical High-Level Output Characteristics

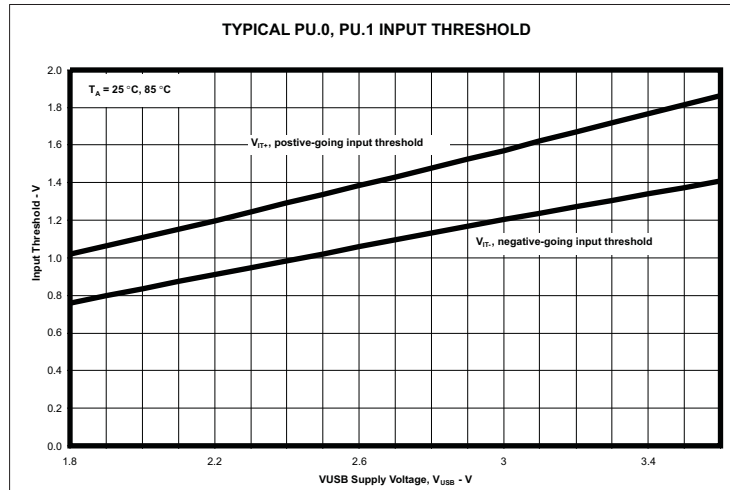


Figure 5-32. Ports PU.0, PU.1 Typical Input Threshold Characteristics

Table 5-52. USB Output Ports DP and DM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|---|-----|-----|------|
| V _{OH} | D+, D– single ended USB 2.0 load conditions | 2.8 | 3.6 | V |
| V _{OL} | D+, D– single ended USB 2.0 load conditions | 0 | 0.3 | V |
| Z _(DRV) | D+, D– impedance Including external series resistor of 27 Ω | 28 | 44 | Ω |
| t _{RISE} | Rise time Full speed, differential, C _L = 50 pF, 10%/90%, R _{pu} on D+ | 4 | 20 | ns |
| t _{FALL} | Fall time Full speed, differential, C _L = 50 pF, 10%/90%, R _{pu} on D+ | 4 | 20 | ns |

Table 5-53. USB Input Ports DP and DM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | MIN | MAX | UNIT | |
|-------------------|--------------------------------------|-----|------|----|
| V _(CM) | Differential input common mode range | 0.8 | 2.5 | V |
| Z _(IN) | Input impedance | 300 | | kΩ |
| V _{CRS} | Crossover voltage | 1.3 | 2.0 | V |
| V _{IL} | Static SE input logic low level | 0.8 | | V |
| V _{IH} | Static SE input logic high level | | 2.0 | V |
| VDI | Differential input voltage | | 0.2 | V |

Table 5-54. USB-PWR (USB Power System)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--|-------------------------------------|------|-----|------|------|
| V _{LAUNCH} | V _{BUS} detection threshold | | | | 3.75 | V |
| V _{BUS} | USB bus voltage | Normal operation | 3.76 | | 5.5 | V |
| V _{USB} | USB LDO output voltage | | | 3.3 | ±9% | V |
| V ₁₈ | Internal USB voltage ⁽¹⁾ | | | 1.8 | | V |
| I _{USB_EXT} | Maximum external current from V _{USB} terminal ⁽²⁾ | USB LDO is on | | | 12 | mA |
| I _{DET} | USB LDO current overload detection ⁽³⁾ | | 60 | | 100 | mA |
| I _{SUSPEND} | Operating supply current into V _{BUS} terminal ⁽⁴⁾ | USB LDO is on, USB PLL disabled | | | 250 | µA |
| C _{BUS} | V _{BUS} terminal recommended capacitance | | | 4.7 | | µF |
| C _{USB} | V _{USB} terminal recommended capacitance | | | 220 | | nF |
| C ₁₈ | V ₁₈ terminal recommended capacitance | | | 220 | | nF |
| t _{ENABLE} | Settling time V _{USB} and V ₁₈ | Within 2%, recommended capacitances | | | 2 | ms |
| RPUR | Pullup resistance of PUR terminal | | 70 | 110 | 150 | Ω |

- (1) This voltage is for internal use only. No external DC loading should be applied.
- (2) This represents additional current that can be supplied to the application from the V_{USB} terminal beyond the needs of the USB operation.
- (3) A current overload is detected when the total current supplied from the USB LDO, including I_{USB_EXT}, exceeds this value.
- (4) Does not include current contribution of R_{pu} and R_{pd} as outlined in the USB specification.

Table 5-55. USB-PLL (USB Phase-Locked Loop)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------------|--------------------------|-----|------|-----|------|
| I _{PLL} | Operating supply current | | | 7 | mA |
| f _{PLL} | PLL frequency | | 48 | | MHz |
| f _{UPD} | PLL reference frequency | 1.5 | | 3 | MHz |
| t _{LOCK} | PLL lock time | | | 2 | ms |
| t _{Jitter} | PLL jitter | | 1000 | | ps |

5.5.18 Flash

Table 5-56. Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----------------------|-----------------|-----------------|-----|--------|
| DV _{CC(PGM/ERASE)} | Program and erase supply voltage | | 1.8 | | 3.6 | V |
| I _{PGM} | Average supply current from DV _{CC} during program | | | 3 | 5 | mA |
| I _{ERASE} | Average supply current from DV _{CC} during erase | | | 6 | 11 | mA |
| I _{MERASE} , I _{BANK} | Average supply current from DV _{CC} during mass erase or bank erase | | | 6 | 11 | mA |
| t _{CPT} | Cumulative program time | See ⁽¹⁾ | | | 16 | ms |
| | Program and erase endurance | | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | T _J = 25°C | 100 | | | years |
| t _{Word} | Word or byte program time | See ⁽²⁾ | 64 | | 85 | μs |
| t _{Block, 0} | Block program time for first byte or word | See ⁽²⁾ | 49 | | 65 | μs |
| t _{Block, 1–(N–1)} | Block program time for each additional byte or word, except for last byte or word | See ⁽²⁾ | 37 | | 49 | μs |
| t _{Block, N} | Block program time for last byte or word | See ⁽²⁾ | 55 | | 73 | μs |
| t _{Seg Erase} | Erase time for segment, mass erase, and bank erase when available | See ⁽²⁾ | 23 | | 32 | ms |
| f _{MCLK,MGR} | MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1) | | 0 | | 1 | MHz |

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.

(2) These values are hardwired into the state machine of the flash controller.

5.5.19 Debug and Emulation

Table 5-57. JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|-----------------|-------|-----|-----|------|
| f _{SBW} | Spy-Bi-Wire input frequency | 2.2 V, 3 V | 0 | | 20 | MHz |
| t _{SBW,Low} | Spy-Bi-Wire low clock pulse duration | 2.2 V, 3 V | 0.025 | | 15 | μs |
| t _{SBW,En} | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾ | 2.2 V, 3 V | | | 1 | μs |
| t _{SBW,Rst} | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | μs |
| f _{TCK} | TCK input frequency (4-wire JTAG) ⁽²⁾ | 2.2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | MHz |
| R _{internal} | Internal pulldown resistance on TEST | 2.2 V, 3 V | 45 | 60 | 80 | kΩ |

(1) Tools that access the Spy-Bi-Wire interface must wait for the t_{SBW,En} time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 Overview

The MSP430FG6626 and MSP430FG6625 are microcontroller configurations with a high-performance 16-bit analog-to-digital converter (ADC), dual 12-bit digital-to-analog converters (DACs), dual low-power operational amplifiers (OAs), a comparator (COMPB), two universal serial communication interfaces (USCIs), USB 2.0, a hardware multiplier (MPY32), DMA, four 16-bit timers, a real-time clock (RTC) module with alarm capabilities, an LCD driver, and up to 73 I/O pins.

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6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

6.3 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. [Table 6-1](#) shows examples of the three types of instruction formats; [Table 6-2](#) shows the address modes.

Table 6-1. Instruction Word Formats

| INSTRUCTION WORD FORMAT | EXAMPLE | OPERATION |
|-----------------------------------|-----------|-----------------------|
| Dual operands, source-destination | ADD R4,R5 | R4 + R5 → R5 |
| Single operands, destination only | CALL R8 | PC → (TOS), R8 → PC |
| Relative jump, un/conditional | JNE | Jump-on-equal bit = 0 |

Table 6-2. Address Mode Descriptions

| ADDRESS MODE | S ⁽¹⁾ | D ⁽¹⁾ | SYNTAX | EXAMPLE | OPERATION |
|-------------------------|------------------|------------------|------------------|------------------|-------------------------------|
| Register | + | + | MOV Rs,Rd | MOV R10,R11 | R10 → R11 |
| Indexed | + | + | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5) → M(6+R6) |
| Symbolic (PC relative) | + | + | MOV EDE,TONI | | M(EDE) → M(TONI) |
| Absolute | + | + | MOV &MEM, &TCDAT | | M(MEM) → M(TCDAT) |
| Indirect | + | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) → M(Tab+R6) |
| Indirect auto-increment | + | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) → R11 R10 + 2 → R10 |
| Immediate | + | | MOV #X,TONI | MOV #45,TONI | #45 → M(TONI) |

(1) S = source, D = destination

6.4 Operating Modes

The devices have one active mode and seven software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
 - FLL loop control remains active
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - FLL loop control is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO's DC generator remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO's DC generator is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO's DC generator is disabled
 - Crystal oscillator is stopped
 - Complete data retention
- Low-power mode 3.5 (LPM3.5)
 - Internal regulator disabled
 - No data retention
 - RTC enabled and clocked by low-frequency oscillator
 - Wake up from $\overline{\text{RST}}/\text{NMI}$, RTC_B, P1, P2, P3, and P4
- Low-power mode 4.5 (LPM4.5)
 - Internal regulator disabled
 - No data retention
 - Wake up from $\overline{\text{RST}}/\text{NMI}$, P1, P2, P3, and P4

6.5 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-3. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|--|------------------|--------------|-------------|
| System Reset Power-Up, External Reset Watchdog Time-out, Key Violation Flash Memory Key Violation | WDTIFG, KEYV (SYSRSTIV) ⁽¹⁾⁽²⁾ | Reset | 0FFFEh | 63, highest |
| System NMI PMM Vacant Memory Access JTAG Mailbox | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) ⁽¹⁾ | (Non)maskable | 0FFFCh | 62 |
| User NMI NMI Oscillator Fault Flash Memory Access Violation | NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV) ⁽¹⁾⁽²⁾ | (Non)maskable | 0FFFAh | 61 |
| Comp_B | Comparator B interrupt flags (CBIV) ⁽¹⁾⁽³⁾ | Maskable | 0FFF8h | 60 |
| Timer TB0 | TB0CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFF6h | 59 |
| Timer TB0 | TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TBIV) ⁽¹⁾⁽³⁾ | Maskable | 0FFF4h | 58 |
| Watchdog Interval Timer Mode | WDTIFG | Maskable | 0FFF2h | 57 |
| USCI_A0 Receive or Transmit | UCA0RXIFG, UCA0TXIFG (UCA0IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFF0h | 56 |
| USCI_B0 Receive or Transmit | UCB0RXIFG, UCB0TXIFG (UCB0IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFEEh | 55 |
| CTSD16 | CTSD16IFG0, CTSD16OVIFG0 ⁽¹⁾⁽³⁾ | Maskable | 0FFECCh | 54 |
| Timer TA0 | TA0CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFEAh | 53 |
| Timer TA0 | TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFE8h | 52 |
| USB_UBM ⁽⁴⁾ | USB interrupts (USBIV) ⁽¹⁾⁽³⁾ | Maskable | 0FFE6h | 51 |
| LDO-PWR ⁽⁵⁾ | LDOOFFIFG, LDOONIFG, LDOOVLIFG | | | |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG, DMA3IFG, DMA4IFG, DMA5IFG (DMAIV) ⁽¹⁾⁽³⁾ | Maskable | 0FFE4h | 50 |
| Timer TA1 | TA1CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFE2h | 49 |
| Timer TA1 | TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFE0h | 48 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFDEh | 47 |
| USCI_A1 Receive or Transmit | UCA1RXIFG, UCA1TXIFG (UCA1IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFDCh | 46 |
| USCI_B1 Receive or Transmit | UCB1RXIFG, UCB1TXIFG (UCB1IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFDAh | 45 |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFD8h | 44 |
| LCD_B | LCD_B Interrupt Flags (LCDBIV) ⁽¹⁾ | Maskable | 0FFD6h | 43 |
| RTC_B | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV) ⁽¹⁾⁽³⁾ | Maskable | 0FFD4h | 42 |
| DAC12_A | DAC12_0IFG, DAC12_1IFG ⁽¹⁾⁽³⁾ | Maskable | 0FFD2h | 41 |
| Timer TA2 | TA2CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFD0h | 40 |
| Timer TA2 | TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFCEh | 39 |
| I/O Port P3 | P3IFG.0 to P3IFG.7 (P3IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFCCh | 38 |
| I/O Port P4 | P4IFG.0 to P4IFG.7 (P4IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFCAh | 37 |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

(3) Interrupt flags are located in the module.

(4) Only on devices with peripheral module USB (MSP430FG6626 and MSP430FG6625)

(5) Only on devices with peripheral module LDO-PWR (MSP430FG6426 and MSP430FG6425)

Table 6-3. Interrupt Sources, Flags, and Vectors (continued)

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|------------------|-------------------------|------------------|--------------|-----------|
| Reserved | Reserved ⁽⁶⁾ | | 0FFC8h | 36 |
| | | | ⋮ | ⋮ |
| | | | 0FF80h | 0, lowest |

(6) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

6.6 USB BSL

The devices MSP430FG6626 and MSP430FG6625 come pre-programmed with the USB BSL. Use of the USB BSL requires external access to the six pins shown in Table 6-4. In addition to these pins, the application must support external components necessary for normal USB operation; for example, the proper crystal on XT2IN and XT2OUT, proper decoupling, and so on.

Table 6-4. USB BSL Pin Requirements and Functions

| DEVICE SIGNAL | BSL FUNCTION |
|---|------------------------------|
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | Entry sequence signal |
| PU.0/DP | USB data terminal DP |
| PU.1/DM | USB data terminal DM |
| PUR | USB pullup resistor terminal |
| VBUS | USB bus power supply |
| VSSU | USB ground supply |

NOTE

The default USB BSL evaluates the logic level of the PUR pin after a BOR reset. If it is pulled high externally, then the BSL is invoked. Therefore, unless the application is invoking the BSL, it is important to keep PUR pulled low after a BOR reset, even if BSL or USB is never used. TI recommends applying a 1-M Ω resistor to ground.

6.7 UART BSL

On devices without an USB module (MSP430FG642x) come pre-programmed with the UART BSL. A UART BSL is also available for devices with the USB module (MSP430FG662x), and it can be programmed by the user into the BSL memory by replacing the pre-programmed factory-supplied USB BSL. Use of the UART BSL requires external access to the six pins shown in Table 6-5.

Table 6-5. UART BSL Pin Requirements and Functions

| DEVICE SIGNAL | BSL FUNCTION |
|---|-----------------------|
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | Entry sequence signal |
| TEST/SBWTK | Entry sequence signal |
| P1.1 | Data transmit |
| P1.2 | Data receive |
| VCC | Power supply |
| VSS | Ground supply |

6.8 JTAG Operation

6.8.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/Os. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in Table 6-6. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 6-6. JTAG Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|-----------|-----------------------------|
| PJ.3/TCK | IN | JTAG clock input |
| PJ.2/TMS | IN | JTAG state control |
| PJ.1/TDI/TCLK | IN | JTAG data input, TCLK input |
| PJ.0/TDO | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | IN | External reset |
| VCC | | Power supply |
| VSS | | Ground supply |

6.8.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in Table 6-7. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 6-7. Spy-Bi-Wire Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|-----------|-------------------------------|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | IN, OUT | Spy-Bi-Wire data input/output |
| VCC | | Power supply |
| VSS | | Ground supply |

6.9 Flash Memory

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

6.10 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data is lost. Features of the RAM include:

- RAM has n sectors. The size of a sector can be found in [Section 6.14](#).
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.
- For devices that contain USB memory, the USB memory can be used as normal RAM if USB is not required.

6.11 Backup RAM

The backup RAM provides a limited number of bytes of RAM that are retained during LPMx.5 and during operation from a backup supply if the Battery Backup System module is implemented.

There are 8 bytes of backup RAM. It can be word-wise accessed through the control registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3.

6.12 Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)).

6.12.1 Digital I/O

There are up to nine 8-bit I/O ports implemented: P1 through P9 are complete except P5.2, and port PJ contains four individual I/O ports.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- Edge-selectable interrupt input capability for all the eight bits of ports P1, P2, P3, and P4.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P9) or word-wise (P1 through P8) in pairs (PA through PD).

6.12.2 Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P2 (see [Table 6-8](#)).

Table 6-8. Port Mapping Mnemonics and Functions

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|--------------------------|-----------------|--|--------------------------------------|
| 0 | PM_NONE | None | DVSS |
| 1 | PM_CBOUT | - | Comparator_B output |
| | PM_TB0CLK | Timer TB0 clock input | - |
| 2 | Reserved | - | Reserved |
| | PM_DMAE0 | DMAE0 Input | - |
| 3 | PM_SVMOUT | - | SVM output |
| | PM_TB0OUTH | Timer TB0 high impedance input TB0OUTH | - |
| 4 | PM_TB0CCR0B | Timer TB0 CCR0 capture input CCI0B | Timer TB0: TB0.0 compare output Out0 |
| 5 | PM_TB0CCR1B | Timer TB0 CCR1 capture input CCI1B | Timer TB0: TB0.1 compare output Out1 |
| 6 | PM_TB0CCR2B | Timer TB0 CCR2 capture input CCI2B | Timer TB0: TB0.2 compare output Out2 |
| 7 | PM_TB0CCR3B | Timer TB0 CCR3 capture input CCI3B | Timer TB0: TB0.3 compare output Out3 |
| 8 | PM_TB0CCR4B | Timer TB0 CCR4 capture input CCI4B | Timer TB0: TB0.4 compare output Out4 |
| 9 | PM_TB0CCR5B | Timer TB0 CCR5 capture input CCI5B | Timer TB0: TB0.5 compare output Out5 |
| 10 | PM_TB0CCR6B | Timer TB0 CCR6 capture input CCI6B | Timer TB0: TB0.6 compare output Out6 |
| 11 | PM_UCA0RXD | USCI_A0 UART RXD (Direction controlled by USCI - input) | |
| | PM_UCA0SOMI | USCI_A0 SPI slave out master in (direction controlled by USCI) | |
| 12 | PM_UCA0TXD | USCI_A0 UART TXD (Direction controlled by USCI - output) | |
| | PM_UCA0SIMO | USCI_A0 SPI slave in master out (direction controlled by USCI) | |
| 13 | PM_UCA0CLK | USCI_A0 clock input/output (direction controlled by USCI) | |
| | PM_UCB0STE | USCI_B0 SPI slave transmit enable (direction controlled by USCI - input) | |
| 14 | PM_UCB0SOMI | USCI_B0 SPI slave out master in (direction controlled by USCI) | |
| | PM_UCB0SCL | USCI_B0 I ² C clock (open drain and direction controlled by USCI) | |
| 15 | PM_UCB0SIMO | USCI_B0 SPI slave in master out (direction controlled by USCI) | |
| | PM_UCB0SDA | USCI_B0 I ² C data (open drain and direction controlled by USCI) | |
| 16 | PM_UCB0CLK | USCI_B0 clock input/output (direction controlled by USCI) | |
| | PM_UCA0STE | USCI_A0 SPI slave transmit enable (direction controlled by USCI - input) | |
| 17 | PM_MCLK | - | MCLK |
| 18-30 | Reserved | None | DVSS |
| 31 (0FFh) ⁽¹⁾ | PM_ANALOG | Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals. | |

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide and the upper bits are ignored, which results in a read out value of 31.

Table 6-9. Default Mapping

| PIN | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|------------------------|----------------------------|---|---------------------|
| P2.0/P2MAP0 | PM_UCB0STE, PM_UCA0CLK | USCI_B0 SPI slave transmit enable (direction controlled by USCI - input), USCI_A0 clock input/output (direction controlled by USCI) | |
| P2.1/P2MAP1 | PM_UCB0SIMO, PM_UCB0SDA | USCI_B0 SPI slave in master out (direction controlled by USCI), USCI_B0 I ² C data (open drain and direction controlled by USCI) | |
| P2.2/P2MAP2 | PM_UCB0SOMI, PM_UCB0SCL | USCI_B0 SPI slave out master in (direction controlled by USCI), USCI_B0 I ² C clock (open drain and direction controlled by USCI) | |
| P2.3/P2MAP3 | PM_UCB0CLK, PM_UCA0STE | USCI_B0 clock input/output (direction controlled by USCI), USCI_A0 SPI slave transmit enable (direction controlled by USCI - input) | |
| P2.4/P2MAP4 | PM_UCA0TXD, PM_UCA0SIMO | USCI_A0 UART TXD (direction controlled by USCI - output), USCI_A0 SPI slave in master out (direction controlled by USCI) | |
| P2.5/P2MAP5/R23 | PM_UCA0RXD, PM_UCA0SOMI | USCI_A0 UART RXD (direction controlled by USCI - input), USCI_A0 SPI slave out master in (direction controlled by USCI) | |
| P2.6/P2MAP6/R03 | PM_NONE | - | DVSS |
| P2.7/P2MAP7/LCDREF/R13 | PM_NONE | - | DVSS |

6.12.3 Oscillator and System Clock

The clock system in the MSP430FG662x and MSP430FG642x devices are supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (in XT1 LF mode; XT1 HF mode is not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2. The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turnon clock source and stabilizes in 3 μs (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator (DCO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

6.12.4 Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit provides the proper internal reset signal to the device during power on and power off. The SVS and SVM circuitry detect if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and the core supply.

6.12.5 Hardware Multiplier (MPY32)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

6.12.6 Real-Time Clock (RTC_B)

The RTC_B module can be configured for real-time clock (RTC) or calendar mode providing seconds, minutes, hours, day of week, day of month, month, and year. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_B also supports flexible alarm functions and offset-calibration hardware. The implementation on this device supports operation in LPM3.5 mode and operation from a backup supply.

6.12.7 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.12.8 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, bootstrap loader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application.

Table 6-10. System Module Interrupt Vector Registers

| INTERRUPT VECTOR REGISTER | INTERRUPT EVENT | WORD ADDRESS | OFFSET | PRIORITY |
|---------------------------|------------------------------------|--------------|--------|----------|
| SYSRSTIV, System Reset | No interrupt pending | 019Eh | 00h | |
| | Brownout (BOR) | | 02h | Highest |
| | $\overline{\text{RST}}$ /NMI (BOR) | | 04h | |
| | PMMSWBOR (BOR) | | 06h | |
| | LPM3.5 or LPM4.5 wakeup (BOR) | | 08h | |
| | Security violation (BOR) | | 0Ah | |
| | SVSL (POR) | | 0Ch | |
| | SVSH (POR) | | 0Eh | |
| | SVML_OVP (POR) | | 10h | |
| | SVMH_OVP (POR) | | 12h | |
| | PMMSWPOR (POR) | | 14h | |
| | WDT time-out (PUC) | | 16h | |
| | WDT key violation (PUC) | | 18h | |
| | KEYV flash key violation (PUC) | | 1Ah | |
| | Reserved | | 1Ch | |
| | Peripheral area fetch (PUC) | | 1Eh | |
| | PMM key violation (PUC) | | 20h | |
| Reserved | 22h to 3Eh | Lowest | | |

Table 6-10. System Module Interrupt Vector Registers (continued)

| INTERRUPT VECTOR REGISTER | INTERRUPT EVENT | WORD ADDRESS | OFFSET | PRIORITY |
|---------------------------|-------------------------|----------------------|----------------------|----------|
| SYSSNIV, System NMI | No interrupt pending | 019Ch | 00h | Highest |
| | SVMLIFG | | 02h | |
| | SVMHIFG | | 04h | |
| | DLYLIFG | | 06h | |
| | DLYHIFG | | 08h | |
| | VMAIFG | | 0Ah | |
| | JMBINIFG | | 0Ch | |
| | JMBOUTIFG | | 0Eh | |
| | SVMLVLRIFG | | 10h | |
| | SVMHVLRIFG | | 12h | |
| | Reserved | | 14h to 1Eh | Lowest |
| | SYSUNIV, User NMI | | No interrupt pending | 019Ah |
| NMIFG | | 02h | | |
| OFIFG | | 04h | | |
| ACCVIFG | | 06h | | |
| BUSIFG | | 08h | | |
| Reserved | | 0Ah to 1Eh | Lowest | |
| SYSBERRIV, Bus Error | | No interrupt pending | 0198h | |
| | USB wait state time-out | 02h | | Highest |
| | Reserved | 04h to 1Eh | | Lowest |

6.12.9 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

The USB timestamp generator also uses the channel 0, 1, and 2 DMA trigger assignments described in [Table 6-11](#). The USB timestamp generator is only available on devices with USB module (MSP430FG662x).

Table 6-11. DMA Trigger Assignments⁽¹⁾

| TRIGGER | CHANNEL | | | | | |
|---------|--------------------------|---------|---------|---------|---------|---------|
| | 0 | 1 | 2 | 3 | 4 | 5 |
| 0 | DMAREQ | | | | | |
| 1 | TA0CCR0 CCIFG | | | | | |
| 2 | TA0CCR2 CCIFG | | | | | |
| 3 | TA1CCR0 CCIFG | | | | | |
| 4 | TA1CCR2 CCIFG | | | | | |
| 5 | TA2CCR0 CCIFG | | | | | |
| 6 | TA2CCR2 CCIFG | | | | | |
| 7 | TBCCR0 CCIFG | | | | | |
| 8 | TBCCR2 CCIFG | | | | | |
| 9 | Reserved | | | | | |
| 10 | Reserved | | | | | |
| 11 | Reserved | | | | | |
| 12 | Reserved | | | | | |
| 13 | Reserved | | | | | |
| 14 | Reserved | | | | | |
| 15 | Reserved | | | | | |
| 16 | UCA0RXIFG | | | | | |
| 17 | UCA0TXIFG | | | | | |
| 18 | UCB0RXIFG | | | | | |
| 19 | UCB0TXIFG | | | | | |
| 20 | UCA1RXIFG | | | | | |
| 21 | UCA1TXIFG | | | | | |
| 22 | UCB1RXIFG | | | | | |
| 23 | UCB1TXIFG | | | | | |
| 24 | CTSD16IFG0 | | | | | |
| 25 | DAC12_0IFG | | | | | |
| 26 | DAC12_1IFG | | | | | |
| 27 | USB FNRXD ⁽²⁾ | | | | | |
| 28 | USB ready ⁽²⁾ | | | | | |
| 29 | MPY ready | | | | | |
| 30 | DMA5IFG | DMA0IFG | DMA1IFG | DMA2IFG | DMA3IFG | DMA4IFG |
| 31 | DMAE0 | | | | | |

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause any DMA trigger event when selected.

(2) Only on devices with peripheral module USB (MSP430FG662x), otherwise reserved (MSP430FG642x).

6.12.10 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3-pin or 4-pin) or I²C.

The MSP430FG662x and MSP430FG642x include two complete USCI modules (n = 0 to 1).

6.12.11 Timer TA0

Timer TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. TA0 supports multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-12. Timer TA0 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|---------|---------------------|---------------------------|--------------|----------------------|----------------------|-------------------|---------|
| PZ | ZQW | | | | | | PZ | ZQW |
| 34-P1.0 | L5-P1.0 | TA0CLK | TACLK | Timer | NA | NA | | |
| | | ACLK | ACLK | | | | | |
| | | SMCLK | SMCLK | | | | | |
| 34-P1.0 | L5-P1.0 | TA0CLK | $\overline{\text{TACLK}}$ | | | | | |
| 35-P1.1 | M5-P1.1 | TA0.0 | CCIOA | CCR0 | TA0 | TA0.0 | 35-P1.1 | M5-P1.1 |
| | | DV _{SS} | CCIOB | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 36-P1.2 | J6-P1.2 | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 | 36-P1.2 | J6-P1.2 |
| 40-P1.6 | J7-P1.6 | TA0.1 | CCI1B | | | | 40-P1.6 | J7-P1.6 |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 37-P1.3 | H6-P1.3 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 | 37-P1.3 | H6-P1.3 |
| 41-P1.7 | M7-P1.7 | TA0.2 | CCI2B | | | | 41-P1.7 | M7-P1.7 |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 38-P1.4 | M6-P1.4 | TA0.3 | CCI3A | CCR3 | TA3 | TA0.3 | 38-P1.4 | M6-P1.4 |
| | | DV _{SS} | CCI3B | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 39-P1.5 | L6-P1.5 | TA0.4 | CCI4A | CCR4 | TA4 | TA0.4 | 39-P1.5 | L6-P1.5 |
| | | DV _{SS} | CCI4B | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |

6.12.12 Timer TA1

Timer TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 supports multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-13. Timer TA1 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|---------|---------------------|---------------------------|--------------|----------------------|----------------------|---|---------|
| PZ | ZQW | | | | | | PZ | ZQW |
| 42-P3.0 | L7-P3.0 | TA1CLK | TACLK | Timer | NA | NA | | |
| | | ACLK | ACLK | | | | | |
| | | SMCLK | SMCLK | | | | | |
| 42-P3.0 | L7-P3.0 | TA1CLK | $\overline{\text{TACLK}}$ | | | | | |
| 43-P3.1 | H7-P3.1 | TA1.0 | CCI0A | CCR0 | TA0 | TA1.0 | 43-P3.1 | H7-P3.1 |
| | | DV _{SS} | CCI0B | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 44-P3.2 | M8-P3.2 | TA1.1 | CCI1A | CCR1 | TA1 | TA1.1 | 44-P3.2 | M8-P3.2 |
| | | CBOUT (internal) | CCI1B | | | | DAC12_A DAC12_0, DAC12_1 (internal) | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 45-P3.3 | L8-P3.3 | TA1.2 | CCI2A | CCR2 | TA2 | TA1.2 | 45-P3.3 | L8-P3.3 |
| | | ACLK (internal) | CCI2B | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |

6.12.13 Timer TA2

Timer TA2 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA2 supports multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-14. Timer TA2 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|----------|---------------------|---------------------------|--------------|----------------------|----------------------|-------------------|----------|
| PZ | ZQW | | | | | | PZ | ZQW |
| 46-P3.4 | J8-P3.4 | TA2CLK | TACLK | Timer | NA | NA | | |
| | | ACLK | ACLK | | | | | |
| | | SMCLK | SMCLK | | | | | |
| 46-P3.4 | J8-P3.4 | TA2CLK | $\overline{\text{TACLK}}$ | | | | | |
| 47-P3.5 | M9-P3.5 | TA2.0 | CCI0A | CCR0 | TA0 | TA2.0 | 47-P3.5 | M9-P3.5 |
| | | DV _{SS} | CCI0B | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 48-P3.6 | L9-P3.6 | TA2.1 | CCI1A | CCR1 | TA1 | TA2.1 | 48-P3.6 | L9-P3.6 |
| | | CBOU (internal) | CCI1B | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 49-P3.7 | M10-P3.7 | TA2.2 | CCI2A | CCR2 | TA2 | TA2.2 | 49-P3.7 | M10-P3.7 |
| | | ACLK (internal) | CCI2B | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |

6.12.14 Timer TB0

Timer TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. TB0 supports multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-15. Timer TB0 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|--|---|---------------------|---------------------|--------------|----------------------|----------------------|---|-----------------------------------|
| PZ | ZQW | | | | | | PZ | ZQW |
| 58-P8.0 P2MAP _x ⁽¹⁾ | J11-P8.0 P2MAP _x ⁽¹⁾ | TB0CLK | TB0CLK | Timer | NA | NA | | |
| | | ACLK | ACLK | | | | | |
| | | SMCLK | SMCLK | | | | | |
| 58-P8.0 P2MAP _x ⁽¹⁾ | J11-P8.0 P2MAP _x ⁽¹⁾ | TB0CLK | <u>TB0CLK</u> | | | | | |
| 50-P4.0 P2MAP _x ⁽¹⁾ | J9-P4.0 P2MAP _x ⁽¹⁾ | TB0.0 | CCIOA | CCR0 | TB0 | TB0.0 | 50-P4.0 | J9-P4.0 |
| | | TB0.0 | CCIOB | | | | P2MAP _x ⁽¹⁾ | P2MAP _x ⁽¹⁾ |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 51-P4.1 P2MAP _x ⁽¹⁾ | M11-P4.1 P2MAP _x ⁽¹⁾ | TB0.1 | CCI1A | CCR1 | TB1 | TB0.1 | 51-P4.1 | M11-P4.1 |
| | | TB0.1 | CCI1B | | | | P2MAP _x ⁽¹⁾ | P2MAP _x ⁽¹⁾ |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 52-P4.2 P2MAP _x ⁽¹⁾ | L10-P4.2 P2MAP _x ⁽¹⁾ | TB0.2 | CCI2A | CCR2 | TB2 | TB0.2 | 52-P4.2 | L10-P4.2 |
| | | TB0.2 | CCI2B | | | | P2MAP _x ⁽¹⁾ | P2MAP _x ⁽¹⁾ |
| | | DV _{SS} | GND | | | | DAC12_A DAC12_0, DAC12_1 (internal) | |
| | | DV _{CC} | V _{CC} | | | | | |
| 53-P4.3 P2MAP _x ⁽¹⁾ | M12-P4.3 P2MAP _x ⁽¹⁾ | TB0.3 | CCI3A | CCR3 | TB3 | TB0.3 | 53-P4.3 | M12-P4.3 |
| | | TB0.3 | CCI3B | | | | P2MAP _x ⁽¹⁾ | P2MAP _x ⁽¹⁾ |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 54-P4.4 P2MAP _x ⁽¹⁾ | L12-P4.4 P2MAP _x ⁽¹⁾ | TB0.4 | CCI4A | CCR4 | TB4 | TB0.4 | 54-P4.4 | L12-P4.4 |
| | | TB0.4 | CCI4B | | | | P2MAP _x ⁽¹⁾ | P2MAP _x ⁽¹⁾ |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 55-P4.5 P2MAP _x ⁽¹⁾ | L11-P4.5 P2MAP _x ⁽¹⁾ | TB0.5 | CCI5A | CCR5 | TB5 | TB0.5 | 55-P4.5 | L11-P4.5 |
| | | TB0.5 | CCI5B | | | | P2MAP _x ⁽¹⁾ | P2MAP _x ⁽¹⁾ |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 56-P4.6 P2MAP _x ⁽¹⁾ | K11-P4.6 P2MAP _x ⁽¹⁾ | TB0.6 | CCI6A | CCR6 | TB6 | TB0.6 | 56-P4.6 | K11-P4.6 |
| | | TB0.6 | CCI6B | | | | P2MAP _x ⁽¹⁾ | P2MAP _x ⁽¹⁾ |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |

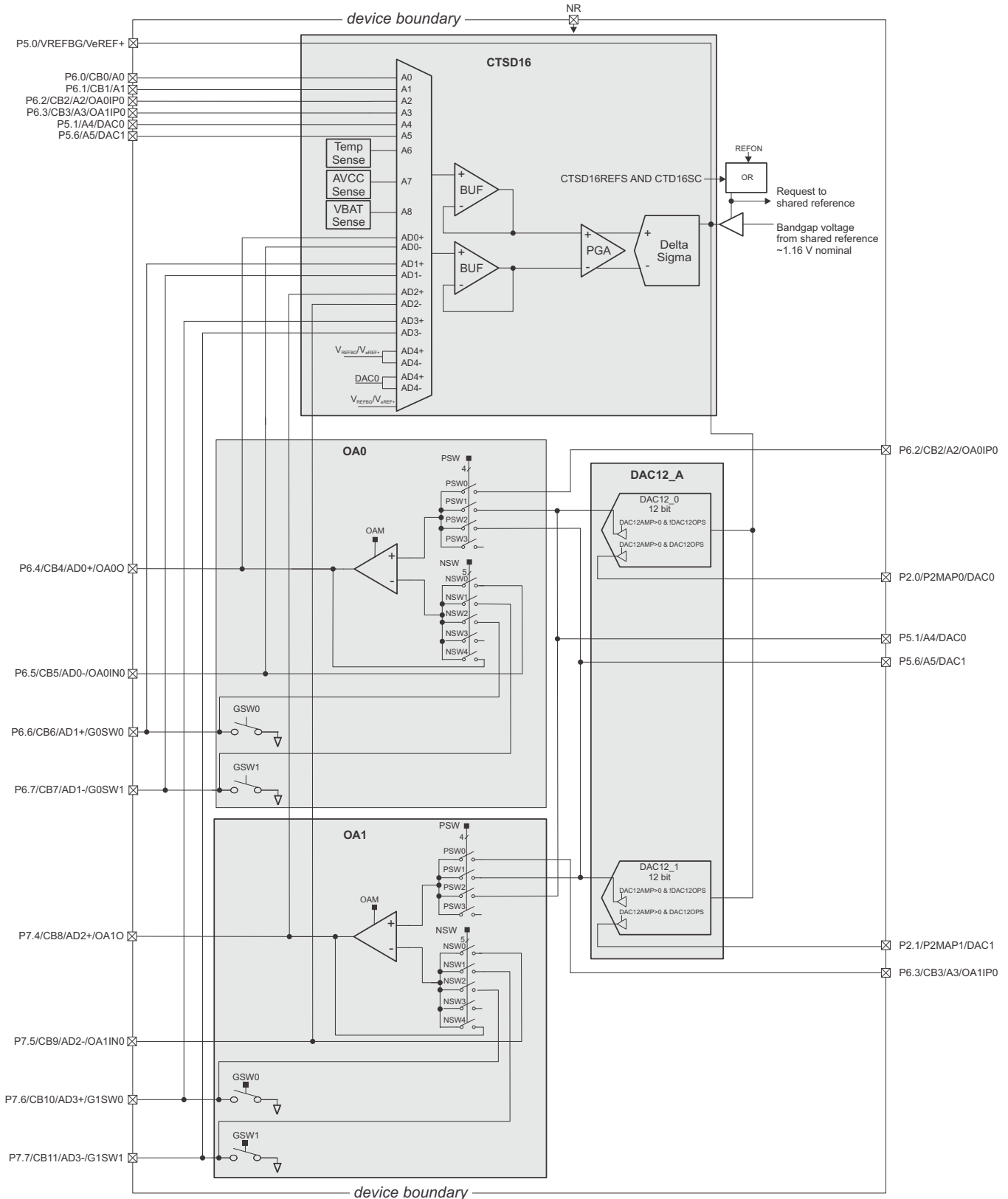
(1) Timer functions are selectable by the port mapping controller.

6.12.15 *Comparator_B*

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.12.16 *Signal Chain*

All devices include all the building blocks to construct a complete signal chain. These blocks include two digital-to-analog converter (DAC) channels, two integrated operational amplifiers (OAs), a sigma-delta analog-to-digital converter (CTSD16), and low-ohmic switches (GSW). [Figure 6-1](#) shows the various signal chain blocks and their interconnections in the overall system.



NOTE: Refer to the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)* for additional module details.

Figure 6-1. Signal Chain

6.12.16.1 CTSD16

The CTSD16 module integrates a single sigma-delta ADC with ten external inputs and four internal inputs. The converter is designed with a fully differential analog input pair and a programmable gain amplifier input stage. The converter is based on second-order over-sampling sigma-delta modulators and digital decimation filters. The decimation filters are comb type filters with selectable oversampling ratios of up to 256.

The CTSD16 is preceded by an analog multiplexer which is used for channel selection, followed by a unity gain buffer stage useful when sampling high impedance sensors.

The CTSD16 can use as its reference the internal bandgap voltage from the REF module or an external reference at the VeREF+ pin.

6.12.16.2 DAC12_A

The DAC12_A module is a 12-bit R-ladder voltage-output DAC. The DAC12_A may be used in 8-bit or 12-bit mode, and may be used in conjunction with the DMA controller. When multiple DAC12_A modules are present, they may be grouped together for synchronous operation. There are two complete channels available, DAC12_0 and DAC12_1.

6.12.16.3 Operational Amplifiers (OA)

The device integrates two low power operational amplifiers. The operational amplifiers can perform signal conditioning of low-level analog signals before conversion by the ADC. Each operational amplifier can be individually controlled by software.

6.12.16.4 Ground Switches (GSW)

The device integrates four low-ohmic switches to ground that are individually controllable in software. These can switch in and out various components in the measurement system.

6.12.17 REF Voltage Reference

The reference module (REF) generates all of the critical reference voltages that can be used by the various analog peripherals in the device.

6.12.18 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.12.19 LCD_B

The LCD_B driver generates the segment and common signals that are required to drive a liquid crystal display (LCD). The LCD_B controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, and 4-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage, and thus contrast, by software. The module also provides an automatic blinking capability for individual segments.

6.12.20 USB Universal Serial Bus

The USB module is a fully integrated USB interface that is compliant with the USB 2.0 specification. The module supports full-speed operation of control, interrupt, and bulk transfers. The module includes an integrated LDO, PHY, and PLL. The PLL is highly flexible and can support a wide range of input clock frequencies. USB RAM, when not used for USB communication, can be used by the system.

The USB module is only available on the MSP430FG662x devices.

6.12.21 LDO and PU Port

The integrated 3.3-V power system incorporates an integrated 3.3-V LDO regulator that allows the entire MSP430 microcontroller to be powered from nominal 5-V LDO1 when it is made available for the system. Alternatively, the power system can supply power only to other components within the system, or it can be unused altogether.

The Port U Pins (PU.0 and PU.1) function as general-purpose high-current I/O pins. These pins can only be configured together as either both inputs or both outputs. Port U is supplied by the LDO0 rail. If the 3.3-V LDO is not being used in the system (disabled), the LDO0 pin can be supplied externally.

The LDO-PWR module (LDO and PU Port) is only available on the MSP430FG6426 and MSP430FG6425 devices.

6.12.22 Embedded Emulation Module (EEM) (L Version)

The EEM supports real-time in-system debugging. The L version of the EEM has the following features:

- Eight hardware triggers or breakpoints on memory access
- Two hardware triggers or breakpoints on CPU register write access
- Up to ten hardware triggers can be combined to form complex triggers or breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

6.12.23 Input/Output Schematics

6.12.23.1 Port P1, P1.0 to P1.7, Input/Output With Schmitt Trigger

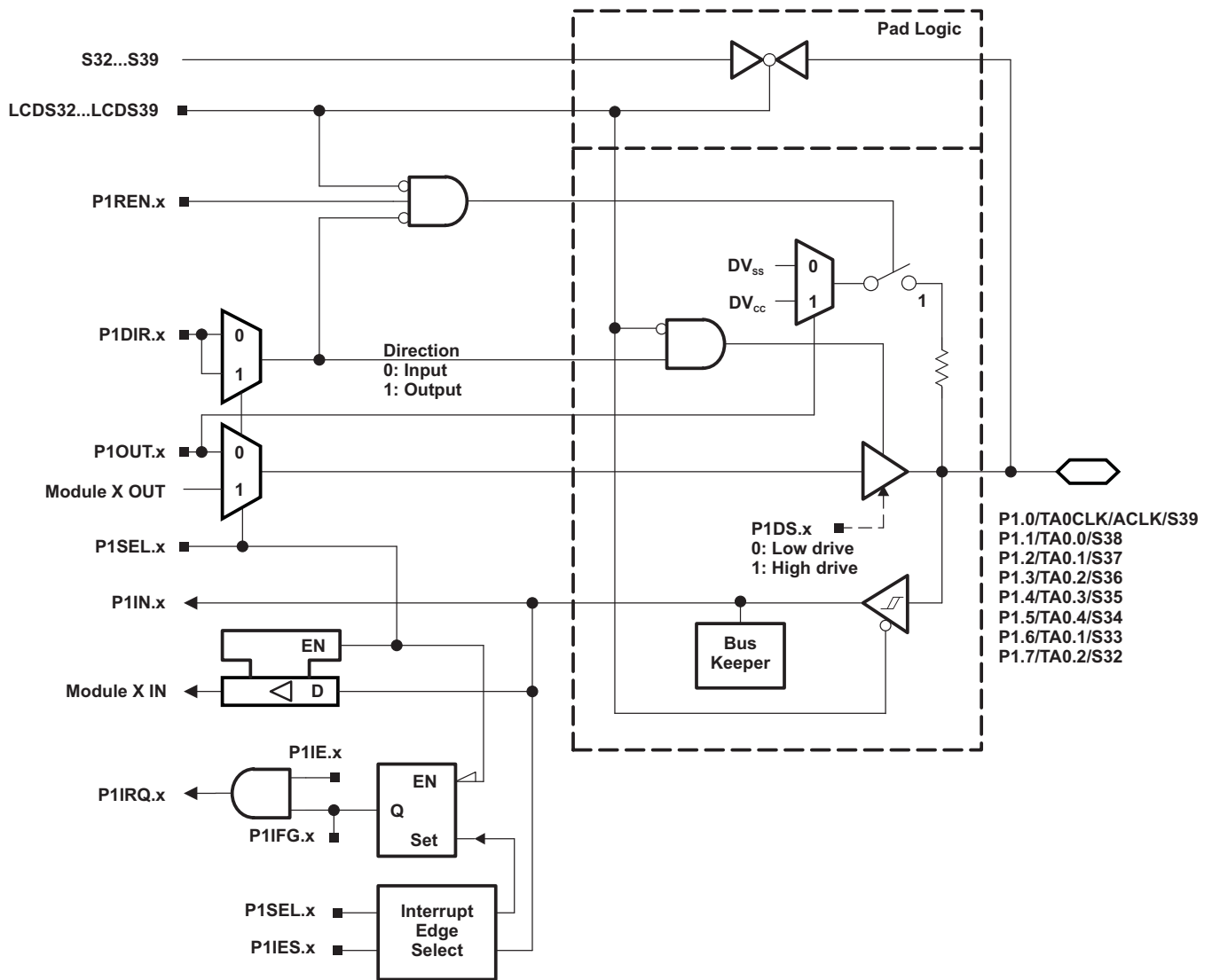


Table 6-16. Port P1 (P1.0 to P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|----------------------|---|-------------------------------|--|---------|-------------|
| | | | P1DIR.x | P1SEL.x | LCDS32...39 |
| P1.0/TA0CLK/ACLK/S39 | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.TA0CLK | 0 | 1 | 0 |
| | | ACLK | 1 | 1 | 0 |
| | | S39 | X | X | 1 |
| P1.1/TA0.0/S38 | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI0A capture input | 0 | 1 | 0 |
| | | Timer TA0.0 output | 1 | 1 | 0 |
| | | S38 | X | X | 1 |
| P1.2/TA0.1/S37 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI1A capture input | 0 | 1 | 0 |
| | | Timer TA0.1 output | 1 | 1 | 0 |
| | | S37 | X | X | 1 |
| P1.3/TA0.2/S36 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI2A capture input | 0 | 1 | 0 |
| | | Timer TA0.2 output | 1 | 1 | 0 |
| | | S36 | X | X | 1 |
| P1.4/TA0.3/S35 | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI3A capture input | 0 | 1 | 0 |
| | | Timer TA0.3 output | 1 | 1 | 0 |
| | | S35 | X | X | 1 |
| P1.5/TA0.4/S34 | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI4A capture input | 0 | 1 | 0 |
| | | Timer TA0.4 output | 1 | 1 | 0 |
| | | S34 | X | X | 1 |
| P1.6/TA0.1/S33 | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI1B capture input | 0 | 1 | 0 |
| | | Timer TA0.1 output | 1 | 1 | 0 |
| | | S33 | X | X | 1 |
| P1.7/TA0.2/S32 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA0.CCI2B capture input | 0 | 1 | 0 |
| | | Timer TA0.2 output | 1 | 1 | 0 |
| | | S32 | X | X | 1 |

(1) X = Don't care

6.12.2.3.2 Port P2, P2.0 to P2.7, Input/Output With Schmitt Trigger

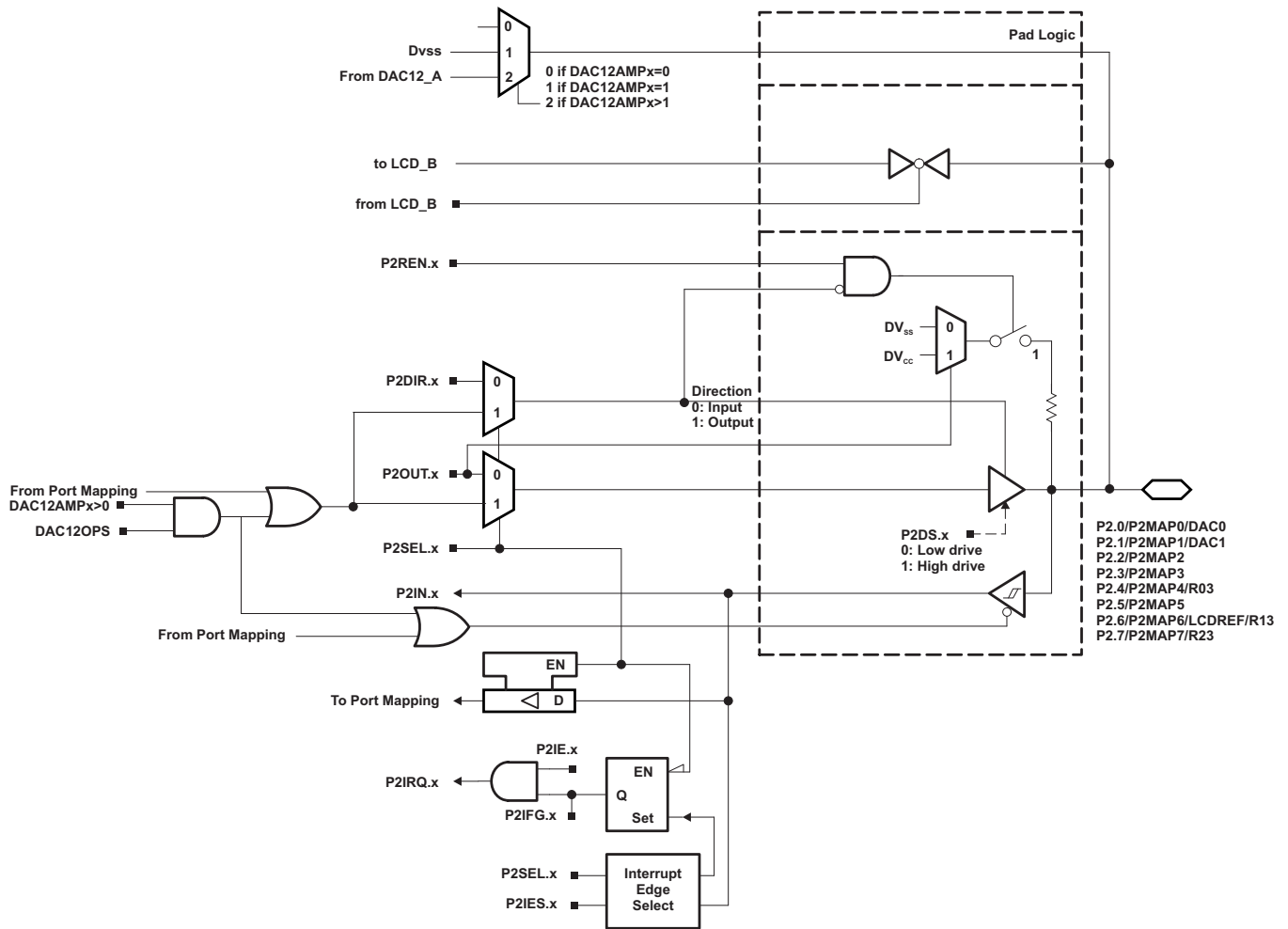


Table 6-17. Port P2 (P2.0 to P2.7) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | | |
|------------------------|---|-----------------------------------|--|---------|--------|----------|-----------|
| | | | P2DIR.x | P2SEL.x | P2MAPx | DAC12OPS | DAC12AMPx |
| P2.0/P2MAP0/DAC0 | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 19 | X | 0 |
| | | DAC0 | X | X | = 31 | 1 | >1 |
| P2.1/P2MAP1/DAC1 | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 19 | X | 0 |
| | | DAC1 | X | X | = 31 | 1 | >1 |
| P2.2/P2MAP2 | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 19 | X | 0 |
| P2.3/P2MAP3 | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 19 | X | 0 |
| P2.4/P2MAP4/R03 | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 19 | X | 0 |
| | | R03 | X | 1 | = 31 | X | 0 |
| P2.5/P2MAP5 | 5 | P2.5 (I/O) | I: 0; O: 1 | 0 | | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 19 | X | 0 |
| P2.6/P2MAP6/LCDREF/R13 | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 | | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 19 | X | 0 |
| | | LCDREF/R13 | X | 1 | = 31 | X | 0 |
| P2.7/P2MAP7/R23 | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 | | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 19 | X | 0 |
| | | R23 | X | 1 | = 31 | X | 0 |

(1) X = Don't care

6.12.23.3 Port P3, P3.0 to P3.7, Input/Output With Schmitt Trigger

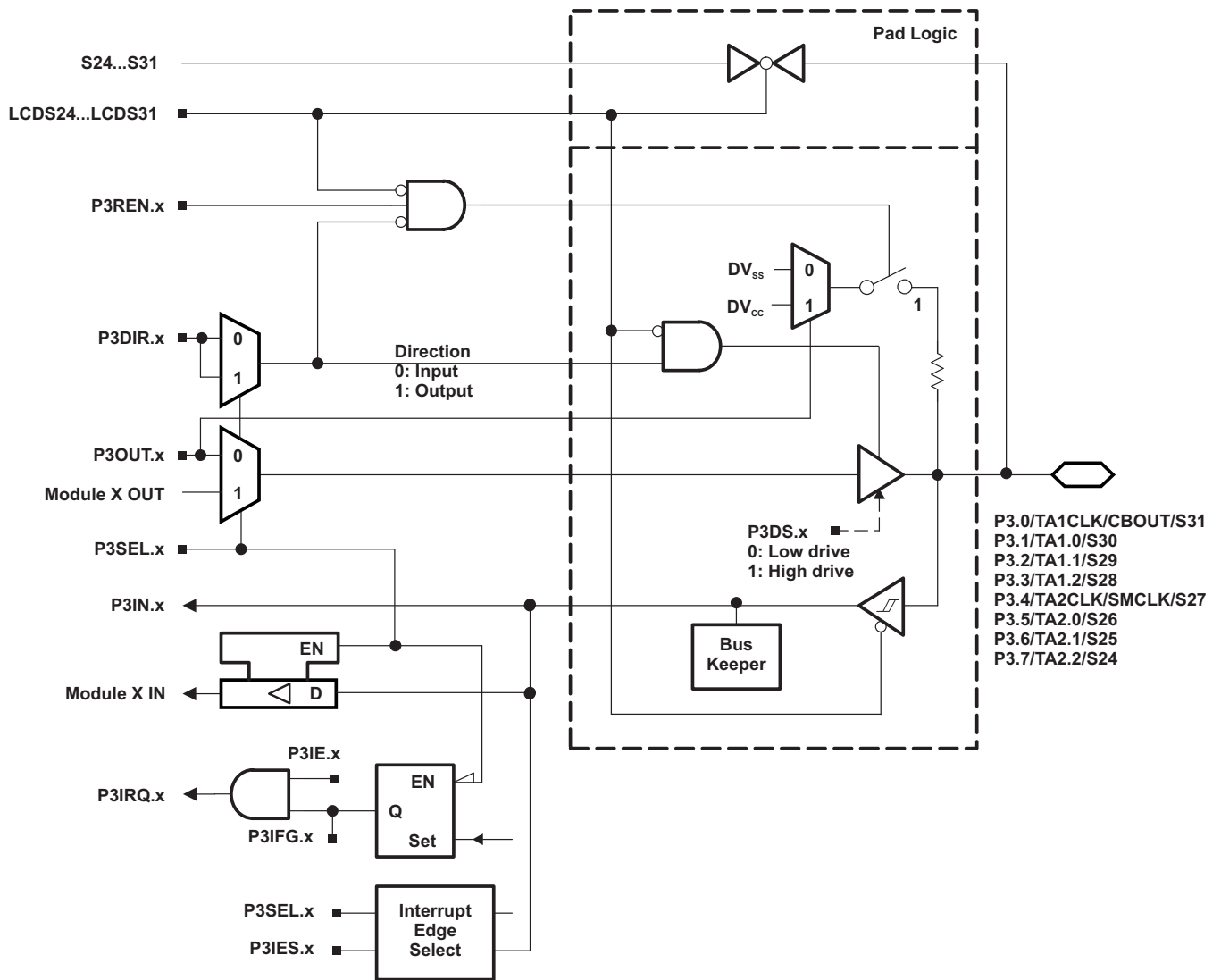


Table 6-18. Port P3 (P3.0 to P3.7) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------------|---|-------------------------------|--|---------|-------------|
| | | | P3DIR.x | P3SEL.x | LCDS24...31 |
| P3.0/TA1CLK/CBOUT/S31 | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA1.TA1CLK | 0 | 1 | 0 |
| | | CBOUT | 1 | 1 | 0 |
| | | S31 | X | X | 1 |
| P3.1/TA1.0/S30 | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA1.CCI0A capture input | 0 | 1 | 0 |
| | | Timer TA1.0 output | 1 | 1 | 0 |
| | | S30 | X | X | 1 |
| P3.2/TA1.1/S29 | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA1.CCI1A capture input | 0 | 1 | 0 |
| | | Timer TA1.1 output | 1 | 1 | 0 |
| | | S29 | X | X | 1 |
| P3.3/TA1.2/S28 | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA1.CCI2A capture input | 0 | 1 | 0 |
| | | Timer TA1.2 output | 1 | 1 | 0 |
| | | S28 | X | X | 1 |
| P3.4/TA2CLK/SMCLK/S27 | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA2.TA2CLK | 0 | 1 | 0 |
| | | SMCLK | 1 | 1 | 0 |
| | | S27 | X | X | 1 |
| P3.5/TA2.0/S26 | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA2.CCI0A capture input | 0 | 1 | 0 |
| | | Timer TA2.0 output | 1 | 1 | 0 |
| | | S26 | X | X | 1 |
| P3.6/TA2.1/S25 | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA2.CCI1A capture input | 0 | 1 | 0 |
| | | Timer TA2.1 output | 1 | 1 | 1 |
| | | S25 | X | X | 1 |
| P3.7/TA2.2/S24 | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TA2.CCI2A capture input | 0 | 1 | 0 |
| | | Timer TA2.2 output | 1 | 1 | 0 |
| | | S24 | X | X | 1 |

(1) X = Don't care

6.12.23.4 Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger

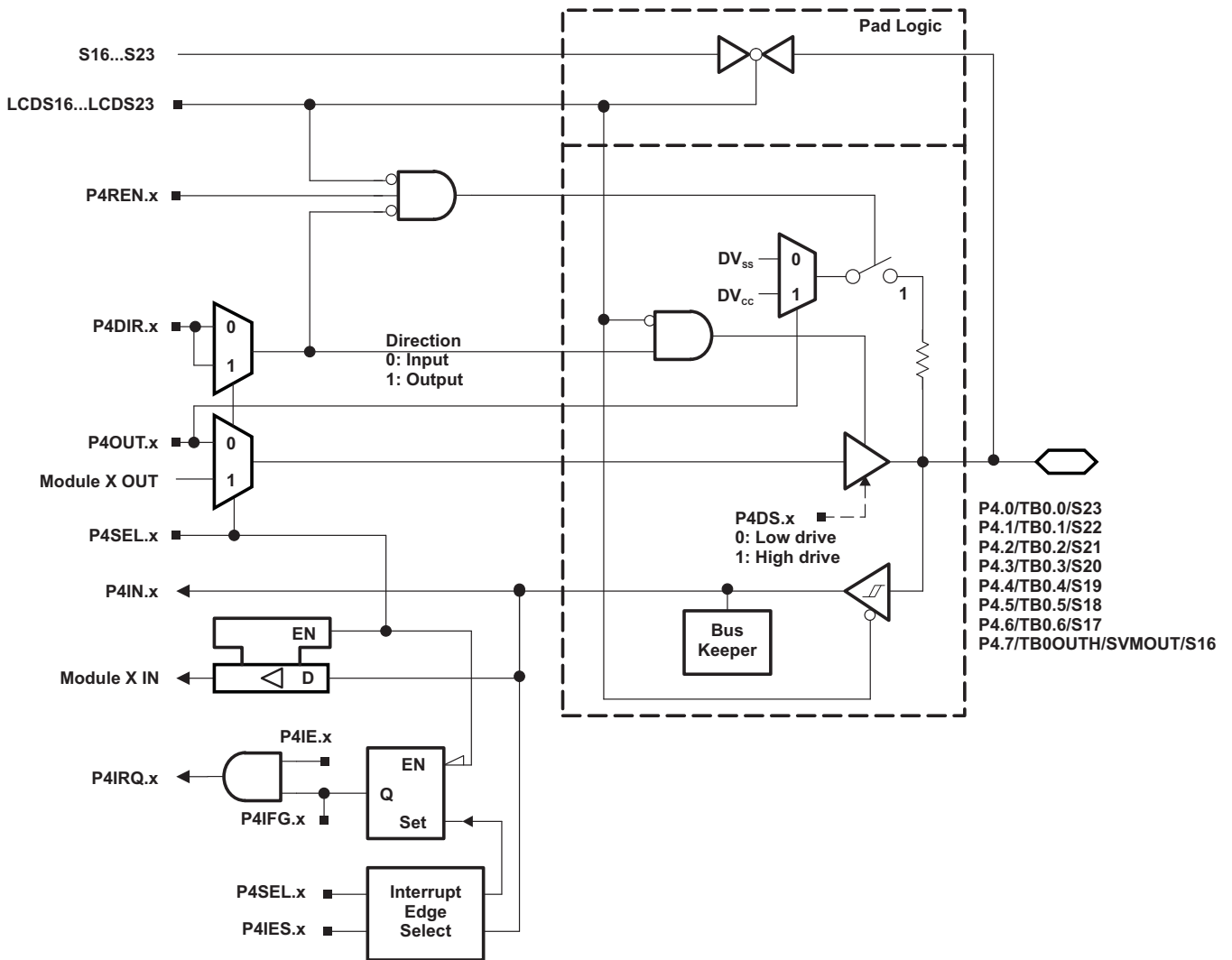


Table 6-19. Port P4 (P4.0 to P4.7) Pin Functions

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------------------|---|-----------------------------------|--|---------|-------------|
| | | | P4DIR.x | P4SEL.x | LCDS16...23 |
| P4.0/TB0.0/S23 | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI0A capture input | 0 | 1 | 0 |
| | | Timer TB0.0 output ⁽²⁾ | 1 | 1 | 0 |
| | | S23 | X | X | 1 |
| P4.1/TB0.1/S22 | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI1A capture input | 0 | 1 | 0 |
| | | Timer TB0.1 output ⁽²⁾ | 1 | 1 | 0 |
| | | S22 | X | X | 1 |
| P4.2/TB0.2/S21 | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI2A capture input | 0 | 1 | 0 |
| | | Timer TB0.2 output ⁽²⁾ | 1 | 1 | 0 |
| | | S21 | X | X | 1 |
| P4.3/TB0.3/S20 | 3 | P4.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI3A capture input | 0 | 1 | 0 |
| | | Timer TB0.3 output ⁽²⁾ | 1 | 1 | 0 |
| | | S20 | X | X | 1 |
| P4.4/TB0.4/S19 | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI4A capture input | 0 | 1 | 0 |
| | | Timer TB0.4 output ⁽²⁾ | 1 | 1 | 0 |
| | | S19 | X | X | 1 |
| P4.5/TB0.5/S18 | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI5A capture input | 0 | 1 | 0 |
| | | Timer TB0.5 output ⁽²⁾ | 1 | 1 | 0 |
| | | S18 | X | X | 1 |
| P4.6/TB0.6/S17 | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.CCI6A capture input | 0 | 1 | 0 |
| | | Timer TB0.6 output ⁽²⁾ | 1 | 1 | 0 |
| | | S17 | X | X | 1 |
| P4.7/TB0OUTH/ SVMOUT/S16 | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.TB0OUTH | 0 | 1 | 0 |
| | | SVMOUT | 1 | 1 | 0 |
| | | S16 | X | X | 1 |

(1) X = Don't care

(2) Setting TB0OUTH causes all Timer_B configured outputs to be set to high impedance.

6.12.23.5 Port P5, P5.0, Input/Output With Schmitt Trigger

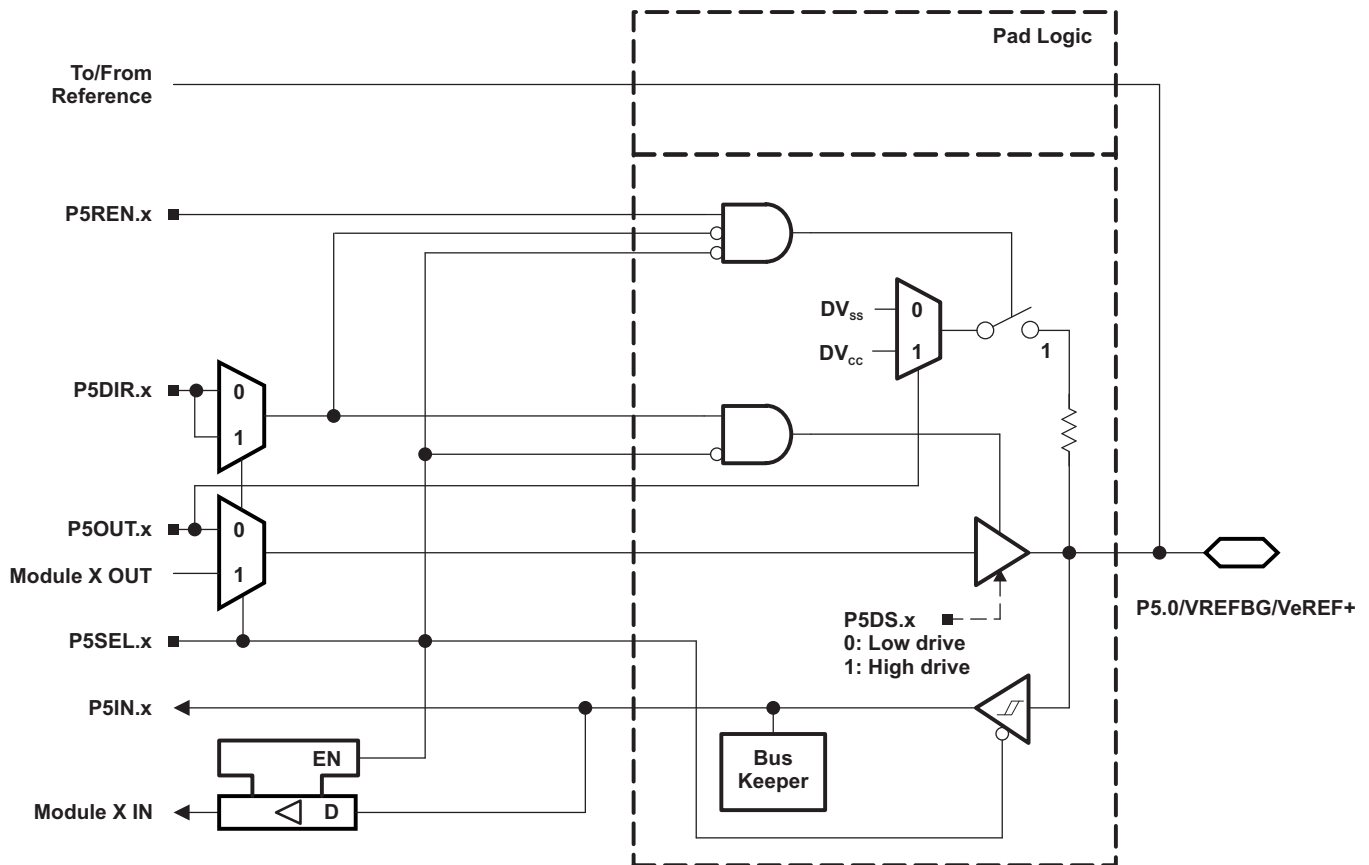


Table 6-20. Port P5 (P5.0) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | | |
|--------------------|---|---------------------------|--|---------|--------|----------------------|---------------------------|
| | | | P5DIR.x | P5SEL.x | REFOUT | REFON ⁽²⁾ | CTSD16REFS ⁽³⁾ |
| P5.0/VREFBG/VeREF+ | 0 | P5.0 (I/O) ⁽⁴⁾ | I: 0; O: 1 | 0 | X | X | X |
| | | VeREF+ ⁽⁵⁾ | X | 1 | 0 | X | 0 |
| | | VREFBG ⁽⁶⁾ | X | 1 | 1 | 1 | 1 |

- (1) X = Don't care
- (2) If a module is requesting a reference then REFON need not be set to 1 for VREFBG to be selected on P5.0.
- (3) If CTSD16 is active, this bit must be set as shown in the table. Otherwise if set to 1, it will force VREFBG to be selected regardless of REFOUT setting and if P5SEL.x is set to 0 it will cause possible contention on the I/O.
- (4) Default condition
- (5) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the CTSD16 or DAC.
- (6) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The internal reference voltage signal, V_{REFBG}, is available at the pin.

6.12.23.6 Port P5, P5.1 and P5.6, Input/Output With Schmitt Trigger

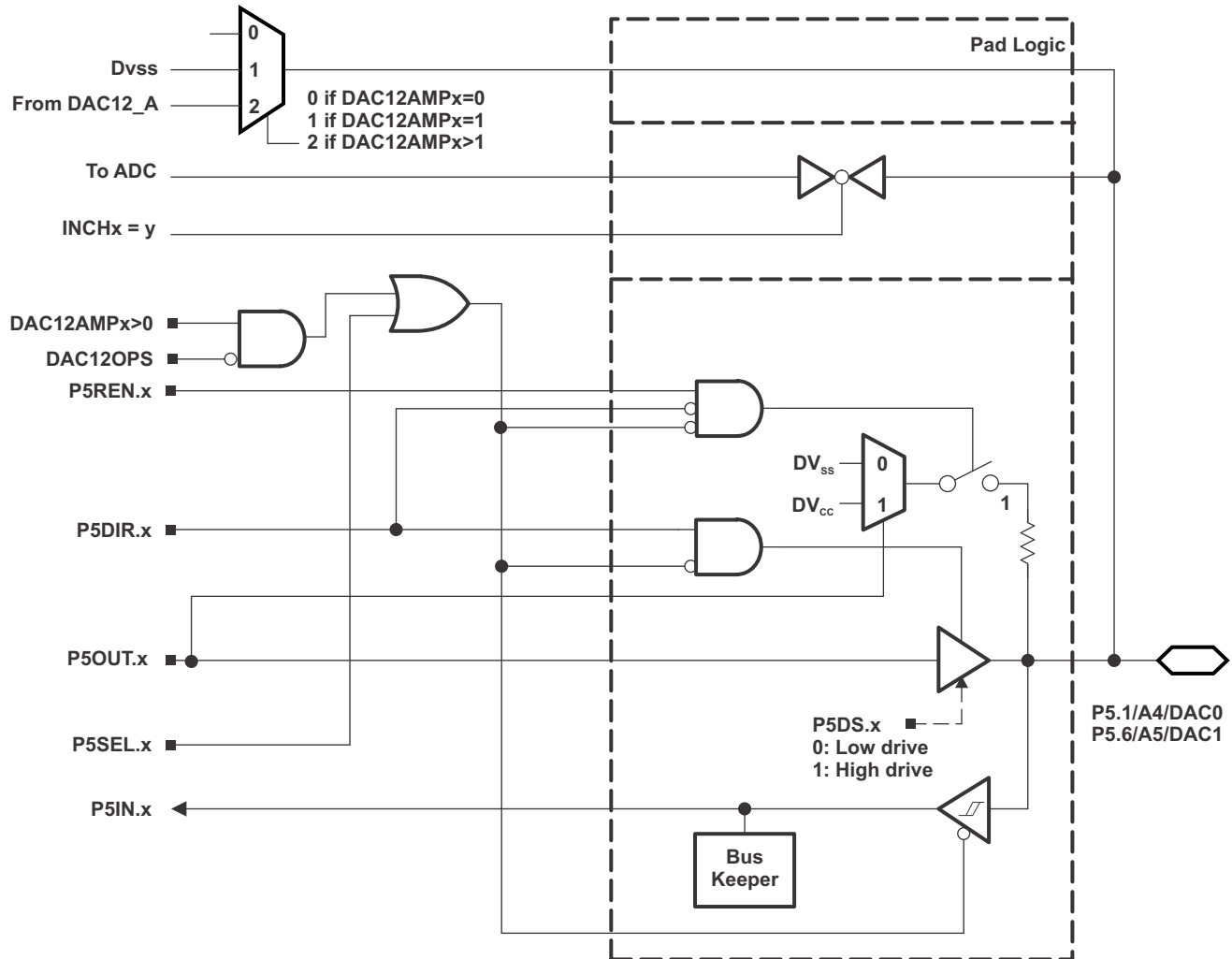


Table 6-21. Port P5 (P5.1 and P5.6) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-----------------|---|-----------------------|--|---------|----------|-----------|
| | | | P5DIR.x | P5SEL.x | DAC12OPS | DAC12AMPx |
| P5.1/A4/DAC0 | 1 | P5.1(I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | A4 ^{(2) (3)} | X | 1 | X | 0 |
| | | DAC0 | X | X | 0 | >1 |
| P5.6/A5/DAC1 | 1 | P5.6(I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | A5 ^{(2) (3)} | X | 1 | X | 0 |
| | | DAC1 | X | X | 0 | >1 |

- (1) X = Don't care
- (2) Setting the P5SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (3) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

6.12.23.7 Port P5, P5.3 to P5.5, P5.7, Input/Output With Schmitt Trigger

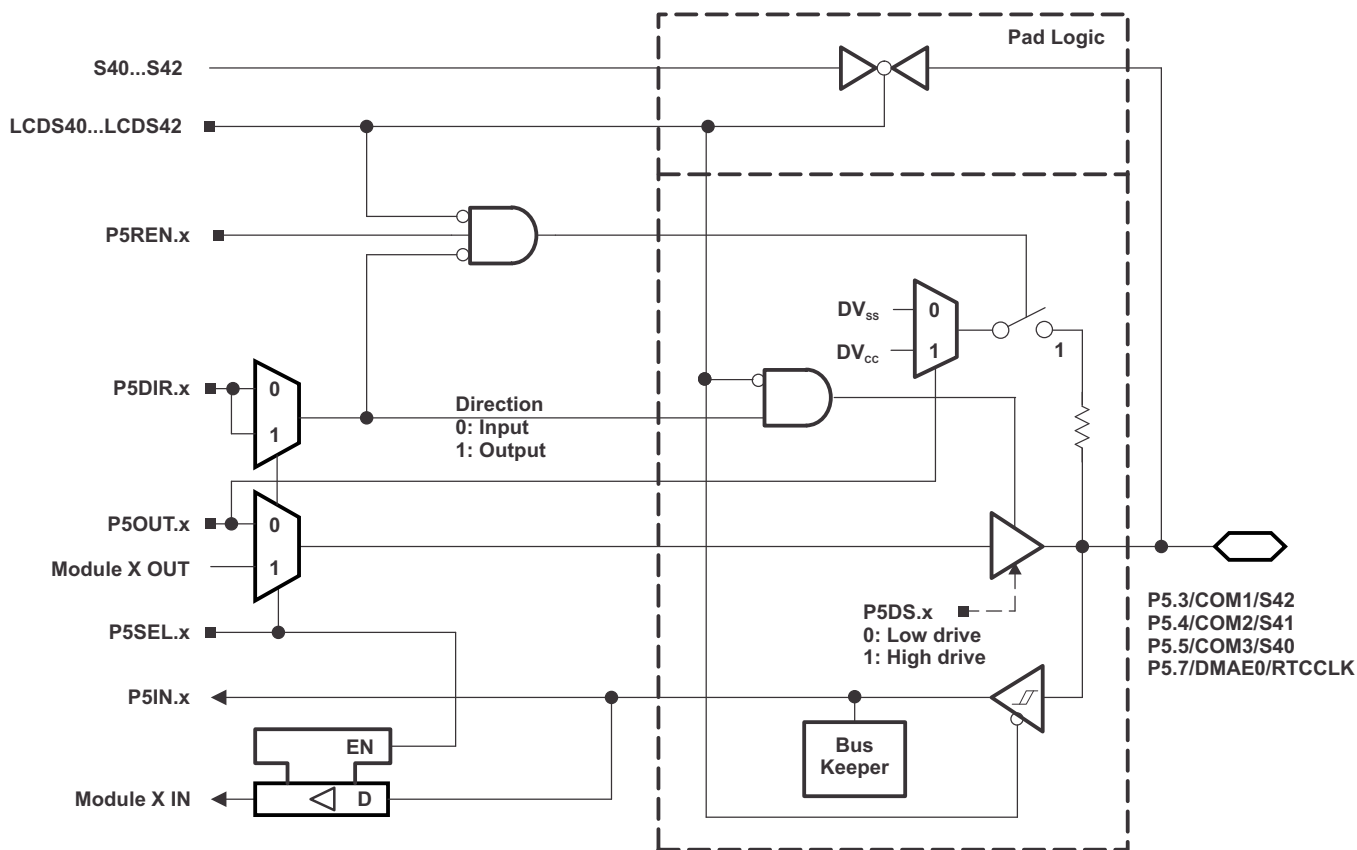


Table 6-22. Port P5 (P5.3 to P5.5, P5.7) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-------------------|---|------------|--|---------|-------------|
| | | | P5DIR.x | P5SEL.x | LCDS40...42 |
| P5.3/COM1/S42 | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | COM1 | X | 1 | X |
| | | S42 | X | 0 | 1 |
| P5.4/COM2/S41 | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | COM2 | X | 1 | X |
| | | S41 | X | 0 | 1 |
| P5.5/COM3/S40 | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | COM3 | X | 1 | X |
| | | S40 | X | 0 | 1 |
| P5.7/DMAE0/RTCCLK | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 | na |
| | | DMAE0 | 0 | 1 | na |
| | | RTCCLK | 1 | 1 | na |

(1) X = Don't care

6.12.23.8 Port P6, P6.0 to P6.1, Input/Output With Schmitt Trigger

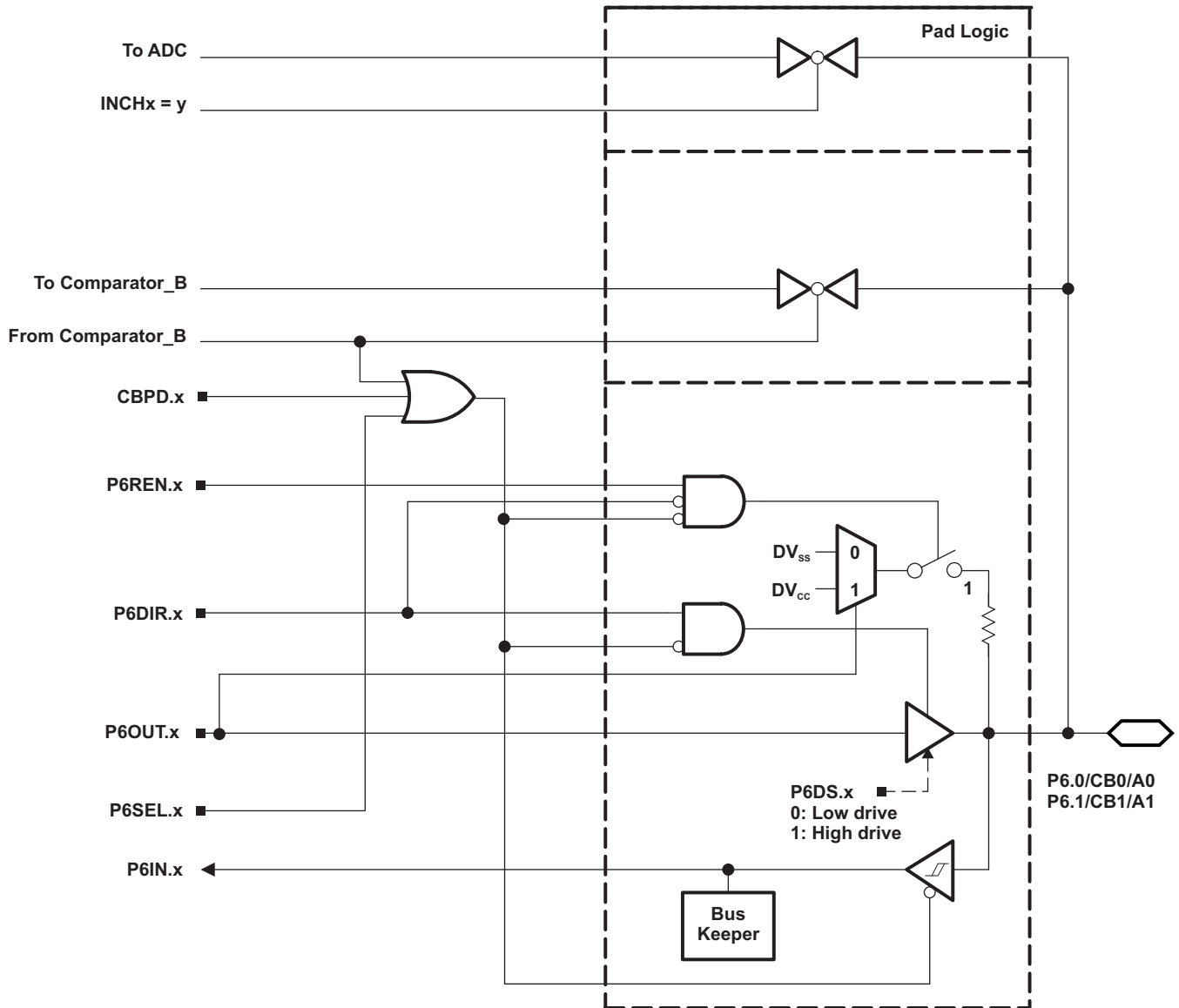


Table 6-23. Port P6 (P6.0 to P6.1) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|----------------------------------|--|---------|--------|
| | | | P6DIR.x | P6SEL.x | CBPD.x |
| P6.0/CB0/A0 | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | CB0 | X | X | 1 |
| | | A0 ⁽²⁾ ⁽³⁾ | X | 1 | X |
| P6.1/CB1/A1 | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | CB1 | X | X | 1 |
| | | A1 ⁽²⁾ ⁽³⁾ | X | 1 | X |

(1) X = Don't care

(2) Setting the P6SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

6.12.23.9 Port P6, P6.2 to P6.3, Input/Output With Schmitt Trigger

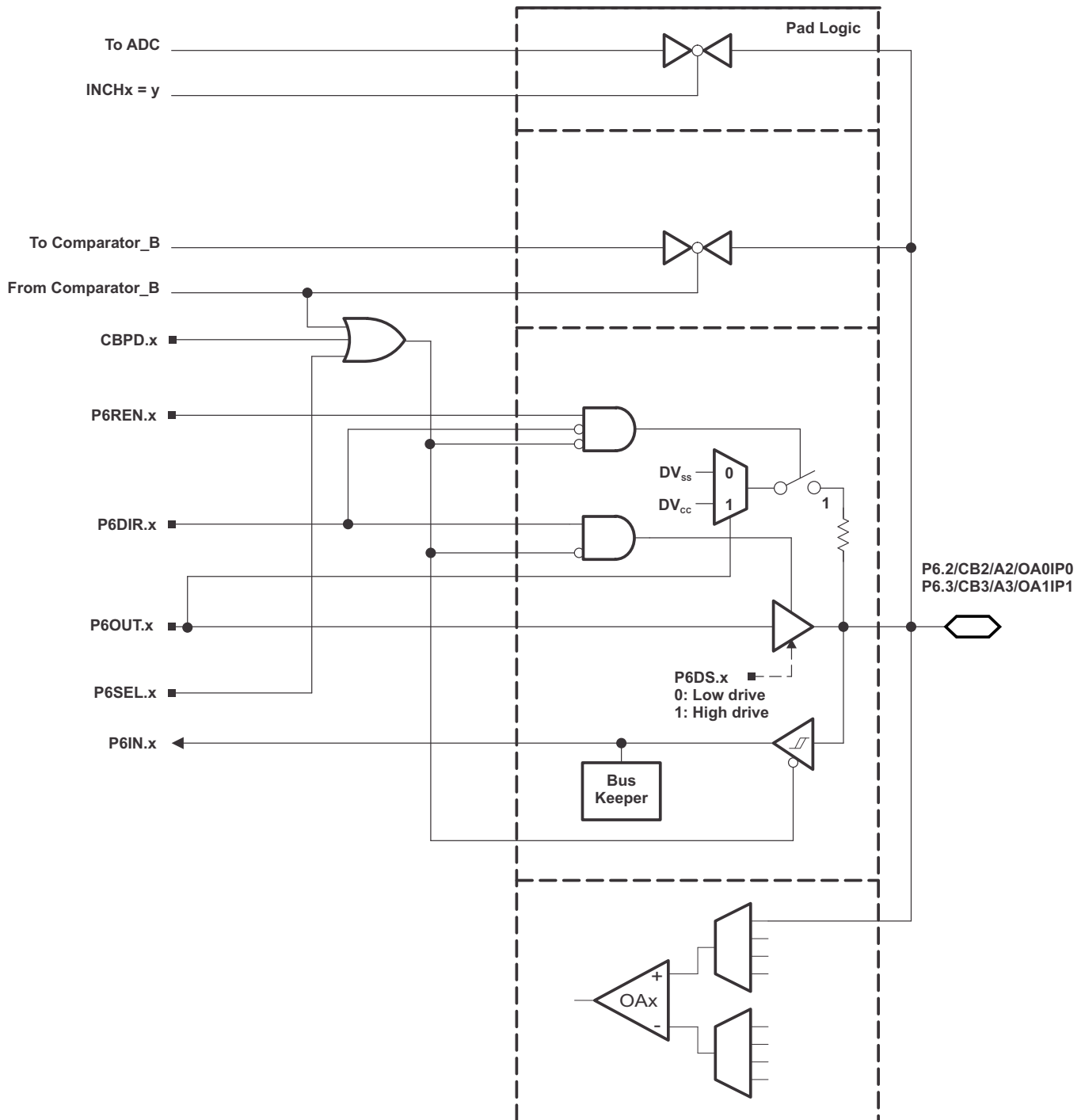


Table 6-24. Port P6 (P6.2 to P6.3) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|--------------------|---|-----------------------|--|------------------------|-----------------------|
| | | | P6DIR.x | P6SEL.x ⁽²⁾ | CBPD.x ⁽²⁾ |
| P6.2/CB2/A2/OA0IP0 | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | CB2 | X | X | 1 |
| | | A2 ⁽³⁾ | X | 1 | X |
| | | OA0IP0 ⁽²⁾ | X | 1 | X |
| P6.3/CB3/A3/OA1IP0 | 3 | P6.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | CB3 | X | X | 1 |
| | | A3 ⁽⁴⁾ | X | 1 | X |
| | | OA1IP0 ⁽²⁾ | X | 1 | X |

(1) X = Don't care

(2) Setting the P6SEL.x bit or CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

(4) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

6.12.23.10 Port P6, P6.4, Input/Output With Schmitt Trigger

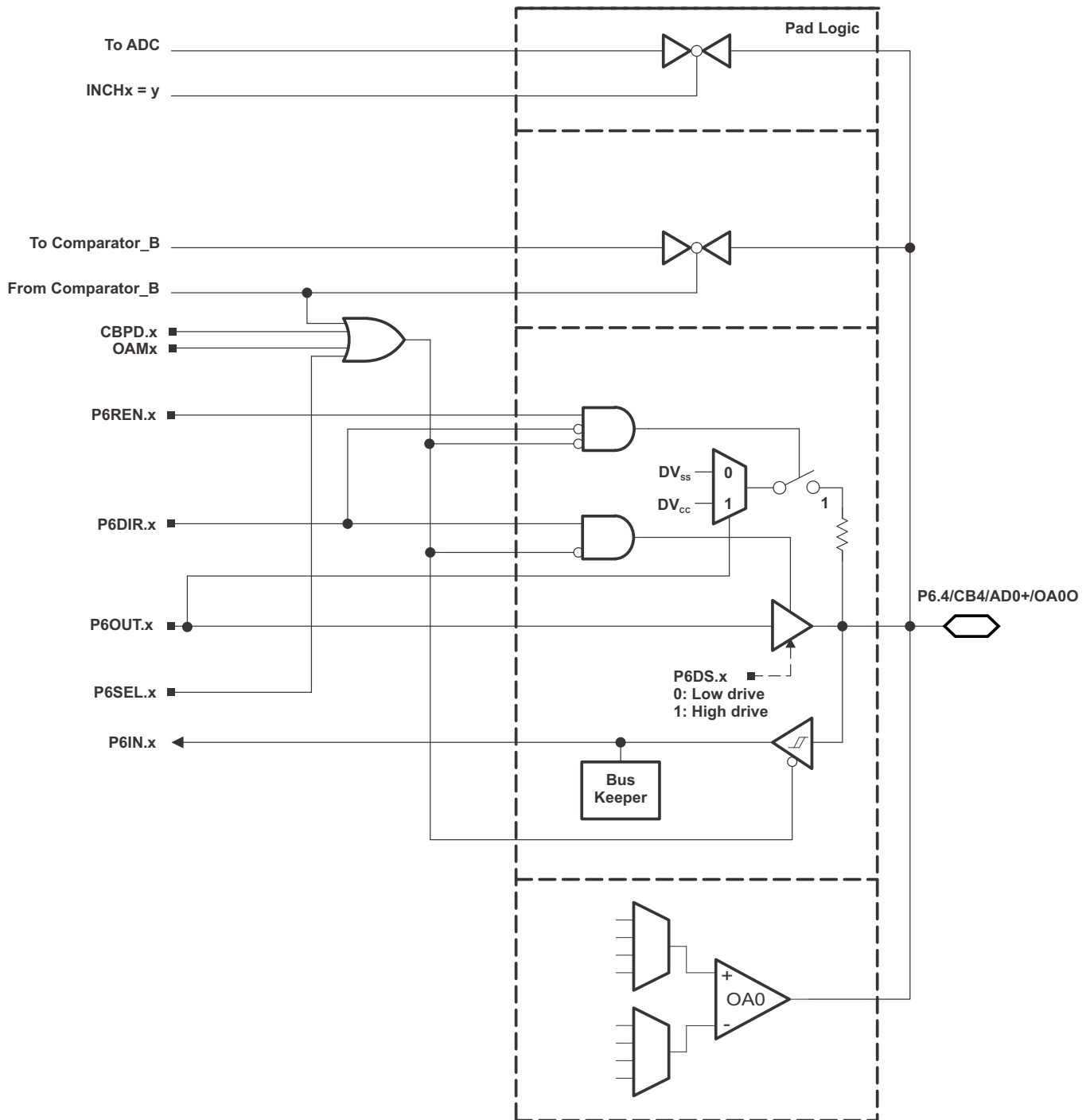


Table 6-25. Port P6 (P6.4) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|--------------------|---|---------------------|--|------------------------|-----------------------|--------------------|
| | | | P6DIR.x | P6SEL.x ⁽²⁾ | CBPD.x ⁽²⁾ | OAMx |
| P6.4/CB4/AD0+/OA00 | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 | 0 | 0 ⁽³⁾ |
| | | CB4 | X | X | 1 | 0 ⁽³⁾ |
| | | AD0+ ⁽⁴⁾ | X | 1 | X | 0 ⁽³⁾ |
| | | OA00 | X | X | X | = 1 ⁽³⁾ |

- (1) X = Don't care
- (2) Setting the P6SEL.x bit, the CBPD.x bit, or the OAMx bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (3) Setting OAMx = 0 disables the operational amplifier and its output is high impedance. Setting OAMx = 1 enables the operational amplifier output. Because the operational amplifier output is shared with the ADC channel, selection of the respective ADC channel allows for direct measurement of the amplifier's output voltage.
- (4) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

6.12.23.11 Port P6, P6.5, Input/Output With Schmitt Trigger

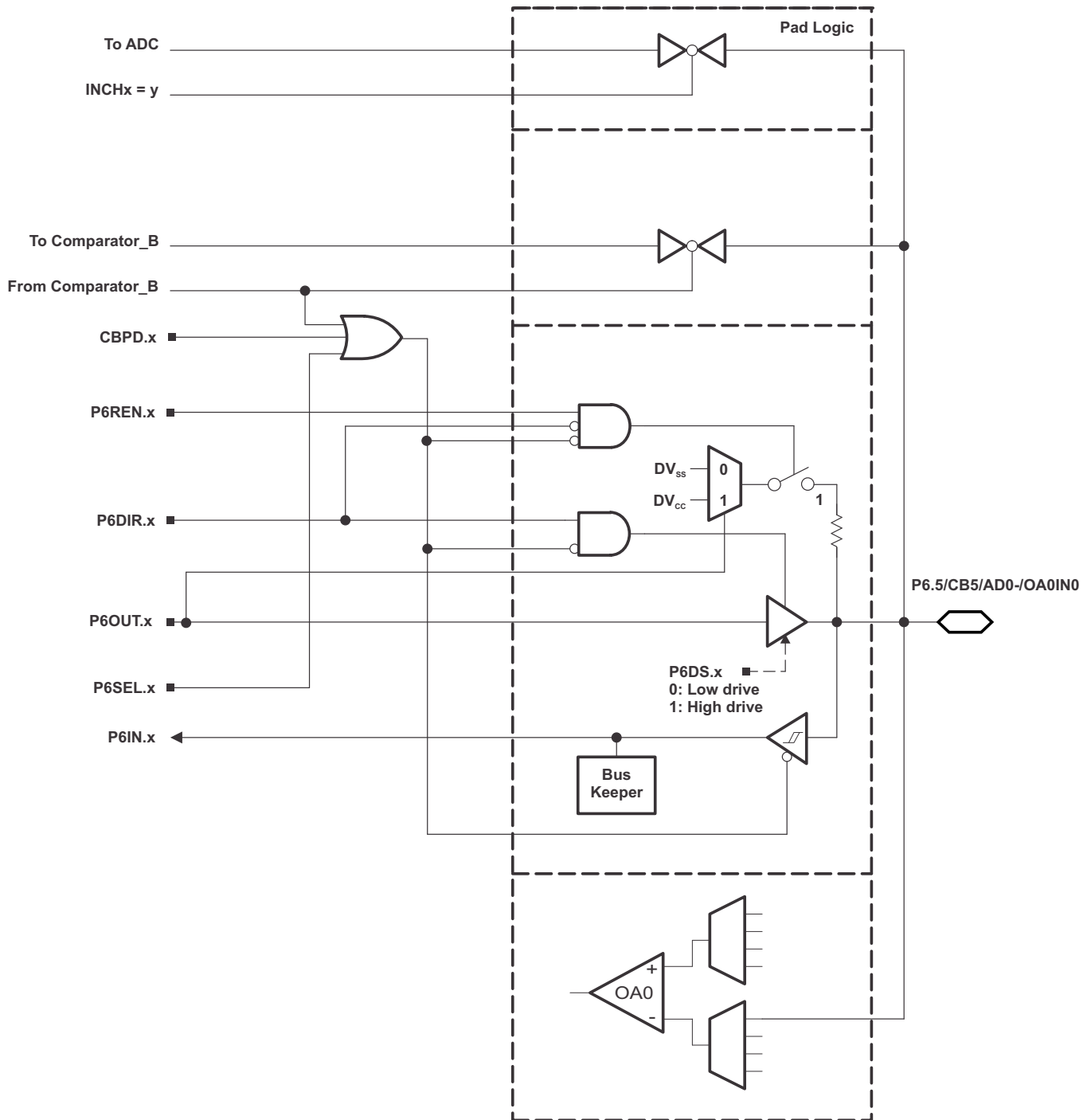


Table 6-26. Port P6 (P6.5) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|----------------------|---|-----------------------|--|------------------------|-----------------------|
| | | | P6DIR.x | P6SEL.x ⁽²⁾ | CBPD.x ⁽²⁾ |
| P6.5/CB5/AD0-/OA0IN0 | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | CB5 | X | X | 1 |
| | | AD0- ⁽³⁾ | X | 1 | X |
| | | OA0IN0 ⁽⁴⁾ | X | 1 | X |

- (1) X = Don't care
- (2) Setting the P6SEL.x bit or CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (3) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.
- (4) Setting the P6SEL.x bit or CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.12.23.12 Port P6, P6.6, Input/Output With Schmitt Trigger

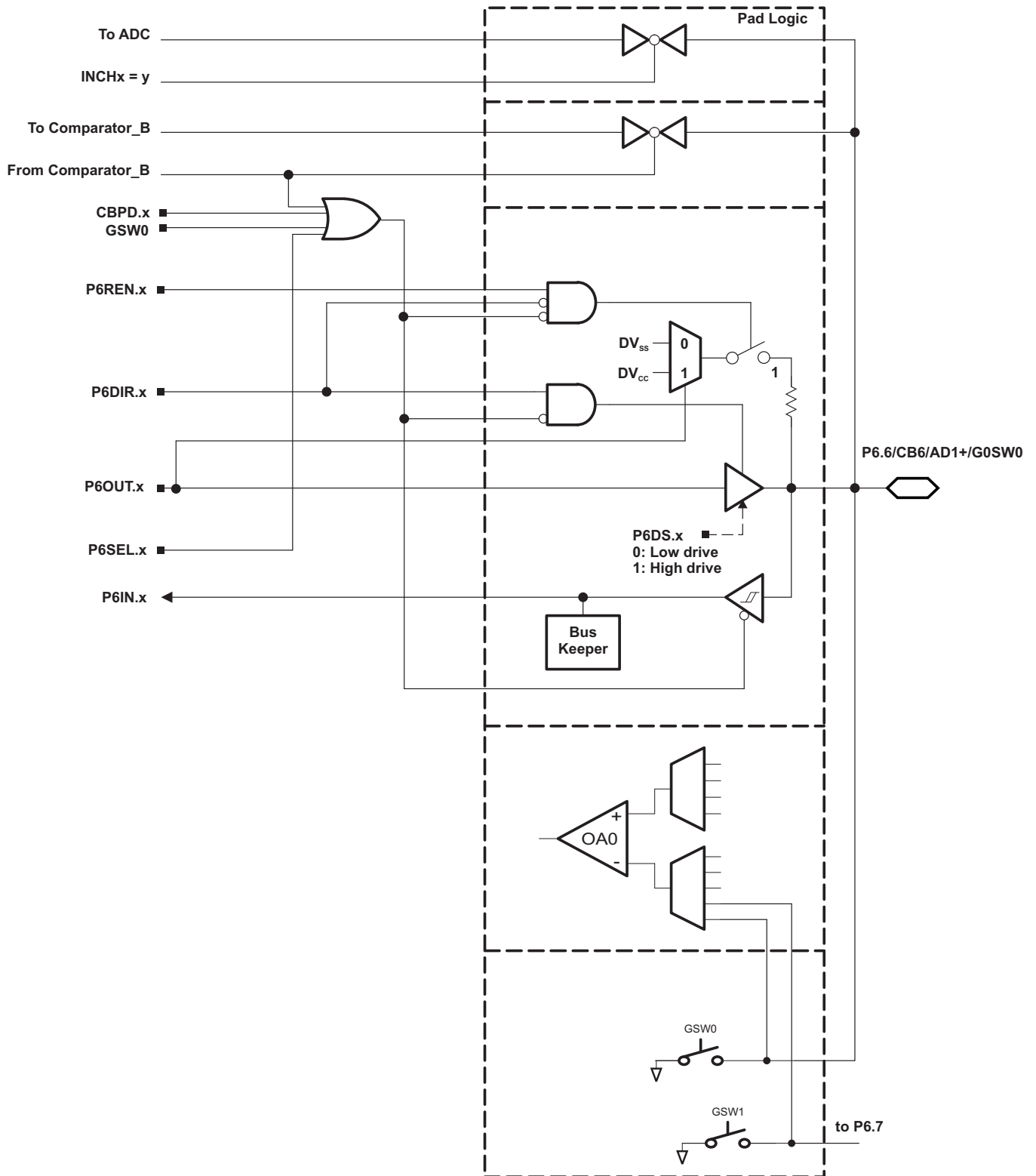


Table 6-27. Port P6 (P6.6) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|---------------------|---|----------------------|--|------------------------|-----------------------|---------------------|
| | | | P6DIR.x | P6SEL.x ⁽²⁾ | CBPD.x ⁽²⁾ | GSW0 ⁽²⁾ |
| P6.6/CB6/AD1+/G0SW0 | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | CB6 | X | X | 1 | 0 |
| | | AD1+ ⁽³⁾ | X | 1 | X | 0 |
| | | G0SW0 ⁽⁴⁾ | X | X | X | 1 |

- (1) X = Don't care
- (2) Setting the P6SEL.x bit, the CBPD.x bit, or the GSW0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (3) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.
- (4) Setting GSW0 = 1 closes the switch and forces the pin to be switched to ground. All switches are independent of each other, so different settings can impose different voltages on the pin. Application must ensure there are no conflicts.

6.12.23.13 Port P6, P6.7, Input/Output With Schmitt Trigger

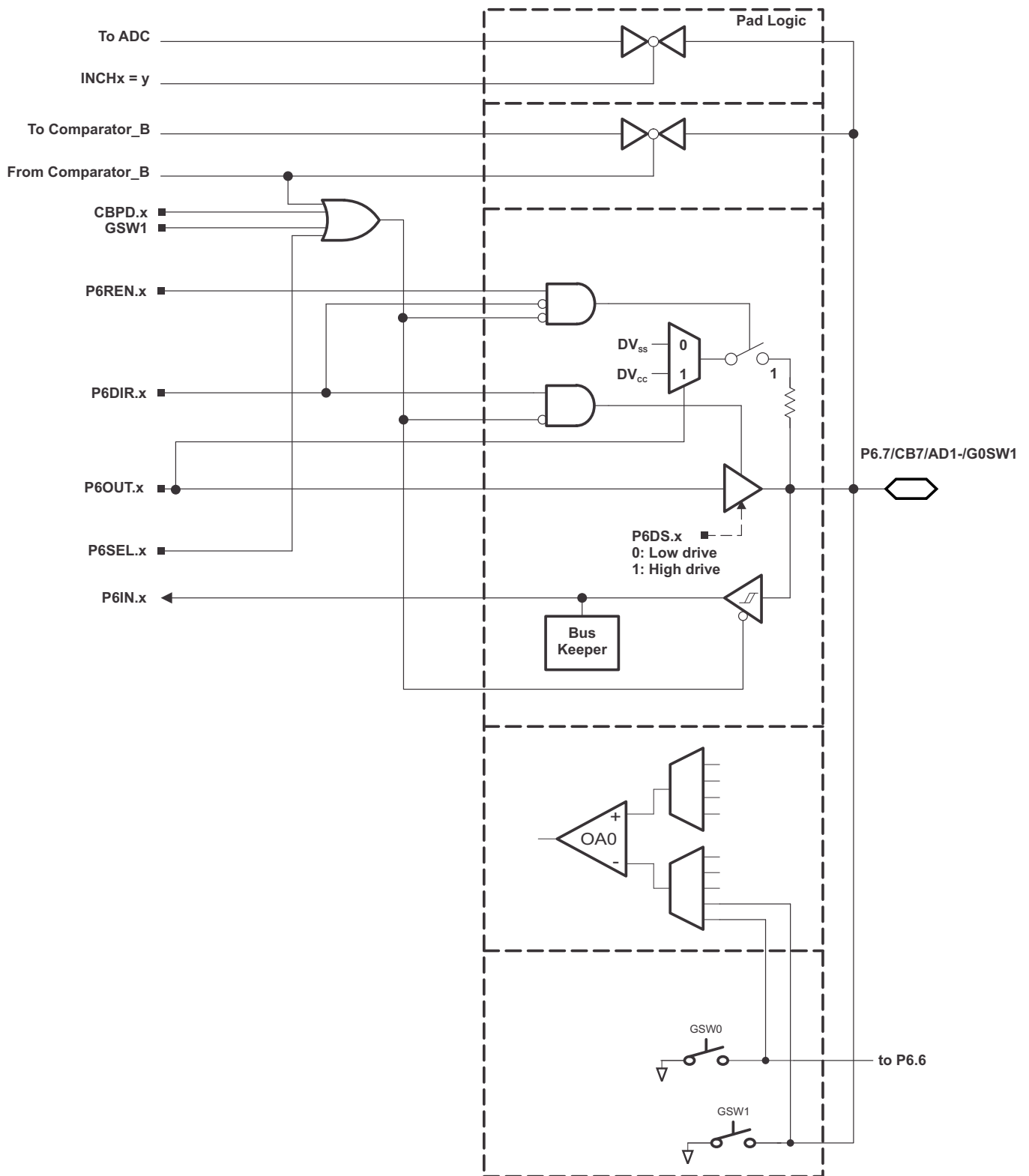


Table 6-28. Port P6 (P6.7) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|---------------------|---|----------------------|--|------------------------|-----------------------|---------------------|
| | | | P6DIR.x | P6SEL.x ⁽²⁾ | CBPD.x ⁽²⁾ | GSW1 ⁽²⁾ |
| P6.7/CB7/AD1-/G0SW1 | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | CB7 | X | X | 1 | 0 |
| | | AD1- ⁽³⁾ | X | 1 | X | 0 |
| | | G0SW1 ⁽⁴⁾ | X | X | X | 1 |

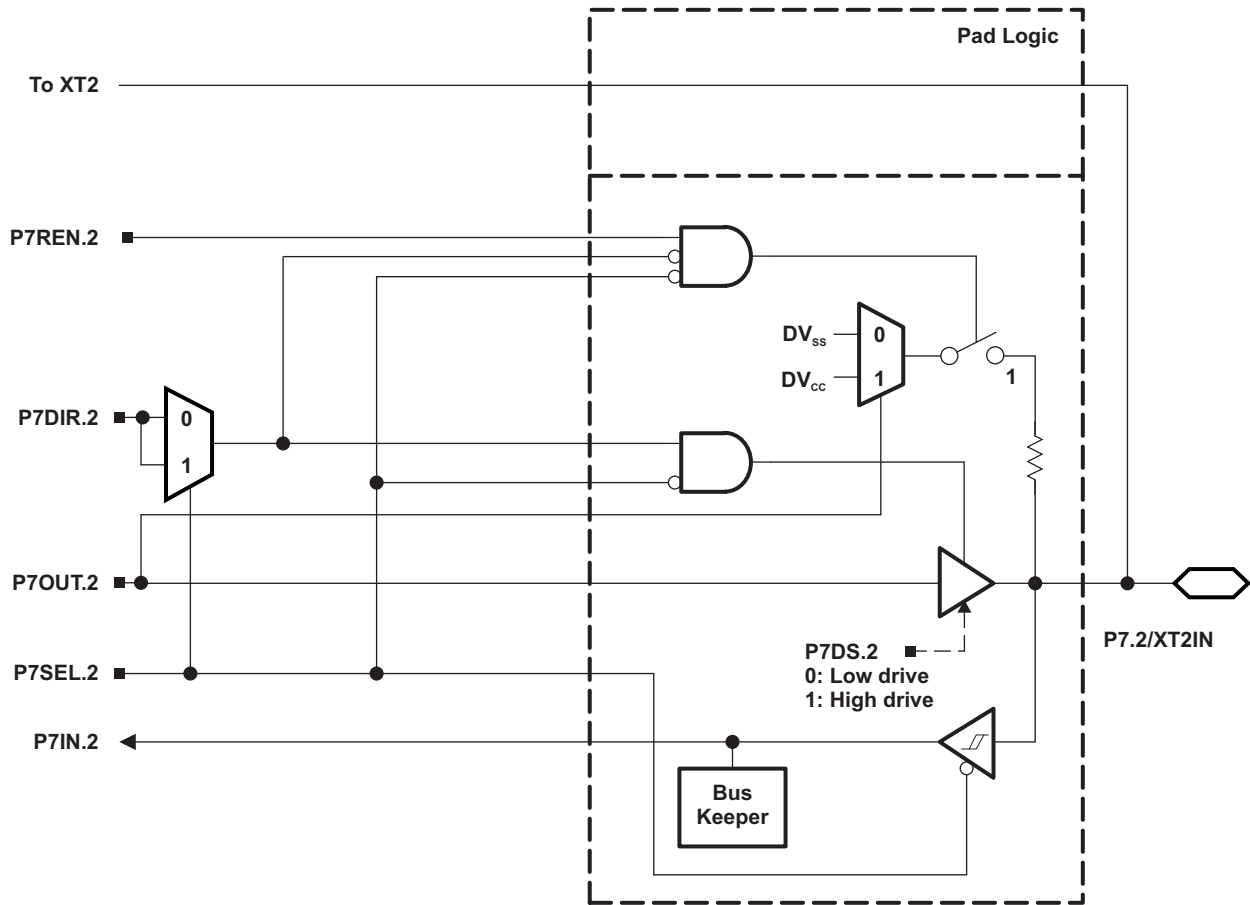
(1) X = Don't care

(2) Setting the P6SEL.x bit, the CBPD.x bit, or the GSW0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

(4) Setting GSW1 = 1 closes the switch and forces the pin to be switched to ground. All switches are independent of each other, so different settings can impose different voltages on the pin. Application must ensure there are no conflicts.

6.12.23.14 Port P7, P7.2, Input/Output With Schmitt Trigger



6.12.23.15 Port P7, P7.3, Input/Output With Schmitt Trigger

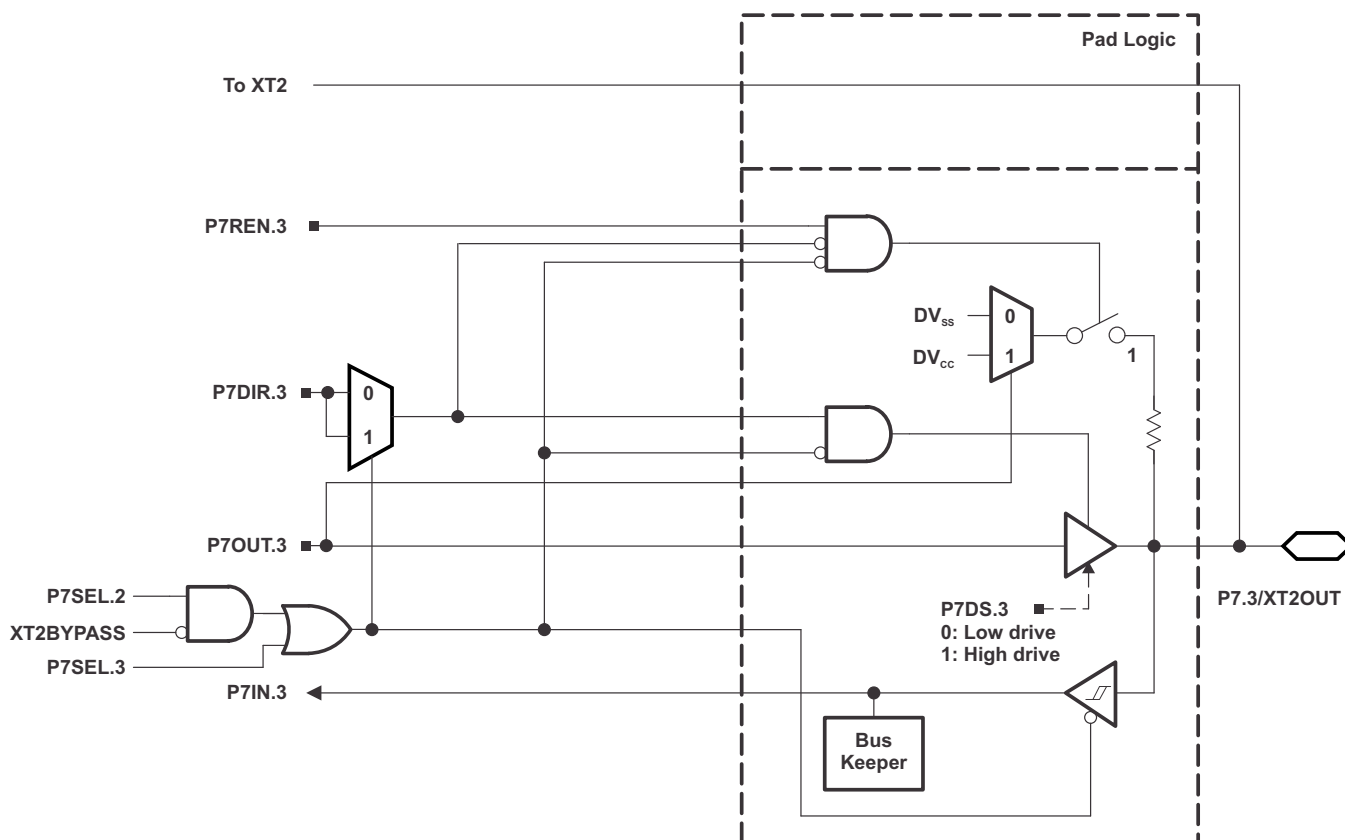


Table 6-29. Port P7 (P7.2 and P7.3) Pin Functions

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-----------------|---|------------------------------------|--|---------|---------|-----------|
| | | | P7DIR.x | P7SEL.2 | P7SEL.3 | XT2BYPASS |
| P7.2/XT2IN | 2 | P7.2 (I/O) | I: 0; O: 1 | 0 | X | X |
| | | XT2IN crystal mode ⁽²⁾ | X | 1 | X | 0 |
| | | XT2IN bypass mode ⁽²⁾ | X | 1 | X | 1 |
| P7.3/XT2OUT | 3 | P7.3 (I/O) | I: 0; O: 1 | 0 | X | X |
| | | XT2OUT crystal mode ⁽³⁾ | X | 1 | X | 0 |
| | | P7.3 (I/O) ⁽³⁾ | X | 1 | X | 1 |

(1) X = Don't care

(2) Setting P7SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P7.2 is configured for crystal mode or bypass mode.

(3) Setting P7SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P7.3 can be used as general-purpose I/O.

6.12.23.16 Port P7, P7.4, Input/Output With Schmitt Trigger

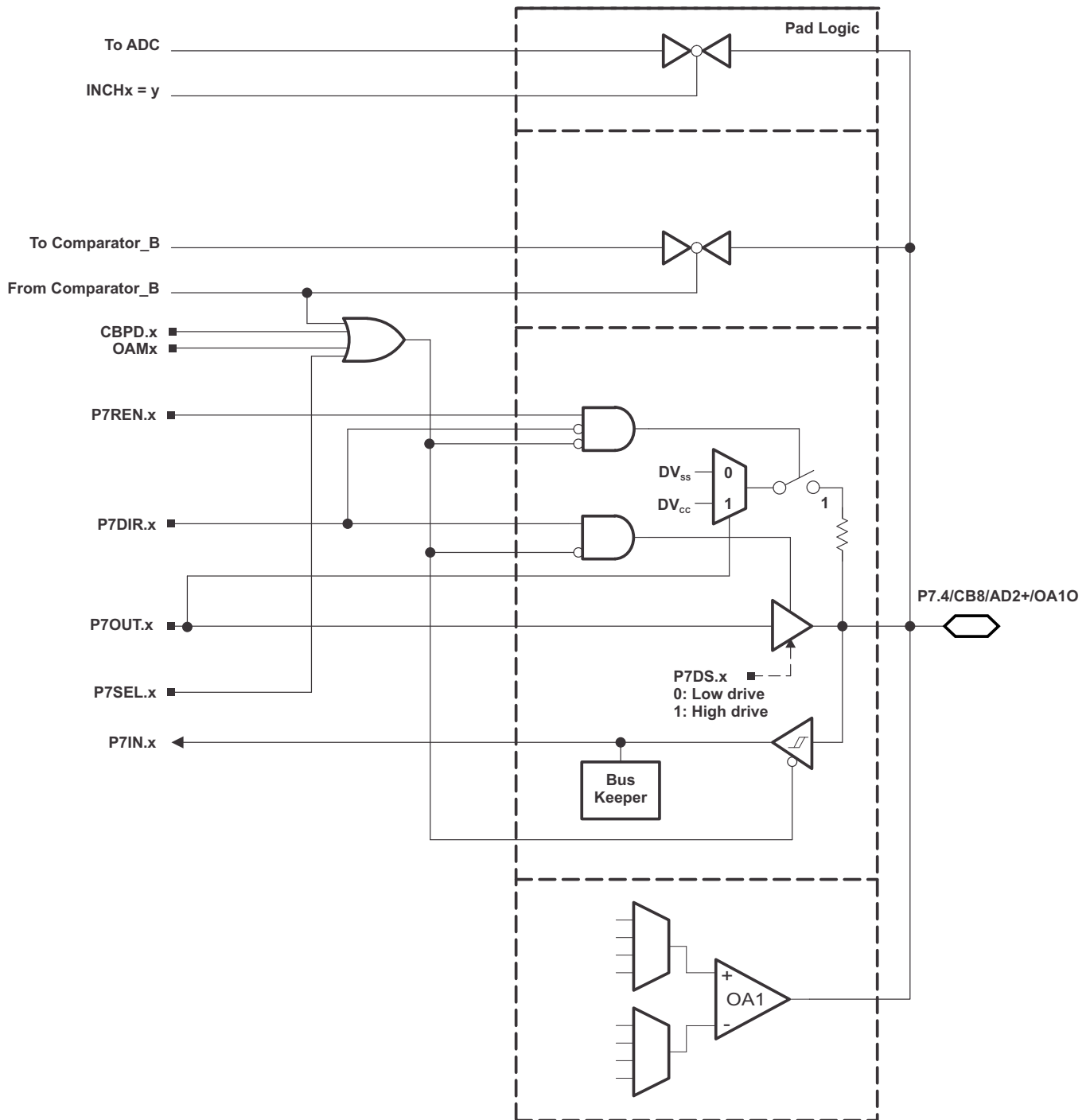


Table 6-30. Port P7 (P7.4) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|--------------------|---|---------------------|--|------------------------|-----------------------|---------------------|
| | | | P6DIR.x | P7SEL.x ⁽²⁾ | CBPD.x ⁽²⁾ | OAMx ⁽²⁾ |
| P7.4/CB8/AD2+/OA1O | 4 | P7.4 (I/O) | I: 0; O: 1 | 0 | 0 | 0 ⁽³⁾ |
| | | CB8 | X | X | 1 | 0 ⁽³⁾ |
| | | AD2+ ⁽⁴⁾ | X | 1 | X | 0 ⁽³⁾ |
| | | OA1O | X | X | X | 1 ⁽³⁾ |

- (1) X = Don't care
- (2) Setting the P6SEL.x bit, the CBPD.x bit, or the OAMx bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (3) Setting OAMx = 0 disables the operational amplifier and its output is high impedance. Setting OAMx = 1 enables the operational amplifier output. Because the operational amplifier output is shared with the ADC channel, selection of the respective ADC channel allows for direct measurement of the amplifier's output voltage.
- (4) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

6.12.23.17 Port P7, P7.5, Input/Output With Schmitt Trigger

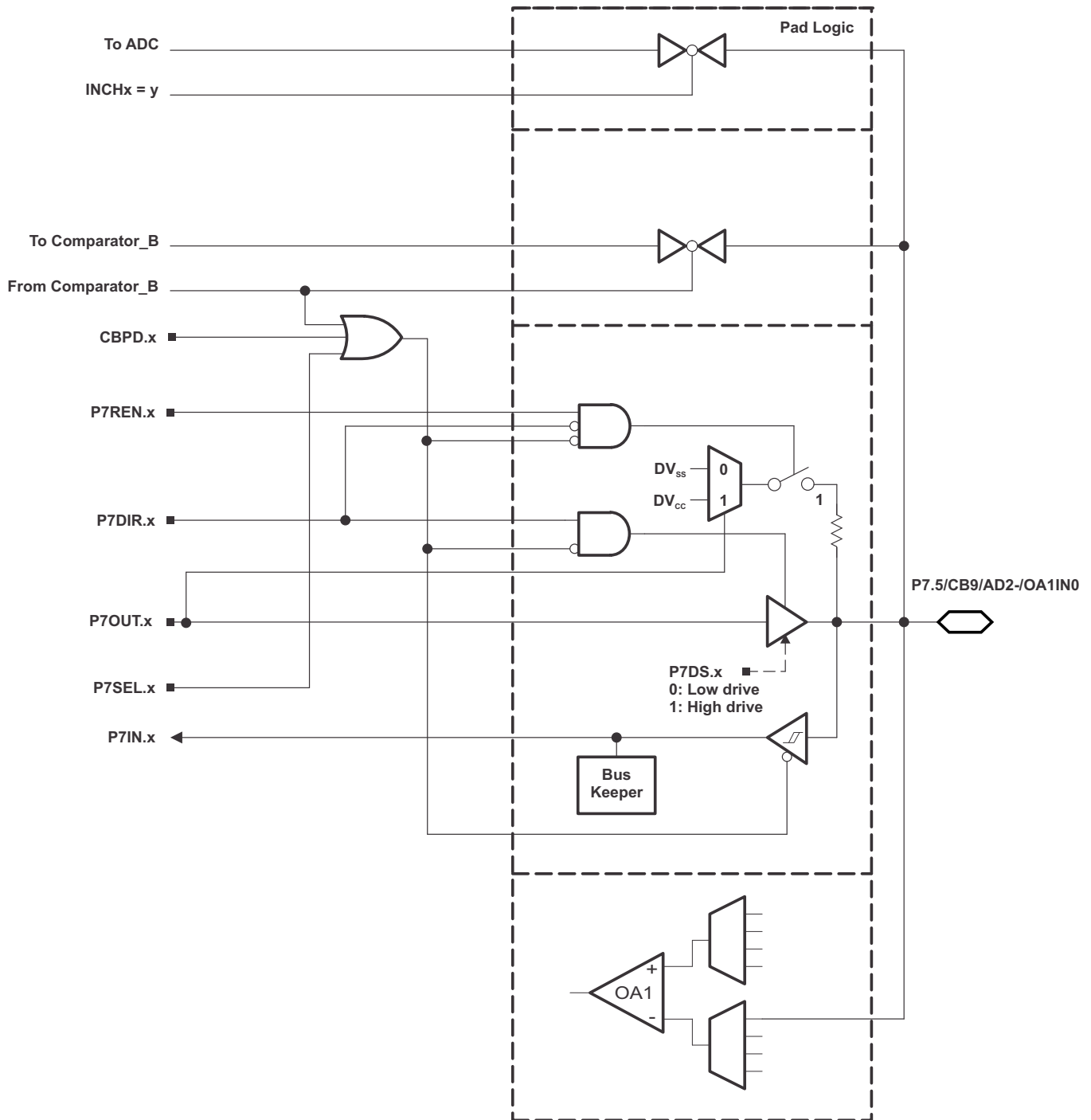


Table 6-31. Port P7 (P7.5) Pin Functions

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|---------------------|---|----------------------|--|------------------------|-----------------------|
| | | | P7DIR.x | P7SEL.x ⁽²⁾ | CBPD.x ⁽²⁾ |
| P7.5/CB9/AD2-/OAIN0 | 5 | P7.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | CB9 | X | X | 1 |
| | | AD2- ⁽³⁾ | X | 1 | X |
| | | OAIN0 ⁽²⁾ | X | 1 | X |

(1) X = Don't care

(2) Setting the P7SEL.x bit or the CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

6.12.23.18 Port P7, P7.6, Input/Output With Schmitt Trigger

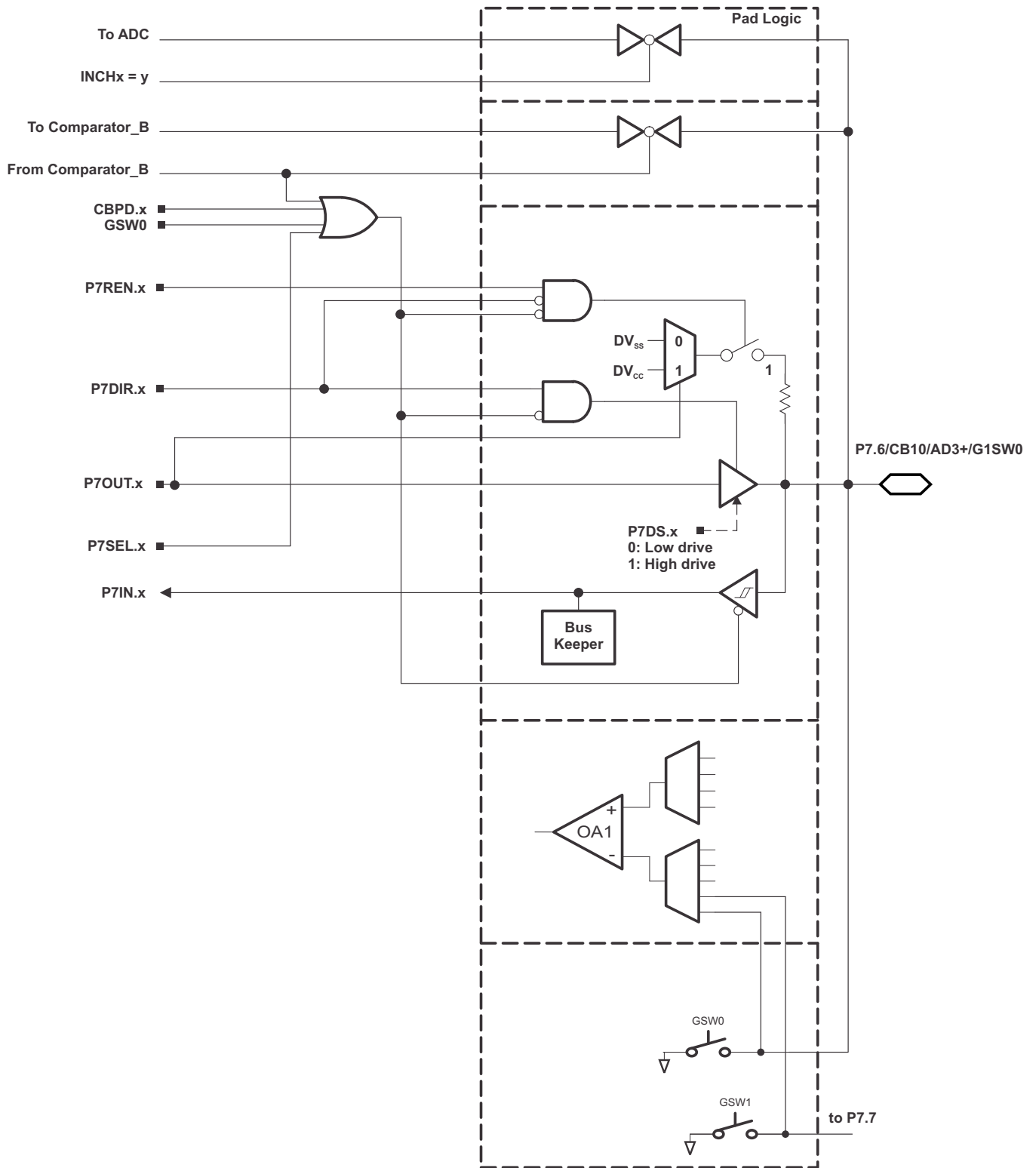


Table 6-32. Port P7 (P7.6) Pin Functions

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|----------------------|---|----------------------|--|------------------------|-----------------------|---------------------|
| | | | P6DIR.x | P7SEL.x ⁽²⁾ | CBPD.x ⁽²⁾ | GSW0 ⁽²⁾ |
| P7.6/CB10/AD3+/G1SW0 | 6 | P7.6 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | CB10 | X | X | 1 | 0 |
| | | AD3+ ⁽³⁾ | X | 1 | X | 0 |
| | | G1SW0 ⁽⁴⁾ | X | X | X | 1 |

- (1) X = Don't care
- (2) Setting the P7SEL.x bit, the CBPD.x bit, or the GSW0 disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (3) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.
- (4) Setting GSW0 = 1 closes the switch and forces the pin to be switched to ground. All switches are independent of each other, so different settings can impose different voltages on the pin. Application must ensure there are no conflicts.

6.12.23.19 Port P7, P7.7, Input/Output With Schmitt Trigger

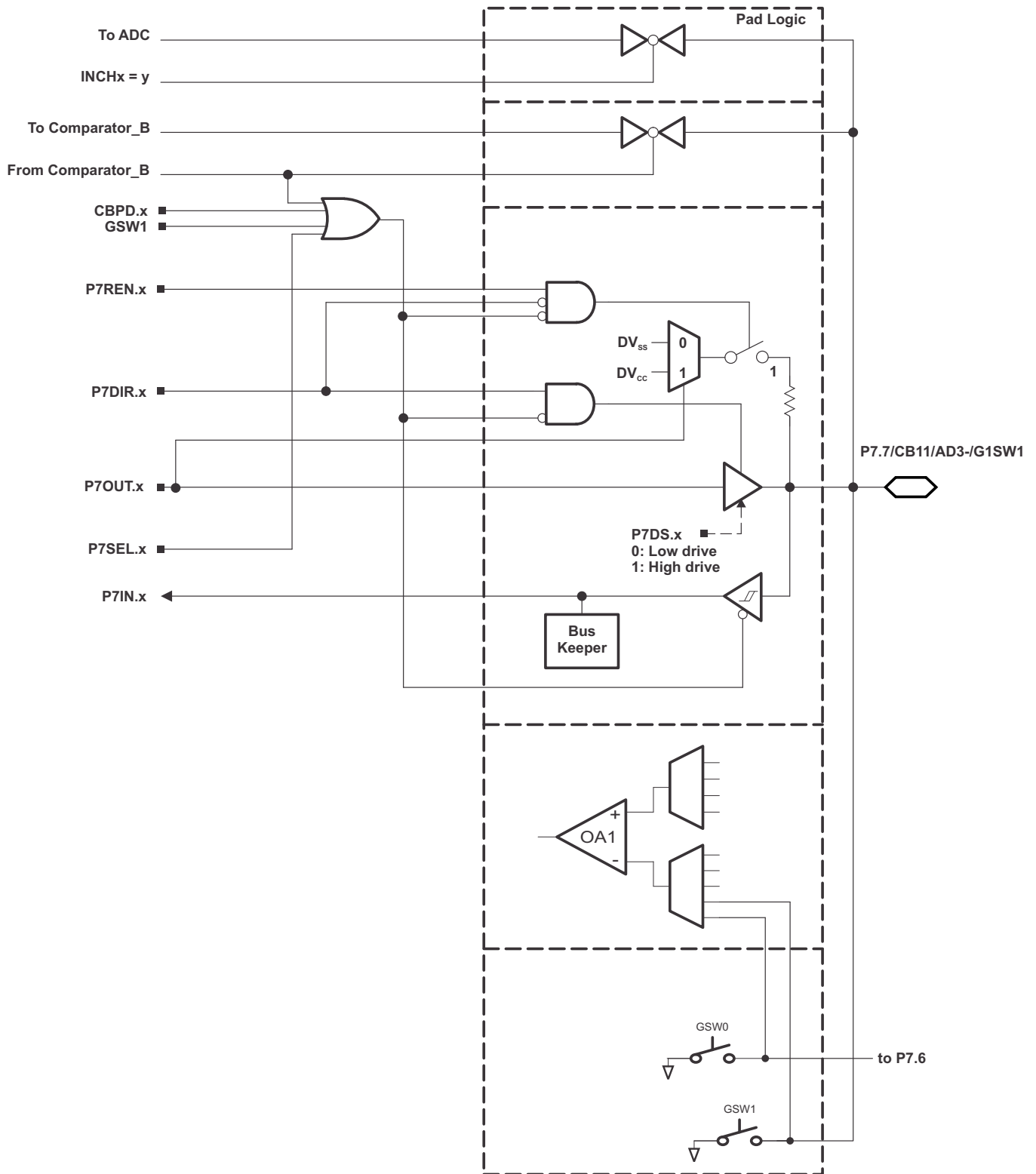


Table 6-33. Port P7 (P7.7) Pin Functions

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|----------------------|---|----------------------|--|------------------------|-----------------------|---------------------|
| | | | P6DIR.x | P7SEL.x ⁽²⁾ | CBPD.x ⁽²⁾ | GSW1 ⁽²⁾ |
| P7.7/CB11/AD3-/G1SW1 | 7 | P7.7 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | CB11 | X | X | 1 | 0 |
| | | AD3- ⁽³⁾ | X | 1 | X | 0 |
| | | G1SW1 ⁽⁴⁾ | X | X | X | 1 |

- (1) X = Don't care
- (2) Setting the P7SEL.x bit, the CBPD.x bit, or the GSW1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (3) The ADC channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.
- (4) Setting GSW1 = 1 closes the switch and forces the pin to be switched to ground. All switches are independent of each other, so different settings can impose different voltages on the pin. Application must ensure there are no conflicts.

6.12.23.20 Port P8, P8.0 to P8.7, Input/Output With Schmitt Trigger

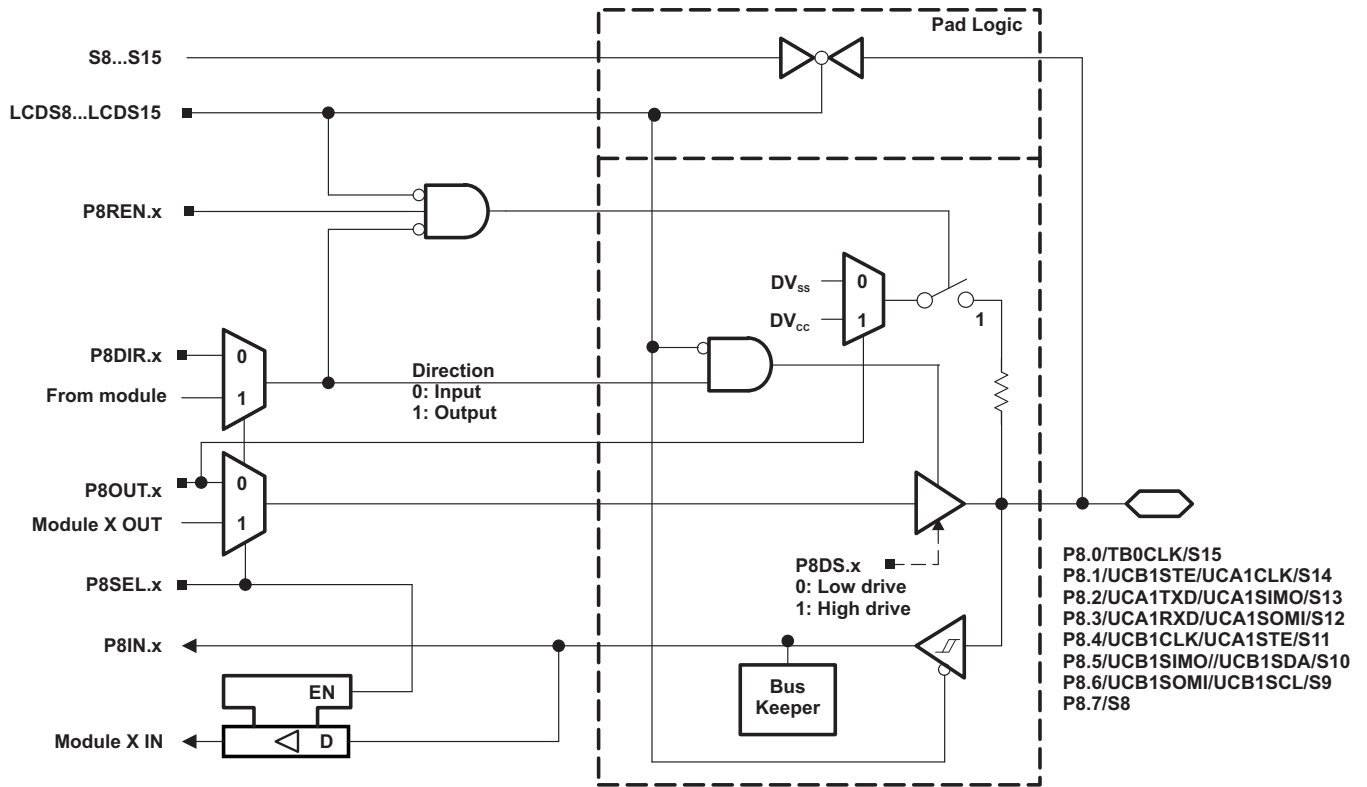


Table 6-34. Port P8 (P8.0 to P8.7) Pin Functions

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|---------------------------|---|------------------------------|--|---------|------------|
| | | | P8DIR.x | P8SEL.x | LCDS8...16 |
| P8.0/TB0CLK/S15 | 0 | P8.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer TB0.TB0CLK clock input | 0 | 1 | 0 |
| | | S15 | X | X | 1 |
| P8.1/UCB1STE/UCA1CLK/S14 | 1 | P8.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB1STE/UCA1CLK | X | 1 | 0 |
| | | S14 | X | X | 1 |
| P8.2/UCA1TXD/UCA1SIMO/S13 | 2 | P8.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA1TXD/UCA1SIMO | X | 1 | 0 |
| | | S13 | X | X | 1 |
| P8.3/UCA1RXD/UCA1SOMI/S12 | 3 | P8.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA1RXD/UCA1SOMI | X | 1 | 0 |
| | | S12 | X | X | 1 |
| P8.4/UCB1CLK/UCA1STE/S11 | 4 | P8.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB1CLK/UCA1STE | X | 1 | 0 |
| | | S11 | X | X | 1 |
| P8.5/UCB1SIMO/UCB1SDA/S10 | 5 | P8.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB1SIMO/UCB1SDA | X | 1 | 0 |
| | | S10 | X | X | 1 |
| P8.6/UCB1SOMI/UCB1SCL/S9 | 6 | P8.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB1SOMI/UCB1SCL | X | 1 | 0 |
| | | S9 | X | X | 1 |
| P8.7/S8 | 7 | P8.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | S8 | X | X | 1 |

(1) X = Don't care

6.12.23.21 Port P9, P9.0 to P9.7, Input/Output With Schmitt Trigger

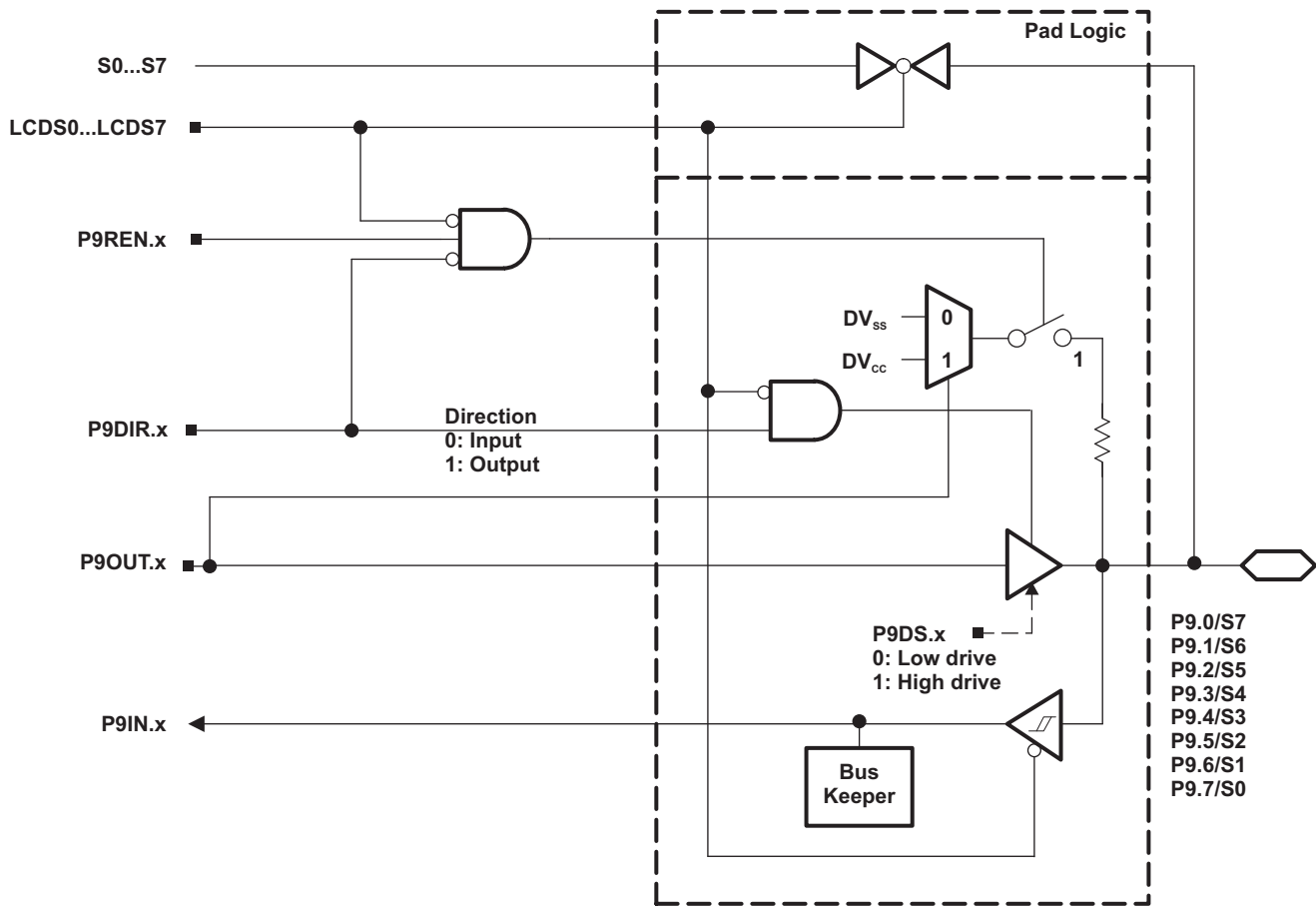


Table 6-35. Port P9 (P9.0 to P9.7) Pin Functions

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|---------|-----------|
| | | | P9DIR.x | P9SEL.x | LCDS0...7 |
| P9.0/S7 | 0 | P9.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | S7 | X | X | 1 |
| P9.1/S6 | 1 | P9.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | S6 | X | X | 1 |
| P9.2/S5 | 2 | P9.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | S5 | X | X | 1 |
| P9.3/S4 | 3 | P9.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | S4 | X | X | 1 |
| P9.4/S3 | 4 | P9.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | S3 | X | X | 1 |
| P9.5/S2 | 5 | P9.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | S2 | X | X | 1 |
| P9.6/S1 | 6 | P9.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | S1 | X | X | 1 |
| P9.7/S0 | 7 | P9.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | S0 | X | X | 1 |

(1) X = Don't care

6.12.23.22 Port PU.0/DP, PU.1/DM, PUR USB Ports for MSP430FG662x

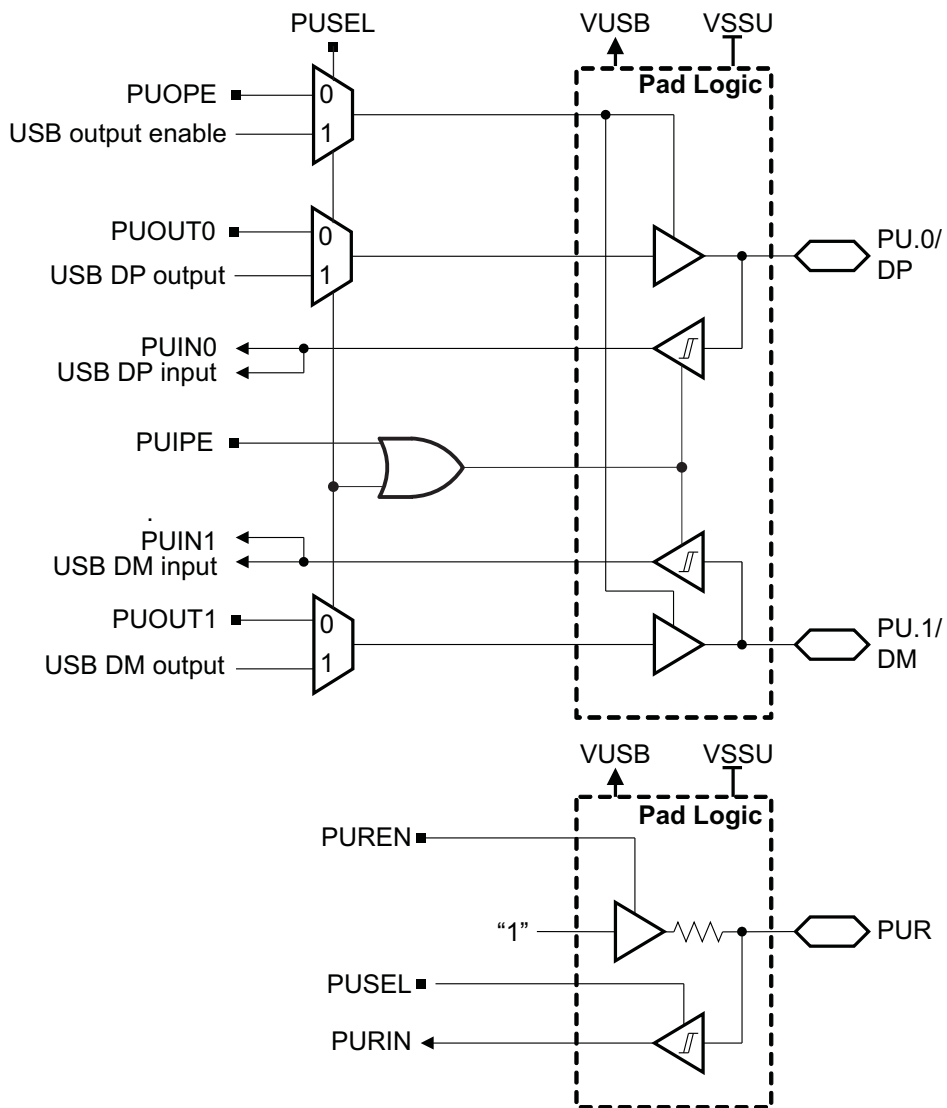


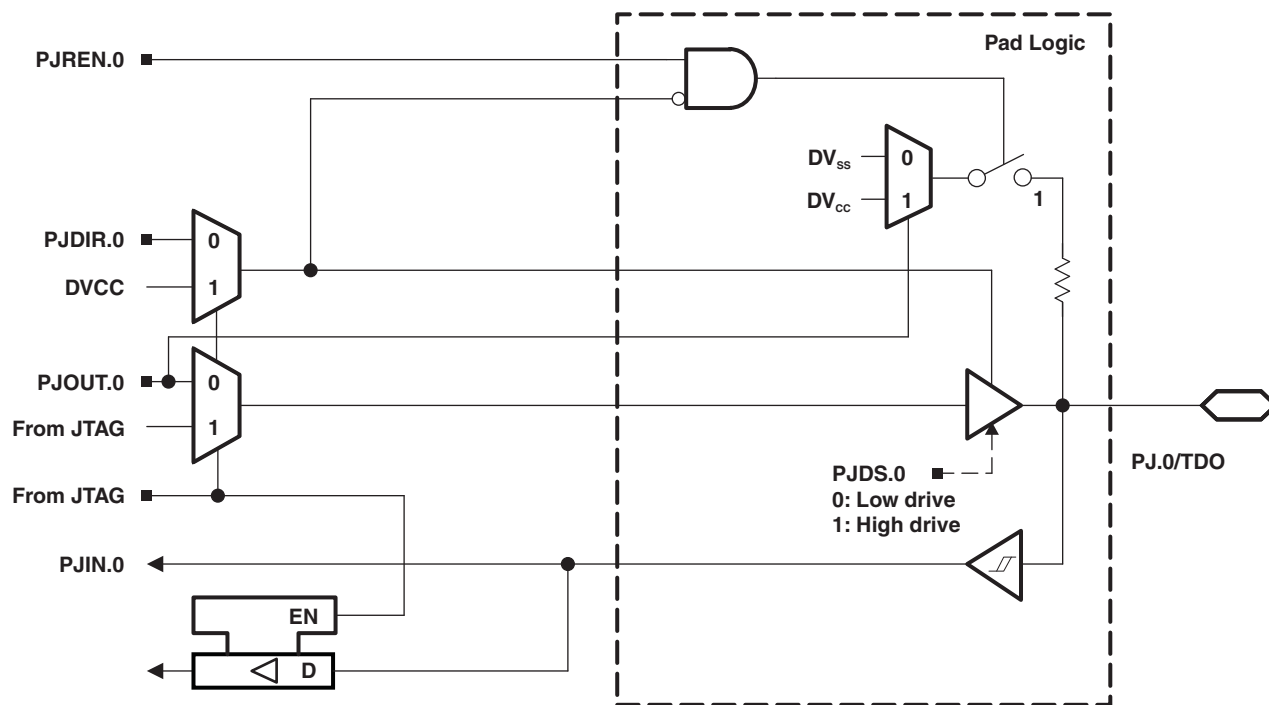
Table 6-36. Port PU.0/DP, PU.1/DM Output Functions for MSP430FG662x

| CONTROL BITS | | | | PIN NAME | | FUNCTION |
|--------------|-------|--------|--------|----------|---------|-----------------------------|
| PUSEL | PUDIR | PUOUT1 | PUOUT0 | PU.1/DM | PU.0/DP | |
| 0 | 0 | X | X | Hi-Z | Hi-Z | Outputs off |
| 0 | 1 | 0 | 0 | 0 | 0 | Outputs enabled |
| 0 | 1 | 0 | 1 | 0 | 1 | Outputs enabled |
| 0 | 1 | 1 | 0 | 1 | 0 | Outputs enabled |
| 0 | 1 | 1 | 1 | 1 | 1 | Outputs enabled |
| 1 | X | X | X | DM | DP | Direction set by USB module |

Table 6-37. Port PUR Input Functions

| CONTROL BITS | | FUNCTION |
|--------------|-------|-----------------------------------|
| PUSEL | PUREN | |
| 0 | 0 | Input disabled Pullup disabled |
| 0 | 1 | Input disabled Pullup enabled |
| 1 | 0 | Input enabled Pullup disabled |
| 1 | 1 | Input enabled Pullup enabled |

6.12.23.23 Port J, J.0 JTAG pin TDO, Input/Output With Schmitt Trigger or Output



6.12.23.24 Port J, J.1 to J.3 JTAG pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

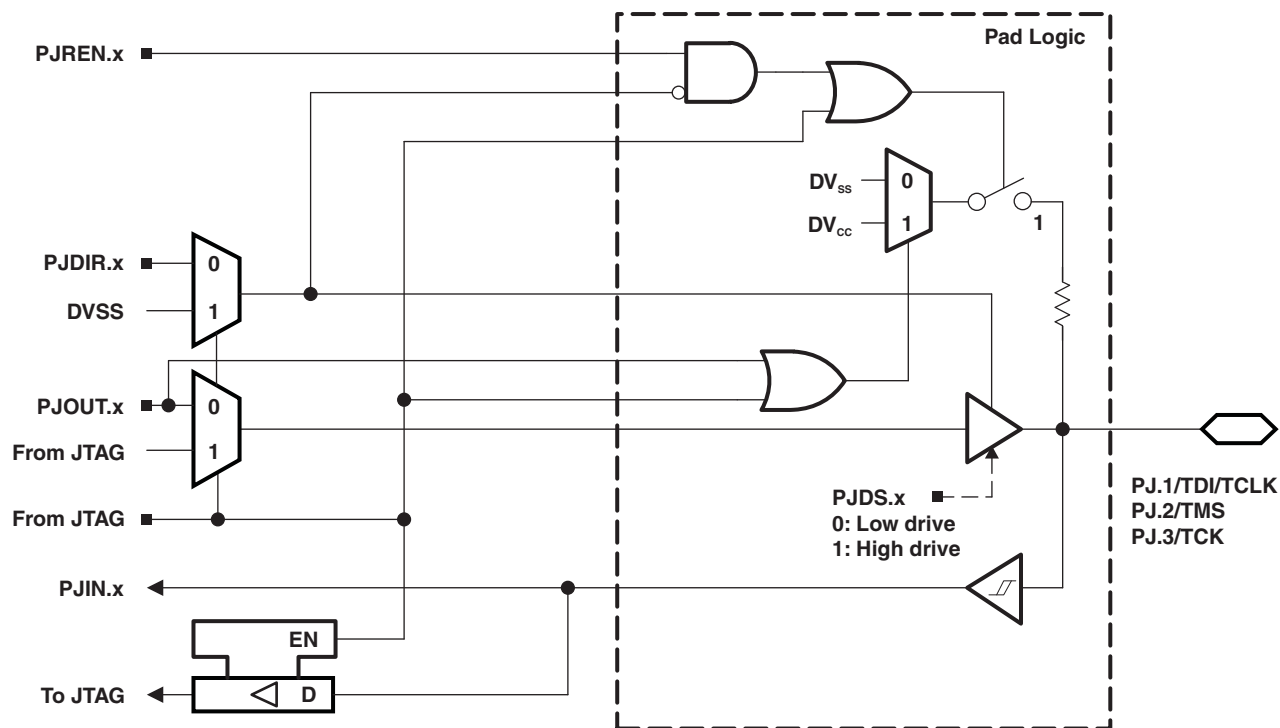


Table 6-38. Port PJ (PJ.0 to PJ.3) Pin Functions

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ |
|-----------------|---|-----------------------------|--|
| | | | PJDIR.x |
| PJ.0/TDO | 0 | PJ.0 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TDO ⁽³⁾ | X |
| PJ.1/TDI/TCLK | 1 | PJ.1 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TDI/TCLK ^{(3) (4)} | X |
| PJ.2/TMS | 2 | PJ.2 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TMS ^{(3) (4)} | X |
| PJ.3/TCK | 3 | PJ.3 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TCK ^{(3) (4)} | X |

- (1) X = Don't care
- (2) Default condition
- (3) The pin direction is controlled by the JTAG module.
- (4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

6.13 Device Descriptors

Table 6-39 summarizes the contents of the device descriptor tag-length-value (TLV) structure.

Table 6-39. Device Descriptor Table

| | DESCRIPTION | ADDRESS | SIZE (bytes) | VALUE | | | |
|--------------------|--|---------|-----------------|----------|----------|----------|----------|
| | | | | FG6626 | FG6625 | FG6426 | FG6425 |
| Info Block | Info length | 01A00h | 1 | 06h | 06h | 06h | 06h |
| | CRC length | 01A01h | 1 | 06h | 06h | 06h | 06h |
| | CRC value | 01A02h | 2 | per unit | per unit | per unit | per unit |
| | Device ID | 01A04h | 2 | 8234h | 8235h | 8236h | 8237h |
| | Hardware revision | 01A06h | 1 | per unit | per unit | per unit | per unit |
| | Firmware revision | 01A07h | 1 | per unit | per unit | per unit | per unit |
| Die Record | Die Record Tag | 01A08h | 1 | 08h | 08h | 08h | 08h |
| | Die Record length | 01A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/Wafer ID | 01A0Ah | 4 | per unit | per unit | per unit | per unit |
| | Die X position | 01A0Eh | 2 | per unit | per unit | per unit | per unit |
| | Die Y position | 01A10h | 2 | per unit | per unit | per unit | per unit |
| | Test results | 01A12h | 2 | per unit | per unit | per unit | per unit |
| CTSD16 Calibration | CTSD16 Calibration Tag | 01A14h | 1 | 1Dh | 1Dh | 1Dh | 1Dh |
| | CTSD16 Calibration length | 01A15h | 1 | 0Ch | 0Ch | 0Ch | 0Ch |
| | CTSD16 gain factor gain=1 | 01A16h | 2 | per unit | per unit | per unit | per unit |
| | CTSD16 gain factor gain=16 | 01A18h | 2 | per unit | per unit | per unit | per unit |
| | CTSD16 offset gain=1 | 01A1Ah | 2 | per unit | per unit | per unit | per unit |
| | CTSD16 offset gain=16 | 01A1Ch | 2 | per unit | per unit | per unit | per unit |
| | CTSD16 Internal Reference Temp. Sensor 30°C | 01A1Eh | 2 | per unit | per unit | per unit | per unit |
| | CTSD16 Internal Reference Temp. Sensor 85°C | 01A20h | 2 | per unit | per unit | per unit | per unit |

6.14 Memory

Table 6-40 summarizes the memory organization for all devices.

Table 6-40. Memory Organization⁽¹⁾⁽²⁾

| | | MSP430FG6626 | MSP430FG6625 | MSP430FG6426 | MSP430FG6425 |
|--|------------|--------------------------|--------------------------|--------------------------|--------------------------|
| Memory (flash) Main: interrupt vector | Total Size | 128KB 00FFFFh–00FF80h | 64KB 00FFFFh–00FF80h | 128KB 00FFFFh–00FF80h | 64KB 00FFFFh–00FF80h |
| Main: code memory | Bank 3 | 32KB 0243FFh–01C400h | NA | 32KB 0243FFh–01C400h | NA |
| | Bank 2 | 32KB 01C3FFh–014400h | NA | 32KB 01C3FFh–014400h | NA |
| | Bank 1 | 32KB 0143FFh–00C400h | 32KB 0143FFh–00C400h | 32KB 0143FFh–00C400h | 32KB 0143FFh–00C400h |
| | Bank 0 | 32KB 00C3FFh–004400h | 32KB 00C3FFh–004400h | 32KB 00C3FFh–004400h | 32KB 00C3FFh–004400h |
| RAM | Sector 3 | 2KB 0043FFh–003C00h | 2KB 0043FFh–003C00h | 2KB 0043FFh–003C00h | 2KB 0043FFh–003C00h |
| | Sector 2 | 2KB 003BFFh–003400h | 2KB 003BFFh–003400h | 2KB 003BFFh–003400h | 2KB 003BFFh–003400h |
| | Sector 1 | 2KB 0033FFh–002C00h | 2KB 0033FFh–002C00h | 2KB 0033FFh–002C00h | 2KB 0033FFh–002C00h |
| | Sector 0 | 2KB 002BFFh–002400h | 2KB 002BFFh–002400h | 2KB 002BFFh–002400h | 2KB 002BFFh–002400h |
| RAM ⁽³⁾ | Sector 7 | NA | NA | 2 KB 0023FFh–001C00h | 2KB 0023FFh–001C00h |
| USB RAM ⁽⁴⁾ | Sector 7 | 2KB 0023FFh–001C00h | 2KB 0023FFh–001C00h | NA | NA |
| TI factory memory (ROM) | A | 128 B 001BFFh–001B80h | 128 B 001BFFh–001B80h | 128 B 001BFFh–001B80h | 128 B 001BFFh–001B80h |
| | B | 128 B 001B7Fh–001B00h | 128 B 001B7Fh–001B00h | 128 B 001B7Fh–001B00h | 128 B 001B7Fh–001B00h |
| | C | 128 B 001AFFh–001A80h | 128 B 001AFFh–001A80h | 128 B 001AFFh–001A80h | 128 B 001AFFh–001A80h |
| | D | 128 B 001A7Fh–001A00h | 128 B 001A7Fh–001A00h | 128 B 001A7Fh–001A00h | 128 B 001A7Fh–001A00h |
| Information memory (flash) | Info A | 128 B 0019FFh–001980h | 128 B 0019FFh–001980h | 128 B 0019FFh–001980h | 128 B 0019FFh–001980h |
| | Info B | 128 B 00197Fh–001900h | 128 B 00197Fh–001900h | 128 B 00197Fh–001900h | 128 B 00197Fh–001900h |
| | Info C | 128 B 0018FFh–001880h | 128 B 0018FFh–001880h | 128 B 0018FFh–001880h | 128 B 0018FFh–001880h |
| | Info D | 128 B 00187Fh–001800h | 128 B 00187Fh–001800h | 128 B 00187Fh–001800h | 128 B 00187Fh–001800h |
| Bootstrap loader (BSL) memory (flash) | BSL 3 | 512 B 0017FFh–001600h | 512 B 0017FFh–001600h | 512 B 0017FFh–001600h | 512 B 0017FFh–001600h |
| | BSL 2 | 512 B 0015FFh–001400h | 512 B 0015FFh–001400h | 512 B 0015FFh–001400h | 512 B 0015FFh–001400h |
| | BSL 1 | 512 B 0013FFh–001200h | 512 B 0013FFh–001200h | 512 B 0013FFh–001200h | 512 B 0013FFh–001200h |
| | BSL 0 | 512 B 0011FFh–001000h | 512 B 0011FFh–001000h | 512 B 0011FFh–001000h | 512 B 0011FFh–001000h |
| Peripherals | Size | 4 KB 000FFFh–000000h | 4KB 000FFFh–000000h | 4KB 000FFFh–000000h | 4KB 000FFFh–000000h |

(1) N/A = Not available.

(2) Backup RAM is accessed through the control registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3.

(3) Only available on FG642x.

(4) Only available on FG662x. USB RAM can be used as general-purpose RAM when not used for USB operation.

6.14.1 Peripheral File Map

Table 6-41 lists all of the the available peripherals and their base addresses. Table 6-42 through Table 6-78 list the registers and their offset addresses for each peripheral.

Table 6-41. Peripherals

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE ⁽¹⁾ |
|---|--------------|-------------------------------------|
| Special Functions (see Table 6-42) | 0100h | 000h-01Fh |
| PMM (see Table 6-43) | 0120h | 000h-010h |
| Flash Control (see Table 6-44) | 0140h | 000h-00Fh |
| CRC16 (see Table 6-45) | 0150h | 000h-007h |
| RAM Control (see Table 6-46) | 0158h | 000h-001h |
| Watchdog (see Table 6-47) | 015Ch | 000h-001h |
| UCS (see Table 6-48) | 0160h | 000h-01Fh |
| SYS (see Table 6-49) | 0180h | 000h-01Fh |
| Shared Reference (see Table 6-50) | 01B0h | 000h-001h |
| Port Mapping Control (see Table 6-51) | 01C0h | 000h-003h |
| Port Mapping Port P2 (see Table 6-51) | 01D0h | 000h-007h |
| Port P1, P2 (see Table 6-52) | 0200h | 000h-01Fh |
| Port P3, P4 (see Table 6-53) | 0220h | 000h-01Fh |
| Port P5, P6 (see Table 6-54) | 0240h | 000h-00Bh |
| Port P7, P8 (see Table 6-55) | 0260h | 000h-00Bh |
| Port P9 (see Table 6-56) | 0280h | 000h-00Bh |
| Port PJ (see Table 6-57) | 0320h | 000h-01Fh |
| Timer TA0 (see Table 6-58) | 0340h | 000h-02Eh |
| Timer TA1 (see Table 6-59) | 0380h | 000h-02Eh |
| Timer TB0 (see Table 6-60) | 03C0h | 000h-02Eh |
| Timer TA2 (see Table 6-61) | 0400h | 000h-02Eh |
| Battery Backup (see Table 6-62) | 0480h | 000h-01Fh |
| RTC_B (see Table 6-63) | 04A0h | 000h-01Fh |
| 32-Bit Hardware Multiplier (see Table 6-64) | 04C0h | 000h-02Fh |
| DMA General Control (see Table 6-65) | 0500h | 000h-00Fh |
| DMA Channel 0 (see Table 6-65) | 0510h | 000h-00Ah |
| DMA Channel 1 (see Table 6-65) | 0520h | 000h-00Ah |
| DMA Channel 2 (see Table 6-65) | 0530h | 000h-00Ah |
| DMA Channel 3 (see Table 6-65) | 0540h | 000h-00Ah |
| DMA Channel 4 (see Table 6-65) | 0550h | 000h-00Ah |
| DMA Channel 5 (see Table 6-65) | 0560h | 000h-00Ah |
| USCI_A0 (see Table 6-66) | 05C0h | 000h-01Fh |
| USCI_B0 (see Table 6-67) | 05E0h | 000h-01Fh |
| USCI_A1 (see Table 6-68) | 0600h | 000h-01Fh |
| USCI_B1 (see Table 6-69) | 0620h | 000h-01Fh |
| DAC12_A (see Table 6-70) | 0780h | 000h-01Fh |
| Comparator_B (see Table 6-71) | 08C0h | 000h-00Fh |
| USB configuration (see Table 6-72) ⁽²⁾ | 0900h | 000h-014h |
| USB control (see Table 6-73) ⁽²⁾ | 0920h | 000h-01Fh |
| LDO-PWR; LDO and Port U configuration (see Table 6-74) ⁽³⁾ | 0900h | 000h-014h |

(1) For a detailed description of the individual control register offset addresses, see the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)*.

(2) Only on devices with peripheral module USB.

(3) Only on devices with peripheral module LDO-PWR.

Table 6-41. Peripherals (continued)

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE ⁽¹⁾ |
|---|--------------|-------------------------------------|
| LCD_B control (see Table 6-75) | 0A00h | 000h-05Fh |
| CTSD16 (see Table 6-76) | 0A80h | 000h-05Fh |
| OA0 and GSW0 (see Table 6-77) | 0AE0h | 000h-00Fh |
| OA1 and GSW1 (see Table 6-78) | 0AF0h | 000h-00Fh |

Table 6-42. Special Function Registers (Base Address: 0100h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

Table 6-43. PMM Registers (Base Address: 0120h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| PMM Control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| SVS high side control | SVSMHCTL | 04h |
| SVS low side control | SVSMLCTL | 06h |
| PMM interrupt flags | PMMIFG | 0Ch |
| PMM interrupt enable | PMMIE | 0Eh |
| PMM power mode 5 control | PM5CTL0 | 10h |

Table 6-44. Flash Control Registers (Base Address: 0140h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Flash control 1 | FCTL1 | 00h |
| Flash control 3 | FCTL3 | 04h |
| Flash control 4 | FCTL4 | 06h |

Table 6-45. CRC16 Registers (Base Address: 0150h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|-----------|--------|
| CRC data input | CRC16DI | 00h |
| CRC result | CRC16NIRE | 04h |

Table 6-46. RAM Control Registers (Base Address: 0158h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| RAM control 0 | RCCTL0 | 00h |

Table 6-47. Watchdog Registers (Base Address: 015Ch)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL | 00h |

Table 6-48. UCS Registers (Base Address: 0160h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 0 | UCSCTL0 | 00h |
| UCS control 1 | UCSCTL1 | 02h |
| UCS control 2 | UCSCTL2 | 04h |

Table 6-48. UCS Registers (Base Address: 0160h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 3 | UCSCTL3 | 06h |
| UCS control 4 | UCSCTL4 | 08h |
| UCS control 5 | UCSCTL5 | 0Ah |
| UCS control 6 | UCSCTL6 | 0Ch |
| UCS control 7 | UCSCTL7 | 0Eh |
| UCS control 8 | UCSCTL8 | 10h |

Table 6-49. SYS Registers (Base Address: 0180h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------------|-----------|--------|
| System control | SYSCTL | 00h |
| Bootstrap loader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus Error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

Table 6-50. Shared Reference Registers (Base Address: 01B0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Shared reference control | REFCTL | 00h |

**Table 6-51. Port Mapping Registers
(Base Address of Port Mapping Control: 01C0h, Port P2: 01D0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port mapping password register | PMAPPWD | 00h |
| Port mapping control register | PMAPCTL | 02h |
| Port P2.0 mapping register | P2MAP0 | 00h |
| Port P2.1 mapping register | P2MAP1 | 01h |
| Port P2.2 mapping register | P2MAP2 | 02h |
| Port P2.3 mapping register | P2MAP3 | 03h |
| Port P2.4 mapping register | P2MAP4 | 04h |
| Port P2.5 mapping register | P2MAP5 | 05h |
| Port P2.6 mapping register | P2MAP6 | 06h |
| Port P2.7 mapping register | P2MAP7 | 07h |

Table 6-52. Port P1, P2 Registers (Base Address: 0200h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pullup/pulldown enable | P1REN | 06h |
| Port P1 drive strength | P1DS | 08h |

Table 6-52. Port P1, P2 Registers (Base Address: 0200h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P1 selection | P1SEL | 0Ah |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pullup/pulldown enable | P2REN | 07h |
| Port P2 drive strength | P2DS | 09h |
| Port P2 selection | P2SEL | 0Bh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

Table 6-53. Port P3, P4 Registers (Base Address: 0220h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 pullup/pulldown enable | P3REN | 06h |
| Port P3 drive strength | P3DS | 08h |
| Port P3 selection | P3SEL | 0Ah |
| Port P3 interrupt vector word | P3IV | 0Eh |
| Port P3 interrupt edge select | P3IES | 18h |
| Port P3 interrupt enable | P3IE | 1Ah |
| Port P3 interrupt flag | P3IFG | 1Ch |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 pullup/pulldown enable | P4REN | 07h |
| Port P4 drive strength | P4DS | 09h |
| Port P4 selection | P4SEL | 0Bh |
| Port P4 interrupt vector word | P4IV | 1Eh |
| Port P4 interrupt edge select | P4IES | 19h |
| Port P4 interrupt enable | P4IE | 1Bh |
| Port P4 interrupt flag | P4IFG | 1Dh |

Table 6-54. Port P5, P6 Registers (Base Address: 0240h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 pullup/pulldown enable | P5REN | 06h |
| Port P5 drive strength | P5DS | 08h |
| Port P5 selection | P5SEL | 0Ah |

Table 6-54. Port P5, P6 Registers (Base Address: 0240h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P6 input | P6IN | 01h |
| Port P6 output | P6OUT | 03h |
| Port P6 direction | P6DIR | 05h |
| Port P6 pullup/pulldown enable | P6REN | 07h |
| Port P6 drive strength | P6DS | 09h |
| Port P6 selection | P6SEL | 0Bh |

Table 6-55. Port P7, P8 Registers (Base Address: 0260h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P7 input | P7IN | 00h |
| Port P7 output | P7OUT | 02h |
| Port P7 direction | P7DIR | 04h |
| Port P7 pullup/pulldown enable | P7REN | 06h |
| Port P7 drive strength | P7DS | 08h |
| Port P7 selection | P7SEL | 0Ah |
| Port P8 input | P8IN | 01h |
| Port P8 output | P8OUT | 03h |
| Port P8 direction | P8DIR | 05h |
| Port P8 pullup/pulldown enable | P8REN | 07h |
| Port P8 drive strength | P8DS | 09h |
| Port P8 selection | P8SEL | 0Bh |

Table 6-56. Port P9 Register (Base Address: 0280h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P9 input | P9IN | 00h |
| Port P9 output | P9OUT | 02h |
| Port P9 direction | P9DIR | 04h |
| Port P9 pullup/pulldown enable | P9REN | 06h |
| Port P9 drive strength | P9DS | 08h |
| Port P9 selection | P9SEL | 0Ah |

Table 6-57. Port J Registers (Base Address: 0320h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ pullup/pulldown enable | PJREN | 06h |
| Port PJ drive strength | PJDS | 08h |

Table 6-58. TA0 Registers (Base Address: 0340h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA0 control | TAOCTL | 00h |
| Capture/compare control 0 | TAOCTL0 | 02h |
| Capture/compare control 1 | TAOCTL1 | 04h |
| Capture/compare control 2 | TAOCTL2 | 06h |
| Capture/compare control 3 | TAOCTL3 | 08h |

Table 6-58. TA0 Registers (Base Address: 0340h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| Capture/compare control 4 | TAOCTL4 | 0Ah |
| TA0 counter register | TAOR | 10h |
| Capture/compare register 0 | TAOCCR0 | 12h |
| Capture/compare register 1 | TAOCCR1 | 14h |
| Capture/compare register 2 | TAOCCR2 | 16h |
| Capture/compare register 3 | TAOCCR3 | 18h |
| Capture/compare register 4 | TAOCCR4 | 1Ah |
| TA0 expansion register 0 | TAOEX0 | 20h |
| TA0 interrupt vector | TAOIV | 2Eh |

Table 6-59. TA1 Registers (Base Address: 0380h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CTL0 | 02h |
| Capture/compare control 1 | TA1CTL1 | 04h |
| Capture/compare control 2 | TA1CTL2 | 06h |
| TA1 counter register | TA1R | 10h |
| Capture/compare register 0 | TA1CCR0 | 12h |
| Capture/compare register 1 | TA1CCR1 | 14h |
| Capture/compare register 2 | TA1CCR2 | 16h |
| TA1 expansion register 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

Table 6-60. TB0 Registers (Base Address: 03C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TB0 control | TB0CTL | 00h |
| Capture/compare control 0 | TB0CTL0 | 02h |
| Capture/compare control 1 | TB0CTL1 | 04h |
| Capture/compare control 2 | TB0CTL2 | 06h |
| Capture/compare control 3 | TB0CTL3 | 08h |
| Capture/compare control 4 | TB0CTL4 | 0Ah |
| Capture/compare control 5 | TB0CTL5 | 0Ch |
| Capture/compare control 6 | TB0CTL6 | 0Eh |
| TB0 register | TBOR | 10h |
| Capture/compare register 0 | TB0CCR0 | 12h |
| Capture/compare register 1 | TB0CCR1 | 14h |
| Capture/compare register 2 | TB0CCR2 | 16h |
| Capture/compare register 3 | TB0CCR3 | 18h |
| Capture/compare register 4 | TB0CCR4 | 1Ah |
| Capture/compare register 5 | TB0CCR5 | 1Ch |
| Capture/compare register 6 | TB0CCR6 | 1Eh |
| TB0 expansion register 0 | TB0EX0 | 20h |
| TB0 interrupt vector | TB0IV | 2Eh |

Table 6-61. TA2 Registers (Base Address: 0400h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA2 control | TA2CTL | 00h |
| Capture/compare control 0 | TA2CCTL0 | 02h |
| Capture/compare control 1 | TA2CCTL1 | 04h |
| Capture/compare control 2 | TA2CCTL2 | 06h |
| TA2 counter register | TA2R | 10h |
| Capture/compare register 0 | TA2CCR0 | 12h |
| Capture/compare register 1 | TA2CCR1 | 14h |
| Capture/compare register 2 | TA2CCR2 | 16h |
| TA2 expansion register 0 | TA2EX0 | 20h |
| TA2 interrupt vector | TA2IV | 2Eh |

Table 6-62. Battery Backup Registers (Base Address: 0480h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Battery Backup Memory 0 | BAKMEM0 | 00h |
| Battery Backup Memory 1 | BAKMEM1 | 02h |
| Battery Backup Memory 2 | BAKMEM2 | 04h |
| Battery Backup Memory 3 | BAKMEM3 | 06h |
| Battery Backup Control | BAKCTL | 1Ch |
| Battery Charger Control | BAKCHCTL | 1Eh |

Table 6-63. Real-Time Clock Registers (Base Address: 04A0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------------------|-----------|--------|
| RTC control register 0 | RTCCTL0 | 00h |
| RTC control register 1 | RTCCTL1 | 01h |
| RTC control register 2 | RTCCTL2 | 02h |
| RTC control register 3 | RTCCTL3 | 03h |
| RTC prescaler 0 control register | RTCPS0CTL | 08h |
| RTC prescaler 1 control register | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds | RTCSEC | 10h |
| RTC minutes | RTCMIN | 11h |
| RTC hours | RTCHOUR | 12h |
| RTC day of week | RTCDOW | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year low | RTCYEARL | 16h |
| RTC year high | RTCYEARH | 17h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |
| Binary-to-BCD conversion register | BIN2BCD | 1Ch |
| BCD-to-binary conversion register | BCD2BIN | 1Eh |

Table 6-64. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|-----------|--------|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension register | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control register 0 | MPY32CTL0 | 2Ch |

Table 6-65. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h, DMA Channel 3: 0540h, DMA Channel 4: 0550h, DMA Channel 5: 0560h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|----------|--------|
| DMA General Control: DMA module control 0 | DMACTL0 | 00h |
| DMA General Control: DMA module control 1 | DMACTL1 | 02h |
| DMA General Control: DMA module control 2 | DMACTL2 | 04h |
| DMA General Control: DMA module control 3 | DMACTL3 | 06h |
| DMA General Control: DMA module control 4 | DMACTL4 | 08h |
| DMA General Control: DMA interrupt vector | DMAIV | 0Ah |
| DMA Channel 0 control | DMA0CTL | 00h |
| DMA Channel 0 source address low | DMA0SAL | 02h |
| DMA Channel 0 source address high | DMA0SAH | 04h |
| DMA Channel 0 destination address low | DMA0DAL | 06h |
| DMA Channel 0 destination address high | DMA0DAH | 08h |
| DMA Channel 0 transfer size | DMA0SZ | 0Ah |
| DMA Channel 1 control | DMA1CTL | 00h |
| DMA Channel 1 source address low | DMA1SAL | 02h |
| DMA Channel 1 source address high | DMA1SAH | 04h |
| DMA Channel 1 destination address low | DMA1DAL | 06h |
| DMA Channel 1 destination address high | DMA1DAH | 08h |
| DMA Channel 1 transfer size | DMA1SZ | 0Ah |
| DMA Channel 2 control | DMA2CTL | 00h |

Table 6-65. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h, DMA Channel 3: 0540h, DMA Channel 4: 0550h, DMA Channel 5: 0560h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA Channel 2 source address low | DMA2SAL | 02h |
| DMA Channel 2 source address high | DMA2SAH | 04h |
| DMA Channel 2 destination address low | DMA2DAL | 06h |
| DMA Channel 2 destination address high | DMA2DAH | 08h |
| DMA Channel 2 transfer size | DMA2SZ | 0Ah |
| DMA Channel 3 control | DMA3CTL | 00h |
| DMA Channel 3 source address low | DMA3SAL | 02h |
| DMA Channel 3 source address high | DMA3SAH | 04h |
| DMA Channel 3 destination address low | DMA3DAL | 06h |
| DMA Channel 3 destination address high | DMA3DAH | 08h |
| DMA Channel 3 transfer size | DMA3SZ | 0Ah |
| DMA Channel 4 control | DMA4CTL | 00h |
| DMA Channel 4 source address low | DMA4SAL | 02h |
| DMA Channel 4 source address high | DMA4SAH | 04h |
| DMA Channel 4 destination address low | DMA4DAL | 06h |
| DMA Channel 4 destination address high | DMA4DAH | 08h |
| DMA Channel 4 transfer size | DMA4SZ | 0Ah |
| DMA Channel 5 control | DMA5CTL | 00h |
| DMA Channel 5 source address low | DMA5SAL | 02h |
| DMA Channel 5 source address high | DMA5SAH | 04h |
| DMA Channel 5 destination address low | DMA5DAL | 06h |
| DMA Channel 5 destination address high | DMA5DAH | 08h |
| DMA Channel 5 transfer size | DMA5SZ | 0Ah |

Table 6-66. USCI_A0 Registers (Base Address: 05C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|------------|--------|
| USCI control 0 | UCA0CTL0 | 00h |
| USCI control 1 | UCA0CTL1 | 01h |
| USCI baud rate 0 | UCA0BR0 | 06h |
| USCI baud rate 1 | UCA0BR1 | 07h |
| USCI modulation control | UCA0MCTL | 08h |
| USCI status | UCA0STAT | 0Ah |
| USCI receive buffer | UCA0RXBUF | 0Ch |
| USCI transmit buffer | UCA0TXBUF | 0Eh |
| USCI LIN control | UCA0ABCTL | 10h |
| USCI IrDA transmit control | UCA0IRTCTL | 12h |
| USCI IrDA receive control | UCA0IRRCTL | 13h |
| USCI interrupt enable | UCA0IE | 1Ch |
| USCI interrupt flags | UCA0IFG | 1Dh |
| USCI interrupt vector word | UCA0IV | 1Eh |

Table 6-67. USCI_B0 Registers (Base Address: 05E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| USCI synchronous control 0 | UCB0CTL0 | 00h |
| USCI synchronous control 1 | UCB0CTL1 | 01h |

Table 6-67. USCI_B0 Registers (Base Address: 05E0h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous bit rate 0 | UCB0BR0 | 06h |
| USCI synchronous bit rate 1 | UCB0BR1 | 07h |
| USCI synchronous status | UCB0STAT | 0Ah |
| USCI synchronous receive buffer | UCB0RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB0TXBUF | 0Eh |
| USCI I2C own address | UCB0I2COA | 10h |
| USCI I2C slave address | UCB0I2CSA | 12h |
| USCI interrupt enable | UCB0IE | 1Ch |
| USCI interrupt flags | UCB0IFG | 1Dh |
| USCI interrupt vector word | UCB0IV | 1Eh |

Table 6-68. USCI_A1 Registers (Base Address: 0600h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|------------|--------|
| USCI control 0 | UCA1CTL0 | 00h |
| USCI control 1 | UCA1CTL1 | 01h |
| USCI baud rate 0 | UCA1BR0 | 06h |
| USCI baud rate 1 | UCA1BR1 | 07h |
| USCI modulation control | UCA1MCTL | 08h |
| USCI status | UCA1STAT | 0Ah |
| USCI receive buffer | UCA1RXBUF | 0Ch |
| USCI transmit buffer | UCA1TXBUF | 0Eh |
| USCI LIN control | UCA1ABCTL | 10h |
| USCI IrDA transmit control | UCA1IRTCTL | 12h |
| USCI IrDA receive control | UCA1IRRCTL | 13h |
| USCI interrupt enable | UCA1IE | 1Ch |
| USCI interrupt flags | UCA1IFG | 1Dh |
| USCI interrupt vector word | UCA1IV | 1Eh |

Table 6-69. USCI_B1 Registers (Base Address: 0620h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 0 | UCB1CTL0 | 00h |
| USCI synchronous control 1 | UCB1CTL1 | 01h |
| USCI synchronous bit rate 0 | UCB1BR0 | 06h |
| USCI synchronous bit rate 1 | UCB1BR1 | 07h |
| USCI synchronous status | UCB1STAT | 0Ah |
| USCI synchronous receive buffer | UCB1RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB1TXBUF | 0Eh |
| USCI I2C own address | UCB1I2COA | 10h |
| USCI I2C slave address | UCB1I2CSA | 12h |
| USCI interrupt enable | UCB1IE | 1Ch |
| USCI interrupt flags | UCB1IFG | 1Dh |
| USCI interrupt vector word | UCB1IV | 1Eh |

Table 6-70. DAC12_A Registers (Base Address: 0780h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|---------------|--------|
| DAC12_A channel 0 control register 0 | DAC12_OCTL0 | 00h |
| DAC12_A channel 0 control register 1 | DAC12_OCTL1 | 02h |
| DAC12_A channel 0 data register | DAC12_ODAT | 04h |
| DAC12_A channel 0 calibration control register | DAC12_0CALCTL | 06h |
| DAC12_A channel 0 calibration data register | DAC12_0CALDAT | 08h |
| DAC12_A channel 1 control register 0 | DAC12_1CTL0 | 10h |
| DAC12_A channel 1 control register 1 | DAC12_1CTL1 | 12h |
| DAC12_A channel 1 data register | DAC12_1DAT | 14h |
| DAC12_A channel 1 calibration control register | DAC12_1CALCTL | 16h |
| DAC12_A channel 1 calibration data register | DAC12_1CALDAT | 18h |
| DAC12_A interrupt vector word | DAC12IV | 1Eh |

Table 6-71. Comparator_B Registers (Base Address: 08C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------|----------|--------|
| Comp_B control register 0 | CBCTL0 | 00h |
| Comp_B control register 1 | CBCTL1 | 02h |
| Comp_B control register 2 | CBCTL2 | 04h |
| Comp_B control register 3 | CBCTL3 | 06h |
| Comp_B interrupt register | CBINT | 0Ch |
| Comp_B interrupt vector word | CBIV | 0Eh |

Table 6-72. USB Configuration Registers (Base Address: 0900h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|-----------|--------|
| USB key/ID | USBKEYID | 00h |
| USB module configuration | USBCNF | 02h |
| USB PHY control | USBPHYCTL | 04h |
| USB power control | USBPWRCTL | 08h |
| USB power voltage setting | USBPWRVSR | 0Ah |
| USB PLL control | USBPLLCTL | 10h |
| USB PLL divider | USBPLLDIV | 12h |
| USB PLL interrupts | USBPLLIR | 14h |

Table 6-73. USB Control Registers (Base Address: 0920h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------------------|--------------|--------|
| Input endpoint_0 configuration | USBIEPCNF_0 | 00h |
| Input endpoint_0 byte count | USBIEPBCNT_0 | 01h |
| Output endpoint_0 configuration | USBOEPCNFG_0 | 02h |
| Output endpoint_0 byte count | USBOEPBCNT_0 | 03h |
| Input endpoint interrupt enables | USBIEPIE | 0Eh |
| Output endpoint interrupt enables | USBOEPIE | 0Fh |
| Input endpoint interrupt flags | USBIEPIFG | 10h |
| Output endpoint interrupt flags | USBOEPIFG | 11h |
| USB interrupt vector | USBIV | 12h |
| USB maintenance | USBMAINT | 16h |
| Time stamp | USBTSREG | 18h |
| USB frame number | USBFN | 1Ah |

Table 6-73. USB Control Registers (Base Address: 0920h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|-----------|--------|
| USB control | USBCTL | 1Ch |
| USB interrupt enables | USBIE | 1Dh |
| USB interrupt flags | USBIFG | 1Eh |
| Function address | USBFUNADR | 1Fh |

Table 6-74. LDO and Port U Configuration Registers (Base Address: 0900h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|-----------|--------|
| LDO key and ID register | LDOKEYPID | 00h |
| PU port control | PUCTL | 04h |
| LDO power control | LDOPWRCTL | 08h |

Table 6-75. LCD_B Registers (Base Address: 0A00h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|------------|--------|
| LCD_B control register 0 | LCDBCTL0 | 000h |
| LCD_B control register 1 | LCDBCTL1 | 002h |
| LCD_B blinking control register | LCDBBLKCTL | 004h |
| LCD_B memory control register | LCDBMEMCTL | 006h |
| LCD_B voltage control register | LCDBVCTL | 008h |
| LCD_B port control register 0 | LCDBPCTL0 | 00Ah |
| LCD_B port control register 1 | LCDBPCTL1 | 00Ch |
| LCD_B port control register 2 | LCDBPCTL2 | 00Eh |
| LCD_B charge pump control register | LCDBCTL0 | 012h |
| LCD_B interrupt vector word | LCDBIV | 01Eh |
| LCD_B memory 1 | LCDM1 | 020h |
| LCD_B memory 2 | LCDM2 | 021h |
| ⋮ | ⋮ | ⋮ |
| LCD_B memory 22 | LCDM22 | 035h |
| LCD_B blinking memory 1 | LCDBM1 | 040h |
| LCD_B blinking memory 2 | LCDBM2 | 041h |
| ⋮ | ⋮ | ⋮ |
| LCD_B blinking memory 22 | LCDBM22 | 055h |

Table 6-76. CTSD16 Registers (Base Address: 0A80h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|--------------|--------|
| CTSD16 Control | CTSD16CTL | 00h |
| CTSD16 Channel 0 Control | CTSD16CCTL0 | 02h |
| CTSD16 Channel 0 Input Control | CTSD16INCTL0 | 04h |
| CTSD16 Channel 0 Preload | CTSD16PRE0 | 06h |
| CTSD16 Interrupt Flag Register | CTSD16IFG | 2Ch |
| CTSD16 Interrupt Enable Register | CTSD16IE | 2Eh |
| CTSD16 Interrupt Vector | CTSD16IV | 30h |
| CTSD16 Channel 0 Conversion Memory | CTSD16MEM0 | 32h |

Table 6-77. OA0 Registers (Base Address: 0AE0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------------|----------|--------|
| OA0 Control 0 register | OA0CTL0 | 00h |
| OA0 Positive Input Terminal Switches | OA0PSW | 02h |
| OA0 Negative Input Terminal Switches | OA0NSW | 04h |
| OA0 Ground Switches | OA0GSW | 0Eh |

Table 6-78. OA1 Registers (Base Address: 0AF0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------------|----------|--------|
| OA1 Control 0 register | OA1CTL0 | 00h |
| OA1 Positive Input Terminal Switches | OA1PSW | 02h |
| OA1 Negative Input Terminal Switches | OA1NSW | 04h |
| OA1 Ground Switches | OA1GSW | 0Eh |

6.15 Identification

6.15.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see [Section 8.2](#).

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in [Section 6.13](#).

6.15.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see [Section 8.2](#).

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in [Section 6.13](#).

6.15.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the *MSP430 Programming Via the JTAG Interface User's Guide* ([SLAU320](#)).

7 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 1- μF plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, separated grounds with a single-point connection are recommended for better noise isolation from digital to analog circuits on the board and are especially recommended to achieve high analog accuracy.

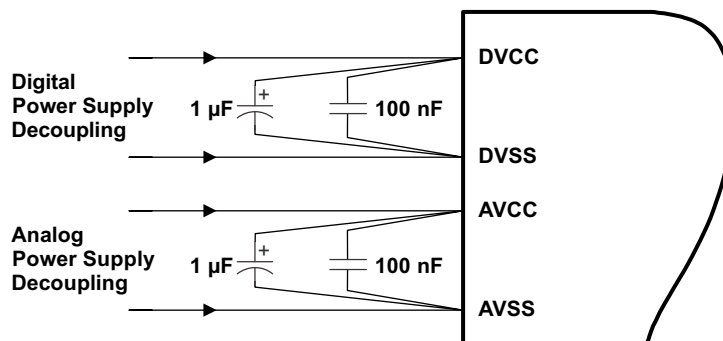


Figure 7-1. Power Supply Decoupling

7.1.2 External Oscillator

Depending on the device variant (see [Section 3](#)), the device can support a low-frequency crystal (32 kHz) on the XT1 pins, a high-frequency crystal on the XT2 pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the XIN and XT2IN input pins that meet the specifications of the respective oscillator if the appropriate XT1BYPASS or XT2BYPASS mode is selected. In this case, the associated XOUT and XT2OUT pins can be used for other purposes. If they are left unused, they must be terminated according to [Table 4-4](#).

[Figure 7-2](#) shows a typical connection diagram.

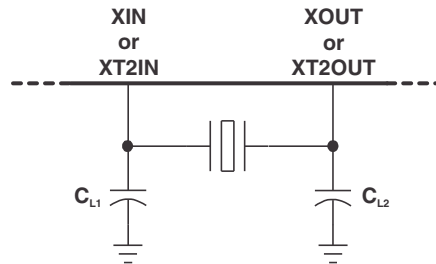


Figure 7-2. Typical Crystal Connection

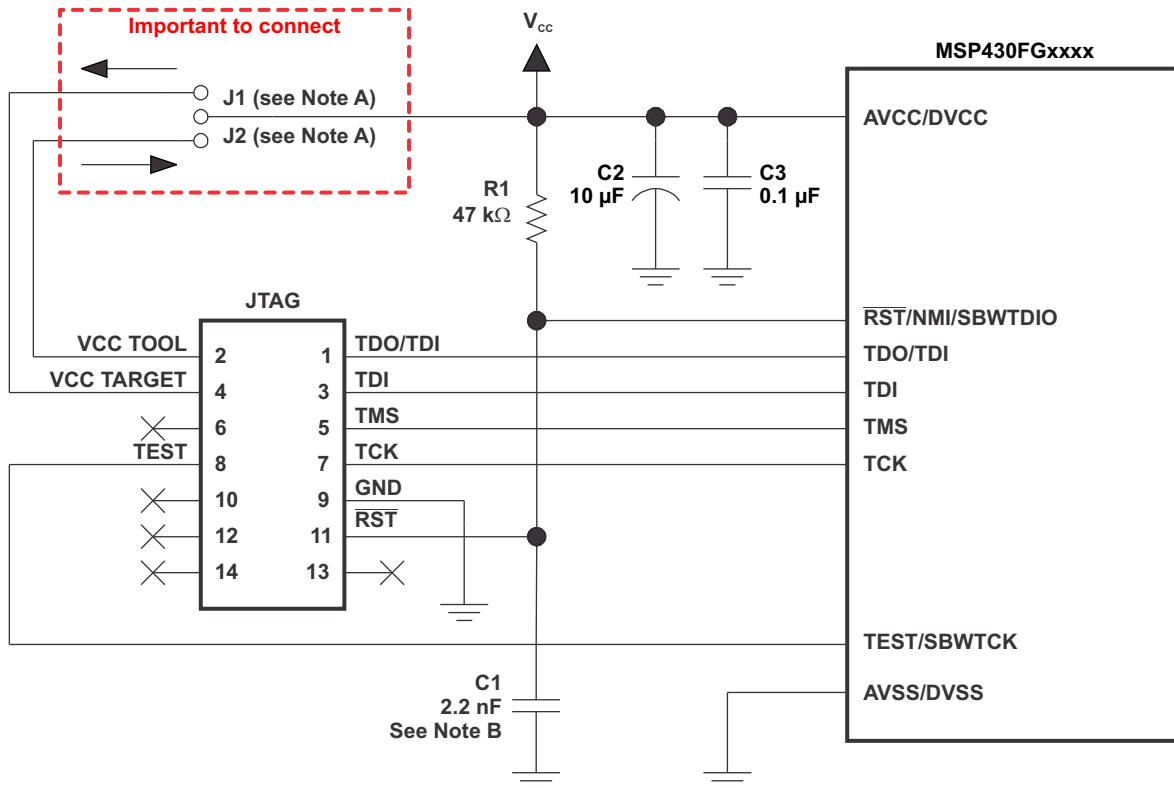
See the application report *MSP430 32-kHz Crystal Oscillators* ([SLAA322](#)) for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. [Figure 7-3](#) shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. [Figure 7-4](#) shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

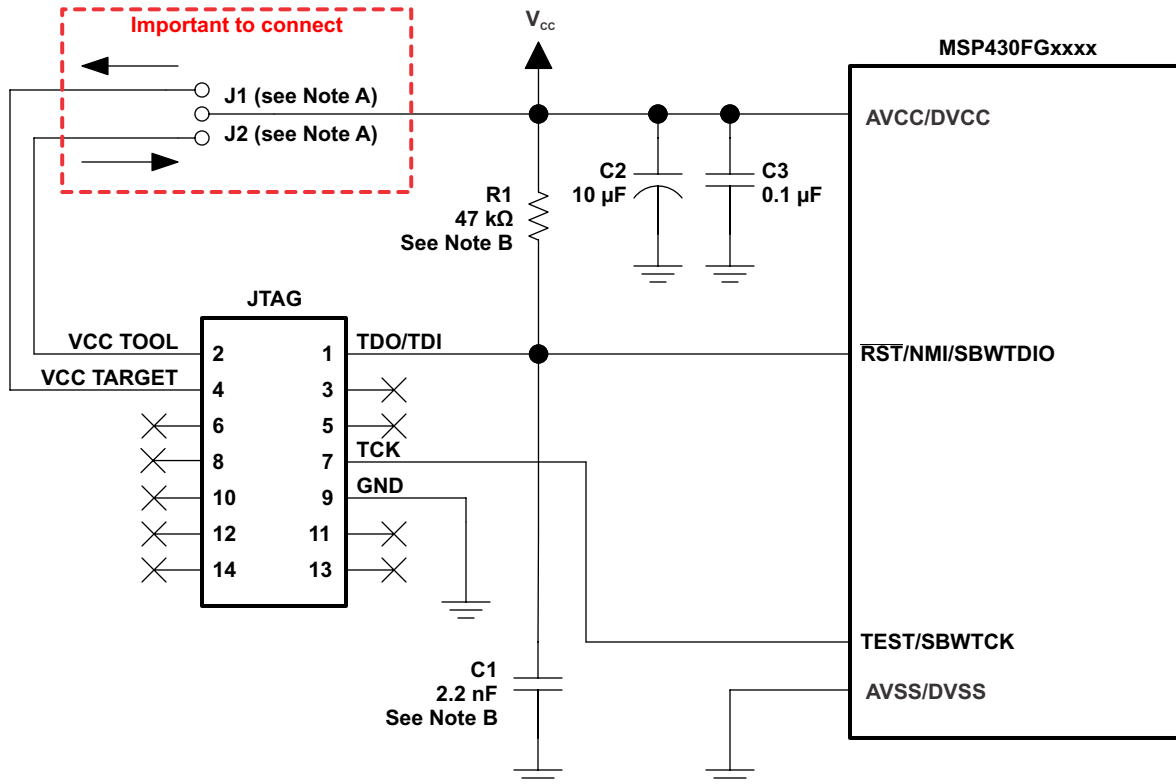
The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply VCC to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a VCC sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature senses the local VCC present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. [Figure 7-3](#) and [Figure 7-4](#) show a jumper block that supports both scenarios of supplying VCC to the target board. If this flexibility is not required, the desired VCC connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide* ([SLAU278](#)).



- A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
- B. The upper limit for C1 is 2.2 nF when using current TI tools.

Figure 7-3. Signal Connections for 4-Wire JTAG Communication



- Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.
- The device $\overline{\text{RST}}/\text{NMI}/\text{SBWTIO}$ pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2 nF when using current TI tools.

Figure 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the $\overline{\text{RST}}/\text{NMI}$ pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}/\text{NMI}$ pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}/\text{NMI}$ pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}/\text{NMI}$ pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-k Ω pullup resistor to the $\overline{\text{RST}}/\text{NMI}$ pin with a 2.2-nF pulldown capacitor. The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the device family user's guide ([SLAU208](#)) for more information on the referenced control registers and bits.

7.1.5 Unused Pins

For details on the connection of unused pins, see [Section 4.5](#).

7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See the application report *MSP430 32-kHz Crystal Oscillators* ([SLAA322](#)) for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Refer to the *Circuit Board Layout Techniques* design guide ([SLOA089](#)) for a detailed discussion of PCB layout considerations. This document is written primarily about op amps, but the guidelines are generally applicable for all mixed-signal applications.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See the application report *MSP430 System-Level ESD Considerations* ([SLAA530](#)) for guidelines.

7.1.7 Do's and Don'ts

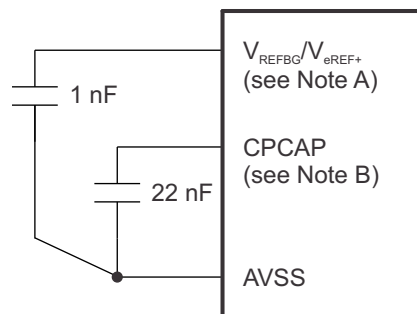
TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in [Section 5.1, Absolute Maximum Ratings](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and flash.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 CTSD16 Peripheral

For internal connections between signal chain modules such as CTSD16, OA, and DAC12, see [Section 6.12.16](#). When internal connections are available, they should be chosen over external connections to reduce noise and save pins.

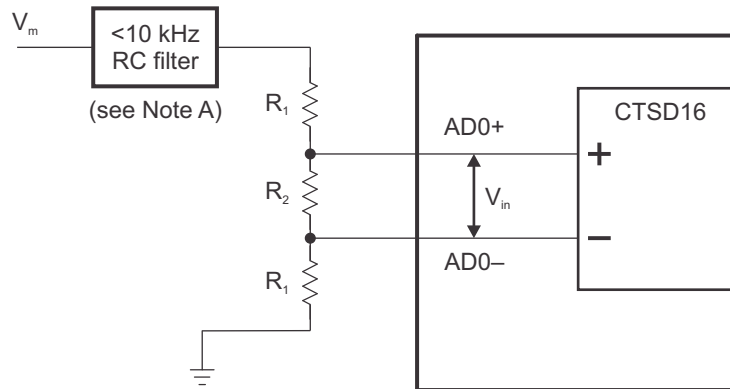
Solid decoupling on both the digital and analog supply are also required (best with two capacitors, one 10 μF and one 100 nF, as shown in [Section 7.1.1](#)).



- The capacitor reduces noise when using internal V_{REFBG} setting. This pin is also used for the external reference input for the CTSD16 or DAC, and when doing so the capacitor is not needed. Because of the shared signal path and pin, the internal and external references (V_{REFBG} and $V_{\text{eREF+}}$, respectively) cannot be used at the same time.
- The capacitor on CPCAP is required when the charge pump is enabled. The charge pump can be enabled by rail-to-rail operation of the CTSD16 or by the OA module. See the register settings for each module in the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)) for enabling this operation.

Figure 7-5. CTSD16 Partial Schematic

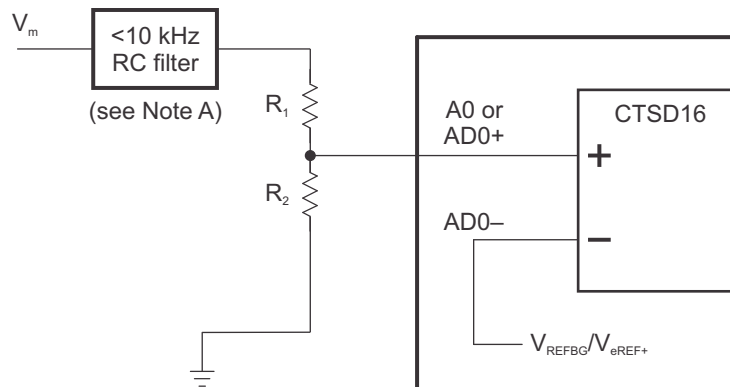
7.2.1.1 Example Measurement Schematic – Differential Input



- A. TI recommends an external RC antialiasing low-pass filter for the CTSD16 to prevent aliasing of the input signal. The cutoff frequency should be <10 kHz for a 1-MHz modulator clock and OSR = 256. The cutoff frequency may be set to a lower frequency for applications that have lower bandwidth requirements. It is up to the user to determine the configuration and type of low-pass filter used.

Figure 7-6. CTSD16 Measurement Schematic – Differential Input

7.2.1.2 Example Measurement Schematic – Single-Ended Input



- A. TI recommends an external RC antialiasing low-pass filter for the CTSD16 to prevent aliasing of the input signal. The cutoff frequency should be <10 kHz for a 1-MHz modulator clock and OSR = 256. The cutoff frequency may be set to a lower frequency for applications that have lower bandwidth requirements. It is up to the user to determine the configuration and type of low-pass filter used.

Figure 7-7. CTSD16 Measurement Schematic – Single-Ended Input

7.2.1.3 Design Requirements

As with any high-resolution ADC, appropriate printed circuit board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. Therefore, solid decoupling on both the digital and analog supply is required (best with two capacitors, one 10 μ F and one 100 nF, as shown in [Section 7.1.1](#)).

In addition to grounding, ripple and noise spikes on the power-supply lines due to digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

If the internal reference is used, the reference voltage should be buffered externally by connecting a small (approximately 1 nF) capacitor to the VREFBG pin to reduce the noise on the reference.

The CTSD16 has a fixed 1.024-MHz clock (f_M). Fault flags for this oscillator are described in the CTSD16 and UCS section of the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)).

Rail-to-rail operation mode is available when the OA module is used to buffer the CTSD16 inputs. For more information, see the CTSD16 and the OA modules in the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)).

7.2.1.4 Detailed Design Procedure

7.2.1.4.1 OSR and Sampling Frequency

A simple equation guides the relationship between effective sampling frequency and oversampling ratio (OSR) for CTSD16.

$$f_s = \frac{f_m}{\text{OSR}} \quad (1)$$

Where

- f_s = effective sampling frequency
- f_m = modulation frequency

For the CTSD16, the modulation frequency is set to 1.024 MHz. Using [Equation 1](#) with an example OSR of 256, the effective sampling frequency would be 4 kHz. The OSR value also affects the number of bits in the digital filter output. See the CTSD16 chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)) for additional information and available OSR values.

7.2.1.4.2 Differential Input Range Explanation

The following equations can give guidance on the input range for the CTSD16 while using an external reference. Keep in mind the absolute bounds of an external reference as mentioned in the specifications section of this module. The external and internal references cannot be used at the same time, because they share the same signal path and pin. For internal reference ranges, see [Section 5.5.11](#).

$$V_{\text{FSR}+} = \frac{+V_R}{\text{GAIN}} \quad (2)$$

$$V_{\text{FSR}-} = \frac{-V_R}{\text{GAIN}} \quad (3)$$

$$\text{Full-Scale Range} = V_{\text{FSR}+} - V_{\text{FSR}-} = 2 \times \frac{V_R}{\text{GAIN}} \quad (4)$$

$$V_{\text{ID}} = 0.8 V_{\text{FSR}-} \text{ to } 0.8 V_{\text{FSR}+}, \text{ with externally sourced } V_R \quad (5)$$

Where

- V_{FSR} is the full-scale range voltage
- V_{ID} is the differential input voltage
- V_R is the reference voltage

The differential input voltage range with internal voltage reference at different GAIN settings is given in [Section 5.5.11](#). Using [Equation 2](#) through [Equation 5](#), determine the absolute maximum differential input ranges for the CTSD16 with a given external voltage reference. [Equation 6](#) corresponds to the example circuit in [Figure 7-6](#) and can be used after a range is chosen to limit differential input voltage to acceptable levels by solving for the external resistors R1 and R2.

$$V_{in} = V_m \times \frac{R_2}{R_2 + 2R_1} \times \frac{1}{1 + \frac{R_{eff}}{2R_{in}}} \quad (6)$$

Where

- $R_{eff} = (R_2 \times 2R_1) / (R_2 + 2R_1)$
- V_{in} is the differential voltage input to CTSD16
- V_m is the voltage to measure
- R_{in} is the internal resistance of the CTSD16 (see [Section 5.5.11](#))

7.2.1.4.3 Single-Ended Input Mode

The CTSD16 has six single-ended analog inputs and four differential inputs that can be placed in single-ended mode by the CTSDINCHx bits in the CTSD16INCTLx registers. These single-ended modes use the fully differential path of the CTSD16 by internally tying the negative input to the V_{REFBG}/V_{eREF+} signal. This means for the differential inputs in single-ended mode, the external pin normally tied to the negative input can be used for its alternate functions. [Equation 7](#) through [Equation 10](#) apply for full-scale range while in single-ended mode.

$$V_{FSR+} = V_R + \frac{V_R}{GAIN} \quad (7)$$

$$V_{FSR-} = V_R - \frac{V_R}{GAIN} \quad (8)$$

$$\text{Full-Scale Range} = V_{FSR+} - V_{FSR-} = \left(V_R + \frac{V_R}{GAIN} \right) - \left(V_R - \frac{V_R}{GAIN} \right) = 2 \times \frac{V_R}{GAIN} \quad (9)$$

$$V_I = V_R - 0.8 \times \left(\frac{V_R}{GAIN} \right) \text{ to } V_R + 0.8 \times \left(\frac{V_R}{GAIN} \right) \quad (10)$$

Where

- V_{FSR} is the full-scale range voltage
- V_I is the single-ended input voltage range for data-sheet specified performance
- V_R is the reference voltage

To ensure the measured voltage is within the single-ended voltage range, a simple voltage divider circuit can be used to condition the desired input signal. In single-ended mode, additional error may be introduced by noise when compared to a fully differential measurement. [Equation 11](#) corresponds to the example circuit in [Figure 7-7](#) and can be used after a range is chosen to limit differential input voltage to acceptable levels by solving for the external resistors R1 and R2.

$$V_{in} = V_m \times \frac{R_2}{R_1 + R_2} \quad (11)$$

Where

- V_{in} is the single-ended voltage input to CTSD16
- V_m is the voltage to measure

7.2.1.4.4 Offset Calibration

In some applications, it is necessary to calibrate the module for offset error. This module allows an easy way to do this by providing internal connections from input to VREF or DAC0. To short AD4+ and AD4- to VREF or DAC0, change the CTSD16INCHx setting for each channel to 0x11 for VREF and 0x12 for DAC0. This allows calibration of the CTSD16 input stage by what is measured from the ideal value. The total signal chain offset depends on the impedance of the external circuitry; thus, the actual offset seen at any of the analog inputs may be different.

7.2.1.5 Layout Guidelines

Components that are shown in the partial schematic (see [Figure 7-5](#)) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

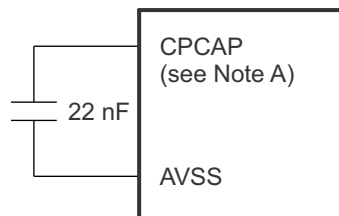
The analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

7.2.2 Operational Amplifier With Ground Switches Peripheral

For internal connections between signal chain modules such as CTSD16, OA, and DAC12, see [Section 6.12.16](#). When internal connections are available, they should be chosen over external connections to reduce noise and save pins.

Solid decoupling on both the digital and analog supply are also required (best with two capacitors, one 10 μ F and one 100 nF, as shown in [Section 7.1.1](#)).

7.2.2.1 Reference Schematic



- A. The capacitor on CPCAP is required when the charge pump is enabled. The charge pump can be enabled by rail-to-rail operation of the PGA buffers of the CTSD16 or by the OA module. See the register settings for each module in the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)) for enabling this operation.

Figure 7-8. RTC_B with Battery Backup Partial Schematic

7.2.2.2 Design Requirements

As with any analog signals, appropriate printed circuit board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

In addition to grounding, ripple and noise spikes on the power-supply lines due to digital switching or switching power supplies can corrupt the signal. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy. For more information about noise and its effects on op amps, see *Noise Analysis in Operational Amplifiers* ([SLVA043](#)).

Rail-to-rail operation mode is available with the OA module at the cost of increased current. This should be used when OA input is near the AVCC rail. Refer to the V_{CM} specification (see [Section 5.5.14](#)) to see if rail-to-rail operation is required for your application. For more information, see the OA chapter of the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)).

Ground switches are also available for use. See [Section 6.12.16](#) for connections. These ground switches provide a low ohmic connection to ground to both internal connections and to the external pin. When a ground switch is active, the Digital I/O logic for the corresponding pin is ignored.

7.2.2.3 Detailed Design Procedure

Operational amplifiers are a diverse and useful tool in many applications. Some common configurations that might prove to be useful to the user are transimpedance amplifiers to convert currents to voltage, voltage-gain amplifiers, and buffering configurations. For more information about how to design these circuits along with other common configurations, see the following application notes.

- *Op Amps for Everyone Design Guide* ([SLOD006](#))
- *Handbook of Operational Amplifier Applications* ([SBOA092](#))
- *Understanding Basic Analog – Ideal Op Amps* ([SLAA068](#))
- *An Applications Guide for Op Amps* ([SNOA621](#))

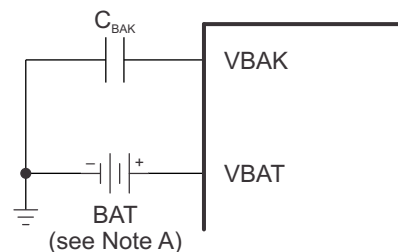
7.2.2.4 Layout Guidelines

Components that are shown in the partial schematic (see [Figure 7-8](#)) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal. Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal. When possible, use internal connections to other modules to limit the potential of error introduction.

7.2.3 RTC_B With Battery Backup System

If not using a separate battery backup supply in the system, see [Section 4.5](#) for VBAT and VBAK connections.

7.2.3.1 Partial Schematic



- A. BAT can be a battery or super-capacitor. See [Section 5.5.8](#) for specifications.

Figure 7-9. OA Partial Schematic

7.2.3.2 Retaining an Accurate Real-Time Clock (RTC) Through Main Supply Interrupts

The RTC_B module with Battery Backup System is designed to keep an accurate RTC during main supply interruptions and during low-power modes. For more details on when the Backup Battery System engages, see the Battery Backup System chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)). See *Using the MSP430 RTC_B Module With Battery Backup Supply* ([SLAA665](#)) for more information and example code on how to keep an accurate RTC through power loss.

7.2.3.3 Charging Super-Capacitors With Built-In Resistive Charger

In applications that use a super-capacitor instead of a battery for secondary supply, the charging circuit functionality of the Battery Backup System can be used to charge the super-capacitor. The resistive charger circuit connects VBAT to DVCC with selectable resistor values found in [Section 5.5.8](#). This means that if DVCC is not present, you cannot use this feature to charge a super-capacitor connected to VBAT. The CTSD16 module can be used to sense the voltage level on VBAT divided by a factor of three. Typical values during VBAT sensing are listed in [Section 5.5.8](#). Channel A8 of the CTSD16 is routed internally for this. See the CTSD16 chapter of the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)) for more information. The BAKADC bit in the BAKCTL register must also be enabled for this feature to

operate. Additionally, RTC interrupts can be used to wake up from LPMx.5 states to charge the super-capacitor. While in an LPMx.5 state, the super-capacitor on VBAT drains. This means that the "wake up to charge" interrupt interval must be designed so that charging starts before the leftover charge in the super-capacitor is too small to accommodate the worst-case backup time if the system were to suddenly lose power. To estimate this time, use [Equation 12](#) for capacitor discharge in an RC circuit.

$$V(t) = V_0 e^{-\frac{t}{RC}} \quad (12)$$

Where

- V_0 = initial voltage of capacitor
- t = time
- R = circuit resistance
- C = capacitance

Because the operational current is given for when RTC is operating within the specifications section, R can be replaced with $V_0/I_{LPM3.5}$ by Ohm's Law. By setting $V(t)$ to the minimum voltage for RTC operation while in backup supply, V_0 as voltage of capacitor when fully charged, and C as the super-capacitor capacitance, the estimated RTC operation time can be calculated. If periodic wakeups from LPM3.5 are not desirable for a given application, external means of charging the super-capacitor must be implemented by the user.

For a detailed list of when the secondary supply VBAT powers the backup-supplied subsystem, see the Battery Backup System chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)).

7.2.4 LCD_B Peripheral

7.2.4.1 Partial Schematic

Required LCD connections greatly vary by the type of display that is used (static or multiplexed), whether external or internal biasing is used, and also whether the on-chip charge pump is employed. For any display used, there is flexibility as to how the segment (Sx) and common (COMx) signals are connected to the MCU which (assuming that the correct choices are made) can be advantageous for the PCB layout and for the design of the application software.

Because LCD connections are application specific, it is difficult to provide a single one-fits-all schematic. However for an example of a schematic using the LCD_B module with an MSP430F6638, see the TI Design *Flow Meter host MCU board with segment LCD and prepayment or dual RF option* ([TIDM-FLOWMETER_DUALRF](#)).

7.2.4.2 Design Requirements

Due to the flexibility of the LCD_B peripheral module to accommodate various segment-based LCDs, selecting the right display for the application in combination with determining specific design requirements is often an iterative process. There can be well-defined requirements in terms of how many individually addressable LCD segments need to be controlled, what the requirements for LCD contrast are, which device pins are available for LCD use and which are required by other application functions, and what the power budget is, to name just a few. TI strongly recommends reviewing the LCD_B peripheral module chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)) during the initial design requirements and decision process. The following table provides a brief overview over different choices that can be made and their impact.

| OPTION OR FEATURE | IMPACT OR USE CASE |
|--------------------------|--|
| Multiplexed LCD | <ul style="list-style-type: none"> • Enable displays with more segments • Use fewer device pins • LCD contrast decreases as mux level increases • Power consumption increases with mux level • Requires multiple intermediate bias voltages |
| Static LCD | <ul style="list-style-type: none"> • Limited number of segments that can be addressed • Use a relatively large number of device pins • Use the least amount of power • Use only V_{CC} and GND to drive LCD signals |
| Internal Bias Generation | <ul style="list-style-type: none"> • Simpler solution – no external circuitry • Independent of V_{LCD} source • Somewhat higher power consumption |
| External Bias Generation | <ul style="list-style-type: none"> • Requires external resistor ladder divider • Resistor size depends on display • Ability to adjust drive strength to optimize tradeoff between power consumption and good drive of large segments (high capacitive load) • External resistor ladder divider can be stabilized through capacitors to reduce ripple |
| Internal Charge Pump | <ul style="list-style-type: none"> • Helps ensure a constant level of contrast despite decaying supply voltage conditions (battery-powered applications) • Programmable voltage levels allow software-driven contrast control • Requires an external capacitor on the LCD_{CAP} pin • Higher current consumption than simply using V_{CC} for the LCD driver |

7.2.4.3 Detailed Design Procedure

A major component in designing the LCD solution is determining the exact connections between the LCD_B peripheral module and the display itself. Two basic design processes can be employed for this step, although in reality often a balanced co-design approach is necessary:

- PCB layout-driven design
- Software-driven design

In the PCB layout-driven design process, the segment S_x and common COM_x signals are connected to respective MSP430 device pins so that the routing of the PCB can be optimized to minimize signal crossings and to keep signals on one side of the PCB only, typically the top layer. For example, using a multiplexed LCD, it is possible to arbitrarily connect the S_x and COM_x signals between the LCD and the MSP430 device as long as segment lines are swapped with segment lines and common lines are swapped with common lines. It is also possible to not contiguously connect all segment lines but rather skip LCD_B module segment connections to optimize layout or to allow access to other functions that may be multiplexed on a particular device port pin. Employing a purely layout-driven design approach, however, can result in the LCD_B module control bits that are responsible for turning on and off segments to appear scattered throughout the memory map of the LCD controller (LCD_{Mx} registers). This approach potentially places a rather large burden on the software design that may also result in increased energy consumption due to the computational overhead required to work with the LCD.

The other extreme is a purely software-driven approach that starts with the idea that control bits for LCD segments that are frequently turned on and off together should be co-located in memory in the same LCD_{Mx} register or in adjacent registers. For example, in case of a 4-mux display that contains several 7-segment digits, from a software perspective it can be very desirable to control all 7 segments of each digit though a single byte-wide access to an LCD_{Mx} register. And consecutive segments are mapped to consecutive LCD_{Mx} registers. This allows use of simple look-up tables or software loops to output numbers on an LCD, reducing computational overhead and optimizing the energy consumption of an application. Establishing the most convenient memory layout must be performed in conjunction with the specific LCD that is being used to understand its design constraints in terms of which segment and which common signals are connected to, for example, a digit.

For design information regarding the LCD controller input voltage selection including internal and external options, contrast control, and bias generation, refer to the LCD_B controller chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#)).

For additional design information, see the application report *Designing With MSP430 and Segment LCD* ([SLAA654](#)).

7.2.4.4 Layout Guidelines

LCD segment (Sx) and common (COMx) signal traces are continuously switching while the LCD is enabled and should, therefore, be kept away from sensitive analog signals such as ADC inputs to prevent any noise coupling. TI recommends keeping the LCD signal traces on one side of the PCB grouped together in a bus-like fashion. A ground plane underneath the LCD traces and guard traces employed alongside the LCD traces can provide shielding.

If the internal charge pump of the LCD module is used, the externally provided capacitor on the LCDCAP pin should be located as close as possible to the MCU. The capacitor should be connected to the device using a short and direct trace and also have a solid connection to the ground plane that is supplying the V_{SS} pins of the MCU.

For an example layout of the LCD_B module with an MSP430F6638, see the TI Design *Flow Meter host MCU board with segment LCD and prepayment or dual RF option* ([TIDM-FLOWMETER_DUALRF](#)).

8 Device and Documentation Support

8.1 Device Support

8.1.1 Getting Started

For more information on the MSP430™ family of devices and the tools and libraries that are available to help with your development, visit the [Getting Started page](#).

8.1.2 Development Tools Support

All MSP430™ microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at www.ti.com/msp430tools.

8.1.2.1 Hardware Features

See the *Code Composer Studio for MSP430 User's Guide* ([SLAU157](#)) for details on the available features.

| MSP430 Architecture | 4-Wire JTAG | 2-Wire JTAG | Break-points (N) | Range Break-points | Clock Control | State Sequencer | Trace Buffer | LPMx.5 Debugging Support |
|---------------------|-------------|-------------|------------------|--------------------|---------------|-----------------|--------------|--------------------------|
| MSP430Xv2 | Yes | Yes | 8+2 | Yes | Yes | Yes | Yes | No |

8.1.2.2 Recommended Hardware Options

8.1.2.2.1 Target Socket Boards

The target socket boards allow easy programming and debugging of the device using JTAG. They also feature header pin outs for prototyping. Target socket boards are orderable individually or as a kit with the JTAG programmer and debugger included. The following table shows the compatible target boards and the supported packages.

| Package | Target Board and Programmer Bundle | Target Board Only |
|-------------------|------------------------------------|------------------------------------|
| 100-pin LQFP (PZ) | MSP-FET430U100AUSB | MSP-TS430PZ100AUSB |

8.1.2.2.2 Experimenter Boards

Experimenter Boards and Evaluation kits are available for some MSP430 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. See www.ti.com/msp430tools for details.

8.1.2.2.3 Debugging and Programming Tools

Hardware programming and debugging tools are available from TI and from its third party suppliers. See the full list of available tools at www.ti.com/msp430tools.

8.1.2.2.4 Production Programmers

The production programmers expedite loading firmware to devices by programming several devices simultaneously.

| Part Number | PC Port | Features | Provider |
|--------------------------|----------------|---|-------------------|
| MSP-GANG | Serial and USB | Program up to eight devices at a time. Works with PC or standalone. | Texas Instruments |

8.1.2.3 Recommended Software Options

8.1.2.3.1 Integrated Development Environments

Software development tools are available from TI or from third parties. Open-source solutions are also available.

This device is supported by Code Composer Studio™ IDE (CCS).

8.1.2.3.2 *MSP430Ware*

[MSP430Ware](#) is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware is available as a component of CCS or as a standalone package.

8.1.2.3.3 *SYS/BIOS*

[SYS/BIOS](#) is an advanced real-time operating system for the MSP430 microcontrollers. It features preemptive deterministic multi-tasking, hardware abstraction, memory management, and real-time analysis. SYS/BIOS is available free of charge and is provided with full source code.

8.1.2.3.4 *MSP430 USB Developer's Package*

The MSP430 USB Developer's Package ([MSP430USBDEVPACK](#)) is an easy-to-use USB stack implementation for the MSP430 microcontrollers.

8.1.2.3.5 *Command-Line Programmer*

[MSP430 Flasher](#) is an open-source, shell-based interface for programming MSP430 microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP430 Flasher can be used to download binary files (.txt or .hex) files directly to the MSP430 Flash without the need for an IDE.

8.1.3 *Device and Development Tool Nomenclature*

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430 MCU devices and support tools. Each MSP430 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP430F5438A). TI recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the electrical specifications for the final device

PMS – Final silicon die that conforms to the electrical specifications for the device but has not completed quality and reliability verification

MSP – Fully qualified production device

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed TI's internal qualification testing.

MSP – Fully-qualified development-support product

XMS and PMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS and PMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). [Figure 8-1](#) provides a legend for reading the complete device name for any family member.

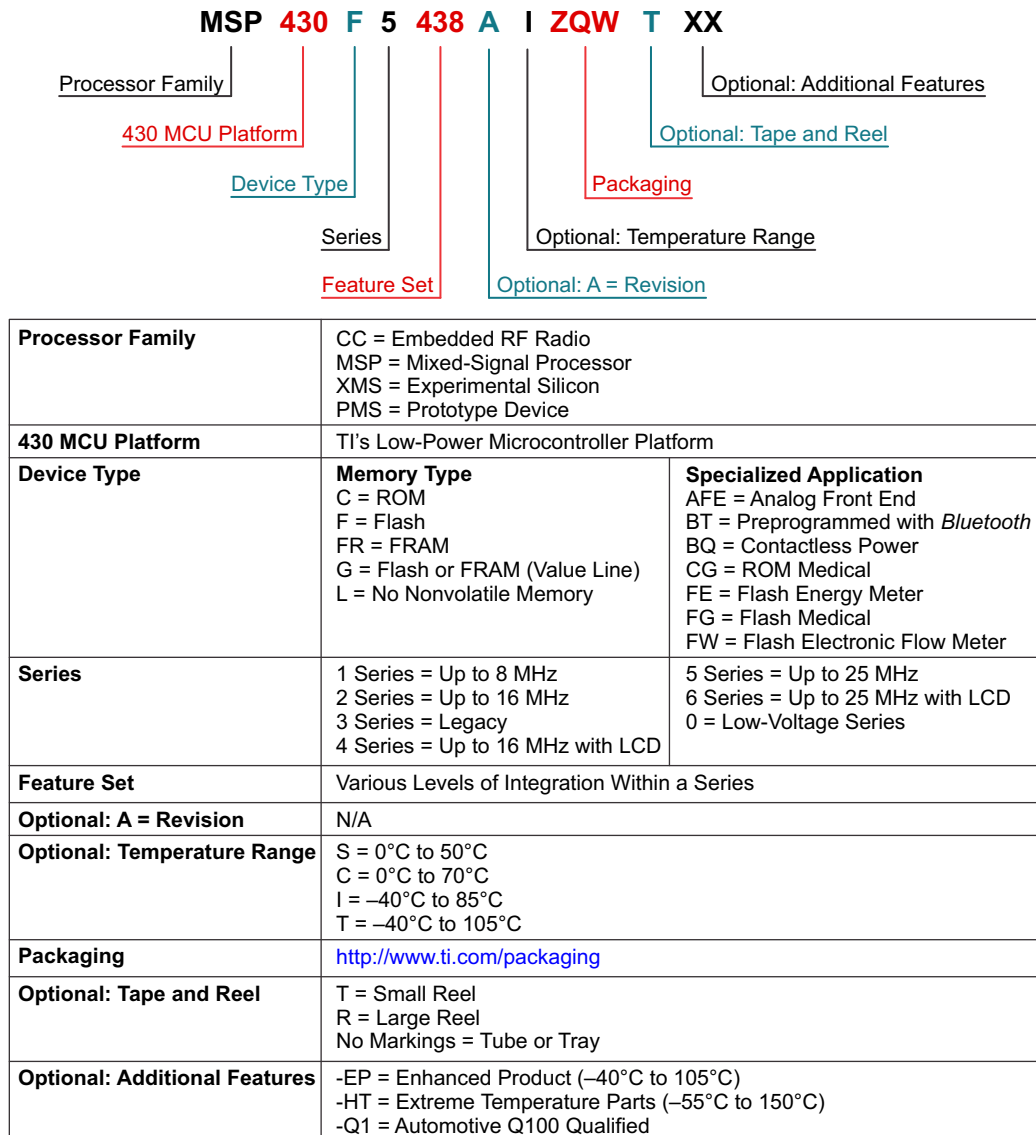


Figure 8-1. Device Nomenclature

8.2 Documentation Support

The following documents describe the MSP430FG662x and MSP430FG642x devices. Copies of these documents are available on the Internet at www.ti.com.

[SLAU208](#) **MSP430x5xx and MSP430x6xx Family User's Guide.** Detailed information on the modules and peripherals available in this device family.

[SLAZ667](#) **MSP430FG6626 Device Erratasheet.** Describes the known exceptions to the functional specifications for all silicon revision of the device.

[SLAZ668](#) **MSP430FG6625 Device Erratasheet.** Describes the known exceptions to the functional specifications for all silicon revision of the device.

[SLAZ669](#) **MSP430FG6426 Device Erratasheet.** Describes the known exceptions to the functional specifications for all silicon revision of the device.

[SLAZ670](#) **MSP430FG6425 Device Erratasheet.** Describes the known exceptions to the functional specifications for all silicon revision of the device.

8.3 Related Links

[Table 8-1](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|--------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| MSP430FG6626 | Click here | Click here | Click here | Click here | Click here |
| MSP430FG6625 | Click here | Click here | Click here | Click here | Click here |
| MSP430FG6426 | Click here | Click here | Click here | Click here | Click here |
| MSP430FG6425 | Click here | Click here | Click here | Click here | Click here |

8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Community](#)

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#)

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.5 Trademarks

MSP430, Code Composer Studio, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

9.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|----------------------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430FG6425IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | FG6425 | Samples |
| MSP430FG6425IZQWR | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | FG6425 | Samples |
| MSP430FG6426IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | FG6426 | Samples |
| MSP430FG6426IZQWR | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | FG6426 | Samples |
| MSP430FG6625IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | FG6625 | Samples |
| MSP430FG6625IZQWR | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | FG6625 | Samples |
| MSP430FG6626IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | FG6626 | Samples |
| MSP430FG6626IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | FG6626 | Samples |
| MSP430FG6626IZQWR | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | FG6626 | Samples |
| MSP430FG6626IZQWT | ACTIVE | BGA MICROSTAR JUNIOR | ZQW | 113 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | FG6626 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

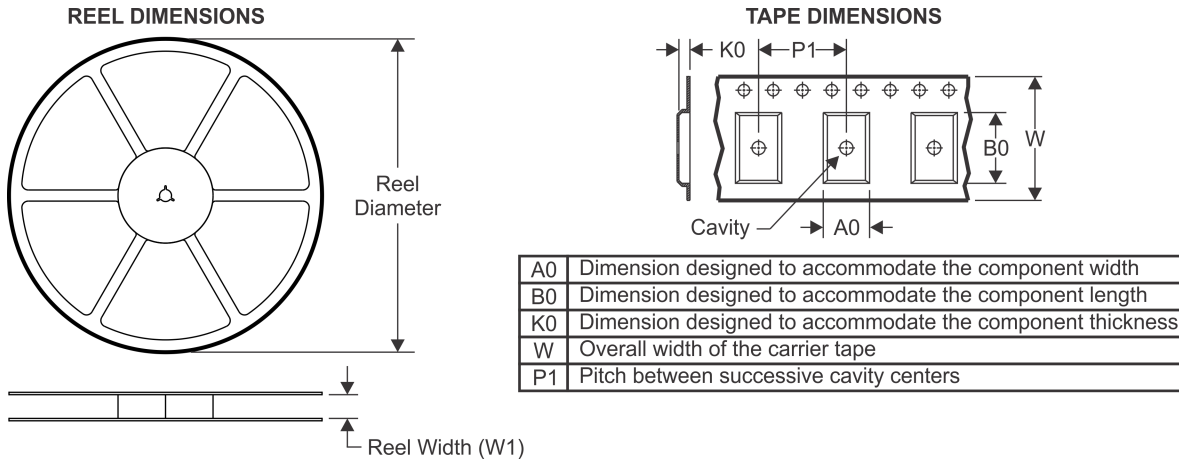
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

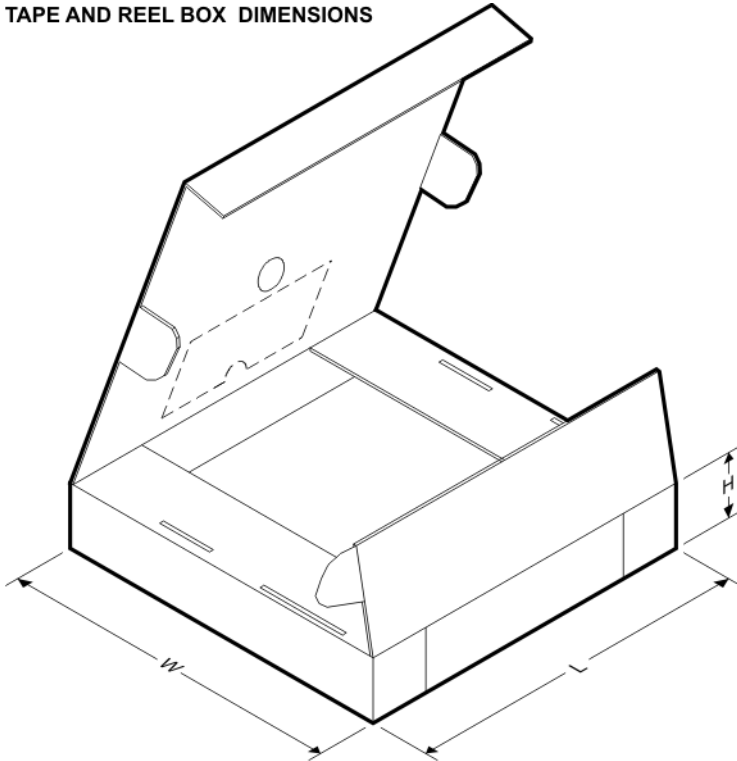


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FG6425IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430FG6425IZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |
| MSP430FG6426IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430FG6426IZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |
| MSP430FG6625IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430FG6625IZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |
| MSP430FG6626IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430FG6626IZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |
| MSP430FG6626IZQWT | BGA MICROSTAR | ZQW | 113 | 250 | 180.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| | R JUNIOR | | | | | | | | | | | |

TAPE AND REEL BOX DIMENSIONS



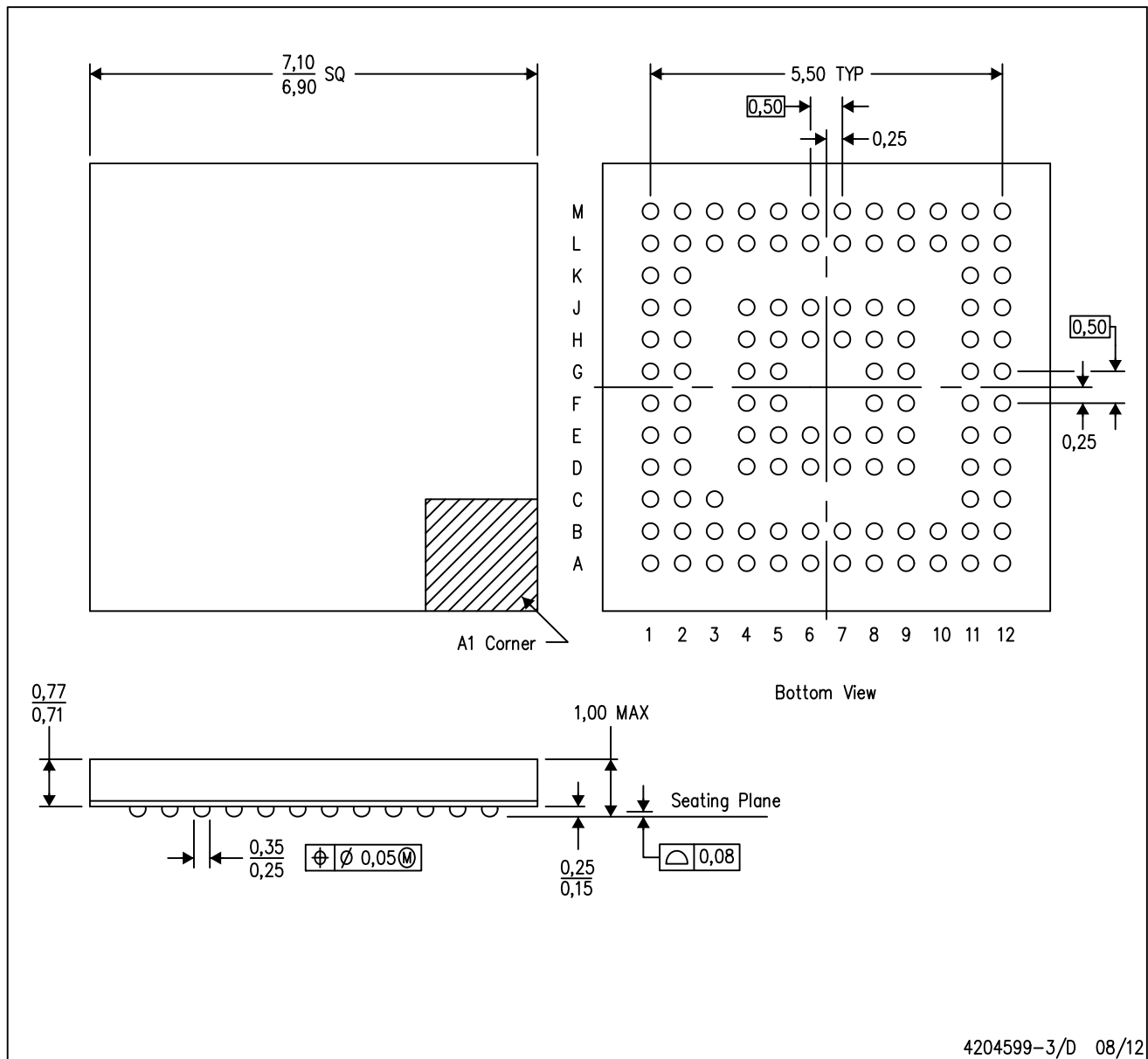
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| MSP430FG6425IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430FG6425IZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 336.6 | 336.6 | 28.6 |
| MSP430FG6426IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430FG6426IZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 336.6 | 336.6 | 28.6 |
| MSP430FG6625IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430FG6625IZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 336.6 | 336.6 | 28.6 |
| MSP430FG6626IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430FG6626IZQWR | BGA MICROSTAR JUNIOR | ZQW | 113 | 2500 | 336.6 | 336.6 | 28.6 |
| MSP430FG6626IZQWT | BGA MICROSTAR JUNIOR | ZQW | 113 | 250 | 213.0 | 191.0 | 55.0 |

MECHANICAL DATA

ZQW (S-PBGA-N113)

PLASTIC BALL GRID ARRAY

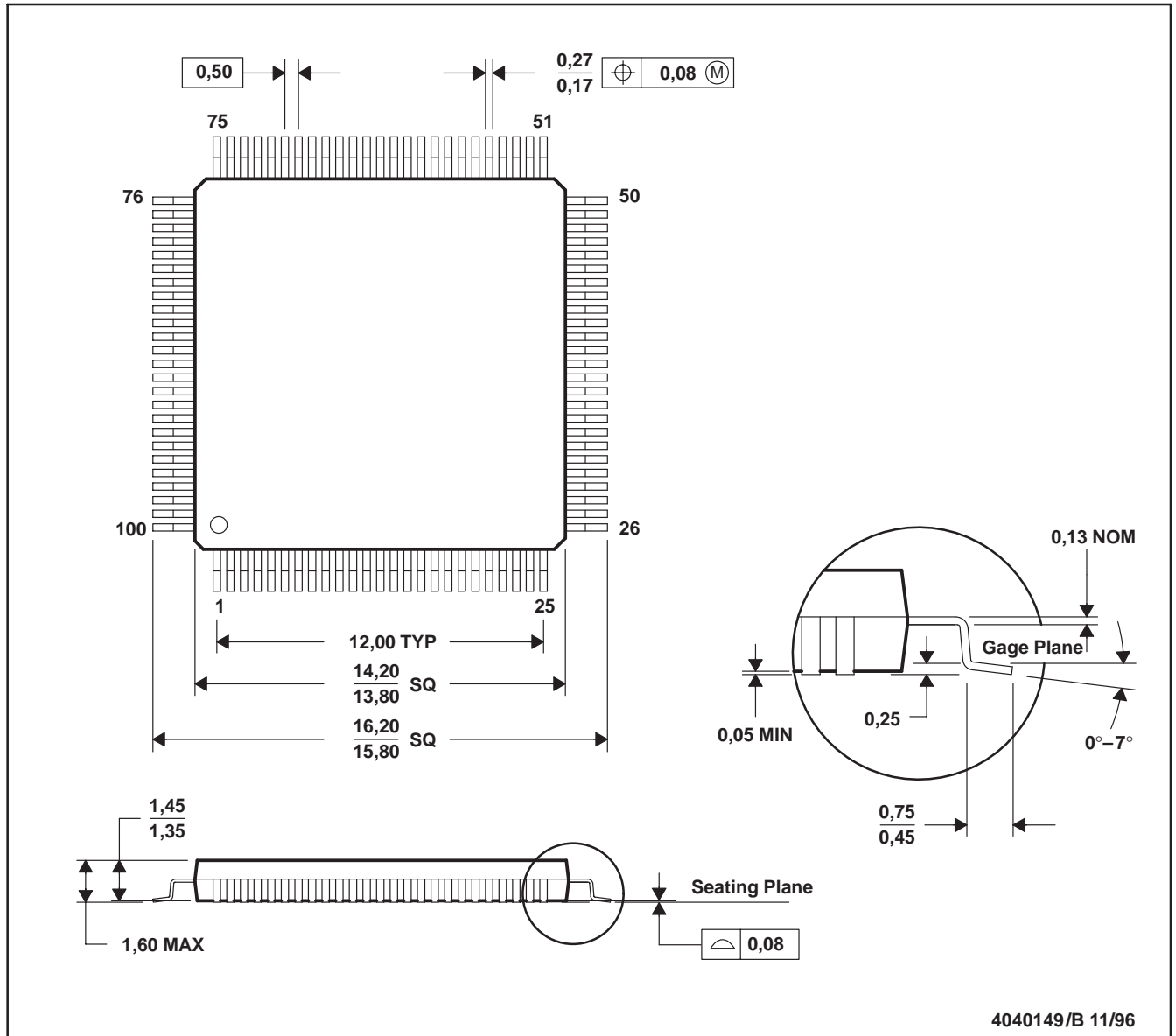


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225
 - D. This is a Pb-free solder ball design.

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PZ (S-PQFP-G100)

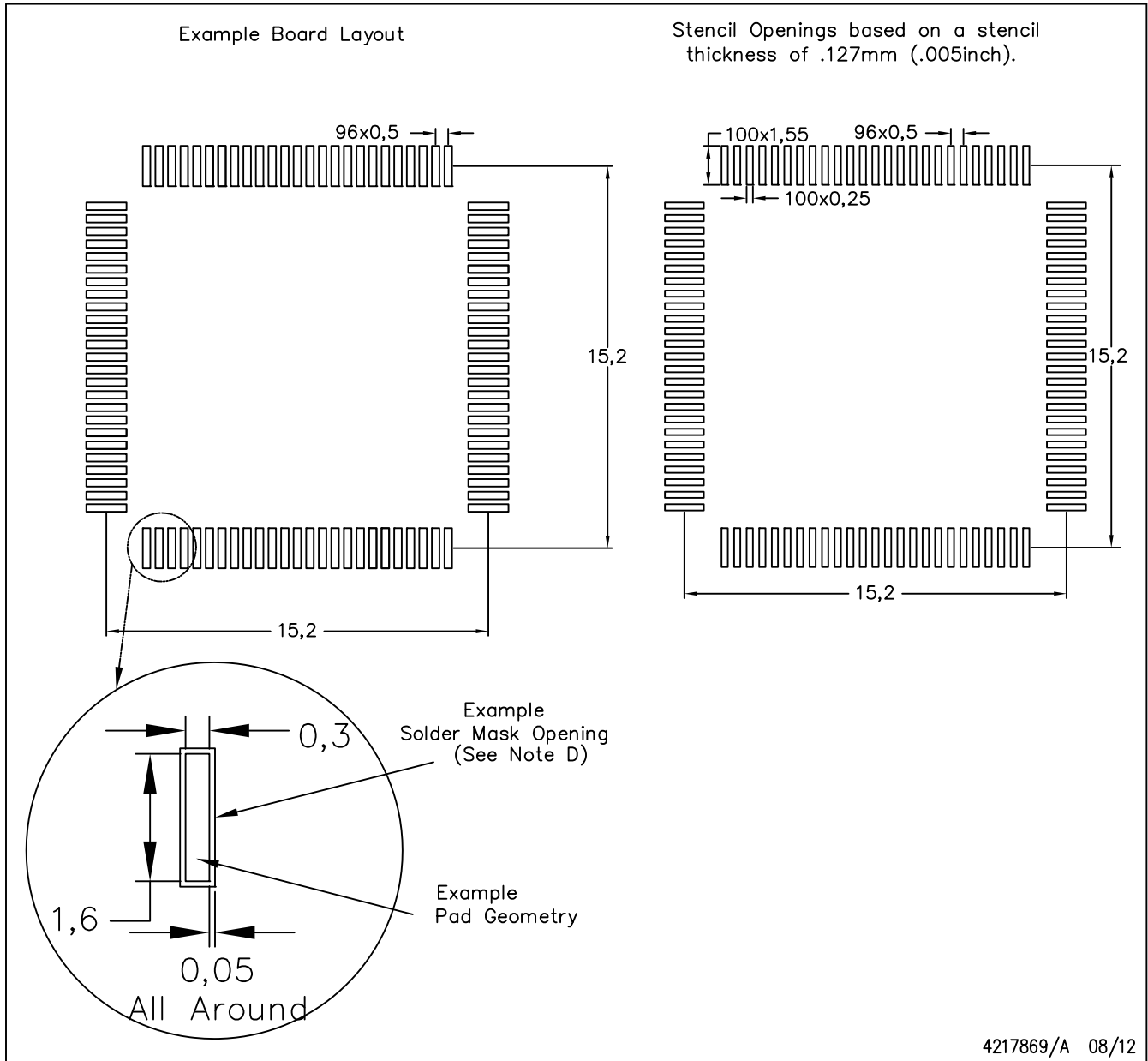
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

PZ (S-PQFP-G100)

PLASTIC QUAD FLAT PACK



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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