11.3 Gbps Modulator Driver

Check for Samples: ONET1141L

FEATURES

- **Digitally Selectable Output Amplitude up to 2.0VPP Single-Ended**
- **Digitally Selectable Bias Current up to 145mA Source**
- **2-wire Digital Interface with Integrated DACs and ADC for Control and Diagnostic Management**
- **Automatic Power Control (APC) Loop**
- **Adjustable Rise and Fall Times**
- **Programmable Input Equalizer**
- **Cross-Point Control**
- **Selectable Monitor PD Current Range and Polarity**
- **Includes Laser Safety Features**
- **Single 3.3V Supply**
- **–40°C to 100°C Operation**
- **Surface Mount Small Footprint 4mm × 4mm 24 Pin RoHS Compliant QFN Package**

APPLICATIONS

- **10 Gigabit Ethernet Optical Transmitters**
- **SONET OC-192/SDH STM-64 Optical Transmitters**
- **10G-EPON and XG-PON**
- **SFP+ and XFP Transceiver Modules**
- **XENPAK, XPAK, X2 and 300-pin MSA Transponder Modules**

DESCRIPTION

The ONET1141L is a high-speed, 3.3V electroabsorption modulator driver designed to bias and modulate an electroabsorptive modulated laser (EML) at data rates from 1 Gbps up to 11.3 Gbps.

The device provides a two-wire serial interface which allows digital control of the modulation and bias currents, eliminating the need for external components. Output waveform control, in the form of cross-point adjustment and rise and fall time adjustment are available to improve the optical eye mask margin. An optional input equalizer can be used for equalization of up to 150mm (6”) of microstrip or stripline transmission line on FR4 printed circuit boards. The device contains internal analog to digital and digital to analog converters to eliminate the need for special purpose microcontrollers.

The ONET1141L includes an integrated automatic power control (APC) loop which compensates for variations in laser average optical power over voltage and temperature and circuitry to support laser safety and transceiver management systems.

The modulator driver is characterized for operation from –40°C to 100°C case temperatures and is available in a small footprint 4mm × 4mm 24 pin RoHS compliant QFN package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM

A simplified block diagram of the ONET1141L is shown in Figure 1. The modulator driver consists of an input equalizer with selectable bypass, a limiter, an output driver, DC offset cancellation with cross point control, power-on reset circuitry, a 2-wire serial interface including a control logic block, a modulation current generator, a bias current generator with automatic power control loop, an analog to digital converter and an analog reference block.

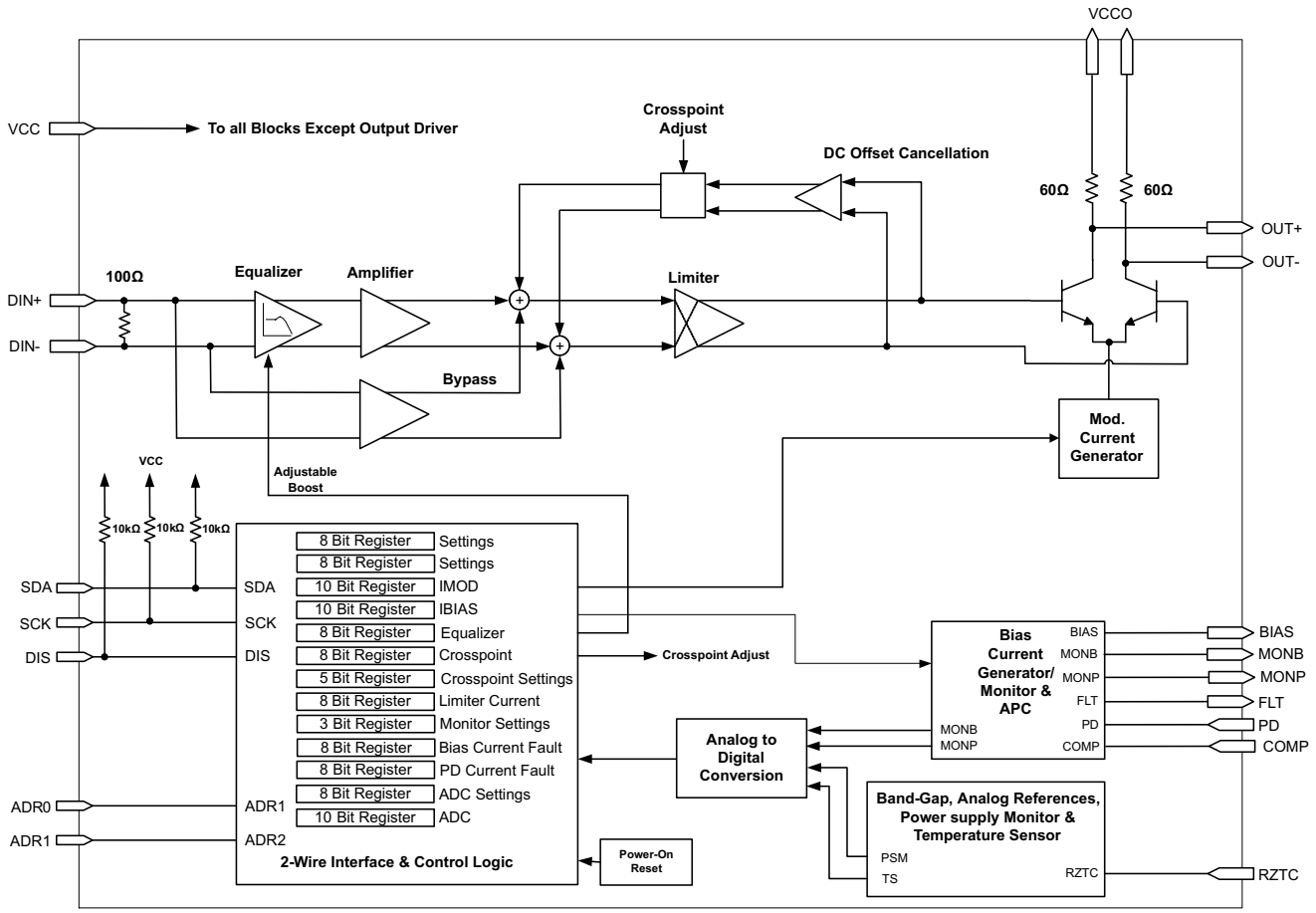
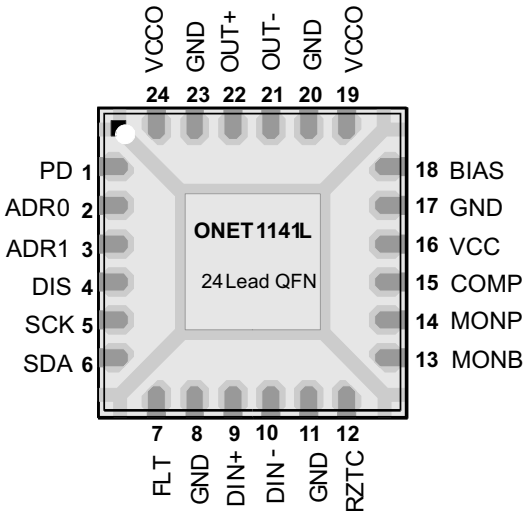


Figure 1. Simplified Block Diagram of the ONET1141L

PACKAGE

The ONET1141L is packaged in a small footprint 4mm X 4mm 24 pin RoHS compliant QFN package with a lead pitch of 0.5mm. The pin out is shown below.

24 PIN QFN PACKAGE, 4mm x 4mm
(TOP VIEW)



PIN FUNCTIONS

NO.		TYPE	DESCRIPTION
PIN	NAME		
1	PD	Analog	Photodiode input. Pin can source or sink current dependent on register setting.
2	ADR0	Digital-in	2-wire interface address programming pin. Leave this pad open for a default address of 0001000. Pulling the pin to VCC changes the 1st address bit to a 1 (address = 0001001)
3	ADR1	Digital-in	2-wire interface address programming pin. Leave this pad open for a default address of 0001000. Pulling the pin to VCC changes the 2nd address bit to a 1 (address = 0001010)
4	DIS	Digital-in	Disables both bias and modulation currents when set to high state. Includes a 10kΩ or 40kΩ pull-up resistor to VCC. Toggle to reset a fault condition.
5	SCK	Digital-in	2-wire interface serial clock input. Includes a 10kΩ or 40kΩ pull-up resistor to VCC.
6	SDA	Digital-in/out	2-wire interface serial data input/output. Includes a 10kΩ or 40kΩ pull-up resistor to VCC.
7	FLT	Digital-out	Fault detection flag. High level indicates that a fault has occurred. Open drain output. Requires an external 4.7kΩ to 10kΩ pull-up resistor to VCC for proper operation.
8, 11, 17, 20, 23, EP	GND	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
9	DIN+	Analog-in	Non-inverted data input. On-chip differentially 100Ω terminated to DIN–. Must be AC coupled.
10	DIN–	Analog-in	Inverted data input. On-chip differentially 100Ω terminated to DIN+. Must be AC coupled.
12	RZTC	Analog	Connect external zero TC 28.7kΩ resistor to ground (GND). Used to generate a defined zero TC reference current for internal DACs.
13	MONB	Analog-out	Bias current monitor. Sources a 1% replica of the bias current. Connect an external resistor to ground (GND) to use the analog monitor (DMONB = 0). If the voltage at this pin exceeds 1.16V a fault is triggered. Typically choose a resistor to give MONB voltage of 0.8V at the maximum desired bias current. If the digital monitor function is used (DMONB = 1) the resistor must be removed.
14	MONP	Analog-out	Photodiode current monitor. Sources a 12.5% replica of the photodiode current when PDRNG = 1X, a 25% replica when PDRNG = 01 and a 50% replica when PDRNG = 00. Connect an external resistor (5kΩ typical) to ground (GND) to use the analog monitor (DMONP = 0). If the voltage at this pin exceeds 1.16V a fault is triggered when MONPFLT = 1. If the digital monitor function is used (DMONP = 1) the resistor must be removed.
15	COMP	Analog	Compensation pin used to control the bandwidth of the APC loop. Connect a 0.01µF capacitor to ground.
16	VCC	Supply	3.3V ± 10% supply voltage.
18	BIAS	Analog	Sinks or sources the bias current for the laser in both APC and open loop modes.
19, 24	VCCO	Supply	3.3V ± 10% supply voltage for the output stage.
21	OUT–	CML-out	Inverted data output.
22	OUT+	CML-out	Non-inverted data output.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE		UNIT
		MIN	MAX	
V_{CC}	Supply voltage (2)	–0.3	4.0	V
V_{ADR0}, V_{ADR1}, V_{DIS}, V_{RZTC}, V_{SCK}, V_{SDA}, V_{DIN+}, V_{DIN-}, V_{FLT}, V_{MONB}, V_{MONP}, V_{COMP}, V_{PD}, V_{BIAS}, V_{OUT+}, V_{OUT-}	Voltage at ADR0, ADR1, DIS, RZTC, SCK, SDA, DIN+, DIN–, FLT, MONB, MONP, COMP, PD, BIAS, OUT+, OUT– (2)	–0.3	4.0	V
I_{DIN-}, I_{DIN+}	Maximum current at input pins		25	mA
I_{OUT+}, $I_{OUT–}$	Maximum current at output pins		120	mA
$I_{BIAS-MAX}$	Maximum bias current		180	mA
ESD	ESD rating at all pins		2	kV (HBM)
$T_{J,max}$	Maximum junction temperature		125	°C
T_{STG}	Storage temperature range	–65	150	°C
T_C	Case temperature	–40	110	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.97	3.3	3.63	V
V_{IH}	Digital input high voltage	DIS, SCK, SDA	2.0			V
V_{IL}	Digital input low voltage	DIS, SCK, SDA			0.8	V
	Photodiode current range	Control bit PDRNG = 1X,step size = 3 µA		3080		µA
		Control bit PDRNG = 01,step size = 1.5 µA		1540		
		Control bit PDRNG = 00,step size = 0.75 µA		770		
R_{RZTC}	Zero TC resistor value (1)	1.16V bandgap bias acrossresistor, E96, 1% accuracy	28.4	28.7	29	kΩ
v_{IN}	Differential input voltage swing	EQENA = 1	160		1000	mV_{p-p}
		EQENA = 0	400		1000	
t_{R-IN}	Input rise time	20%–80%		30	55	ps
t_{F-IN}	Input fall time	20%–80%		30	55	ps
T_C	Temperature at thermal pad		-40		100	°C

(1) Changing the value will alter the DAC ranges.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, with 50Ω output load, open loop operation, V_{OUT} = 2.0Vpp, I_{BIAS} = 80 mA, and R_{RZTC} = 28.7kΩ unless otherwise noted. Typical operating condition is at V_{CC} =3.3V and T_A = 25°C

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.97	3.3	3.63	V
I_{VCC}	Supply current	V_{OUT} = 2.0Vpp, I_{BIAS} = 0mA, EQENA = 0		143	170	mA
		V_{OUT} = 2.0Vpp, I_{BIAS} = 0mA, EQENA = 1		151	182	
		Output off (DIS = HIGH), V_{OUT} = 2.0Vpp, I_{BIAS} = 80 mA, EQENA = 0		40		
R_{IN}	Data input resistance	Differential between DIN+ / DIN–	82	100	118	Ω
R_{OUT}	Output resistance	Single-ended at OUT+ or OUT–	50	60	70	Ω
	Digital input current	SCK, SDA, pull up to VCC	2	360	470	µA
	Digital input current	DIS, pull up to VCC	2	360	470	µA
V_{OH}	Digital output high voltage	FLT, pull-up to V_{CC}, I_{SOURCE} = 50 µA	2.4			V
V_{OL}	Digital output low voltage	FLT, pull-up to V_{CC}, I_{SINK} = 350 µA			0.4	V
$I_{BIAS-MIN}$	Minimum bias current	See (1)			5	mA
$I_{BIAS-MAX}$	Maximum bias current	Source. BIASPOL = 0, DAC set to maximum, open and closed loop	145	160		mA
		Sink. BIASPOL = 1, DAC set to maximum, open and closed loop	93	105		
$I_{BIAS-DIS}$	Bias current during disable				100	µA
	Average power stability	APC loop enabled		±0.5		dB
	Bias pin compliance voltage	Source. BIASPOL = 0	0.9			V
		Sink. BIASPOL = 1			V_{CC}–0.9	
	Temperature sensor accuracy	With 1-point external mid scale calibration		±3		°C
V_{PD}	Photodiode reverse bias voltage	APC active, I_{PD} = max	1.3	2.3		V
	Photodiode fault current level	Percent of target I_{PD} (2)		150%		
	Photodiode current monitor ratio	I_{MONP} / I_{PD} with control bit PDRNG = 1X	10%	12.5%	15%	
		I_{MONP} / I_{PD} with control bit PDRNG = 01	20%	25%	30%	
		I_{MONP} / I_{PD} with control bit PDRNG = 00	40%	50%	60%	
	Monitor diode DMI accuracy	With external calibration at 200 µA	-10%		10%	
	Bias current monitor ratio	I_{MONB} / I_{BIAS} (nominal 1/100 = 1%)	0.9%	1.0%	1.1%	
	Bias current DMI accuracy	Bias current ≥ 30 mA		±10%		
	Power supply monitor accuracy	With external mid scale calibration	–2%		2%	
V_{CC-RST}	V_{CC} reset threshold voltage	V_{CC} voltage level which triggers power-on reset		2.5	2.8	V
$V_{CC-RSTHYS}$	V_{CC} reset threshold voltage hysteresis			100		mV
$V_{MONB-FLT}$	Fault voltage at MONB	Fault occurs if voltage at MONB exceeds value	1.1	1.16	1.24	V

(1) The bias current can be set below the specified minimum according to the corresponding register setting, however in closed loop operation settings below the specified value may trigger a fault.
(2) Assured by simulation over process, supply and temperature variation.

AC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, with 50Ω output load, open loop operation, V_{OUT} = 2.0Vpp, I_{BIAS} = 80 mA, and R_{RZTC} = 28.7kΩ unless otherwise noted. Typical operating condition is at V_{CC} =3.3V and T_A = 25°C

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
SDD11	Differential input return gain	0.01 GHz f < 5 GHz		–15		dB
		5 GHz < f < 11.1 GHz		–8		
SCD11	Differential to common mode conversion gain	0.01 GHz < f < 11.1 GHz		–20		dB
t_{R-OUT}	Output rise time	20%–80%, t_{R-IN} < 40 ps, 50Ω load, single-ended, crosspoint = 50%		28	40	ps
t_{F-OUT}	Output fall time	20%–80%, t_{F-IN} < 40 ps, 50Ω load, single-ended, crosspoint = 50%		28	40	ps
V_{O-MIN}	Minimum output amplitude	50Ω load, single-ended			200	mVpp
V_{O-MAX}	Maximum output amplitude	50Ω load, single-ended	2.0			Vpp
	Output Amplitude Stability	50Ω load, single-ended			250	mV
$V_{MOD-STEP}$	Modulation voltage step size	50Ω load, 10 Bit Register		2.5		mV
DJ	Deterministic output jitter	EQENA = 1 with maximum equalization, K28.5 pattern at 11.3 Gbps, 160mVpp, 600mVpp, 1000mVpp differential input voltage, single-ended output		5	15	ps_{p-p}
		EQENA = 1, K28.5 pattern at 11.3 Gbps, maximum equalization with 6” transmission line at the input, 160mVpp, 600mVpp, 1000mVpp input to transmission line, single-ended output		7		
RJ	Random output jitter			0.2	0.6	ps_{RMS}
τ_{APC}	APC time constant	C_{APC} 0.01 µF, I_{PD} = 100 µA, PD coupling ratio CR = 40 (1)		120		µs
	High cross point control range	50Ω load, single-ended		75%		
	Low cross point contro lrange	50Ω load, single-ended		30%		
	Cross point stability	50Ω load, single-ended, V_{IN} ≥ 400mVpp		±5%		
T_{OFF}	Transmitter disable time	Rising edge of DIS to $I_{BIAS} \le 0.1 \times I_{BIAS-NOMINAL}$ (1)		0.05	5	µs
T_{ON}	Disable negate time	Falling edge of DIS to $I_{BIAS} \ge 0.9 \times I_{BIAS-NOMINAL}$ (1)			1	ms
T_{INIT1}	Power-on to initialize	Power-on to registers ready to be loaded		1	10	ms
T_{INIT2}	Initialize to transmit	Register load STOP command to part ready to transmit valid data (1)			2	ms
T_{RESET}	DIS pulse width	Time DIS must held high to reset part (1)	100			ns
T_{FAULT}	Fault assert time	Time from fault condition to FLT high (1)			50	µs

(1) Assured by simulation over process, supply and temperature variation.

DETAILED DESCRIPTION

EQUIALIZER

The data signal is applied to an input equalizer by means of the input signal pins DIN+/DIN–, which provide on-chip differential 100Ω line-termination. The equalizer is enabled by setting EQENA = 1 (bit 1 of register 0). Equalization of up to 150mm (6”) of microstrip or stripline transmission line on FR4 printed circuit boards can be achieved. The amount of equalization is digitally controlled by the two-wire interface and control logic block and is dependant on the register settings EQADJ[0..7] (register 6). The equalizer can be turned off and bypassed by setting EQENA = 0 and the supply current is reduced. For details about the equalizer settings, see Table 19.

LIMITER

By limiting the output signal of the equalizer to a fixed value, the limiter removes any overshoot after the input equalization and provides the input signal for the output driver. Adjustments to the limiter bias current and emitter follower current can be made to trade off the rise and fall times and supply current. The limiter bias current is adjusted through LIMCSGN (bit 7 of register 9) and LIMC[0..2] (bits 4, 5 and 6 of register 9). The emitter follower current is adjusted through EFCSGN (bit 3 of register 9) and EFC[0..2] (bits 0, 1 and 2 of register 9).

HIGH-SPEED OUTPUT DRIVER

The modulation current is sunk from the common emitter node of the limiting output driver differential pair by means of a modulation current generator, which is digitally controlled by the 2-wire serial interface.

The collector nodes of the output stages are connected to the output pins OUT+ and OUT–. The collectors have internal 60Ω back termination resistors to VCCO. The outputs are optimized to drive a 50Ω single-ended load and to obtain the maximum single-ended output voltage of 2.0Vpp, AC coupling and inductive pull-ups to VCC are required

The polarity of the output pins can be inverted by setting the output polarity switch bit, POL (bit 2 of register 0) to 1.

MODULATION CURRENT GENERATOR

The modulation current generator provides the current for the current modulator described above. The circuit is digitally controlled by the 2-wire interface block.

A 10-bit wide control bus, MODC[0..9] (registers 2 and 3), is used to set the desired modulation current, and therefore, the output voltage. The modulation current can be increased by setting HCENA = 1 (bit 4 of register 1) and enabling the high modulation current mode, however, the single-ended output voltage should be kept below 2Vpp for the best performance.

The modulation current can be disabled by setting the DIS input pin to a high level or setting ENA = 0 (bit 7 of register 0). The modulation current is also disabled in a fault condition if the internal fault detection enable register flag FLTEN is set to 1 (bit 3 of register 0).

DC OFFSET CANCELATION AND CROSS POINT CONTROL

The ONET1141L has DC offset cancellation to compensate for internal offset voltages. The offset cancellation can be disabled by setting OCDIS = 1 (bit 3 of register 1). To adjust the eye crossing point, set CPENA = 1 (bit 2 of register 8). The crossing point can be moved toward the one level be setting CPSGN = 1 (bit 7 of register 7) and it can be moved toward the zero level by setting CPSGN = 0. The percentage of shift depends upon the register settings CPADJ[0..6] (register 7), and the cross point adjustment range bits CPRNG[0..1] (register 8). Setting CPRNG1 = 0 and CPRNG0 = 0 results in minimum adjustment capability and setting CPRNG1 = 1 and CPRNG0 = 1 results in maximum adjustment capability.

BIAS CURRENT GENERATION AND APC LOOP

The bias current generation and APC loop are controlled by means of the 2-wire interface. In open loop operation, selected by setting OLENA = 1 (bit 4 of register 0) the bias current is set directly by the 10-bit wide control word BIASC[0..9] (registers 4 and 5). In automatic power control mode, selected by setting OLENA = 0, the bias current depends on the register settings BIASC[0..9] and the coupling ratio (CR) between the laser bias current and the photodiode current. CR = I_{BIAS}/I_{PD}. If the photodiode anode is connected to the PD pin (PD pin is sinking current), set PDPOL = 1 (bit 0 of register 0) and if the photodiode cathode is connected to the PD pin (PD pin is sourcing current), set PDPOL = 0.

Three photodiode current ranges can be selected by means of the PDRNG[0..1] bits (register 0). The photodiode range should be chosen to keep the laser bias control DAC, BIASC[0..9], close to the center of its range. This keeps the laser bias current set point resolution high. For details regarding the bias current setting in open-loop as well as in closed-loop mode, see Table 19.

The ONET1141L has the ability to source or sink the bias current. The default condition is for the BIAS pin to source the current (BIASPOL = 0). To act as a sink, set BIASPOL = 1 (bit 2 of register 1).

The bias current is monitored using a current mirror with a gain equal to 1/100. By connecting a resistor between MONB and GND, the bias current can be monitored as a voltage across the resistor. A low temperature coefficient precision resistor should be used. The bias current can also be monitored as a 10 bit unsigned digital word through the 2-wire interface by setting DMONB = 1 (bit 0 of register 10) and removing the resistor to ground.

ANALOG REFERENCE AND TEMPERATURE SENSOR

The ONET1141L modulator driver is supplied by a single 3.3V±10% supply voltage connected to the VCC and VCCO pins. This voltage is referred to ground (GND) and can be monitored as a 10 bit unsigned digital word through the 2-wire interface.

On-chip bandgap voltage circuitry generates a reference voltage, independent of the supply voltage, from which all other internally required voltages and bias currents are derived.

An external zero temperature coefficient resistor must be connected from the RZTC pin of the device to ground. This resistor is used to generate a precise, zero-TC current which is required as a reference current for the on-chip DACs.

The ONET1141L provides an on-chip temperature sensor which can be monitored as a 10 bit unsigned digital word through the 2-wire interface.

POWER-ON RESET

The ONE1141L has power on reset circuitry which ensures that all registers are reset to zero during startup. After the power-on to initialize time (t_{INIT1}), the internal registers are ready to be loaded. The part is ready to transmit data after the initialize to transmit time (t_{INIT2}), assuming that the chip enable bit ENA is set to 1 and the disable pin DIS is low. The DIS pin has an internal 10kΩ pull up resistor so the pin must be pulled low to enable the outputs. The ONET1141L can be disabled using either the ENA control register bit or the disable pin DIS. In both cases the internal registers are not reset. After the disable pin DIS is set low and/or the enable bit ENA is set back to 1, the part returns to its prior output settings.

To reduce the disable time, only the output stage can be disabled by setting DISMODE = 1 (bit 1 of register 1).

ANALOG TO DIGITAL CONVERTER

The ONET1141L has an internal 10 bit analog to digital converter (ADC) that converts the analog monitors for temperature, power supply voltage, bias current and photodiode current into a 10 bit unsigned digital word. The first 8 most significant bits (MSBs) are available in register 14 and the 2 least significant bits (LSBs) are available in register 15. Depending on the accuracy required, 8 bits or 10 bits can be read. However, due to the architecture of the 2-wire interface, in order to read the 2 registers, 2 separate read commands have to be sent.

The ADC is enabled by default so to monitor a particular parameter, select the parameter with ADCSEL[0..1] (bits 0 and 1 of register 13). Table 1 shows the ADCSEL bits and the parameter that is monitored.

Table 1. ADC Selection Bits and the Monitored Parameter

ADCSEL1	ADCSEL0	Monitored Parameter
0	0	Temperature
0	1	Supply voltage
1	0	Photodiode current
1	1	Bias current

To digitally monitor the photodiode current, ensure that DMONP = 1 (bit 1 of register 10) and that a resistor is not connected to the MONP pin. To digitally monitor the bias current, ensure that DMONB = 1 (bit 0 of register 10) and that a resistor is not connected to the MONB pin. If it is not desired to use the ADC to monitor the various parameters then the ADC can be disabled by setting ADCDIS = 1 (bit 7 of register 13) and OSCDIS = 1 (bit 6 of register 13).

The digital word read from the ADC can be converted to its analog equivalent through the following formulas:

Temperature Without a Mid-Point Calibration

$$\text{Temperature } (^{\circ}C) = (ADCx - 264)/6 \quad (1)$$

Temperature With a Mid-Point Calibration

$$\text{Temperature } (^{\circ}C) = (T\_cal(^{\circ}C) + 273) \times (ADCx + 1362) \ / \ (ADC\_cal + 1362) - 273 \quad (2)$$

Power Supply Voltage

$$\text{Power supply voltage } (V) = 2.25 \times (ADCx + 1380)/1409 \quad (3)$$

Photodiode Current Monitor

$$IPD(\mu A) = 1.3 \times ADCx \quad (4)$$

Bias Current Monitor

$$\text{Source mode: } IBIAS\ (mA) = 0.177 \times ADCx$$

$$\text{Sink mode: } IBIAS\ (mA) = 0.19 \times ADCx \quad (5)$$

Where:

ADCx = the decimal value read from the ADC
T_cal = the calibration temperature
ADC_cal = the decimal value read from the ADC at the calibration temperature

2-WIRE INTERFACE AND CONTROL LOGIC

The ONET1141L uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microprocessor, for example. The SDA and SCK pins have internal 10kΩ pull ups to VCC. If a common interface is used to control multiple parts, the internal pull ups can be set to 40kΩ by setting TWITERM to 1 (bit 7 of register 1). This will also set the internal pullup on the DIS pin to 40 kΩ.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out the control signals. The ONET1141L is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data write transmission is as follows:

1. START command
2. 7 bit slave address (0001000) followed by an eighth bit (value = 0) which is the data write bit (W).
3. 8 bit register address
4. 8 bit register data word
5. STOP command

The first 2 bits of the slave address can be changed to 1 by grounding the ADR0 and ADR1 pins.

Regarding timing, the ONET1141L is I²C compatible. The typical timing is shown in Figure 2 and complete data write and read transfers are shown in Figure 3. Parameters for Figure 2 are defined in Table 2.

Bus Idle: Both SDA and SCK lines remain HIGH

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCK line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCK line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: Only one data byte can be transferred between a START and a STOP condition. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

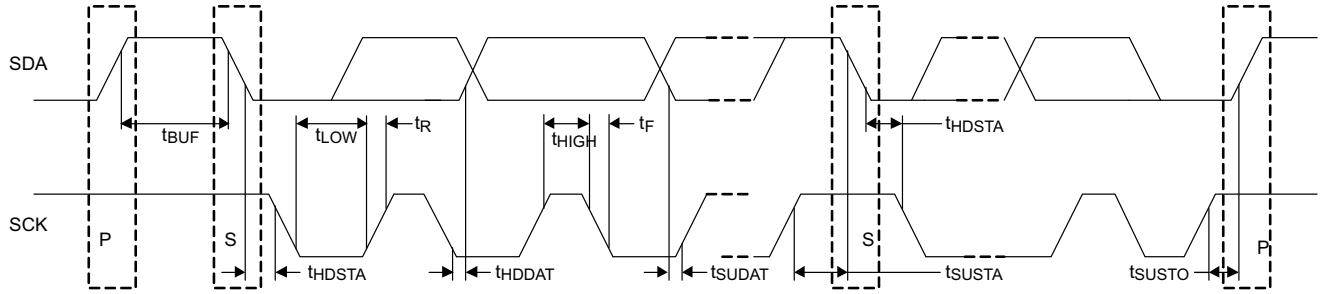


Figure 2. I²C Timing Diagram

Table 2. Timing Diagram Definitions

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{SCK}	SCK clock frequency		400	kHz
t_{BUF}	Bus free time between STOP and START conditions	1.3		µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6		µs
t_{LOW}	Low period of the SCK clock	1.3		µs
t_{HIGH}	High period of the SCK clock	0.6		µs
t_{SUSTA}	Setup time for a repeated START condition	0.6		µs
t_{HDDAT}	Data HOLD time	0		µs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCK signals		300	ns
t_F	Fall time of both SDA and SCK signals		300	ns
t_{SUSTO}	Setup time for STOP condition	0.6		µs

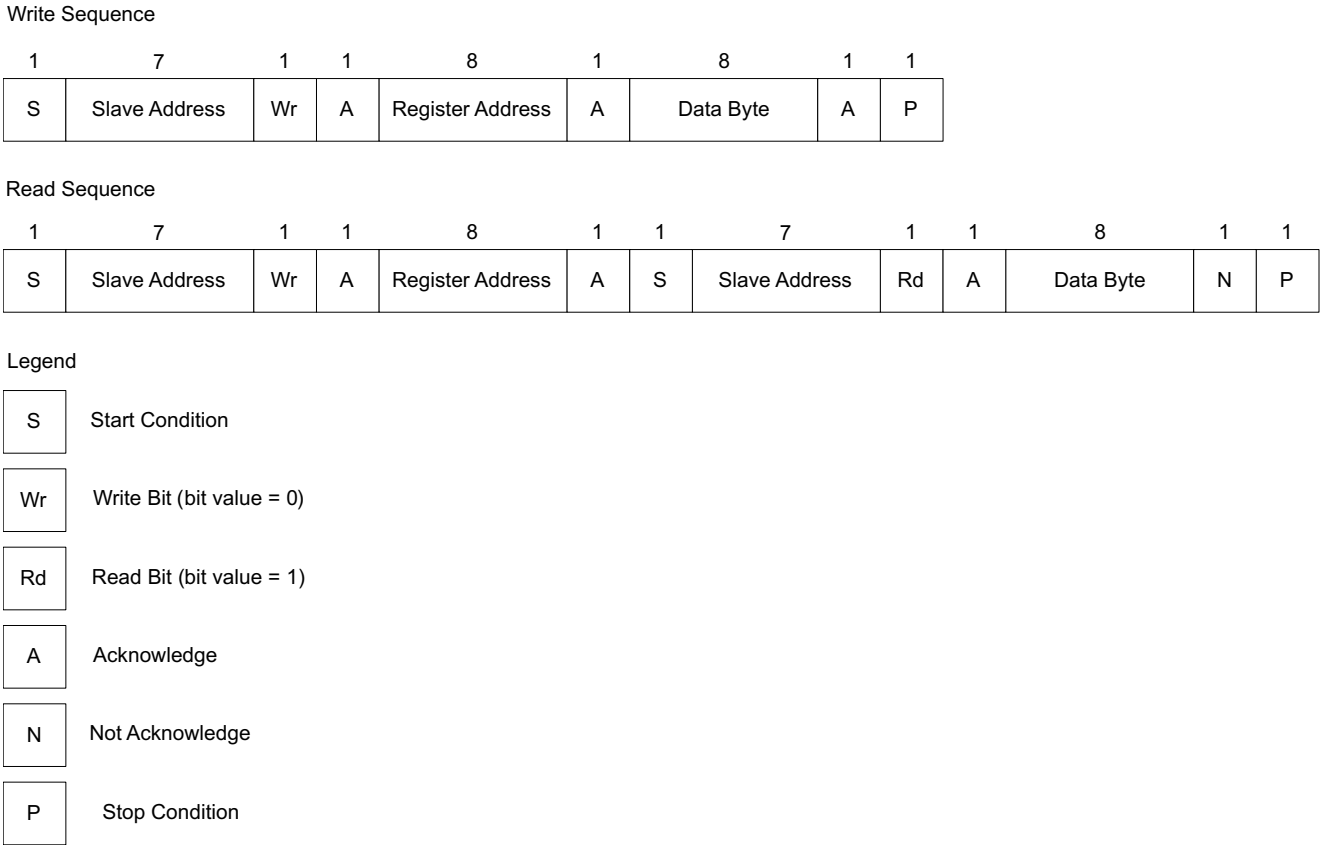


Figure 3. Programming Sequence

REGISTER MAPPING

The register mapping for register addresses 0 (0x00) through 15 (0x0F) are shown in Table 3 through Table 18. Table 19 describes the circuit functionality based on the register settings.

Table 3. Register 0 (0x00) Mapping – Control Settings

register address 0 (0x00)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
ENA	PDRNG1	PDRNG0	OLENA	FLTEN	POL	EQENA	PDPOL

Table 4. Register 1 (0x01) Mapping – Control Settings

register address 1 (0x01)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
TWITERM	HIEFCENA	HIEQGENA	HCENA	OCDIS	BIASPOL	DISMODE	LOGENA

Table 5. Register 2 (0x02) Mapping – Modulation Current

register address 2 (0x02)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	MODC1	MODC0

Table 6. Register 3 (0x03) Mapping – Modulation Current

register address 3 (0x03)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
MODC9	MODC8	MODC7	MODC6	MODC5	MODC4	MODC3	MODC2

Table 7. Register 4 (0x04) Mapping – Bias Current

register address 4 (0x04)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	BIASC1	BIASC0

Table 8. Register 5 (0x05) Mapping – Bias Current

register address 5 (0x05)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
BIASC9	BIASC8	BIASC7	BIASC6	BIASC5	BIASC4	BIASC3	BIASC2

Table 9. Register 6 (0x06) Mapping – Equalizer Adjust

register address 6 (0x06)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
EQADJ7	EQADJ6	EQADJ5	EQADJ4	EQADJ3	EQADJ2	EQADJ1	EQADJ0

Table 10. Register 7 (0x07) Mapping – Cross Point Adjust

register address 7 (0x07)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
CPSGN	CPADJ6	CPADJ5	CPADJ4	CPADJ3	CPADJ2	CPADJ1	CPADJ0

Table 11. Register 8 (0x08) Mapping – Cross Point Control Settings

register address 8 (0x08)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
IDRV	–	–	CPREF	–	CPENA	CPRNG1	CPRNG0

Table 12. Register 9 (0x09) Mapping – Limiter Bias Current Adjust

register address 9 (0x09)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
LIMCSGN	LMC2	LIMC1	LIMC0	EFCSGN	EFC2	EFC1	EFC0

Table 13. Register 10 (0x0A) Mapping – Monitor Settings

register address 10 (0x0A)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	MONPFLT	DMONP	DMONB

Table 14. Register 11 (0x0B) Mapping – Bias Monitor Fault Settings

register address 11 (0x0B)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
BMF7	BMF6	BMF5	BMF4	BMF3	BMF2	BMF1	BMF0

Table 15. Register 12 (0x0C) Mapping – Power Monitor Fault Settings

register address 12 (0x0C)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
PMF7	PMF6	PMF5	PMF4	PMF3	PMF2	PMF1	PMF0

Table 16. Register 13 (0x0D) Mapping – ADC Settings

register address 13 (0x0D)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
ADCDIS	OSCDIS	–	–	–	–	ADCSEL1	ADCSEL0

Table 17. Register 14 (0x0E) Mapping – ADC Output (Read Only)

register address 14 (0x0E)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2

Table 18. Register 15 (0x0F) Mapping – ADC Output (Read Only)

register address 15 (0x0F)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	ADC1	ADC0

Table 19. Register Functionality

REGISTER	BIT	SYMBOL	FUNCTION
0	7	ENA	**Enable chip bit** 1 = Chip enabled. Can be toggled low to reset a fault condition. 0 = Chip disabled
	6 5	PDRNG1 PDRNG0	**Photodiode current range bits** 1X: up to 3080µA / 3µA resolution 01: up to 1540µA / 1.5µA resolution 00: up to 770µA / 0.75µA resolution
	4	OLENA	**Open loop enable bit** 1 = Open loop bias current control, 0 = Closed loop bias current control
	3	FLTEN	**Fault detection enable bit** 1 = Fault detection on 0 = Fault detection off
	2	POL	**Output polarity switch bit** 1: pin 22 = OUT- and pin 21= OUT+ 0: pin 22 = OUT+ and pin 21 = OUT-
	1	EQENA	**Equalizer enable bit** 1 = Equalizer is enabled 0 = Equalizer is disabled and bypassed
	0	PDPOL	**Photodiode polarity bit** 1 = Photodiode cathode connected to V_{CC} 0 = Photodiode anode connected to GND

Table 19. Register Functionality (continued)

REGISTER	BIT	SYMBOL	FUNCTION
1	7	TWITERM	**Two wire interface input termination select bit** 1 = 40kΩ selected 0 = 10kΩ selected
	6	HIEFCENA	**High emitter follower drive current enable bit** 1 = High current enabled 0 = High current disabled
	5	HIEQGENA	**High gain enable for EQ stage (with EQENA = 1)** 1 = High gain enabled 0 = High gain disabled
	4	HCENA	**High modulation current enable bit** 1 = High modulation current enabled 0 = High modulation current disabled
	3	OCDIS	**Offset cancellation disable bit** 1 = DC offset cancellation is disabled 0 = DC offset cancellation is enabled
	2	BIASPOL	**Bias current polarity bit** 1 = Bias pin sinks current 0 = Bias pin sources current
	1	DISMODE	**Disable mode setting bit** 1 = Only the output stage is disabled (fast disable mode) 0 = Major parts of the signal path are disabled
	0	LOGENA	**Low gain enable for input amplifier (with EQENA = 0)** 1 = Low gain enabled 0 = Default gain
3	7	MODC9	**Modulation current setting: sets the output voltage** Output Voltage: 2.3Vpp / 2.5mV steps
	6	MODC8	
	5	MODC7	
	4	MODC6	
	3	MODC5	
	2	MODC4	
	1	MODC3	
	0	MODC2	
2	1	MODC1	
	0	MODC0	
5	7	BIASC9	**Bias curent settings** **Closed loop (APC):**
	6	BIASC8	Coupling ratio CR = I_{BIAS} / I_{PD}, BIASC = 0..1023, I_{BIAS} ≤ 150mA:
	5	BIASC7	
	4	BIASC6	PDRNG = 00 (see above); I_{BIAS} = 0.75µA x CR x BIASC
	3	BIASC5	PDRNG = 01 (see above); I_{BIAS} = 1.5µA x CR x BIASC
	2	BIASC4	PDRNG = 1X (see above); I_{BIAS} = 3µA x CR x BIASC
	1	BIASC3	
	0	BIASC2	**Open loop:**
4	1	BIASC1	IBIAS ~ 150µA x BIASC in source mode
	0	BIASC0	IBIAS ~ 100µA x BIASC in sink mode

Table 19. Register Functionality (continued)

REGISTER	BIT	SYMBOL	FUNCTION
6	7	EQADJ7	**Equalizer adjustment setting**
	6	EQADJ6	
	5	EQADJ5	EQENA = 0 (see above)
	4	EQADJ4	Equalizer is turned off and bypassed
	3	EQADJ3	
	2	EQADJ2	EQENA = 1 (see above)
	1	EQADJ1	Maximum equalization for 00000000
	0	EQADJ0	Minimum equalization for 11111111
7	7	CPSGN	Eye cross-point adjustment setting
	6	CPADJ6	CPSGN = 1 (positive shift)
	5	CPADJ5	Maximum shift for 1111111
	4	CPADJ4	Minimum shift for 0000000
	3	CPADJ3	CPSGN = 0 (negative shift)
	2	CPADJ2	Maximum shift for 1111111
	1	CPADJ1	Minimum shift for 0000000
	0	CPADJ0	
8	7	IDRV	**Output Driver Tail Current Bit** 1 = Output driver tail current is increased 0 = Output driver tail current is set to default
	6	-	
	5	-	
	4	CPREF	**Cross point temperature coefficient selection bit** 1 = Reverses the behavior and EQENA = 1: temperature coefficient disabled and EQENA = 0: temperature coefficient enabled 0 = Default condition and EQENA = 1: temperature coefficient enabled and EQENA = 0: temperature coefficient disabled
	3	-	
	2	CPENA	**Cross point adjustment enable bit** 1 = Cross point adjustment is enabled 0 = Cross point adjustment is disabled
	1 0	CPRNG1 CPRNG0	**Cross point adjustment range bits** Minimum adjustment range for 00 Maximum adjustment range for 11
9	7	**LIMCSGN**	Limiter bias current sign bit 1 = Decrease limiter bias current 0 = Increase limiter bias current
	6 5 4	LIMC2 LIMC1 LIMC0	**Limiter bias current selection bits** 000 = No change 111 = Maximum current change
	3	EFCSGN	**Emitter follower sign bit** 1 = Decrease emitter follower current 0 = Increase emitter follower current
	2 1 0	EFC2 EFC1 EFC0	Emitter follower current selection bits 000 = No change 111 = Maximum current change

Table 19. Register Functionality (continued)

REGISTER	BIT	SYMBOL	FUNCTION
10	7	-	
	6	-	
	5	-	
	4	-	
	3	-	
	2	MONPFLT	**Analog photodiode current monitor fault trigger bit** 1 = Fault trigger on MONP pin is enabled 0 = Fault trigger on MONP pin is disabled
	1	DMONP	**Digital photodiode current monitor selection bit (MONP)** 1 = Digital photodiode monitor is active (external resistor must not be installed) 0 = Analog photodiode monitor is active (external resistor is required)
	0	DMONB	**Digital bias current monitor selection bit (MONB)** 1 = Digital bias current monitor is active (external resistor must not be installed) 0 = Analog bias current monitor is active (external resistor is required)
11	7	BMF7	**Bias current monitor fault threshold** With DMONB = 1 Register sets the value of the bias current that will trigger a fault. The external resistor on the MONB pin must be removed to use this feature.
	6	BMF6	
	5	BMF5	
	4	BMF4	
	3	BMF3	
	2	BMF2	
	1	BMF1	
	0	BMF0	
12	7	PMF7	**Power monitor fault threshold** With DMONP = 1 Register sets the value of the photodiode current that will trigger a fault The external resistor on the MONP pin must be removed to use this feature.
	6	PMF6	
	5	PMF5	
	4	PMF4	
	3	PMF3	
	2	PMF2	
	1	PMF1	
	0	PMF0	
13	7	ADCDIS	**ADC disable bit** 1 = ADC disabled 0 = ADC enabled
	6	OSCDIS	**ADC oscillator bit** 1 = Oscillator disabled 0 = Oscillator enabled
	5		
	4		
	3		
	2		
	1 0	ADCSEL1 ADCSEL0	**ADC input selection bits** 00 selects the temperature sensor 01 selects the power supply monitor 10 selects MONP 11 selects MONB

Table 19. Register Functionality (continued)

REGISTER	BIT	SYMBOL	FUNCTION
14	7	ADC9 (MSB)	**Digital representation of the ADC input source (read only)**
	6	ADC8	
	5	ADC7	
	4	ADC6	
	3	ADC5	
	2	ADC4	
	1	ADC3	
	0	ADC2	
15	7	-	
	6	-	
	5	-	
	4	-	
	3	-	
	2	-	
	1	ADC1	**Digital representation of the ADC input source (read only)**
	0	ADC0 (LSB)	

LASER SAFETY FEATURES AND FAULT RECOVERY PROCEDURE

The ONET1141L provides built in laser safety features. The following fault conditions are detected:

1. Voltage at MONB exceeds the voltage at RZTC (1.16V) or, alternately, if DMONB = 1 and the bias current exceeds the bias current monitor fault threshold set by BMF[0..7] (register 11). When using the digital monitor, the resistor to ground must be removed.
2. Voltage at MONP exceeds the voltage at RZTC (1.16V) and the analog photodiode current monitor fault trigger bit, MONPFLT (bit 2 of register 10), is set to 1. Alternately, a fault can be triggered if DMONP = 1 and the photodiode current exceeds the photodiode current monitor fault threshold set by PMF[0..7] (register 12). When using the digital monitor, the resistor to ground must be removed.
3. Photodiode current exceeds 150% of its set value,
4. Bias control DAC drops in value by more than 50% in one step.

If one or more fault conditions occur and the fault enable bit FLTEN is set to 1, the ONET1141L responds by:

1. Setting the bias current to zero.
2. Setting the modulation current to zero.
3. Asserting and latching the FLT pin.

Fault recovery is performed by the following procedure:

1. The disable pin DIS and/or the internal enable control bit ENA are toggled for at least the fault latch reset time.
2. The FLT pin de-asserts while the disable pin DIS is asserted or the enable bit ENA is de-asserted.
3. If the fault condition is no longer present, the part will return to normal operation with its prior output settings after the disable negate time.
4. If the fault condition is still present, FLT re-asserts once DIS is set to a low level and the part will not return to normal operation.

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3V, T_A = 25°C, I_{BIASC} = 80mA, V_{OUT} = 2V_{PP}, V_{IN} = 400mVpp (unless otherwise noted).

DETERMINISTIC JITTER vs MODULATION CURRENT

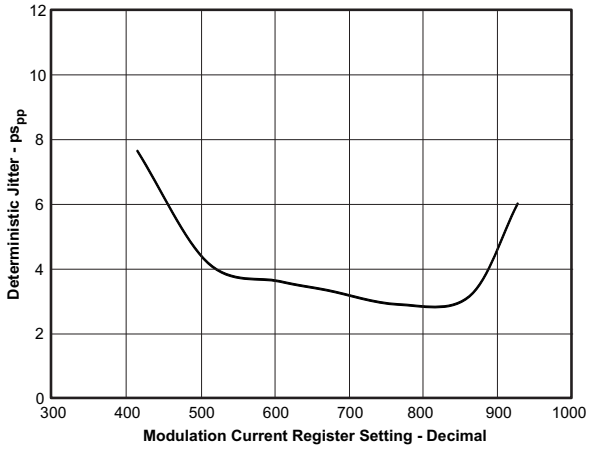


Figure 4.

DETERMINISTIC JITTER vs TEMPERATURE

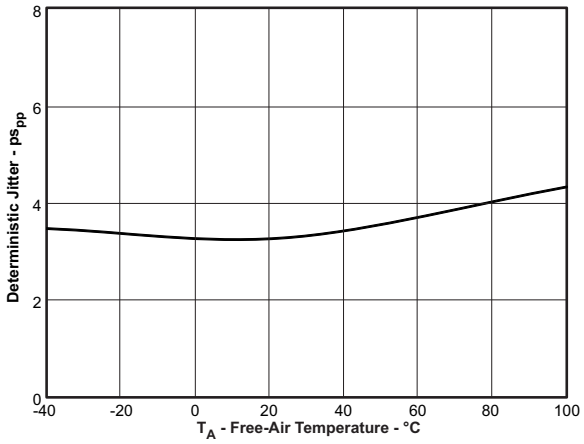


Figure 5.

RANDOM JITTER vs MODULATION CURRENT

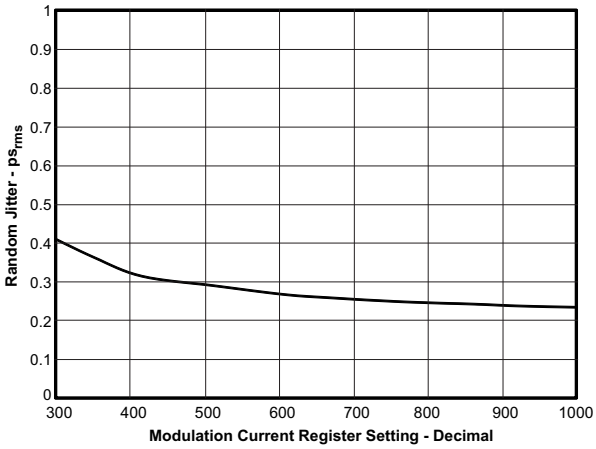


Figure 6.

RANDOM JITTER vs TEMPERATURE

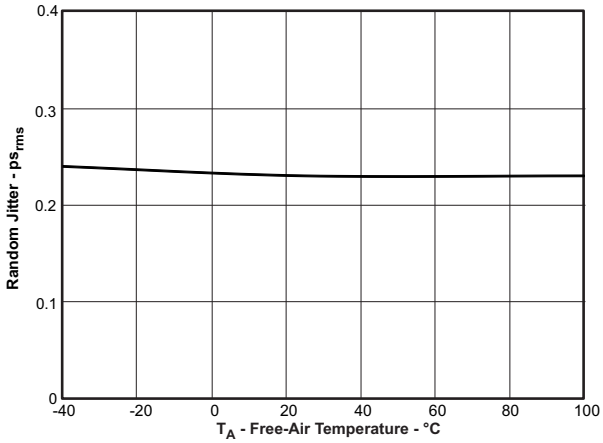


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3V, T_A = 25°C, I_{BIASC} = 80mA, V_{OUT} = 2V_{PP}, V_{IN} = 400mVpp (unless otherwise noted).

RISE-TIME AND FALL-TIME vs MODULATION CURRENT

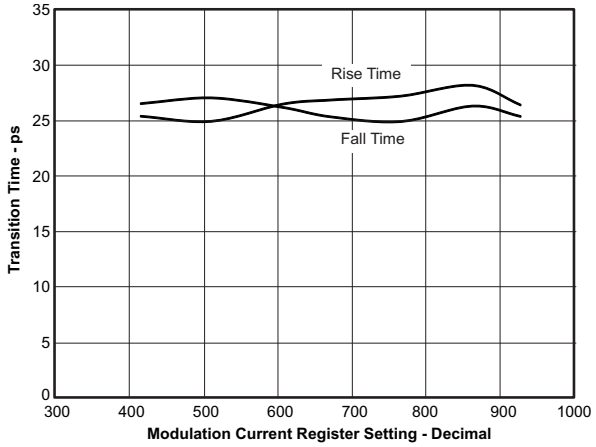


Figure 8.

RISE-TIME AND FALL-TIME vs TEMPERATURE

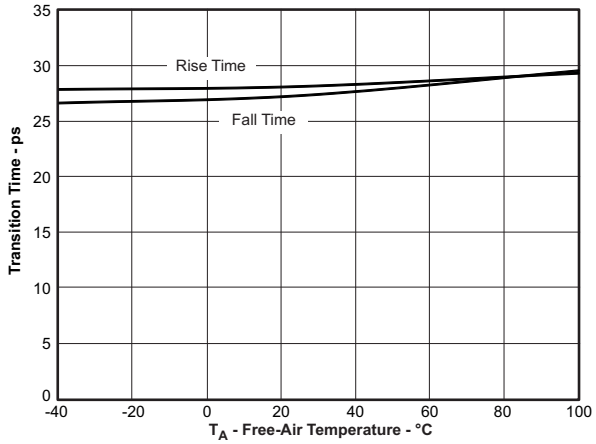


Figure 9.

BIAS CURRENT IN OPEN LOOP MODE vs BIAS CURRENT REGISTER SETTING

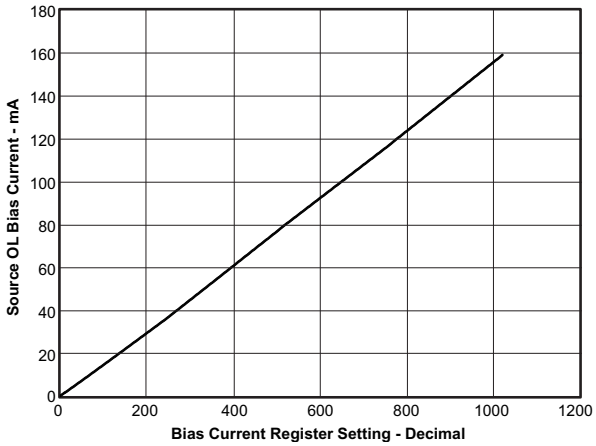


Figure 10.

BIAS CURRENT IN OPEN LOOP MODE vs BIAS CURRENT REGISTER SETTING

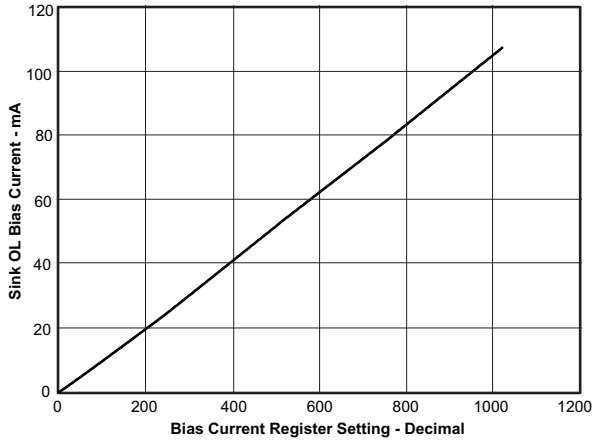


Figure 11.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3V, T_A = 25°C, I_{BIASC} = 80mA, V_{OUT} = 2V_{PP}, V_{IN} = 400mVpp (unless otherwise noted).

BIAS MONITOR CURRENT vs BIAS CURRENT

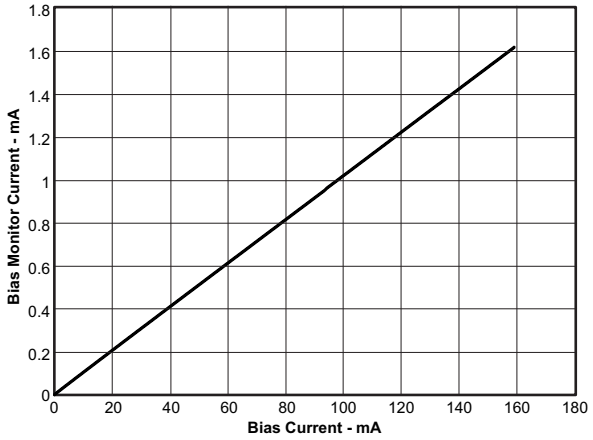


Figure 12.

PHOTODIODE MONITOR CURRENT vs PHOTODIODE CURRENT

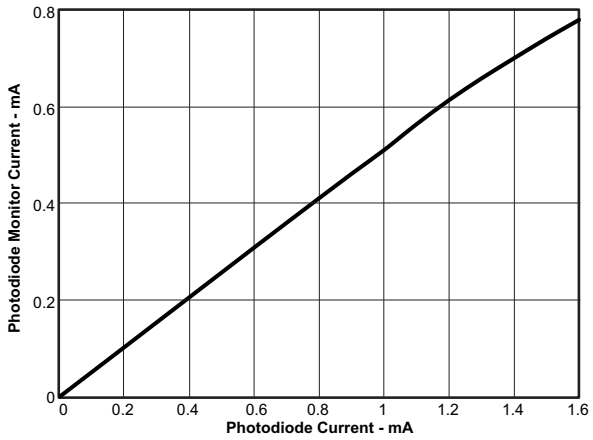


Figure 13.

OUTPUT VOLTAGE vs MODC REGISTER SETTING

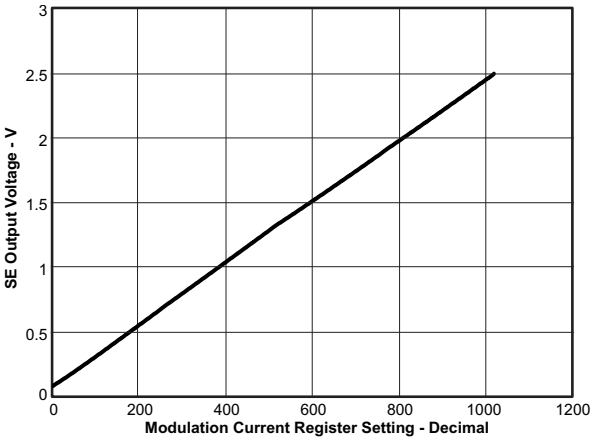


Figure 14.

SUPPLY CURRENT vs TEMPERATURE

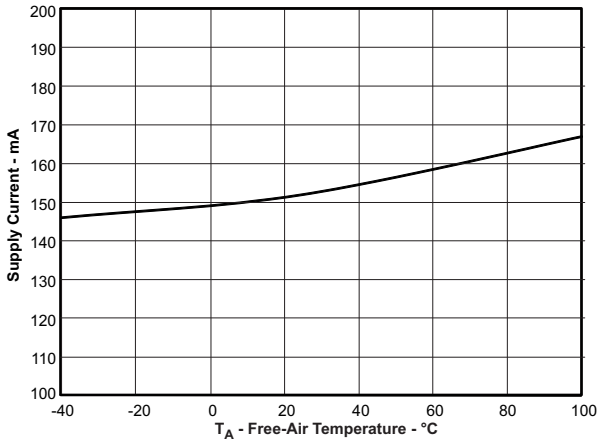


Figure 15.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3V, T_A = 25°C, I_{BIASC} = 80mA, V_{OUT} = 2V_{PP}, V_{IN} = 400mVpp (unless otherwise noted).

EYE-DIAGRAM AT 10.31GBPS
V_{OUT}=2V_{PP}, EQ Set to 00

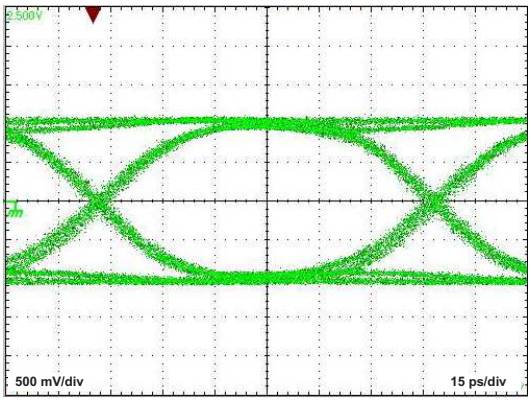


Figure 16.

EYE-DIAGRAM AT 11.3GBPS
V_{OUT}=2V_{PP}, EQ Set to 00, 50% Cross Point

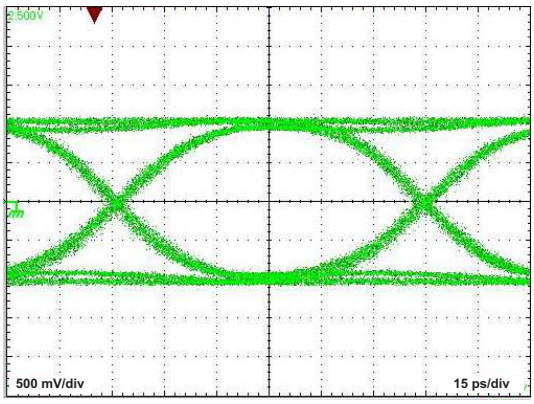


Figure 17.

EYE-DIAGRAM AT 11.3GBPS
V_{OUT}=2V_{PP}, EQ Set to 00, 30% Cross Point

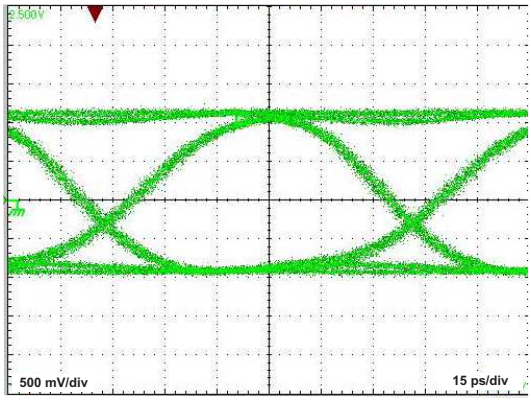


Figure 18.

EYE-DIAGRAM AT 11.3GBPS
V_{OUT}=2V_{PP}, EQ Set to 00, 70% Cross Point

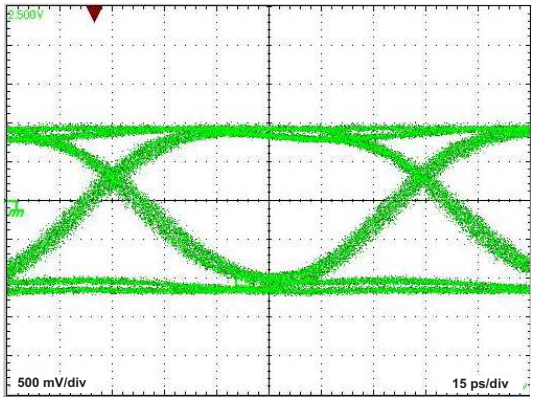


Figure 19.

EYE-DIAGRAM AT 11.3GBPS
V_{OUT}=2V_{PP}, EQ Set to 00,
6'' OF FR4 AT INPUTS

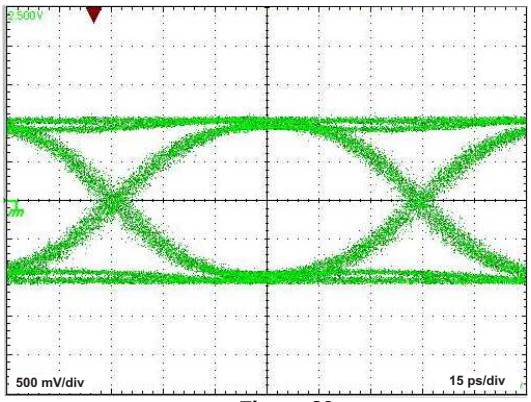


Figure 20.

APPLICATION INFORMATION

Figure 21 and Figure 22 show typical application circuits using the ONET1141L. The modulator must be AC coupled to the driver for proper operation. The laser driver is controlled via the 2-wire interface SDA/SCK by a microcontroller. In a typical application, the FLT, MONB and MONP outputs are also connected to the microcontroller for transceiver management purposes.

The component values in Figure 21 and Figure 22 are typical examples and may be varied according to the intended application.

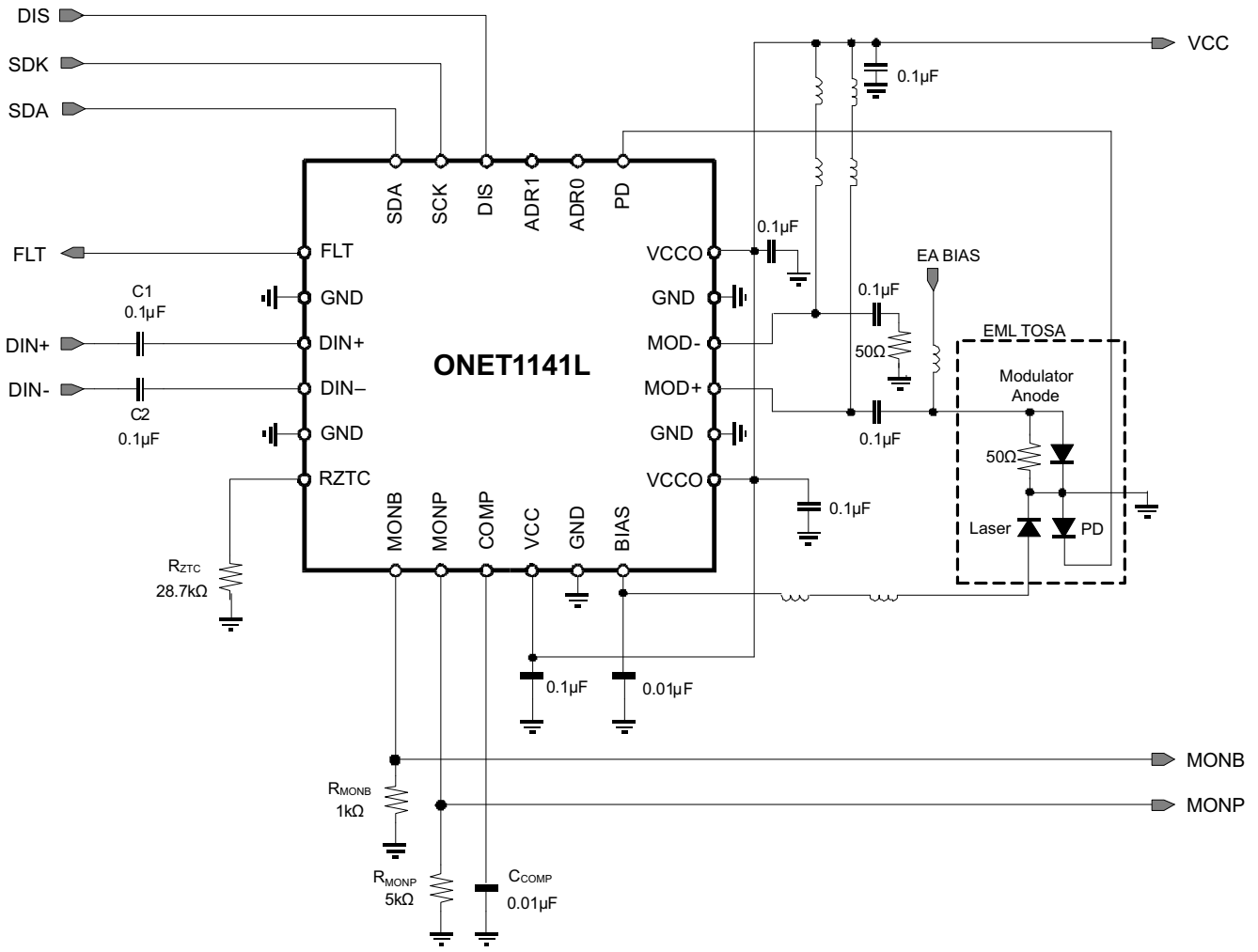


Figure 21. AC Coupled Drive with PD Monitor Cathode Available

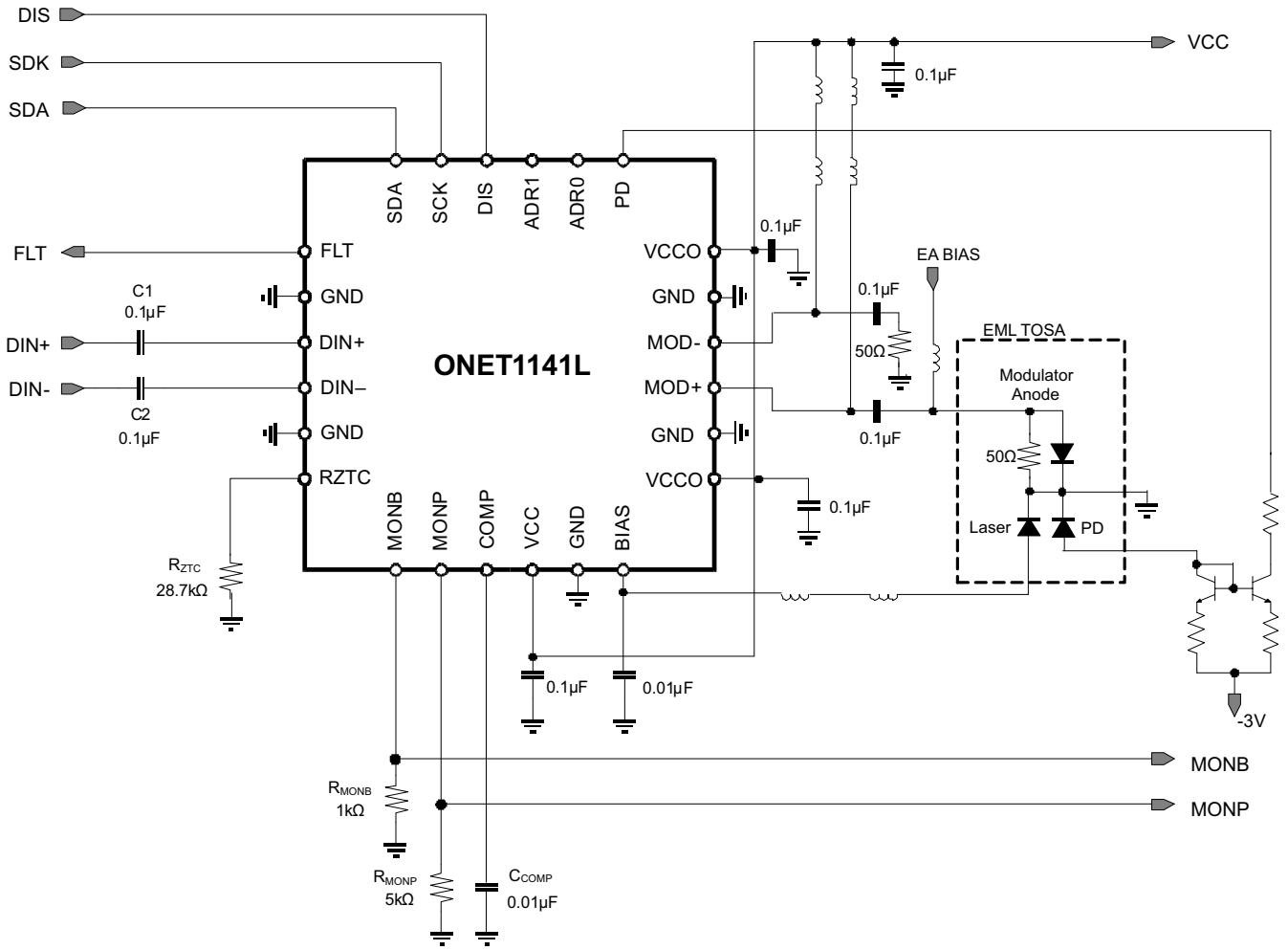


Figure 22. AC Coupled Drive with PD Monitor Anode Available

Layout Guidelines

For optimum performance, use 50Ω transmission lines (100Ω differential) for connecting the signal source to the DIN+ and DIN– pins and 50Ω transmission lines (100Ω differential) for connecting the modulation current outputs, MOD+ and MOD–, to the laser. The length of the transmission lines should be kept as short as possible to reduce loss and pattern-dependent jitter.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ONET1141LRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 100	ONET 1141L	Samples
ONET1141LRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 100	ONET 1141L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

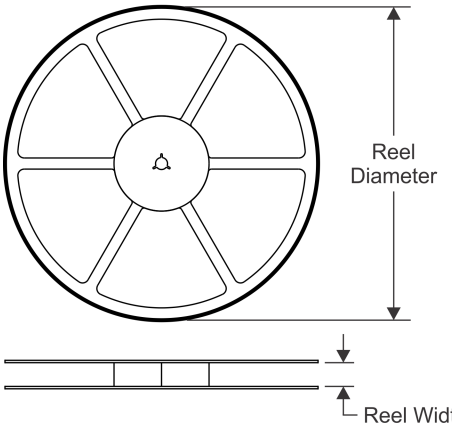
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

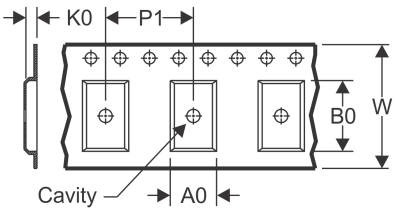
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

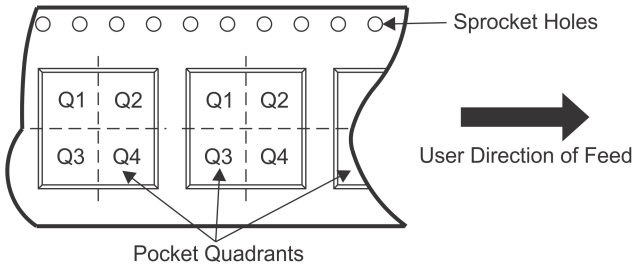


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

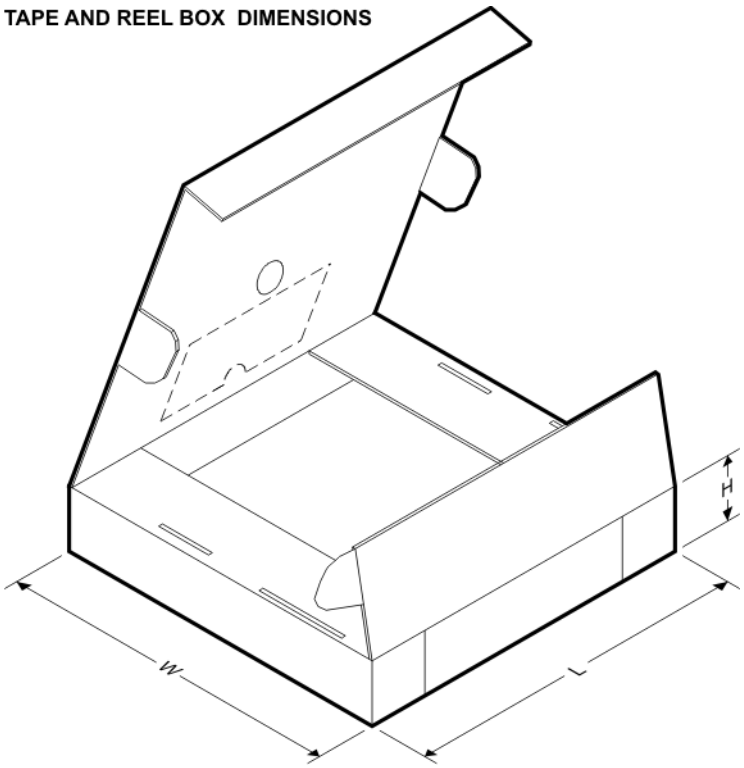
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET1141LRGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
ONET1141LRGET	VQFN	RGE	24	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

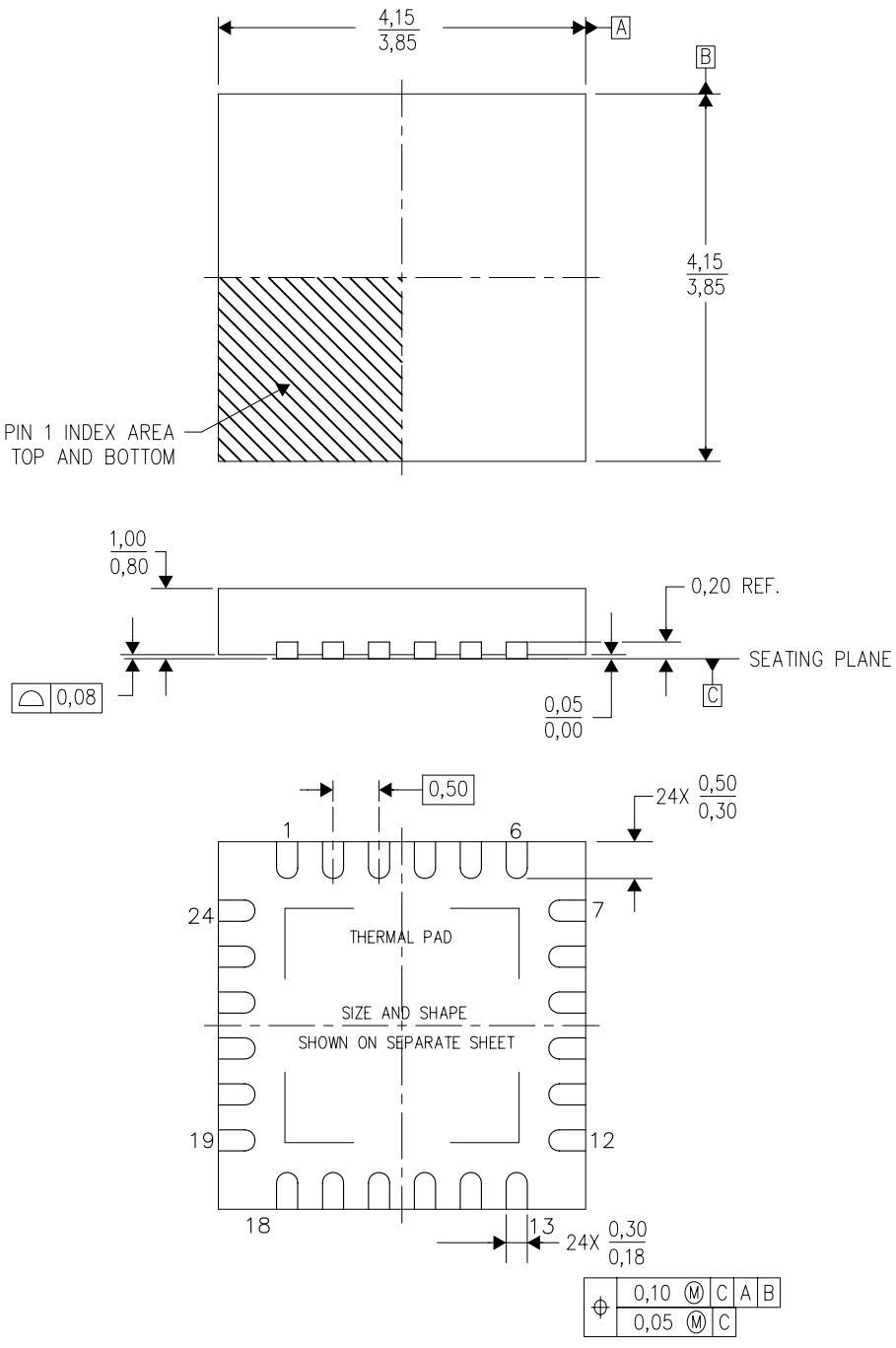
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET1141LRGER	VQFN	RGE	24	3000	338.1	338.1	20.6
ONET1141LRGET	VQFN	RGE	24	250	338.1	338.1	20.6

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

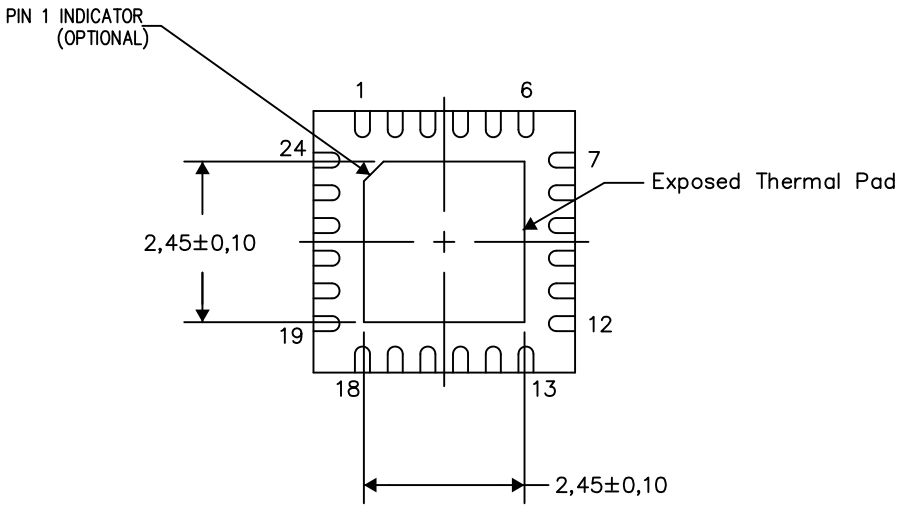
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



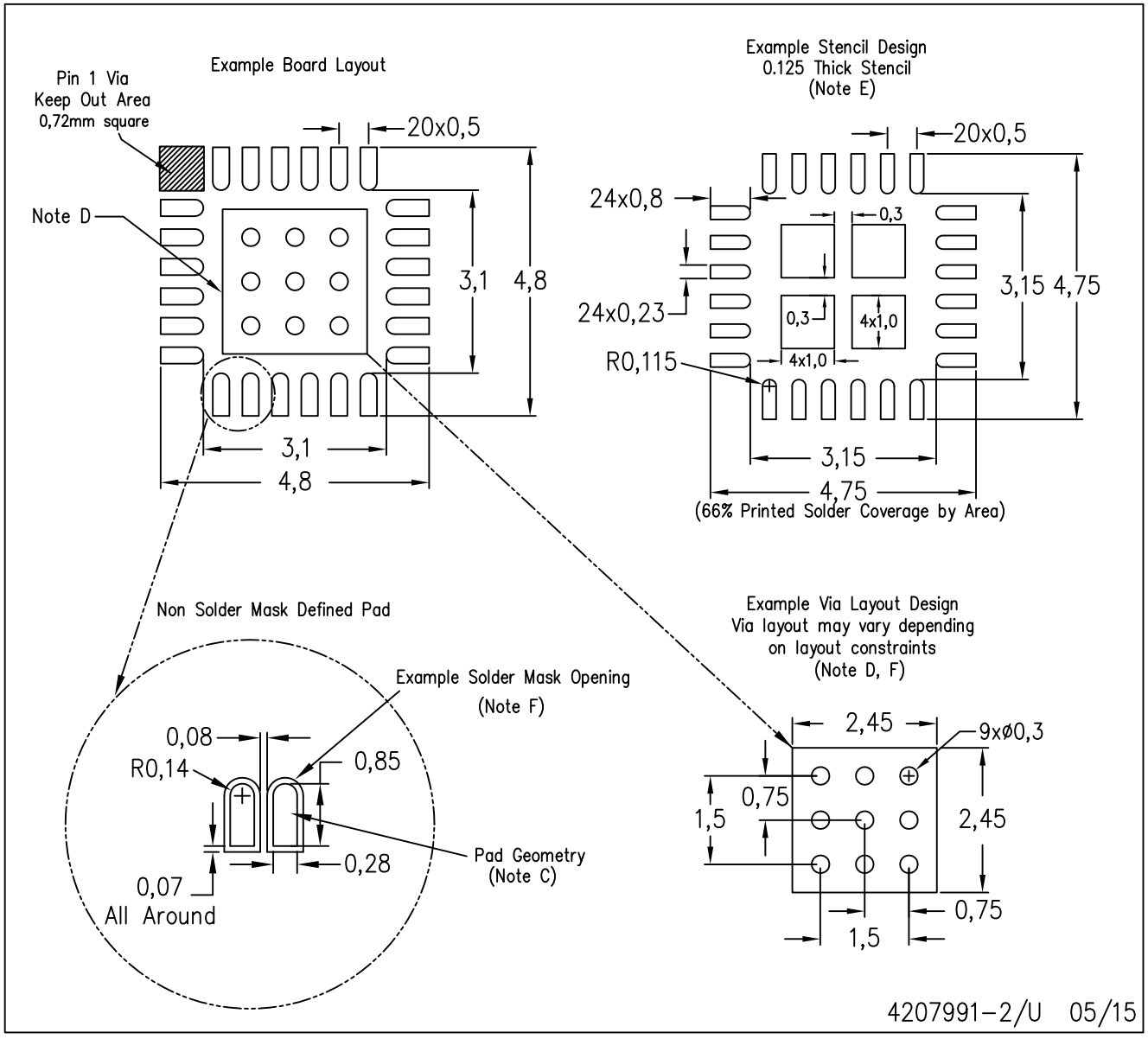
Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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