Low Power, Low Noise, IF and Baseband, Dual 16 bit ADC Driver With Digitally Controlled Gain

Check for Samples: LMH6517

FEATURES

- **Accurate, 0.5dB Gain Steps**
- **200Ω Resistive, Differential Input**
- **Low Impedance, Differential Output**
- **Disable Function for Each Channel**
- **Parallel Gain Control**
- **SPI Compatible Serial Bus**
- **Two Wire, Pulse Mode Control**
- **On Chip Register Stores Gain Setting**
- **Low Sensitivity of Linearity and Phase to Gain Setting**
- **Single 5V Supply Voltage**
- **Small Footprint WQFN Package**

APPLICATIONS

- **Cellular Base Stations**
- **IF Sampling Receivers**
- **Instrumentation**
- **Modems**
- **Imaging**

KEY SPECIFICATIONS

- **OIP3: 43dBm @ 200MHz**
- **Noise figure 5.5dB**
- **Gain step size of 0.5dB**
- **Gain step accuracy: 0.05dB**
- **Frequency Range of 1200 MHz**
- **Supply current 80mA per channel**

DESCRIPTION

The LMH6517 contains two high performance, digitally controlled variable gain amplifiers (DVGA). It has been designed for use in narrowband and broadband IF sampling applications. Typically the LMH6517 drives a high performance ADC in a broad range of mixed signal and digital communication applications such as mobile radio and cellular base stations where automatic gain control (AGC) is required to increase system dynamic range.

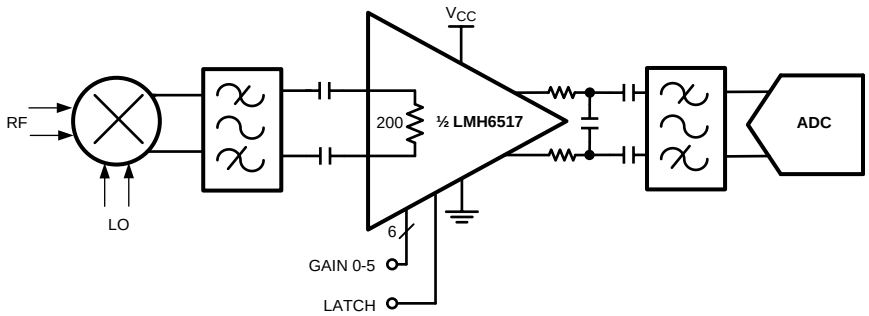
Each channel of LMH6517 has an independent, digitally controlled attenuator and a high linearity, differential output amplifier. Each block has been optimized for low distortion and maximum system design flexibility. Each channel can be individually disabled for power savings.

The LMH6517 digitally controlled attenuator provides precise 0.5dB gain steps over a 31.5dB range. On chip digital latches are provided for local storage of the gain setting. Both serial and parallel programming options are provided. A Pulse mode is also offered where simple up or down commands can change the gain one step at a time.

The output amplifier has a differential output allowing large signal swings on a single 5V supply. The low impedance output provides maximum flexibility when driving filters or analog to digital converters.

The LMH6517 operates over the industrial temperature range of −40°C to +85°C. The LMH6517 is available in a 32-Pin, thermally enhanced, WQFN package.

Typical Application: IF Sampling Receiver



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	2 kV
Machine Model	100V
Charged Device Model	750V
Positive Supply Voltage (Pin 3)	−0.6V to 5.5V
Differential Voltage between Any Two Grounds	<200 mV
Analog Input Voltage Range	−0.6V to V+
Digital Input Voltage Range	−0.6V to 3.6V
Output Short Circuit Duration (one pin to ground)	Infinite
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Infrared or Convection (30 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Operating Ratings (1)

Supply Voltage (Pin 3)	4.5V to 5.25V
Differential Voltage Between Any Two Grounds	<10 mV
Analog Input Voltage Range, AC Coupled	0V to V+
Temperature Range (2)	−40°C to +85°C
Package Thermal Resistance (θ_{JA})	
32-Pin WQFN	42°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

5V Electrical Characteristics (1)

The following specifications apply for single supply with V+ = 5V, Maximum Gain , R_L = 100Ω, V_{OUT} = 2 V_{PP}, fin = 150 MHz. Boldface limits apply at temperature extremes.

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
Dynamic Performance						
SSBW	Frequency Range			1200		MHz
	Maximum Voltage Gain	f = 200 MHz		22		dB
	Input Noise Voltage	Maximum Gain, f > 1MHz, R_{IN}= 0 Ω		1.1		nV/√Hz
	Output Noise Voltage	Maximum Gain, f > 1MHz		22		nV/√Hz
	Noise Figure	Maximum Gain		5.5		dB
OIP3	Output Third Order Intercept Point	f = 150 MHz, V_{OUT} = 4dBm per tone		43		dBm
	Output Third Order Intercept Point	f = 200 MHz, V_{OUT} = 4dBm per tone		43		
IMD3	Third Order Intermodulation Products	f = 150 MHz, V_{OUT} = 4dBm per tone		−78		dBc
	Third Order Intermodulation Products	f = 200 MHz, V_{OUT} = 4dBm per tone		−78		
P1dB	1dB Compression Point	f = 150 MHz, R_L= 100Ω		18.3		dBm
	1dB Compression Point	f= 150 MHz, R_L= 200Ω		15.5		
Analog I/O						
	Input Resistance	Differential	170	200	220	Ω
	Input Capacitance			2		pF
	Input Common Mode Voltage	Self Biased	2.42 **2.24**	2.55	2.71 **2.79**	V
	Input Common Mode Voltage Range	Externally Driven, CMRR > 40dB	1.5		3.5	V
	Maximum Input Voltage Swing	Volts peak to peak, differential		5.5		V
	Output Common Mode Voltage	Self Biased	2.4	2.55	2.7	V
	Maximum DIfferential Output Voltage Swing	Differential		5.9		V_{PP}
	Output Voltage Swing	Single ended (each output)	1.05	1V to 4V	4.00	V
V_{OS}	Output Offset Voltage	All Gain Settings	−25 **-30**	−2	25 **30**	mV
CMRR	Common Mode Rejection Ratio	Maximum Gain, f=100MHz		60		dB
PSRR	Power Supply Rejection Ratio	Maximum Gain, f=100MHz		60		dB
XTLK	Channel to Channel Crosstalk	Maximum Gain, f=100MHz		−85		dBc
XTLK	Channel to Channel Crosstalk	Maximum Gain, f=300MHz		−72		dBc
Gain Parameters						
	Maximum Gain	Gain Code 000000, DC Voltage Gain	21.7 **21.65**	21.85	22 **22.05**	dB
	Minimum Gain	Gain Code 111111, DC Voltage Gain	−9.25 **−9.1**	−9.5	−9.78 **−9.8**	dB
	Gain Adjust Range			31.5		dB
	Gain Step Size			0.5		dB
	Channel Matching	Gain Error between A and B channel.		±0.05		dB
	Channel Matching	Phase Shift between A and B channel.		±0.1		°
	Gain Step Error	Any two steps	−0.3	±0.05	0.3	dB
	Gain Step Error	Maximum Gain to Maximum Gain −12dB	−0.5	±0.1	0.5	dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No specification of parametric performance is indicated in the electrical tables under conditions different than those tested

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

5V Electrical Characteristics [1] (continued)

The following specifications apply for single supply with V+ = 5V, Maximum Gain , R_L = 100Ω, V_{OUT} = 2 V_{PP}, fin = 150 MHz. Boldface limits apply at temperature extremes.

Parameter		Test Conditions	Min [2]	Typ [3]	Max [2]	Units
	Gain Step Phase Shift	between any two steps		0.5		°
	Gain Step Switching Time			15		ns
Power Requirements						
ICC	Supply Current	Each channel (two channels per package)		80	91	mA
P	Power	Each Channel		400		mW
ICC	Disabled Supply Current	Each Channel		7.5		mA
All Digital Inputs						
	Logic Compatibility	TTL, 2.5V CMOS, 3.3V CMOS				
VIL	Logic Input Low Voltage		0		0.4	V
VIH	Logic Input High Voltage		2.0		3.6	V
IIH	Logic Input High Input Current	Digital Input Voltage = 3.3V	−110		110	µA
IIL	Logic Input Low Input Current	Digital Input Voltage = 0V	−110		110	µA
Parallel and Pulse Mode Timing						
t_{GS}	Setup Time		3			ns
t_{GH}	Hold Time		3			ns
t_{LP}	Latch Low Pulse Width		7			ns
t_{PG}	Pulse Gap between Pulses		20			ns
t_{PW}	Minimum Latch Pulse Width		20			ns
t_{RW}	Reset Width		10			ns
Serial Mode Timing and AC Characteristics						
SPI Compatible						
f_{SCLK}	Serial Clock Frequency				10.5	MHz
t_{PH}	SCLK High State Duty Cycle	% of SCLK Period	40		60	%
t_{PL}	SCLK Low State Duty cycle	% of SCLK Period	40		60	%
t_{SU}	Serial Data In Setup Time			0.5		ns
t_H	Serial Data In Hold Time			5		ns
t_{ODZ}	Serial Data Out Driven-to- Tri-State Time	Referenced to Positive edge of CS		40	50	ns
t_{OZD}	Serial Data Out Tri-State-to-Driven Time	Referenced to Negative edge of SCLK		15	20	ns
t_{OD}	Serial Data Out Output Delay TIme	Referenced to Negative edge of SCLK		15	20	ns
t_{CSS}	Serial Chip Select Setup TIme	Referenced to Positive edge of SCLK	10	5		
t_{CSH}	Serial Chip Select Hold TIme	Referenced to Positive edge of SCLK	10	5		
t_{IAG}	Inter-Access Gap	Minimum time Serial Chip Select pin must be asserted between accesses.		3		Cycles of SCLK

CONNECTION DIAGRAM

Top View

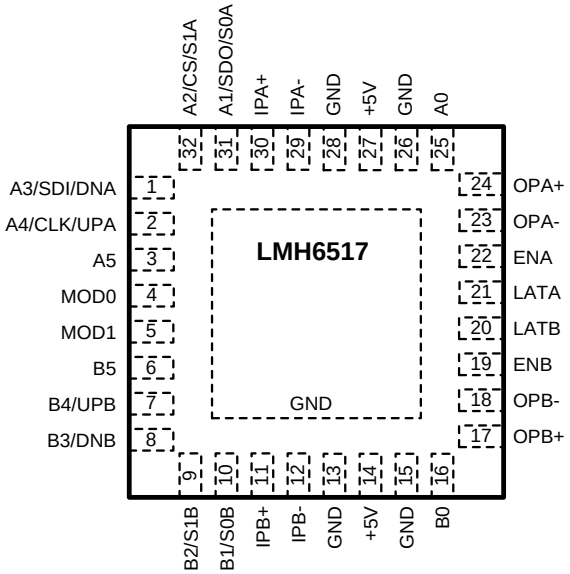


Figure 1. 32-Pin WQFN Package
See Package Number RTV0032A

PIN DESCRIPTIONS

Pin Number	Pin Name	Description
Analog I/O		
30, 11	IPA+, IPB+	Amplifier non—inverting input. Internally biased to mid supply. Input voltage should not exceed V+ or go below GND by more than 0.5V.
29, 12	IPA−, IPB−	Amplifier inverting input. Internally biased to mid supply. Input voltage should not exceed V+ or go below GND by more than 0.5V.
24, 17	OPA+, OPB+	Amplifier non—inverting output. Internally biased to mid supply.
23, 18	OPA−, OPB−	Amplifier inverting output. Internally biased to mid supply.
Power		
13, 15, 26, 28, center pad	GND	Ground pins. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is internally bonded to the ground pins.
14, 27	+5V	Power supply pins. Valid power supply range is 4.5V to 5.25V.
Common Control Pins		
4, 5	MOD0, MOD1	Digital Mode control pins. These pins float to the logic hi state if left unconnected. See below for Mode settings.
22, 19	ENA, ENB	Enable pins. Logic 1 = enabled state. See Application Information for operation in serial mode.
Digital Inputs Parallel Mode (MOD1 = 1, MOD0 = 1)		
25, 16	A0, B0	Gain bit zero = 0.5dB step. Gain steps down from maximum gain (000000 = Maximum Gain)
31, 10	A1, B1	Gain bit one = 1dB step
32, 9	A2, B2	Gain bit two = 2dB step
1, 8	A3, B3	Gain bit three = 4dB step
2, 7	A4, B4	Gain bit four = 8dB step
3, 6	A5, B5	Gain bit five = 16dB step

PIN DESCRIPTIONS (continued)

Pin Number	Pin Name	Description
21, 20	LATA, LATB	Latch pins. Logic zero = active, logic 1 = latched. Gain will not change once latch is high. Connect to ground if the latch function is not desired.

PIN DESCRIPTIONS (continued)

Pin Number	Pin Name	Description
Digital Inputs Serial Mode (MOD1 =1 , MOD0 = 0)		
2	CLK	Serial Clock
1	SDI	Serial Data In (SPI Compatible) See Application Information for more details.
32	CS	Serial Chip Select (SPI compatible)
31	SDO	Serial Data Out (SPI compatible)
3, 4, 6 — 10, 16, 20, 21, 25	GND	Pins unused in Serial Mode, connect to DC ground.
Digital Inputs Pulse Mode (MOD1 = 0 , MOD0 = 1)		
2, 7	UPA, UPB	Up pulse pin. A logic 0 pulse will increase gain one step.
1, 8	DNA, DNB	Down pulse pin. A logic 0 pulse will decrease gain one step.
1 & 2 or 7 & 8		Pulsing both pins together will reset the gain to maximum gain.
31, 32	S0A, S1A	Step size zero and step size 1. (0,0) = 0.5dB; (0, 1)= 1dB; (1,0) = 2dB, and (1, 1)= 6dB
10, 9	S0B, S1B	Step size zero and step size 1. (0,0) = 0.5dB; (0, 1)= 1dB; (1,0) = 2dB, and (1, 1)= 6dB
3, 5, 6, 16, 25	GND	Pins unused in Pulse Mode, connect to DC ground.

Typical Performance Characteristics

V_{CC} = 5V

Frequency Response 2dB Gain Steps

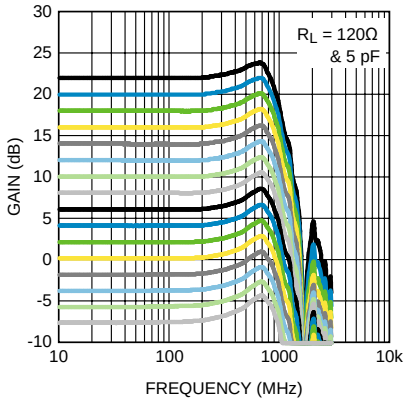


Figure 2.

Frequency Response 2dB Gain Steps Transformer Coupled

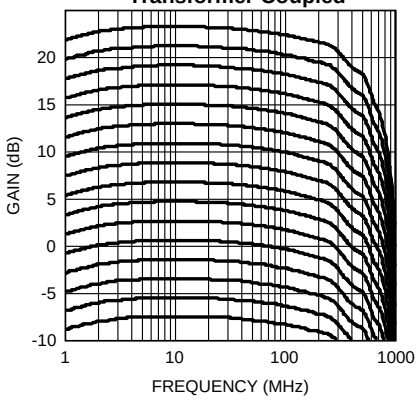


Figure 3.

Gain Flatness over Temperature

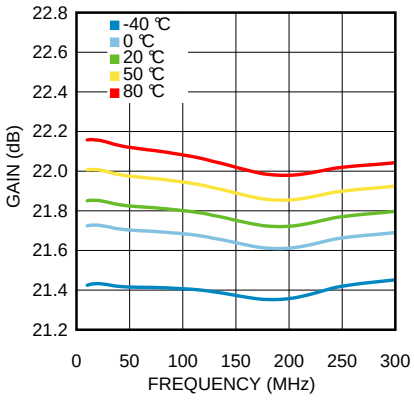


Figure 4.

Group Delay

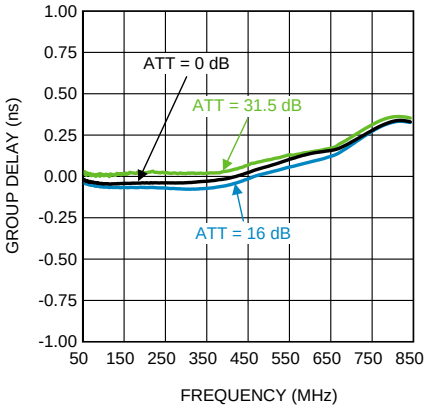


Figure 5.

Third Order Intercept Point vs Frequency

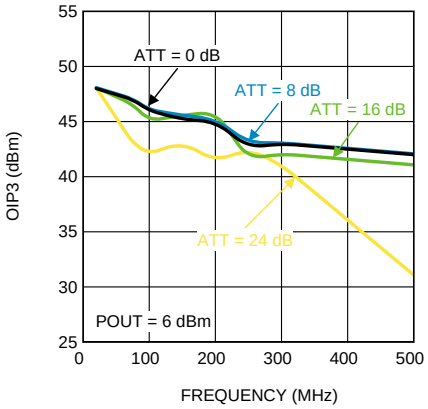


Figure 6.

Third Order Intermodulation Products vs Frequency

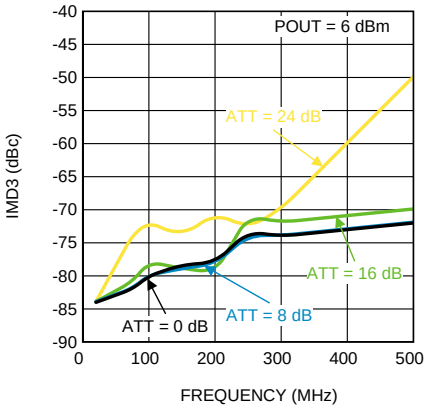


Figure 7.

Typical Performance Characteristics (continued)

V_{CC} = 5V

Third Order Intercept Point at Various Attenuator Settings
f = 150 MHz

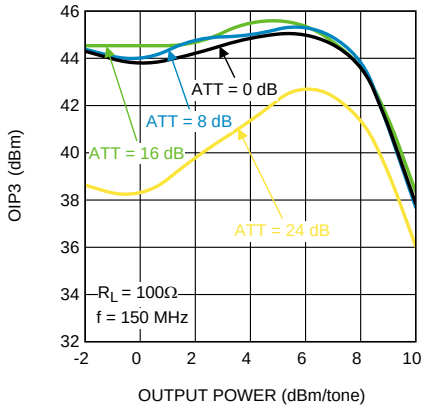


Figure 8.

Third Order Intercept Point at Various Attenuator Settings
f = 200 MHz

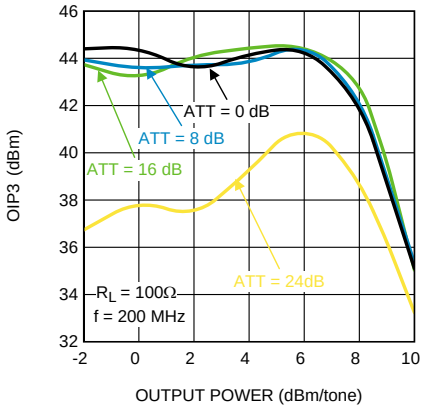


Figure 9.

Third Order Intercept Point at Various Attenuator Settings
f = 250 MHz

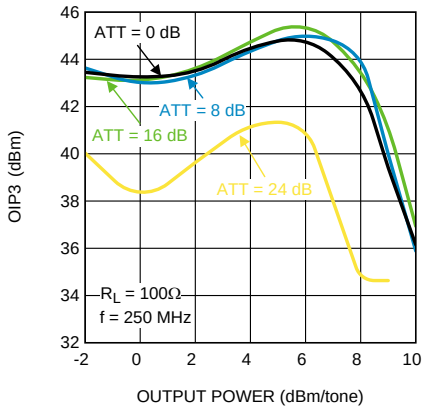


Figure 10.

Third Order Intermodulation at Various Attenuator Settings
f = 200 MHz

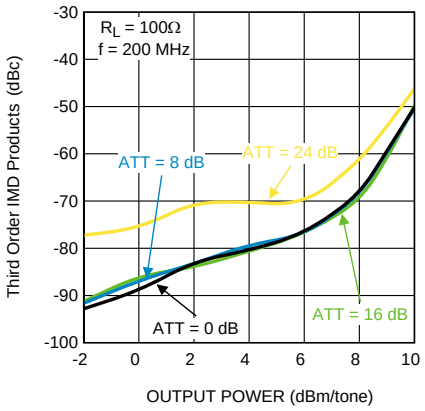


Figure 11.

OIP3
vs
Temperature

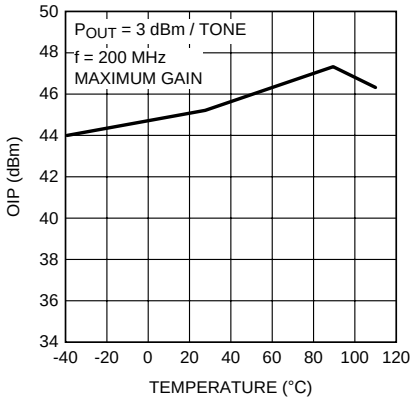


Figure 12.

Gain Shift
vs
Temperature

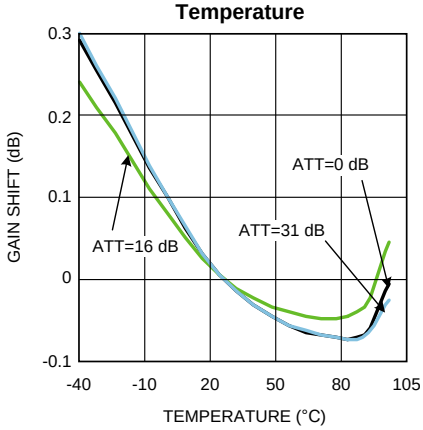


Figure 13.

Typical Performance Characteristics (continued)

V_{CC} = 5V

Cumulative Gain Error vs Attenuator Setting

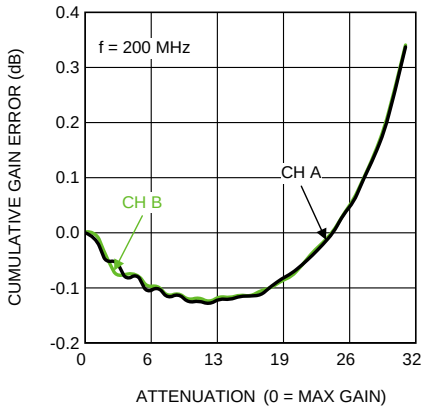


Figure 14.

Cumulative Gain Error over Temperature

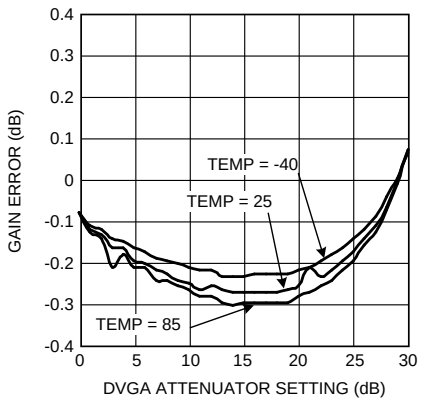


Figure 15.

Phase Shift vs Attenuator Setting

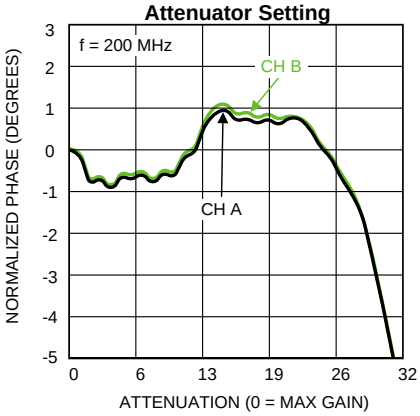


Figure 16.

Noise Figure vs Attenuator Setting

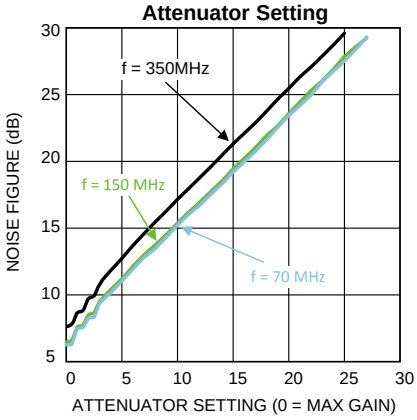


Figure 17.

Noise Figure vs. Temperature

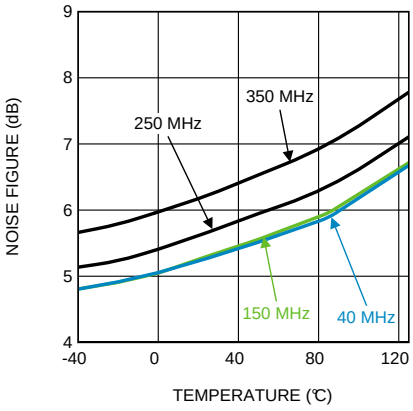


Figure 18.

Noise Figure vs Frequency

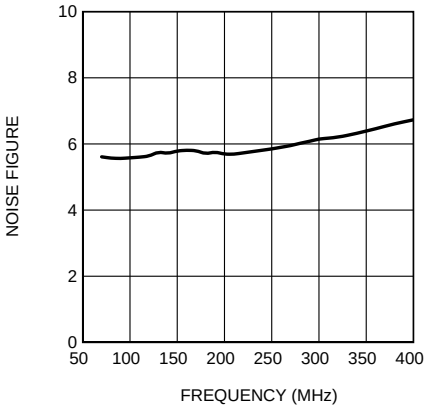


Figure 19.

Typical Performance Characteristics (continued)

V_{CC} = 5V

Second Order Harmonic Distortion at 10 MHz

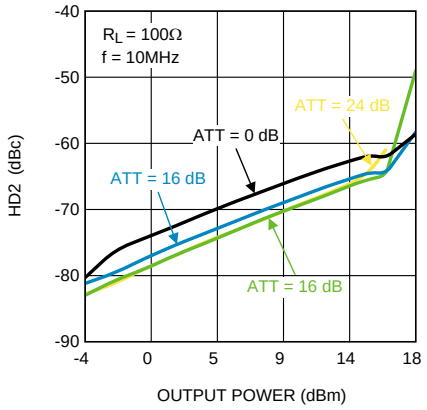


Figure 20.

Third Order Harmonic Distortion at 10 MHz

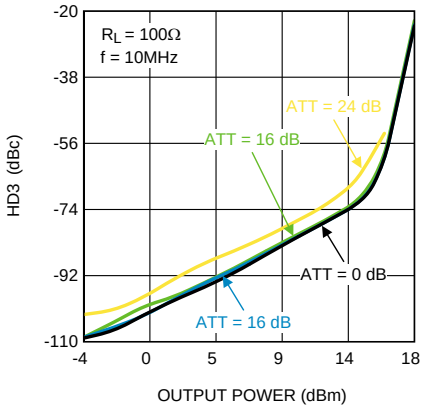


Figure 21.

Second Order Harmonic Distortion at 75 MHz

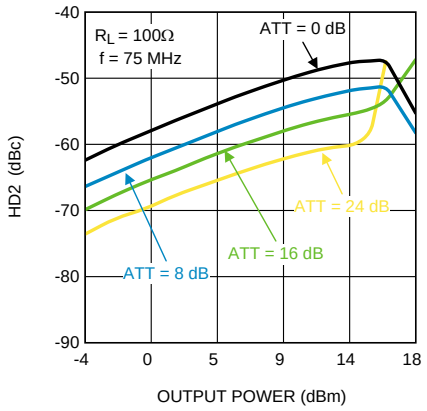


Figure 22.

Third Order Harmonic Distortion at 75 MHz

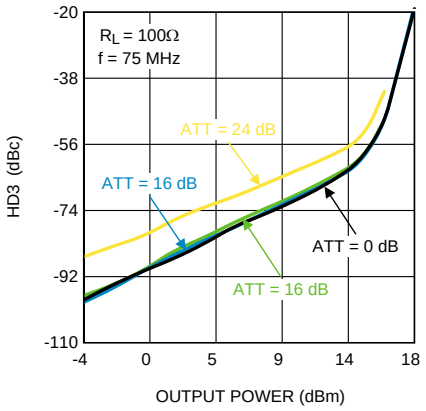


Figure 23.

Second Order Harmonic Distortion at 150 MHz

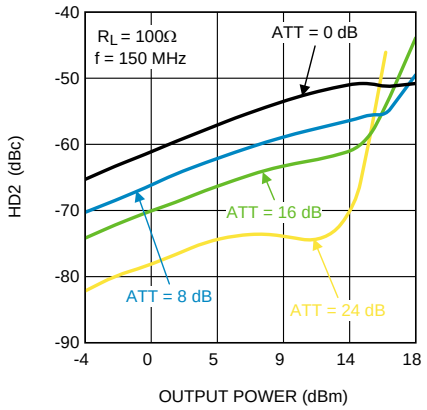


Figure 24.

Third Order Harmonic Distortion at 150 MHz

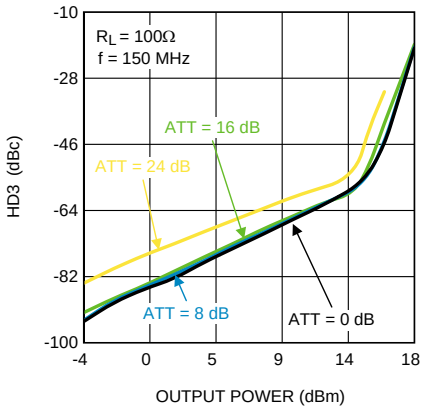


Figure 25.

Typical Performance Characteristics (continued)

V_{CC} = 5V

Second Order Harmonic Distortion at 200 MHz

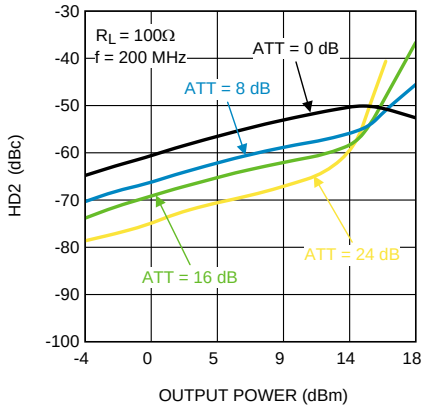


Figure 26.

Third Order Harmonic Distortion at 200 MHz

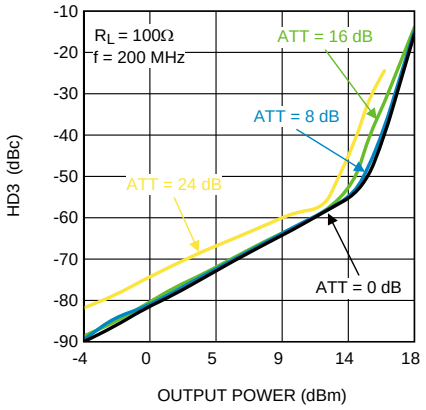


Figure 27.

Second Order Harmonic Distortion at 250 MHz

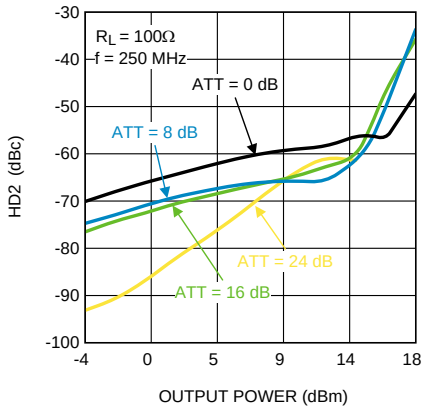


Figure 28.

Third Order Harmonic Distortion at 250 MHz

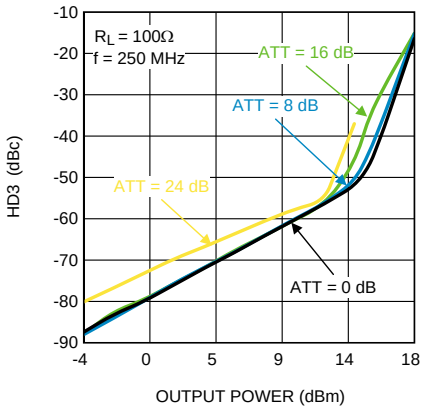


Figure 29.

Max Gain vs. Temperature

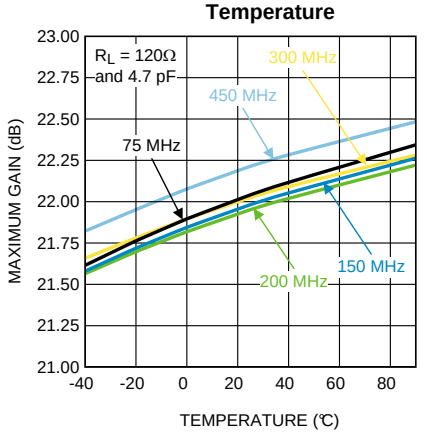


Figure 30.

Supply Current vs Temperature

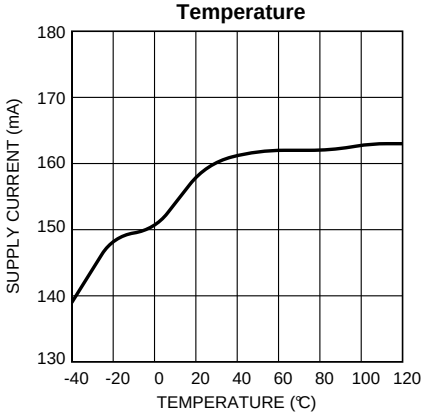


Figure 31.

Typical Performance Characteristics (continued)

V_{CC} = 5V

Output Offset Voltage vs. Temperature

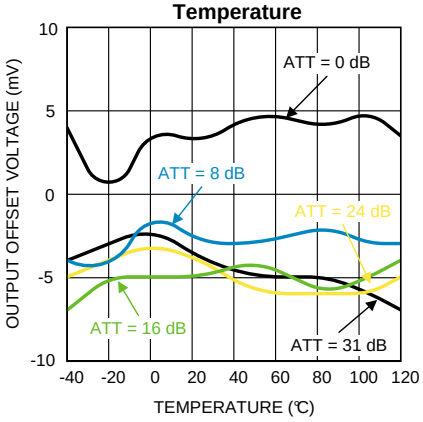


Figure 32.

Pulse Response

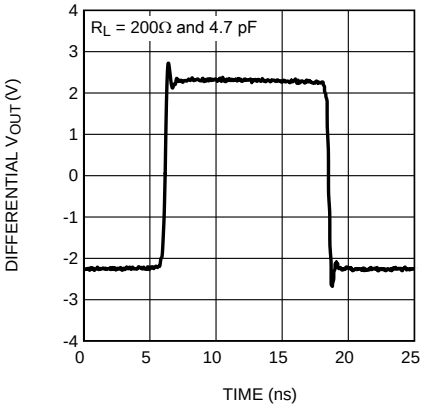


Figure 33.

Gain Change Timing

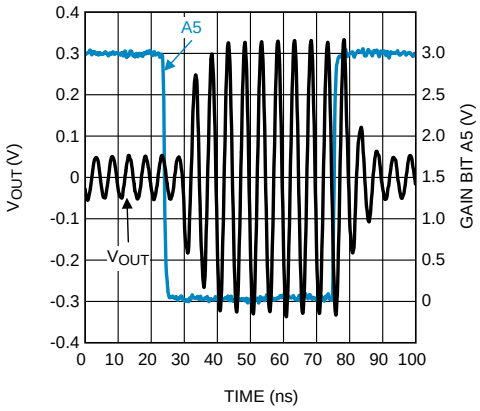


Figure 34.

Enable Timing Maximum Gain

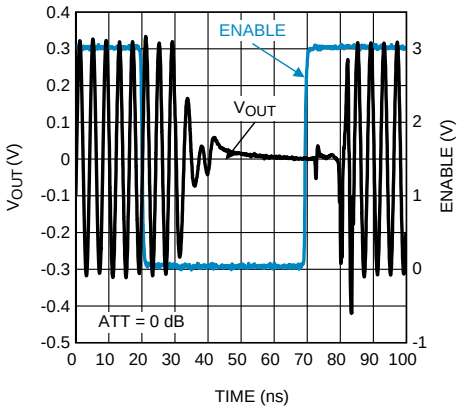


Figure 35.

Enable Timing Minimum Gain

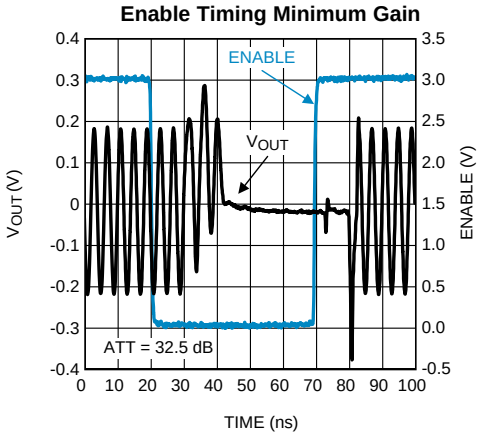


Figure 36.

Channel To Channel Crosstalk

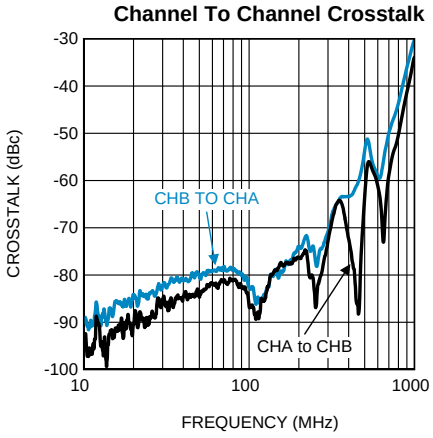


Figure 37.

Typical Performance Characteristics (continued)

V_{CC} = 5V

Input Impedance (S11)

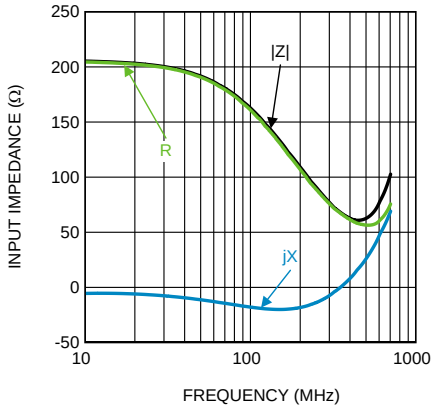


Figure 38.

Output Impedance (S22)

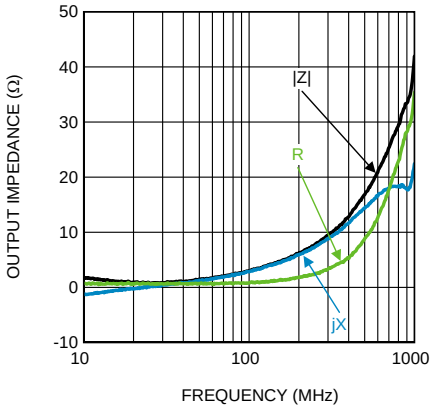


Figure 39.

APPLICATION INFORMATION

The LMH6517 is a fully differential amplifier optimized for signal path applications up to 400 MHz. The LMH6517 has a 200Ω input and a low impedance output. The gain is digitally controlled over a 31.5 dB range from +22dB to −9.5dB. The LMH6517 is optimized for accurate gain steps and minimal phase shift combined with low distortion products. This makes the LMH6517 ideal for voltage amplification and an ideal ADC driver where high linearity is necessary. The LMH6517 was designed for differential signal inputs only. Single ended inputs require a balun or transformer as shown on the evaluation board.

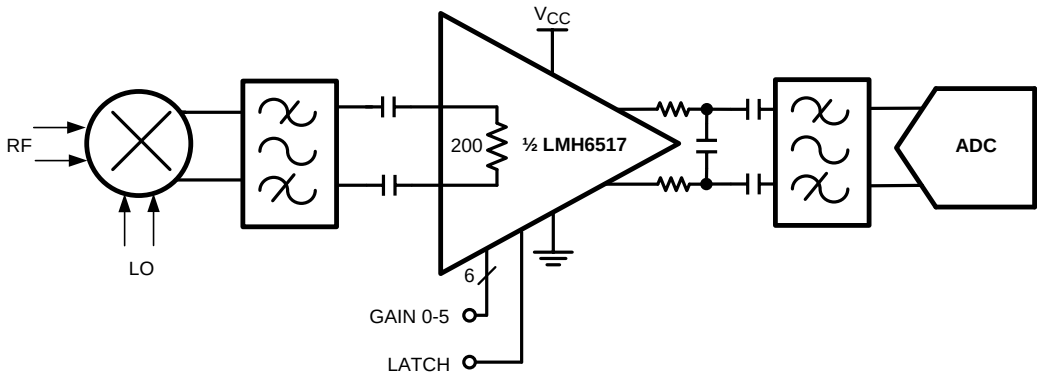


Figure 40. LMH6517 Typical Application

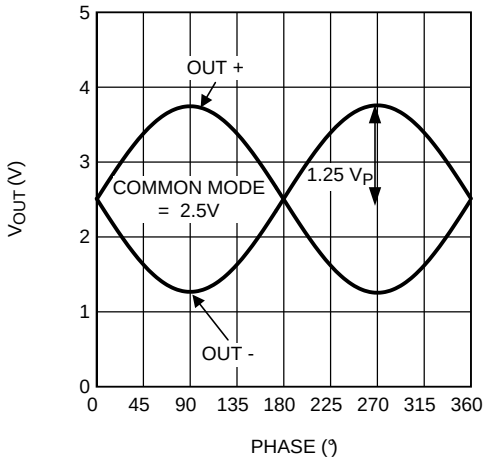


Figure 41. Output Voltage with Respect to the Output Common Mode

In order to help with system design TI offers the SP16160CH1RB High IF Receiver reference design board. This board combines the LMH6517 DVGA with the ADC16DV160 ADC and provides a ready made solution for many IF receiver applications. The SP16160CH1RB delivers an IF chain receiver sensitivity of -105 dBm, with a 9 dB carrier-to-noise ratio in a 200 kHz channel, at 192 MHz input IF. With the digitally-controlled variable gain amplifier (DVGA) set at a maximum gain of 22 dB, the sensitivity is limited primarily by the noise contribution of the DVGA. In the presence of a strong blocker, with the DVGA gain set at 12 dB and blocker level kept at 1.6 dBm input to the ADC, the SP16160CH1RB board delivers sensitivity of -86 dBm. In this blocking condition, the receiver sensitivity is determined by the ADC's high spurious-free dynamic range (SFDR).

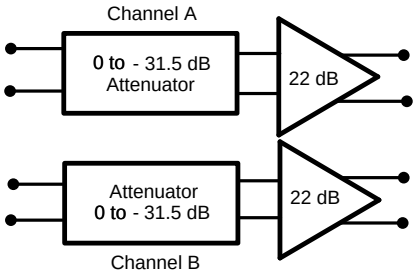


Figure 42. LMH6517 Block Diagram

INPUT CHARACTERISTICS

The LMH6517 input impedance is set by internal resistors to a nominal 200Ω. Process variations will result in a range of values as shown in the 5V Electrical Characteristics table. At higher frequencies parasitic reactances will start to impact the impedance. This characteristic will also depend on board layout and should be verified on the customer's system board.

At maximum gain the digital attenuator is set to 0 dB and the input signal will be much smaller than the output. At minimum gain the output is 9 dB or more smaller than the input. In this configuration the input signal will begin to clip against the ESD protection diodes before the output reaches maximum swing limits. The input signal cannot swing more than 0.5V below the negative supply voltage (normally 0V) nor should it exceed the positive supply voltage. The input signal will clip and cause severe distortion if it is too large. Because the input stage self biases to approximately mid rail the supply voltage will impose the limit for input voltage swing.

At the frequencies where the LMH6517 is the most useful the input impedance is not exactly 200 Ω and it may not be purely resistive. For many AC coupled applications the impedance can be easily changed using LC circuits to transform the actual impedance to the desired impedance.

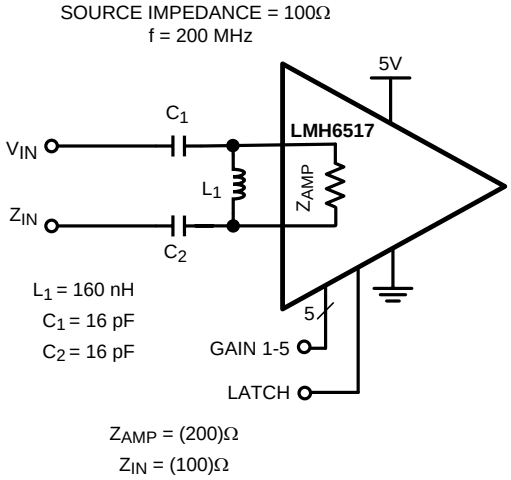


Figure 43. Differential 200Ω LC Conversion Circuit

In Figure 43 a circuit is shown that matches the amplifier 200Ω input with a source of 100Ω. This would be the case when connecting the LMH6517 directly to many common types of 50Ω test equipment. For an easy way to calculate the L and C circuit values there are several options for online tools or down-loadable programs. The following tool might be helpful.

http://www.circuitsage.com/matching/matcher2.html

Excel can also be used for simple circuits; however, the “Analysis ToolPak” add-in must be installed to calculate complex numbers.

OUTPUT CHARACTERISTICS

The LMH6517 has a low impedance output very similar to a traditional Op-amp output. This means that nearly any load can be driven with minimal gain loss. Matching load impedance for proper termination of filters is as easy as inserting the proper value of resistor between the filter and the amplifier. This flexibility makes system design and gain calculations very easy. The LMH6517 was designed to run from a single 5V supply. In spite of this low supply voltage the LMH6517 is still able to deliver very high power gains when driving low impedance loads.

The ability of the LMH6517 to drive low impedance loads creates an opportunity to greatly increase power gain, if required. One example of using power gain to offset filter loss is shown in Figure 59. A graph showing power gain over various load conditions is shown below in Figure 44. This graph clearly shows the reduction in power gain caused by back termination. While many RF amplifiers have internal resistance and deliver maximum power into a matched load the LMH6517 has an output resistance very near to zero Ohms. The graph shows that maximum power transfer does indeed occur with a load of nearly zero Ohms. Another useful feature of the graph is the ability to determine how much gain can be recovered by dropping load resistance when it is necessary to back terminate either a transmission line or a filter.

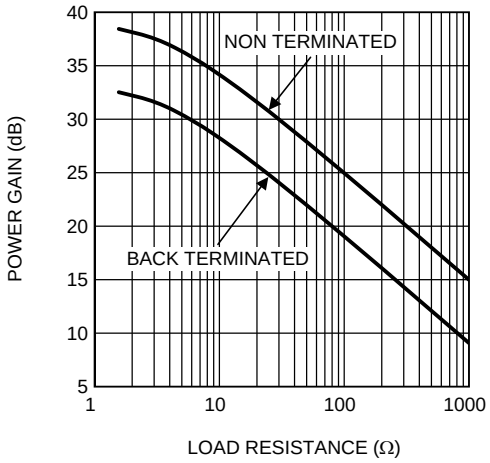


Figure 44. Power Gain vs Load
Note 6dB power loss when adding load matching resistors.

Here is an example of how to use the chart in Figure 44. In a system it is desired to have at least 20dB of maximum gain from the amplifier input to output. The system noise and harmonic distortion requirements dictate a 200 Ohm filter between the amplifier and the ADC. Using the chart we can see that a back terminated 200 Ohm filter will result in a net 16 dB of gain at the filter input. To recover this loss it is possible to use a 1:4 balun to drop the load condition of the filter to 50 Ohms at the amplifier output. This gives an additional 6dB of power gain. Since the transformer has a power loss of approximately 1dB we end up with 21dB of gain at the filter output instead of 16dB. See Figure 59 for an example where the filter performs the impedance transformation function.

The LMH6517, like most high frequency amplifiers, is sensitive to loading conditions on the output. Load conditions that include small amounts of capacitance connected directly to the output can cause stability problems. In order to ensure output stability resistors should be connected directly at the amplifier output followed by a small capacitor. This circuit sets a dominant pole that will cancel out board parasitics in most applications. An example of this is shown in figure Figure 45 . In this example the amplifier and ADC are less than 0.1 wavelength apart and do not require a terminated transmission line. A more sophisticated filter may require better impedance matching. Some example filters are shown later.

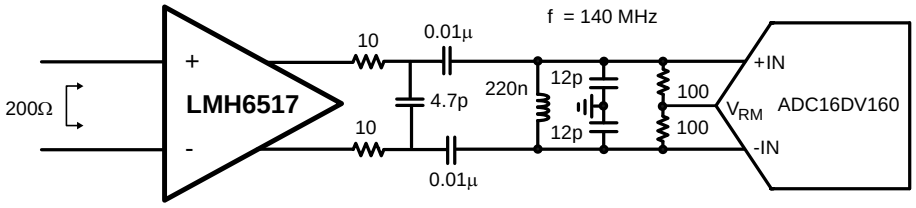


Figure 45. Output Configuration

DIGITAL CONTROL

The LMH6517 will support three modes of control, parallel mode, serial mode (SPI compatible) and pulse mode. Parallel mode is fastest and requires the most board space for logic line routing. Serial mode is compatible with existing SPI compatible systems. The pulse mode is both fast and compact, but must step through intermediate gain steps when making large gain changes.

The LMH6517 has gain settings covering a range of 31.5 dB. To avoid undesirable signal transients the LMH6517 should not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs.

The LMH6517 was designed to interface with 3.3V CMOS logic circuits. If operation with 5V logic is required a simple voltage divider at each logic pin will allow for this. To properly terminate 100Ω transmission lines a divider with a 66.5Ω resistor to ground and a 33.2Ω series resistor will properly terminate the line as well as give the 3.3V logic levels. Care should be taken not to exceed the 3.6V absolute maximum voltage rating of the logic pins.

Some pins on the LMH6517 have different functions depending on the digital control mode. These functions will be described in the sections to follow.

Control Mode	MOD1 Pin Value	MOD0 Pin Value
Parallel	1	1
Serial	1	0
Pulse	0	1
Reserved	0	0

PARALLEL MODE (MOD1= 1, MOD0 = 1)

Parallel mode offers the fastest gain update capability with the drawback of requiring the most board space dedicated to control lines. When designing a system that requires very fast gain changes parallel mode is the best selection.

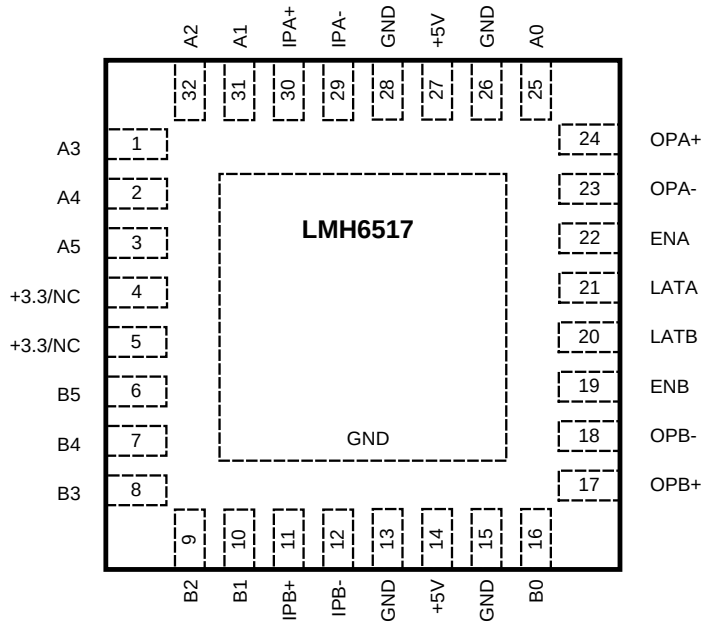


Figure 46. Pin Functions for Parallel Mode

The LMH6517 has a 6-bit gain control bus as well as a Latch pin. When the Latch pin is low, data from the gain control pins is immediately sent to the gain circuit (i.e. gain is changed immediately). When the Latch pin transitions high the current gain state is held and subsequent changes to the gain set pins are ignored. To minimize gain change glitches multiple gain control pins should not change while the latch pin is low. In order to achieve the very fast gain step switching time of 5 ns the internal gain change circuit is very fast. Gain glitches could result from timing skew between the gain set bits. This is especially the case when a small gain change requires a change in state of three or more gain control pins. If continuous gain control is desired the Latch pin can be tied to ground. This state is called transparent mode and the gain pins are always active. In this state the timing of the gain pin logic transitions should be planned carefully to avoid undesirable transients

ENA and ENB pins are provided to reduce power consumption by disabling the highest power portions of the LMH6517. The gain register will preserve the last active gain setting during the disabled state. These pins will float high and can be left disconnected if they won't be used. If the pins are left disconnected a 0.01uF capacitor to ground will help prevent external noise from coupling into these pins. See Typical Performance Characteristics for disable and enable timing information.

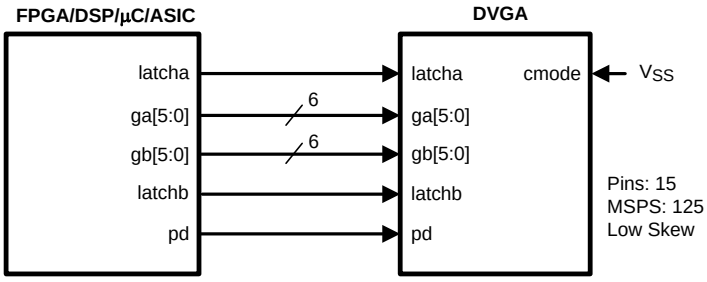


Figure 47. Parallel Mode Connection for Fastest Response

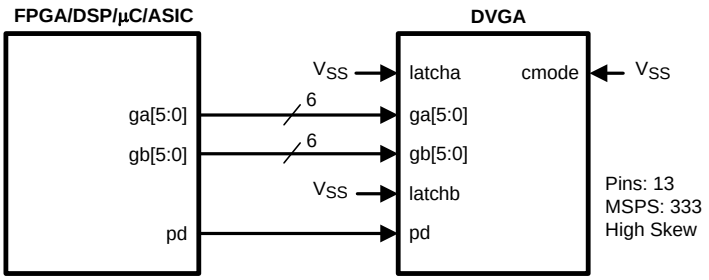


Figure 48. Parallel Mode Connection Not Using Latch Pins (Latch pins tied to logic low state)

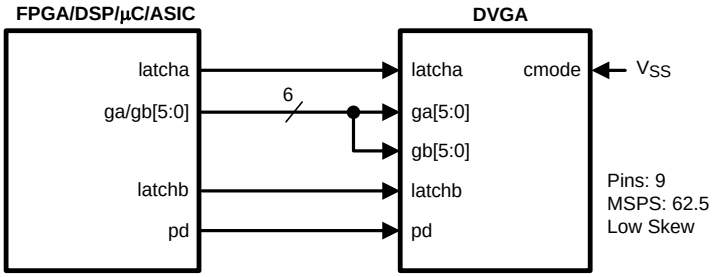


Figure 49. Parallel Mode Connection Using Latch Pins to Mulitplex Digital Data

SPI COMPATIBLE SERIAL INTERFACE (MOD1= 1, MOD0 = 0)

Serial interface allows a great deal of flexibility in gain programming and reduced board complexity. Using only 4 wires for both channels allows for significant board space savings. The trade off for this reduced board complexity is slower response time in gain state changes. For systems where gain is changed only infrequently or where only slow gain changes are required serial mode is the best choice.

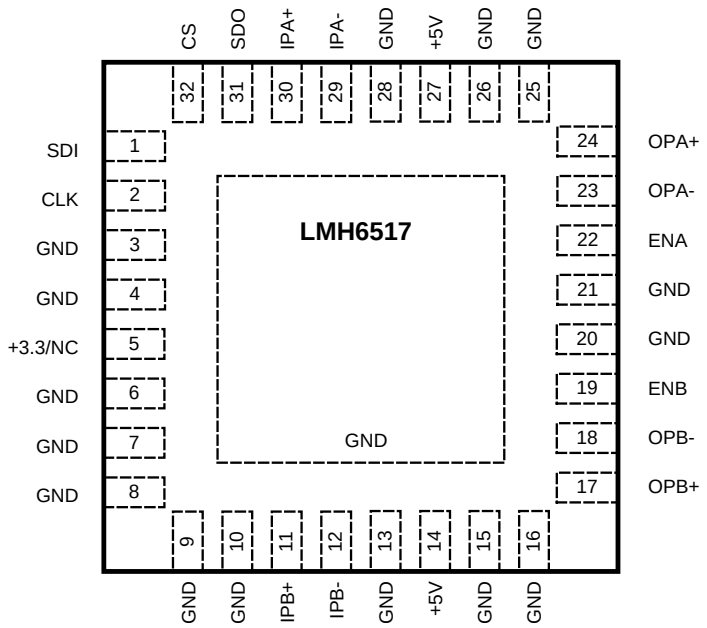


Figure 50. Pin Functions for Serial Mode

The LMH6517 has a serial interface that allows access to the control registers. The serial interface is a generic 4-wire synchronous interface that is compatible with SPI type interfaces that are used on many microcontrollers and DSP controllers.

The serial mode is active when the two mode pins are set as follows: MOD1=1, MOD0=0). In this configuration the pins function as shown in the pin description table. The SPI interface uses the following signals: clock input (CLK), serial data in (SDI), serial data out, and serial chip select (CS)

ENA and ENB pins are active in the serial mode. For fast disable capability these pins can be used and the serial register will hold the last active gain state. These pins will float high and can be left disconnected for serial mode. The serial control bus can also disable the DVGA channels, but at a much slower speed. The serial enable function is an AND function. For a channel to be active both the Enable pin and the serial control register must be in the enabled state. To disable a channel either method will suffice. See Typical Performance Characteristics for disable and enable timing information.

LATA and LATB pins are not active during serial mode.

CLK: This pin is the serial clock pin. It is used to register the input data that is presented on the SDI pin on the rising edge; and to source the output data on the SDO pin on the falling edge. User may disable clock and hold it in the low state, as long as the clock pulse-width minimum specification is not violated when the clock is enabled or disabled.

CS: This pin is the chip select pin. Each assertion starts a new register access - i.e., the SDATA field protocol is required. The user is required to deassert this signal after the 16th clock. If the SCSb is deasserted before the 16th clock, no address or data write will occur. The rising edge captures the address just shifted-in and, in the case of a write operation, writes the addressed register. There is a minimum pulse-width requirement for the deasserted pulse - which is specified in Electrical Characteristics.

SDI: This pin is an input for the serial data. It must observe setup/hold requirements with respect to the SCLK. Each cycle is 16-bits long

SDO: This is the data output pin. Ths SDO pin is an open drain output and requires an external bias resistor. See Figure 51 for resistor sizing guidance. This output is normally at TRI-STATE and is driven only when SCSb is asserted. Upon SCSb assertion, contents of the register addressed during the first byte are shifted out with the second 8 SCLK falling edges. Upon power-up, the default register address is 00h.

Each serial interface access cycle is exactly 16 bits long as shown in Figure 52. Each signal's function is described below. the read timing is shown in Figure 53, while the write timing is shown in figure Figure 54.

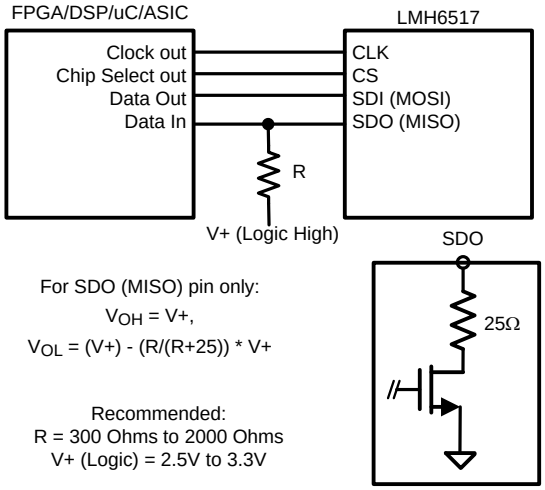


Figure 51. SDO Pin External Bias Resistor Configuration

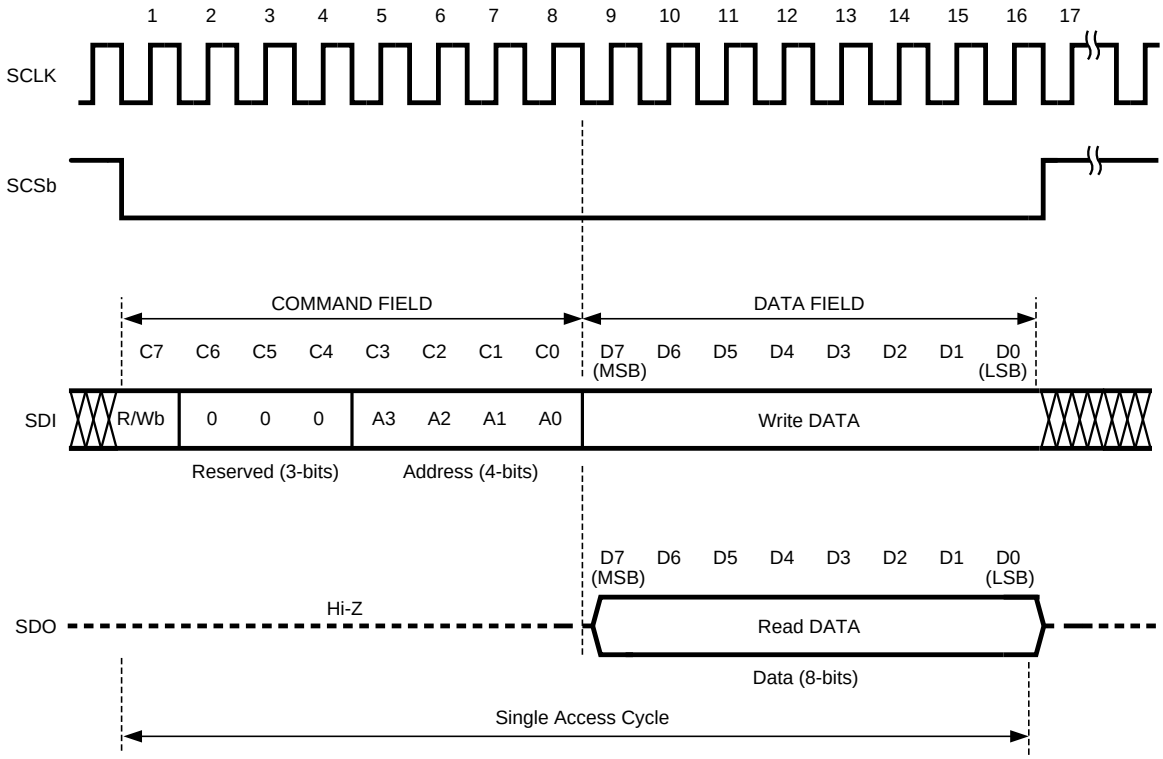


Figure 52. Serial Interface Protocol (SPI compatible)

R/Wb	Read / Write bit. A value of 1 indicates a read operation, while a value of 0 indicates a write operation.
Reserved	Not used. Must be set to 0.
ADDR:	Address of register to be read or written.
DATA	In a write operation the value of this field will be written to the addressed register when the chip select pin is deasserted. In a read operation this field is ignored.

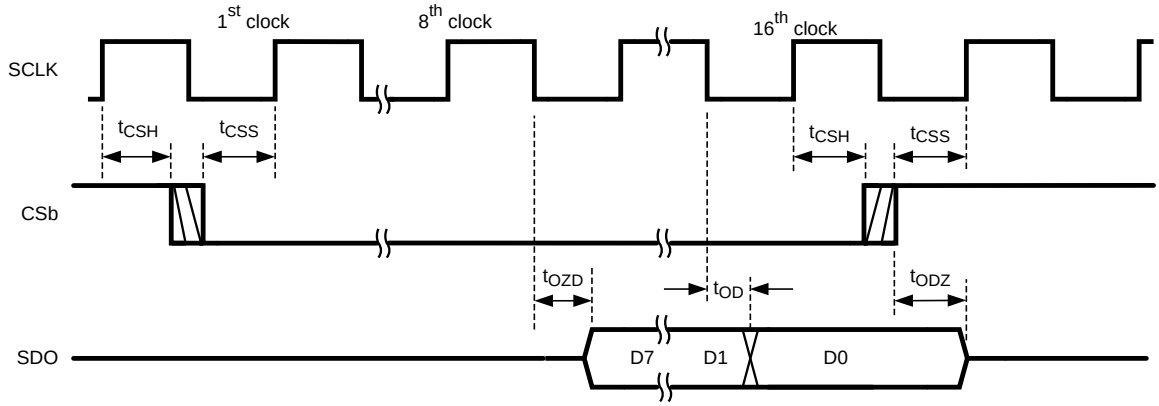


Figure 53. Read Timing

Table 1. Read Timing
Data Output on SDO Pin

Parameter	Description
t_{CSH}	Chip select hold time
t_{CSS}	Chip select setup time
t_{OZD}	Initial output data delay
t_{ODZ}	High impedance delay
t_{OD}	Output data delay

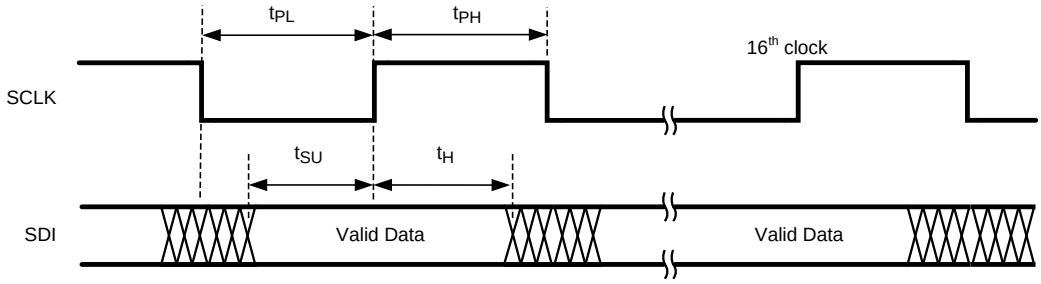


Figure 54. Write Timing
Data Written to SDI Pin

Table 2. Write Timing
Data Input on SDI Pin

Parameter	Description
t_{PL}	Minimum clock low time (clock duty dycle)
t_{PH}	Minimum clock high time (clock duty cycle)
t_{SU}	Input data setup time
t_{H}	Input data hold time

Table 3. Serial Word Format for LMH6517

C7	C6	C5	C4	C3	C2	C1	C0
1= read 0=write	0	0	0	0	0	0	0=Ch A 1=Ch B

Table 4. Serial Word Format for LMH6517 (cont)

Enable	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0	RES
1=On 0=Off	1=+16dB	1=+8dB	1=+4dB	1=+2dB	1=+1dB	1=+0.5dB	0

PULSE MODE (MOD1= 0, MOD0 = 1)

Pulse mode is a simple yet fast way to adjust gain settings. Using only two control lines per device the LMH6517 gain can be changed by simple up and down signals. Gain steps are selectable either by hard wiring the board or using two additional logic inputs. For a system where gain changes can be stepped from one gain to the next and where board space is limited this mode may be the best choice. The ENA and ENB pins are fully active during pulse mode, and the channel gain state is preserved during the disabled state. See Typical Performance Characteristics for disable and enable timing information.

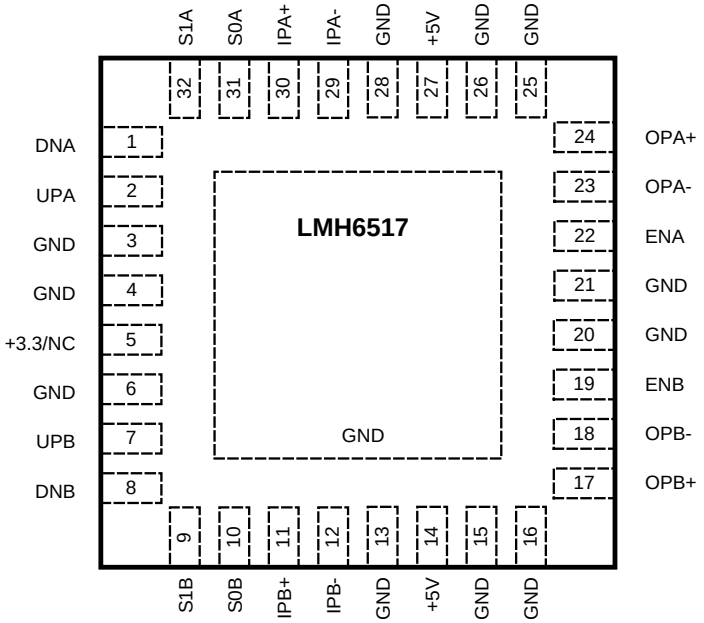


Figure 55. Pin Functions for Pulse Mode

The LMH6517 supports a simple pulse up or pulse down control mode. In this mode the gain step size can be selected from a choice of 0.5, 1, 2 or 6dB steps. In operation the gain can be quickly adjusted either up of down one step at a time by a negative pulse on the UP or DN pins. This mode of operation is most suitable for applications where board space is at a premium and high speed gain changes are desired. As shown in Figure 56 each gain step pulse must have a logic high state of at least t_{PW}= 20 ns and a logic low state of at least t_{PG} 20 ns for the pulse to register as a gain change signal.

To provide a known gain state there is a reset feature in pulse mode. To reset the gain to maximum gain both the UP and DN pins must be strobed low together as shown in Figure 56. There must be an overlap of at least t_{RW}= 20 ns for the reset to register.

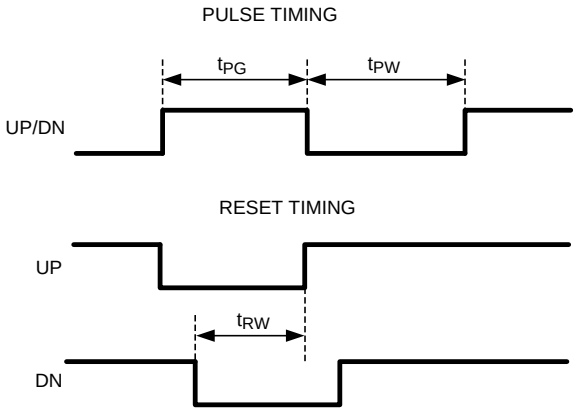


Figure 56. Pulse Mode Timing

EXPOSED PAD WQFN PACKAGE

The LMH6517 is packaged in a thermally enhanced package. The exposed pad is connected to the GND pins. It is recommended, but not necessary, that the exposed pad be connected to the supply ground plane. In any case, the thermal dissipation of the device is largely dependent on the attachment of this pad. The exposed pad should be attached to as much copper on the circuit board as possible, preferably external copper. However, it is also very important to maintain good high speed layout practices when designing a system board. Please refer to the LMH6517 evaluation board for suggested layout techniques.

Package information is available on the Texas Instruments web site.

http://www.ti.com/packaging/

INTERFACING TO ADC

The LMH6517 was designed to be used with high speed ADCs such as the ADC16DV160. As shown in Figure 40, AC coupling provides the best flexibility especially for IF sub-sampling applications. For DC coupled applications the use of a level shifting amplifier or a resistive biasing network may be possible.

The inputs of the LMH6517 will self bias to the optimum voltage for normal operation. The internal bias voltage for the inputs is approximately mid rail which is 2.5V with the typical 5V power supply condition. In most applications the LMH6517 input will need to be AC coupled.

The output common mode voltage is also self biasing to mid supply. This means that for driving most ADCs AC coupling is required. Since most often a band pass filter is desired between the amplifier and ADC the bandpass filter can be configured to block the DC voltage of the amplifier output from the ADC input.

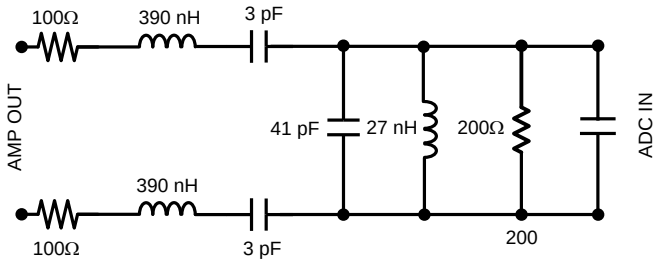


Figure 57. Bandpass Filter

A. Center Frequency is 140 MHz with a 20 MHz Bandwidth. Designed for 200Ω Impedance

ADC Noise Filter

Below are filter schematics and a table of values for some common IF frequencies. The filter shown in Figure 58 offers a good compromise between bandwidth, noise rejection and cost. This filter topology is the same as is used on the ADC14V155KDRB High IF Receiver reference design board. This filter topology works best with the 12 and 14 bit sub-sampling analog to digital converters shown in the Table 6 table.

Table 5. Filter Component Values

Filter Component Values					
	Fc	**75 MHz**	**140 MHz**	**170 MHz**	**250 MHz**
	BW	**40 MHz**	**20 MHz**	**25 MHz**	**Narrow Band**
Components	R1, R2	100Ω	200Ω	100Ω	499Ω
	L1, L2	390 nH	39 0nH	560 nH	—
	C1, C2	10 pF	3 pF	1.4 pF	47 pF
	C3	22 pF	41 pF	32 pF	11 pF
	L5	220 nH	27 nH	30 nH	22 nH
	R3, R4	100Ω	200Ω	100Ω	499Ω

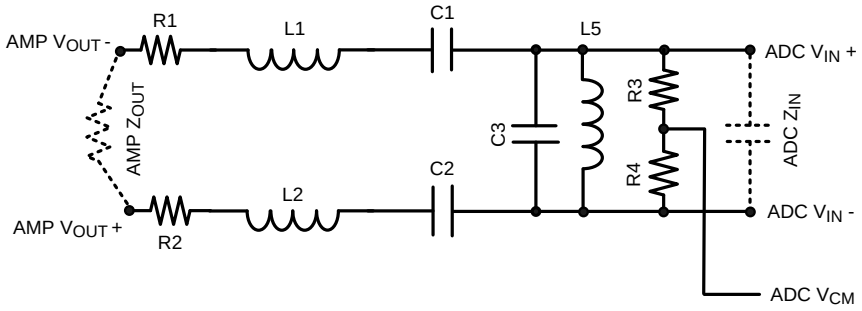


Figure 58. Sample Filter

While the filters shown above have excellent performance in most respects they have one very large drawback, and that is voltage loss. There is a 6dB loss right up front from the matching resistors (R1 and R2 in Figure 58) and there are additional losses in the filter, primarily due to the resistive losses of the inductors. One solution is to use larger inductors with higher Q ratings. An even better solution is to use the filter as an impedance transforming circuit. Designing a filter with a low impedance input and a high impedance output will result in a voltage gain that can be used to offset the voltage losses. While this solution won't work with high impedance amplifiers, the LMH6517's low impedance output stage is perfectly suited for it. In essence the additional power gained from driving a given voltage into a lower value load impedance is used to offset the power lost in the filter and matching resistors.

The filter shown in Figure 59 uses both an impedance transform as well as a slight input impedance mismatch to reduce the voltage loss from the amplifier to the ADC input. This configuration makes use of the strengths of the LMH6517 output stage to deliver the best linearity possible. Due to the low impedance output stage the LMH6517 can drive a lot of current into a low impedance load and still deliver high linearity signals.

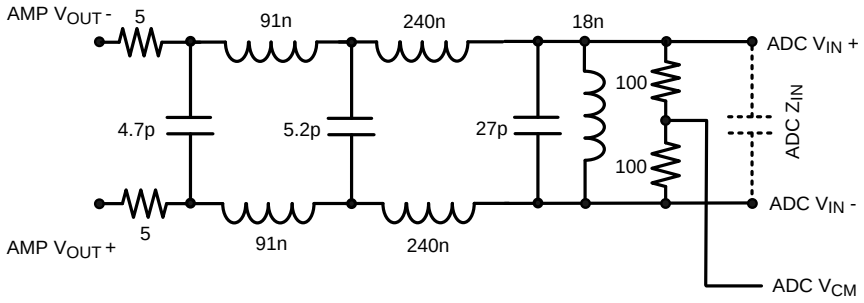


Figure 59. Impedance Transforming Filter
25 Ω Input 200 Ω Output, 210 MHz Center Frequency

POWER SUPPLIES

The LMH6517 was designed primarily to be operated on 5V power supplies. The voltage range for V_{CC} is 4.5V to 5.25V. A 5V supply provides the best performance while lower supplies will result in less power consumption. Power supply regulation of 2.5% or better is advised. When operated on a board with high speed digital signals it is important to provide isolation between digital signal noise and the LMH6517 inputs. The SP16160CH1RB reference board provides an example of good board layout.

Of special note is that the digital circuits are powered from an internal supply voltage of 3.3V. The logic pins should not be driven above the absolute maximum value of 3.6V. See DIGITAL CONTROL for details.

Table 6. Compatible High Speed Analog To Digital Converters

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC12L063	62	12	SINGLE
ADC12DL065	65	12	DUAL
ADC12L066	66	12	SINGLE
ADC12DL066	66	12	DUAL
CLC5957	70	12	SINGLE
ADC12L080	80	12	SINGLE
ADC12DL080	80	12	DUAL
ADC12C080	80	12	SINGLE
ADC12C105	105	12	SINGLE
ADC12C170	170	12	SINGLE
ADC12V170	170	12	SINGLE
ADC14C080	80	14	SINGLE
ADC14C105	105	14	SINGLE
ADC14DS105	105	14	DUAL
ADC14155	155	14	SINGLE
ADC14V155	155	14	SINGLE
ADC16V130	130	16	SINGLE
ADC16DV160	160	16	DUAL
ADC08D500	500	8	DUAL
ADC08500	500	8	SINGLE
ADC08D1000	1000	8	DUAL
ADC081000	1000	8	SINGLE
ADC08D1500	1500	8	DUAL
ADC081500	1500	8	SINGLE
ADC08(B)3000	3000	8	SINGLE

Table 6. Compatible High Speed Analog To Digital Converters (continued)

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC08L060	60	8	SINGLE
ADC08060	60	8	SINGLE
ADC10DL065	65	10	DUAL
ADC10065	65	10	SINGLE
ADC10080	80	10	SINGLE
ADC08100	100	8	SINGLE
ADCS9888	170	8	SINGLE
ADC08(B)200	200	8	SINGLE
ADC11C125	125	11	SINGLE
ADC11C170	170	11	SINGLE

REVISION HISTORY

Changes from Revision J (March 2013) to Revision K **Page**

- Changed layout of National Data Sheet to TI format 27

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6517SQ/NOPB	ACTIVE	WQFN	RTV	32	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L6517SQ	Samples
LMH6517SQE/NOPB	ACTIVE	WQFN	RTV	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L6517SQ	Samples
LMH6517SQX/NOPB	ACTIVE	WQFN	RTV	32	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L6517SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

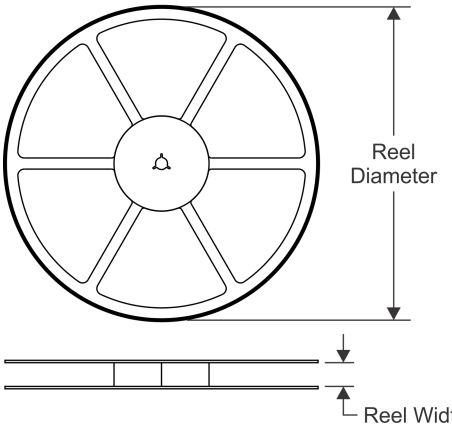
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

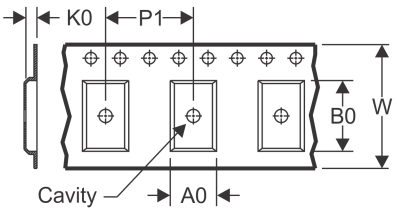
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

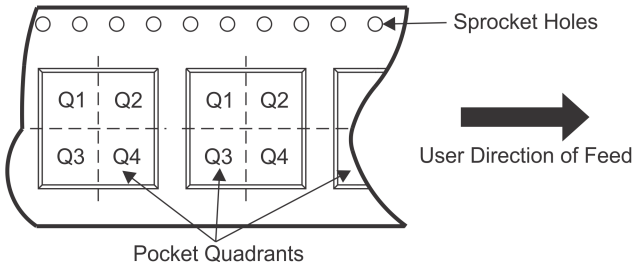


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

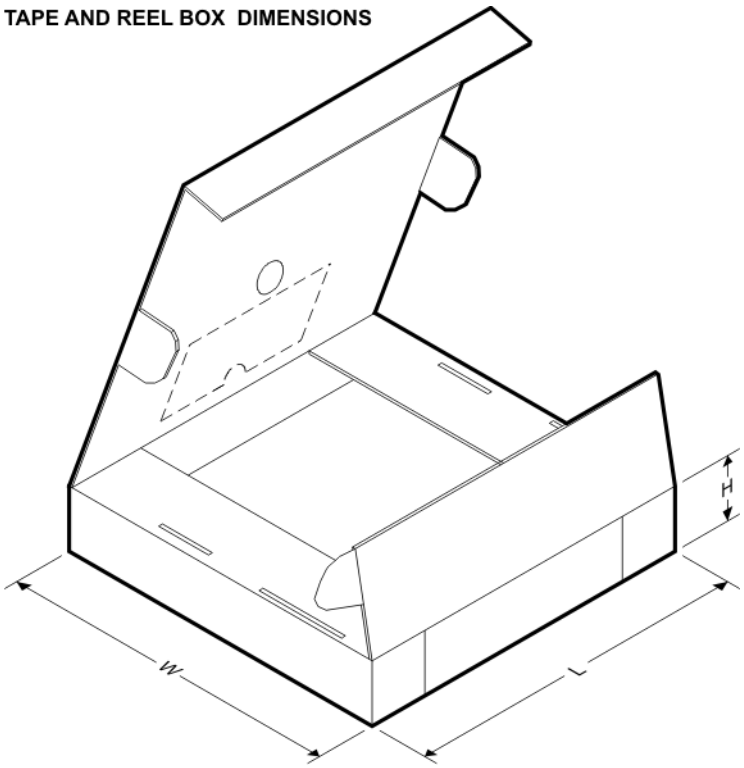
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6517SQ/NOPB	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMH6517SQE/NOPB	WQFN	RTV	32	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMH6517SQX/NOPB	WQFN	RTV	32	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

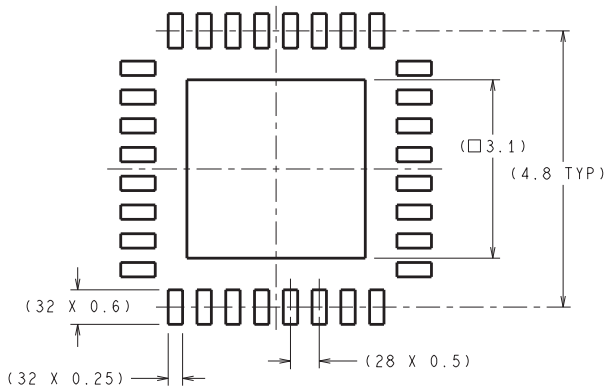
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

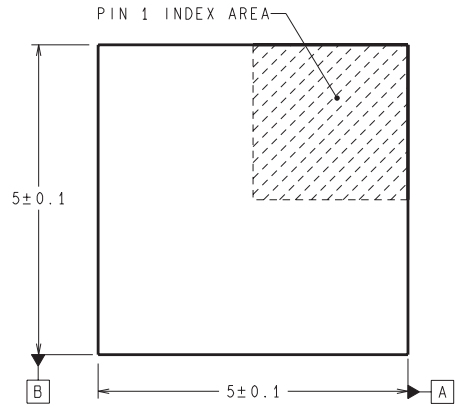
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6517SQ/NOPB	WQFN	RTV	32	1000	210.0	185.0	35.0
LMH6517SQE/NOPB	WQFN	RTV	32	250	210.0	185.0	35.0
LMH6517SQX/NOPB	WQFN	RTV	32	4500	367.0	367.0	35.0

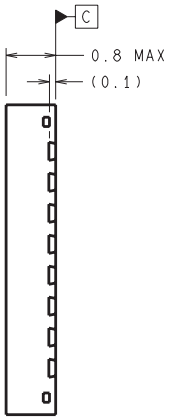
RTV0032A

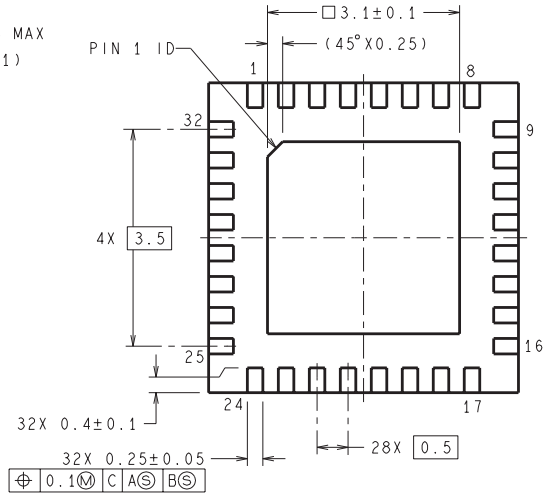


DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN







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