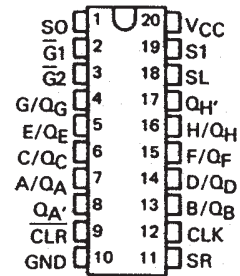# SN54LS299, SN54S299, SN74LS299, SN74S299
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

SDLS156 – MARCH 1974 – REVISED MARCH 1988

- **Multiplexed Inputs/Outputs Provide Improved Bit Density**

- **Four Modes of Operations:**
  Hold (Store)   Shift Left
  Shift Right   Load Data

- **Operates with Outputs Enabled or at High Z**

- **3-State Outputs Drive Bus Lines Directly**

- **Can Be Cascaded for N-Bit Word Lengths**

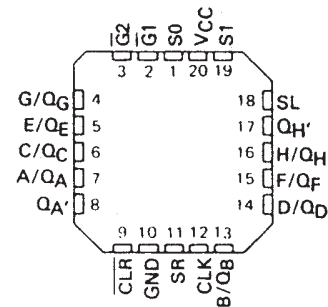- **SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear**

- **Applications:**
  Stacked or Push-Down Registers
  Buffer Storage, and Accumulator
  Registers

SN54LS299, SN54S299 . . . J OR W PACKAGE
SN74LS299, SN74S299 . . . DW OR N PACKAGE
(TOP VIEW)

Pin		Pin
S0	1	20 V_{CC}
$\overline{G1}$	2	19 S1
$\overline{G2}$	3	18 SL
G/Q_G	4	17 Q_H'
E/Q_E	5	16 H/Q_H
C/Q_C	6	15 F/Q_F
A/Q_A	7	14 D/Q_D
Q_A'	8	13 B/Q_B
$\overline{CLR}$	9	12 CLK
GND	10	11 SR

SN54LS299, SN54S299 . . . FK PACKAGE
(TOP VIEW)

Top pins: $\overline{G2}$ (3), $\overline{G1}$ (2), S0 (1), V_{CC} (20), S1 (19)

Left	Right
G/Q_G 4	18 SL
E/Q_E 5	17 Q_H'
C/Q_C 6	16 H/Q_H
A/Q_A 7	15 F/Q_F
Q_A' 8	14 D/Q_D

Bottom pins (9 10 11 12 13): $\overline{CLR}$, GND, SR, CLK, B/Q_B

TYPE	GUARANTEED SHIFT (CLOCK) FREQUENCY	TYPICAL POWER DISSIPATION
'LS299	25 MHz	175 mW
'S299	50 MHz	700 mW

description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

FUNCTION TABLE

MODE	INPUTS									INPUTS/OUTPUTS								OUTPUTS	
	$\overline{CLR}$	FUNCTION SELECT		OUTPUT CONTROL		CLK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
		S1	S0	$\overline{G1}$[†]	$\overline{G2}$[†]		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

[†]When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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logic symbol[†]

[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)

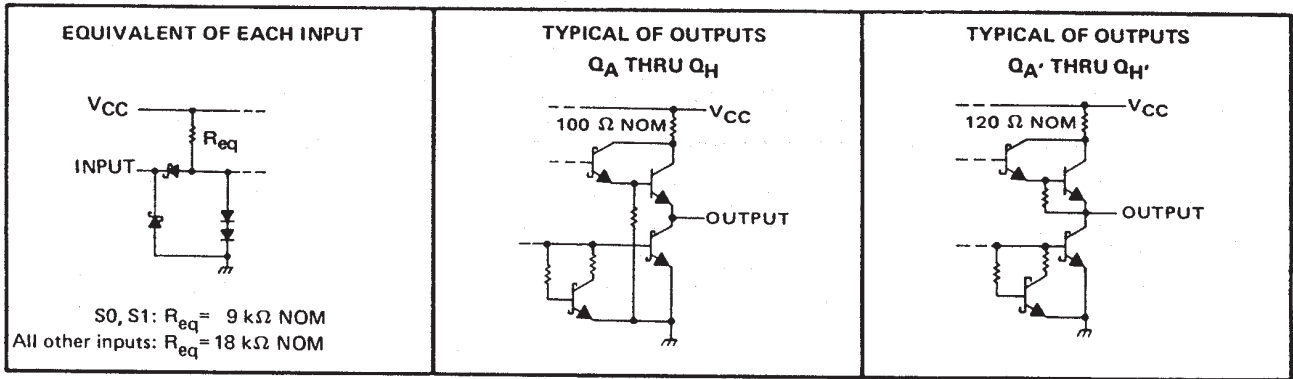Pin numbers shown are for DW, J, N, and W packages.

schematics of inputs and outputs

| EQUIVALENT OF EACH INPUT | TYPICAL OF OUTPUTS Q_A THRU Q_H | TYPICAL OF OUTPUTS $Q_{A'}$ THRU $Q_{H'}$ |

S0, S1: R_{eq} = 9 kΩ NOM
All other inputs: R_{eq} = 18 kΩ NOM

100 Ω NOM

120 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 7 V
Off-state output voltage . . . . 5.5 V
Operating free-air temperature range: SN54LS299 . . . . −55°C to 125°C
 SN74LS299 . . . . 0°C to 70°C
Storage temperature . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS299			SN74LS299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			−1			−2.6	mA
	$Q_{A'}$ or $Q_{H'}$			−0.4			−0.4	
Low-level output current, I_{OL}	Q_A thru Q_H			12			24	mA
	$Q_{A'}$ or $Q_{H'}$			4			8	
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	30			30			ns
	Clock low	18			10			
Width of clear pulse, $t_{w(clear)}$	Clear low	25			20			ns
Setup time, t_{su}	Select	35↑			35↑			ns
	High-level data[†]	20↑			20↑			
	Low-level data[†]	20↑			20↑			
	Clear inactive-state	24↑			20↑			
Hold time, t_h	Select	10↑			10↑			ns
	Data[†]	3↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

[†] Data includes the two serial inputs and the eight input/output data lines.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS299 MIN	SN54LS299 TYP‡	SN54LS299 MAX	SN74LS299 MIN	SN74LS299 TYP‡	SN74LS299 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX	2.4	3.2		2.4	3.1		V
		Q_A' or Q_H'		2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	Q_A thru Q_H	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max — I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
		Q_A' or Q_H'	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
			I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.7 V			40			40	µA
I_{OZL}	Off-state output current, low-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V			–400			–400	µA
I_I	Input current at maximum input voltage	S0, S1	V_{CC} = MAX — V_I = 7 V			200			200	µA
		A thru H	V_I = 5.5 V			100			100	
		Any other	V_I = 7 V			100			100	
I_{IH}	High-level input current	A thru H, S0, S1	V_{CC} = MAX, V_I = 2.7 V			40			40	µA
		Any other				20			20	
I_{IL}	Low-level input current	S0, S1	V_{CC} = MAX, V_I = 0.4 V			–0.8			–0.8	mA
		Any other				–0.4			–0.4	
I_{OS}	Short-circuit output current§	Q_A thru Q_H	V_{CC} = MAX	–30		–130	–30		–130	mA
		Q_A' or Q_H'		–20		–100	–20		–100	
I_{CC}	Supply current		V_{CC} = MAX		33	53		33	53	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	20	35		MHz
t_{PLH}	CLK	Q_A' or Q_H'	R_L = 2 kΩ, C_L = 15 pF		22	33	ns
t_{PHL}					26	39	
t_{PHL}	$\overline{CLR}$	Q_A' or Q_H'			27	40	ns
t_{PLH}	CLK	Q_A thru Q_H	R_L = 665 Ω, C_L = 45 pF		17	25	ns
t_{PHL}					26	39	
t_{PHL}	$\overline{CLR}$	Q_A thru Q_H			26	40	ns
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			13	21	ns
t_{PZL}					19	30	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	R_L = 665 Ω, C_L = 5 pF		10	20	ns
t_{PLZ}					10	15	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. Load circuits and voltage waveforms are shown in Section 1.
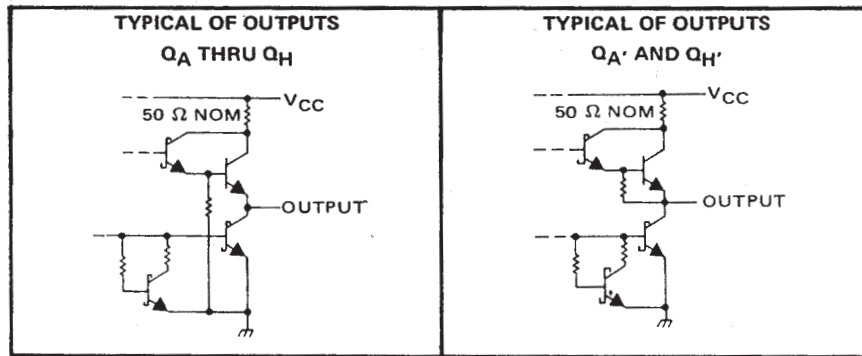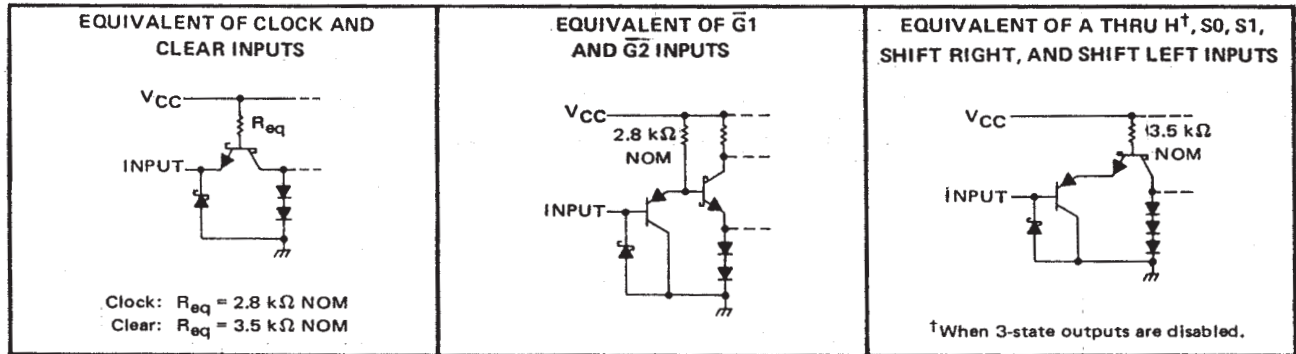
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schematics of inputs and outputs

EQUIVALENT OF CLOCK AND CLEAR INPUTS

Clock: R_{eq} = 2.8 kΩ NOM
Clear: R_{eq} = 3.5 kΩ NOM

EQUIVALENT OF $\overline{G1}$ AND $\overline{G2}$ INPUTS

EQUIVALENT OF A THRU H[†], S0, S1, SHIFT RIGHT, AND SHIFT LEFT INPUTS

[†]When 3-state outputs are disabled.

TYPICAL OF OUTPUTS Q_A THRU Q_H

TYPICAL OF OUTPUTS $Q_{A'}$ AND $Q_{H'}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 5.5 V
Off-state output voltage . . . . 5.5 V
Operating free-air temperature range: SN54S299 (See Note 1) . . . . −55°C to 125°C
　　　　　　　　　　　　　　　　　　　SN74S299 . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S299			SN74S299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			−2			−6.5	mA
	$Q_{A'}$ or $Q_{H'}$			−0.5			−0.5	
Low-level output current, I_{OL}	Q_A thru Q_H			20			20	mA
	$Q_{A'}$ or $Q_{H'}$			6			6	
Clock frequency, f_{clock}		0		50	0		50	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	10			10			ns
	Clock low	10			10			
Width of clear pulse, $t_{w(clear)}$	Clear low	10			10			ns
Setup time, t_{su}	Select	15↑			15↑			ns
	High-level data[‡]	7↑			7↑			
	Low-level data[‡]	5↑			5↑			
	Clear inactive-state	10↑			10↑			
Hold time, t_h	Select	5↑			5↑			ns
	Data[‡]	5↑			5↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

[‡] Data includes the two serial inputs and the eight input/output data lines.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = –18 mA				–1.2	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.2		V
		Q_A' or Q_H'		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V			100	µA
I_{OZL}	Off-state output current, low-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V			–250	µA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	A thru H, S0, S1	V_{CC} = MAX, V_I = 2.7 V			100	µA
		Any other				50	
I_{IL}	Low-level input current	CLK or $\overline{CLR}$				–2	mA
		S0, S1	V_{CC} = MAX, V_I = 0.5 V			–500	µA
		Any other				–250	µA
I_{OS}	Short-circuit output current§	Q_A thru Q_H	V_{CC} = MAX	–40		–100	mA
		Q_A' or Q_H'		–20		–100	
I_{CC}	Supply current		V_{CC} = MAX		140	225	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	50	70		MHz
t_{PLH}	CLK	Q_A' or Q_H'	R_L = 1 kΩ, C_L = 15 pF		12	20	ns
t_{PHL}					13	20	
t_{PHL}	$\overline{CLR}$	Q_A' or Q_H'			14	21	ns
t_{PLH}	CLK	Q_A thru Q_H			15	21	ns
t_{PHL}			R_L = 280 Ω, C_L = 45 pF		15	21	
t_{PHL}	$\overline{CLR}$	Q_A thru Q_H			16	24	ns
t_{PZH}	$\overline{G1}$, $\overline{G2}$	Q_A thru Q_H			10	18	ns
t_{PZL}					12	18	
t_{PHZ}	$\overline{G1}$, $\overline{G2}$	Q_A thru Q_H	R_L = 280 Ω, C_L = 5 pF		7	12	ns
t_{PLZ}					7	12	

¶ f_{max} = maximum clock frequency
t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level
NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.
Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
78024012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK	Samples
7802401RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J	Samples
7802401RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J	Samples
7802401SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W	Samples
7802401SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W	Samples
SN54LS299J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS299J	Samples
SN54LS299J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS299J	Samples
SN54S299J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125		
SN54S299J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125		
SN74LS299DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS299	Samples
SN74LS299DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS299	Samples
SN74LS299N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS299N	Samples
SN74LS299N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS299N	Samples
SN74LS299NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS299N	Samples
SN74LS299NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS299N	Samples
SN74S299DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74S299DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74S299DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74S299DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74S299N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74S299N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74S299N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74S299N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SNJ54LS299FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK	Samples
SNJ54LS299FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK	Samples
SNJ54LS299J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J	Samples
SNJ54LS299J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J	Samples
SNJ54LS299W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W	Samples
SNJ54LS299W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W	Samples
SNJ54S299FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54S299FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54S299J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54S299J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54S299W	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54S299W	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS299, SN54S299, SN74LS299, SN74S299 :

- Catalog: SN74LS299, SN74S299

- Military: SN54LS299, SN54S299

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

CERAMIC DUAL IN-LINE PACKAGE

DIM \ PINS **	14	16	18	20
[A]	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

0.065 (1,65)
0.045 (1,14)

1   7

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

[A]

0°-15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE
16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) △D

0.045 (1,14) / 0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)
⊕ 0.010 (0,25) ⓜ

14/18 Pin Only
20 Pin vendor option △D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
     △C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
     △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

10.63
9.97 TYP

A

PIN 1 ID
AREA

1

18X 1.27

20

C

SEATING PLANE

0.1 C

13.0
12.6
NOTE 3

2X

11.43

10

11

B

7.6
7.4
NOTE 4

20X 0.51
0.31

0.25 M C A B

2.65 MAX

0.33 TYP
0.10

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

1.27
0.40

0.3
0.1

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R−GDFP−F20)   CERAMIC DUAL FLATPACK

0.045 (1,14)
0.026 (0,66)

0.300 (7,62)
0.245 (6,22)

Base and Seating Plane

0.100 (2,45)
0.045 (1,14)

0.009 (0,23)
0.004 (0,10)

0.320 (8,13) MAX

1   20

0.022 (0,56)
0.015 (0,38)

0.540 (13,72) MAX

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

0.370 (9,40)
0.250 (6,35)

0.370 (9,40)
0.250 (6,35)

4040180−4/F   04/14

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within Mil−Std 1835 GDFP2−F20

FK (S−CQCC−N**) LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

B SQ
A SQ

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.080\ (2,03)}{0.064\ (1,63)}$

$\frac{0.055\ (1,40)}{0.045\ (1,14)}$

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

$\frac{0.028\ (0,71)}{0.022\ (0,54)}$

0.050 (1,27)

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a metal lid.
         D.   Falls within JEDEC MS−004

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