

# SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688, SN74LS682, SN74LS684 THRU SN74LS688 8-BIT MAGNITUDE/IDENTITY COMPARATORS

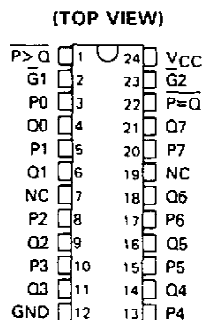
D2617, JANUARY 1981—REVISED MARCH 1988

SDLS008

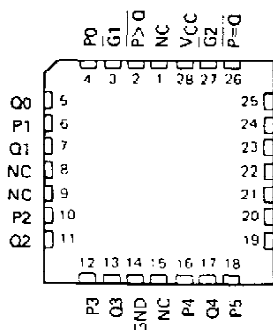
- Compares Two-8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 has 20-k $\Omega$  Pullup Resistors on the Q Inputs
- SN74LS686 and 'LS687 . . . JT and NT 24-Pin, 300-Mil Packages

TYPE	P = Q	P > Q	OUTPUT ENABLE	OUTPUT CONFIGURATION	20-k $\Omega$ PULLUP
'LS682	yes	yes	no	totem-pole	yes
'LS684	yes	yes	no	totem-pole	no
'LS685	yes	yes	no	open-collector	no
SN74LS686	yes	yes	yes	totem-pole	no
'LS687	yes	yes	yes	open-collector	no
'LS688	yes	no	yes	totem-pole	no

SN54LS687 . . . JT PACKAGE  
SN74LS686, SN74LS687 . . . DW OR NT PACKAGE



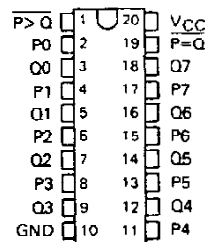
SN54LS687 . . . FK PACKAGE  
(TOP VIEW)



NC—No internal connection

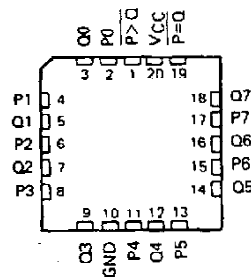
SN54LS682, SN54LS684, SN54LS685 . . . J PACKAGE  
SN74LS682, SN74LS684, SN74LS685 . . . DW OR N PACKAGE

(TOP VIEW)



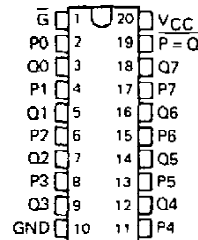
SN54LS682, SN54LS684, SN54LS685 . . . FK PACKAGE

(TOP VIEW)



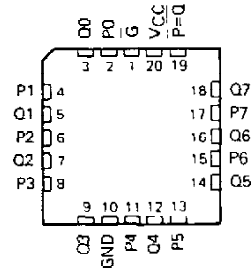
SN54LS688 . . . J PACKAGE  
SN74LS688 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS688 . . . FK PACKAGE

(TOP VIEW)



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

**SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688**  
**SN74LS682, SN74LS684 THRU SN74LS688**  
**8-BIT MAGNITUDE/IDENTITY COMPARATORS**

**description**

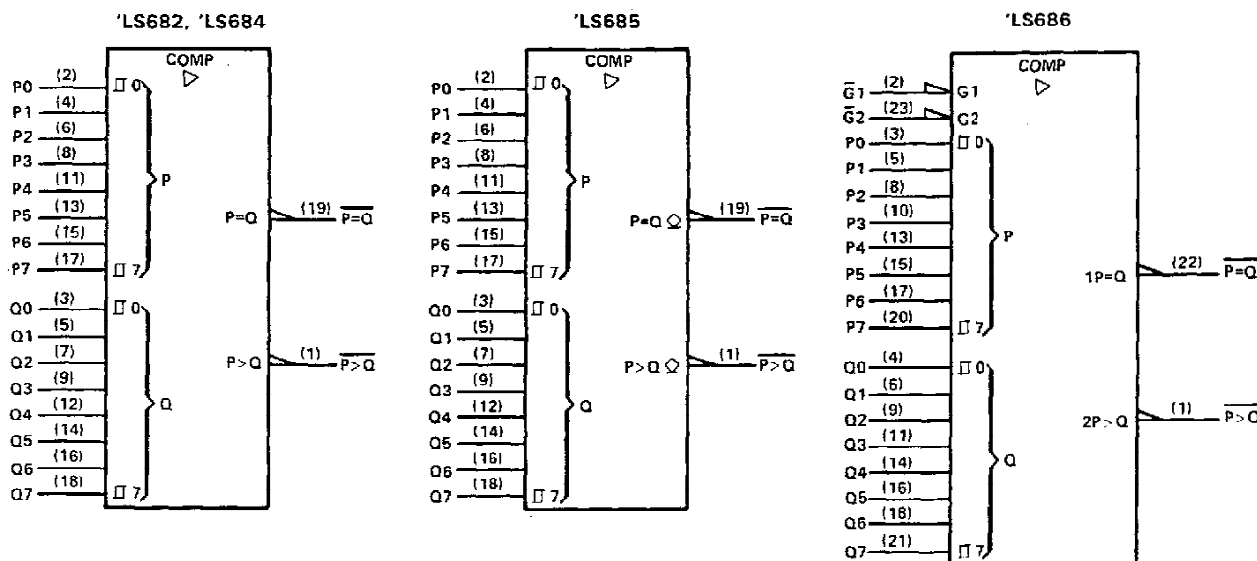
These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide  $P = Q$  outputs and all except 'LS688 provide  $P > Q$  outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS685 and 'LS687 have open-collector outputs. The 'LS682 features 20-k $\Omega$  pullup termination resistors on the Q inputs for analog or switch data.

**FUNCTION TABLE**

INPUTS			OUTPUTS	
DATA	ENABLES		$P = Q$	$P > Q$
P, Q	$\bar{G}, \bar{G}1$	$\bar{G}2$		
$P = Q$	L	X	L	H
$P > Q$	X	L	H	L
$P < Q$	X	X	H	H
$P = Q$	H	X	H	H
$P > Q$	X	H	H	H
X	H	H	H	H

- NOTES: 1. The last three lines of the function table applies only to the devices having enable inputs, i.e., 'LS686 thru 'LS688.
2. The  $P < Q$  function can be generated by applying the  $P = Q$  and  $P > Q$  outputs to a 2-input NAND gate.
3. For 'LS686 and 'LS687,  $\bar{G}1$  enables  $P = Q$  and  $\bar{G}2$  enables  $P > Q$ .

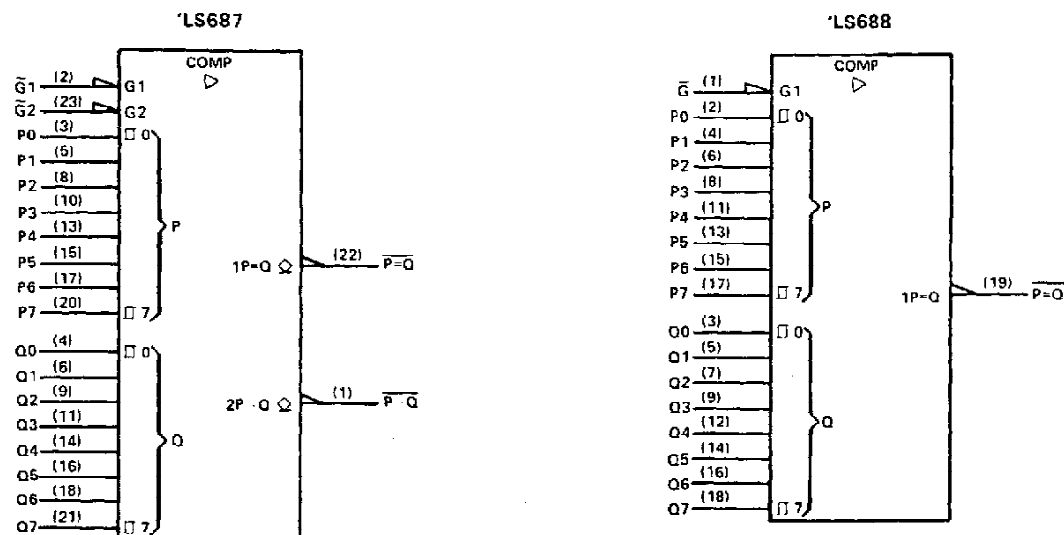
**logic symbols†**



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, JT, N, and NT packages.

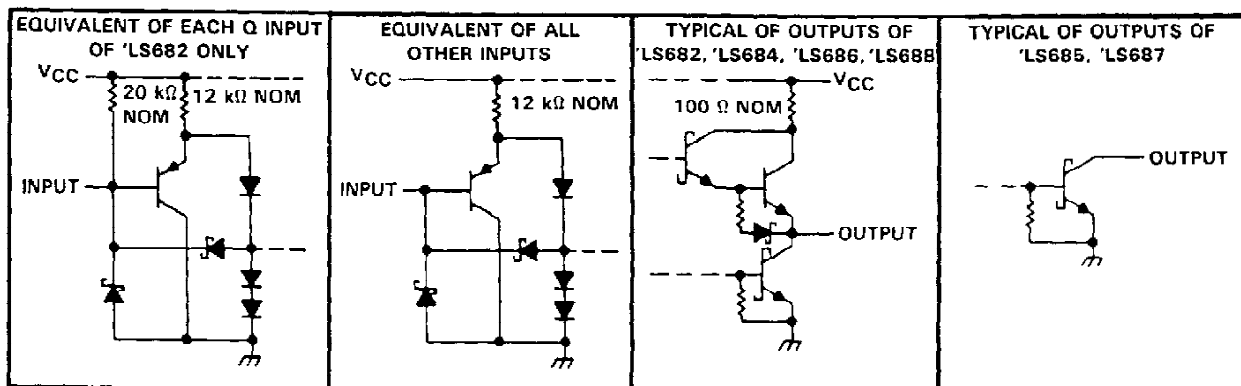
**SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688,  
SN74LS682, SN74LS684 THRU SN74LS688  
8-BIT MAGNITUDE/IDENTITY COMPARATORS**

logic symbols† (continued)



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for DW, J, JT, N, and NT packages.

**schematics of inputs and outputs**

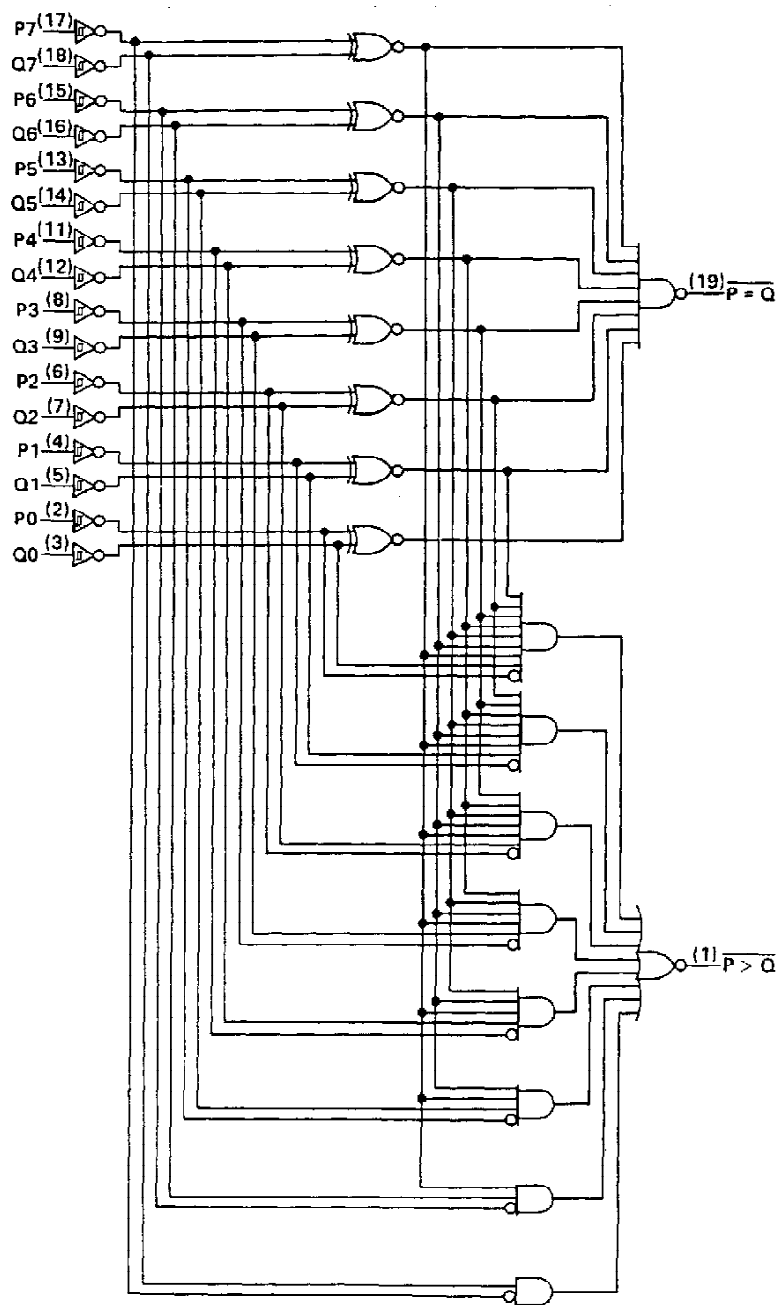


**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

**SN54LS682, SN54LS684, SN54LS685  
SN74LS682, SN74LS684, SN74LS685  
8-BIT MAGNITUDE/IDENTITY COMPARATORS**

'LS682, 'LS684, 'LS685 logic diagram (positive logic)



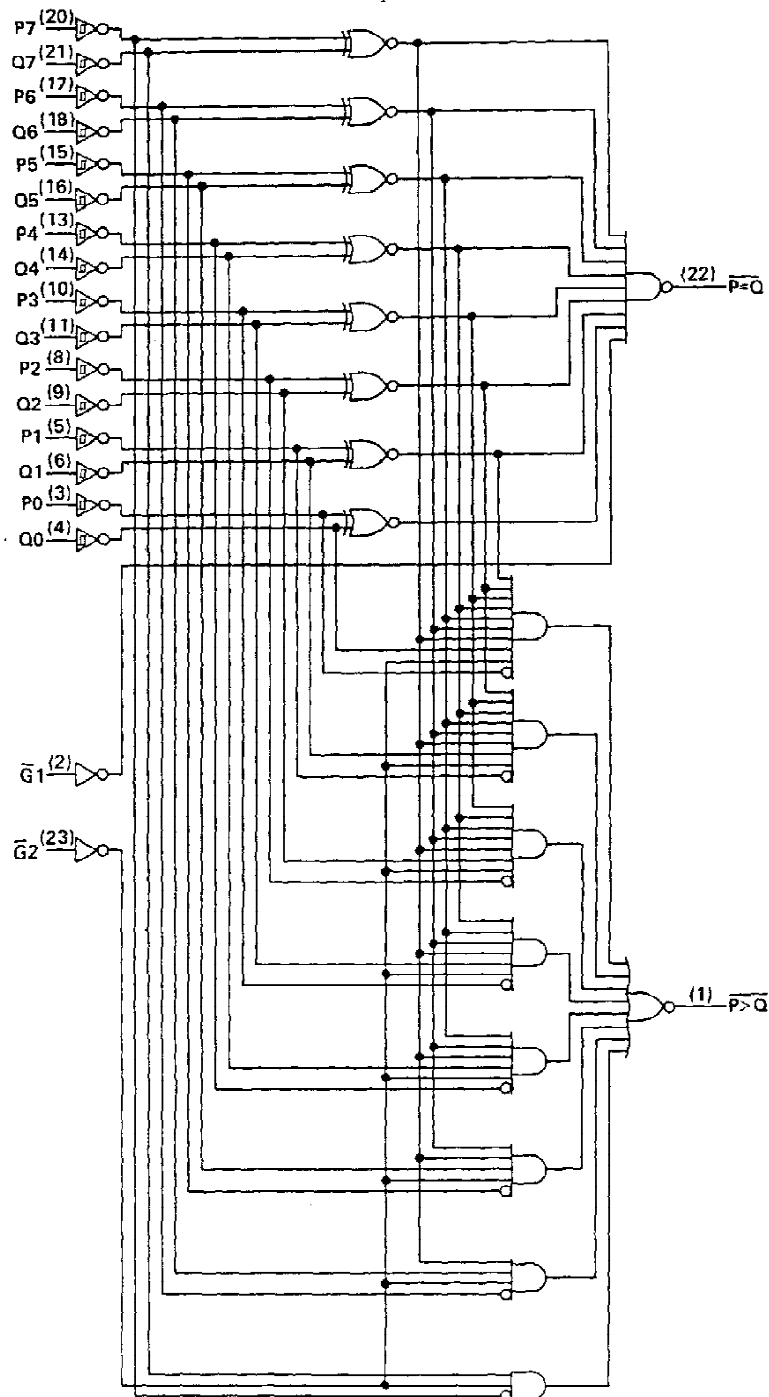
Pin numbers shown are for DW, J, and N packages.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS687  
SN74LS686, SN74LS687  
8-BIT MAGNITUDE/IDENTITY COMPARATORS

'LS686, 'LS687 logic diagram (positive logic)



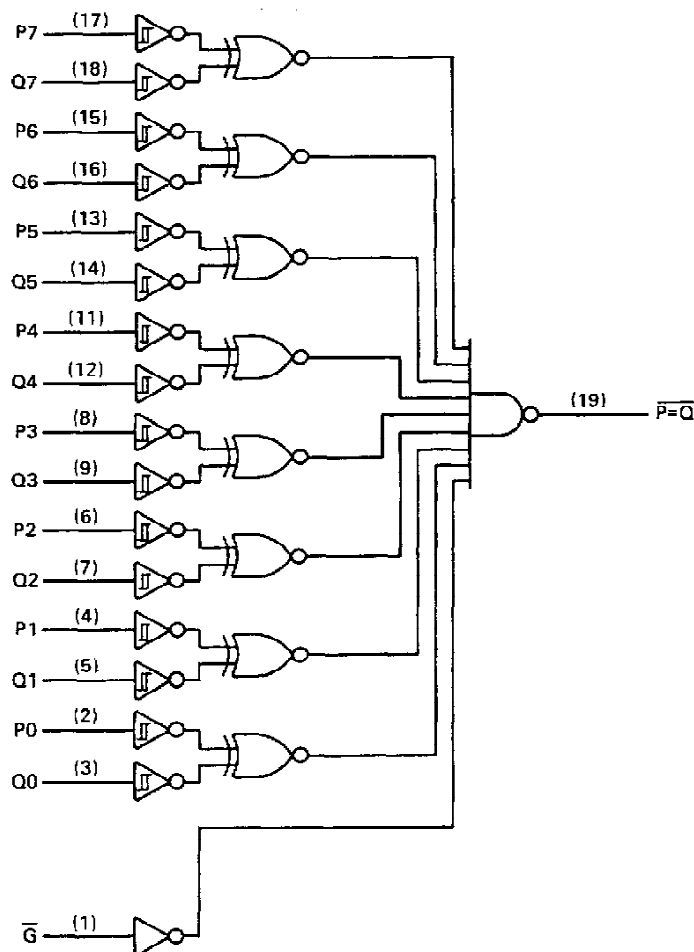
Pin numbers shown are for DW, JT, and NT packages.

TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

**SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688  
SN74LS682, SN74LS684 THRU SN74LS688  
8-BIT IDENTITY COMPARATORS**

'LS688 logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: Q inputs of 'LS682	5.5 V
All other inputs	7 V
Off-state output voltage: 'LS685, 'LS687	7 V
Operating free-air temperature range:	
SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688	-55°C to 125°C
SN74LS682, SN74LS684 thru SN74LS688	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

**SN54LS682, SN54LS684, SN54LS688**  
**SN74LS682, SN74LS684, SN74LS686, SN74LS688**  
**8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS**

**recommended operating conditions**

	SN54LS <sup>*</sup>			SN74LS <sup>*</sup>			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.85	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			12			24	mA
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER			TEST CONDITIONS†	SN54LS*		SN74LS*		UNIT
				MIN	TYP‡	MAX	MIN	
V <sub>IH</sub>	High-level input voltage			2		2		V
V <sub>IL</sub>	Low-level input voltage				0.7		0.8	V
V <sub>T+</sub> - V <sub>T-</sub>	Hysteresis	P or Q inputs	V <sub>CC</sub> = MIN	0.4		0.4		V
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA		-1.5		-1.5	V
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub> , I <sub>OH</sub> = -400 μA	2.5		2.7		V
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub>	0.25	0.4	0.25	0.4	V
			I <sub>OL</sub> = 12 mA			0.35	0.5	
I <sub>I</sub>	Input current at maximum input voltage	Q inputs, 'LS682	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	0.1		0.1	mA	
		All other inputs	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V					
I <sub>IH</sub>	High-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V	20		20	μA	
I <sub>IL</sub>	Low-level input current	Q inputs, 'LS682	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	-0.4		-0.4	mA	
		All other inputs		-0.2		-0.2		
I <sub>OS</sub> ‡	Short-circuit output current		V <sub>CC</sub> = MAX, V <sub>O</sub> = 0	-20	-100	-20	-100	mA
I <sub>CC</sub>	Supply current	'LS682	V <sub>CC</sub> = MAX, See Note 1	42	70	42	70	mA
		'LS684		40	65	40	65	
		'LS686		44	75	44	75	
		'LS688		40	65	40	65	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>\S</sup> Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 1:  $I_{CC}$  is measured with any  $\bar{Q}$  inputs grounded, all other inputs at 4.5 V, and all outputs open.

TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

**SN54LS682, SN54LS684, SN54LS688**  
**SN74LS682, SN74LS684, SN74LS686, SN74LS688**  
**8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS682		'LS684		'LS686		'LS688		UNIT
				MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	
tPLH	P	$\overline{P} = \overline{Q}$	RL = 667 Ω, CL = 45 pF, All other inputs low, See Note 2	13	25	15	25	13	25	12	18	ns
tPHL				15	25	17	25	20	30	17	23	
tPLH	Q	$\overline{P} = \overline{Q}$		14	26	16	25	13	25	12	18	ns
tPHL				15	25	15	25	21	30	17	23	
tPLH	$\overline{Q}, \overline{Q}1$	$\overline{P} = \overline{Q}$						11	20	12	18	ns
tPHL								19	30	13	20	
tPLH	P	$\overline{P} > \overline{Q}$		20	30	22	30	19	30			ns
tPHL				15	30	17	30	15	30			
tPLH	Q	$\overline{P} > \overline{Q}$		21	30	24	30	18	30			ns
tPHL				19	30	20	30	19	30			
tPLH	$\overline{Q}2$	$\overline{P} > \overline{Q}$						21	30			ns
tPHL								16	25			

† $t_{PLH}$  = propagation delay time, low-to-high-level outputs;  $t_{PHL}$  = propagation delay time, high-to-low-level output.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265



**SN54LS685, SN54LS687**  
**SN74LS685, SN74LS687, SN74LS688**

**8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS**

**recommended operating conditions**

	SN54LS <sup>*</sup>			SN74LS <sup>*</sup>			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.85	5	5.25	V
High-level output current, $I_{OH}$			5.5			5.5	V
Low-level output current, $I_{OL}$			12			24	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS <sup>†</sup>	SN54LS <sup>*</sup>			SN74LS <sup>*</sup>			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IH}$	High-level input voltage		2			2			V
$V_{IL}$	Low-level input voltage				0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs		0.4			0.4		V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
$I_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, V_{OH} = 5.5 \text{ V}$			250			100	$\mu\text{A}$
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$				0.35	0.5		
$I_I$		$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.2			-0.2		mA
$I_{CC}$	Supply current	'LS685		40	65		40	65	mA
		'LS687		44	75		44	75	

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

<sup>\*</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

NOTE 1:  $I_{CC}$  is measure with any  $\bar{Q}$  inputs grounded, all other inputs at 4.5 V, and all outputs open.

TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS685, SN54LS687

SN74LS685, SN74LS687

8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH OPEN-COLLECTOR OUTPUTS

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS685			'LS687			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PLH</sub>	P	$\overline{P=Q}$	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF, All other inputs low, See Note 2		30	45		24	35	ns
t <sub>PHL</sub>					19	35		20	30	
t <sub>PLH</sub>	Q	$\overline{P=Q}$			24	45		24	35	ns
t <sub>PHL</sub>					23	35		20	30	
t <sub>PLH</sub>	$\overline{Q}, \overline{Q1}$	$\overline{P=Q}$						21	35	ns
t <sub>PHL</sub>								18	30	
t <sub>PLH</sub>	P	$\overline{P>Q}$			32	45		24	35	ns
t <sub>PHL</sub>					16	35		16	30	
t <sub>PLH</sub>	Q	$\overline{P>Q}$			30	45		24	35	ns
t <sub>PHL</sub>					20	35		16	30	
t <sub>PLH</sub>	$\overline{Q2}$	$\overline{P>Q}$						24	35	ns
t <sub>PHL</sub>								15	30	

<sup>†</sup> $t_{PLH}$  = propagation delay time, low-to-high-level outputs;  $t_{PHL}$  = propagation delay time, high-to-low-level output.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75286

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
8415101RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415101RA SNJ54LS682J	<a href="#">Samples</a>
8415101SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415101SA SNJ54LS682W	<a href="#">Samples</a>
84152012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84152012A SNJ54LS 684FK	<a href="#">Samples</a>
8415201RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415201RA SNJ54LS684J	<a href="#">Samples</a>
84153012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84153012A SNJ54LS 688FK	<a href="#">Samples</a>
8415301RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415301RA SNJ54LS688J	<a href="#">Samples</a>
8415301SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415301SA SNJ54LS688W	<a href="#">Samples</a>
SN54LS682J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS682J	<a href="#">Samples</a>
SN54LS684J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS684J	<a href="#">Samples</a>
SN54LS688J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS688J	<a href="#">Samples</a>
SN74LS682DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS682	<a href="#">Samples</a>
SN74LS682DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS682	<a href="#">Samples</a>
SN74LS682DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS682	<a href="#">Samples</a>
SN74LS682N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS682N	<a href="#">Samples</a>
SN74LS682NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS682	<a href="#">Samples</a>
SN74LS684DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS684	<a href="#">Samples</a>
SN74LS684DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS684	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS684N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS684N	<a href="#">Samples</a>
SN74LS684NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS684N	<a href="#">Samples</a>
SN74LS684NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS684	<a href="#">Samples</a>
SN74LS686DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
SN74LS686NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74LS687NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74LS688DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS688	<a href="#">Samples</a>
SN74LS688DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS688	<a href="#">Samples</a>
SN74LS688DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS688	<a href="#">Samples</a>
SN74LS688N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS688N	<a href="#">Samples</a>
SN74LS688N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74LS688NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS688N	<a href="#">Samples</a>
SN74LS688NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS688	<a href="#">Samples</a>
SNJ54LS682J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415101RA SNJ54LS682J	<a href="#">Samples</a>
SNJ54LS682W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415101SA SNJ54LS682W	<a href="#">Samples</a>
SNJ54LS684FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84152012A SNJ54LS 684FK	<a href="#">Samples</a>
SNJ54LS684J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415201RA SNJ54LS684J	<a href="#">Samples</a>
SNJ54LS688FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84153012A SNJ54LS 688FK	<a href="#">Samples</a>
SNJ54LS688J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415301RA SNJ54LS688J	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS688W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415301SA SNJ54LS688W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS682, SN54LS684, SN54LS688, SN74LS682, SN74LS684, SN74LS688 :**

- Catalog: [SN74LS682](#), [SN74LS684](#), [SN74LS688](#)
- Military: [SN54LS682](#), [SN54LS684](#), [SN54LS688](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS682DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS682NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	12.0	24.0	Q1
SN74LS684DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS684NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	12.0	24.0	Q1
SN74LS688DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS688NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS682DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS682NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS684DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS684NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS688DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS688NSR	SO	NS	20	2000	367.0	367.0	45.0



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within Mil-Std 1835 GDFP2-F20

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

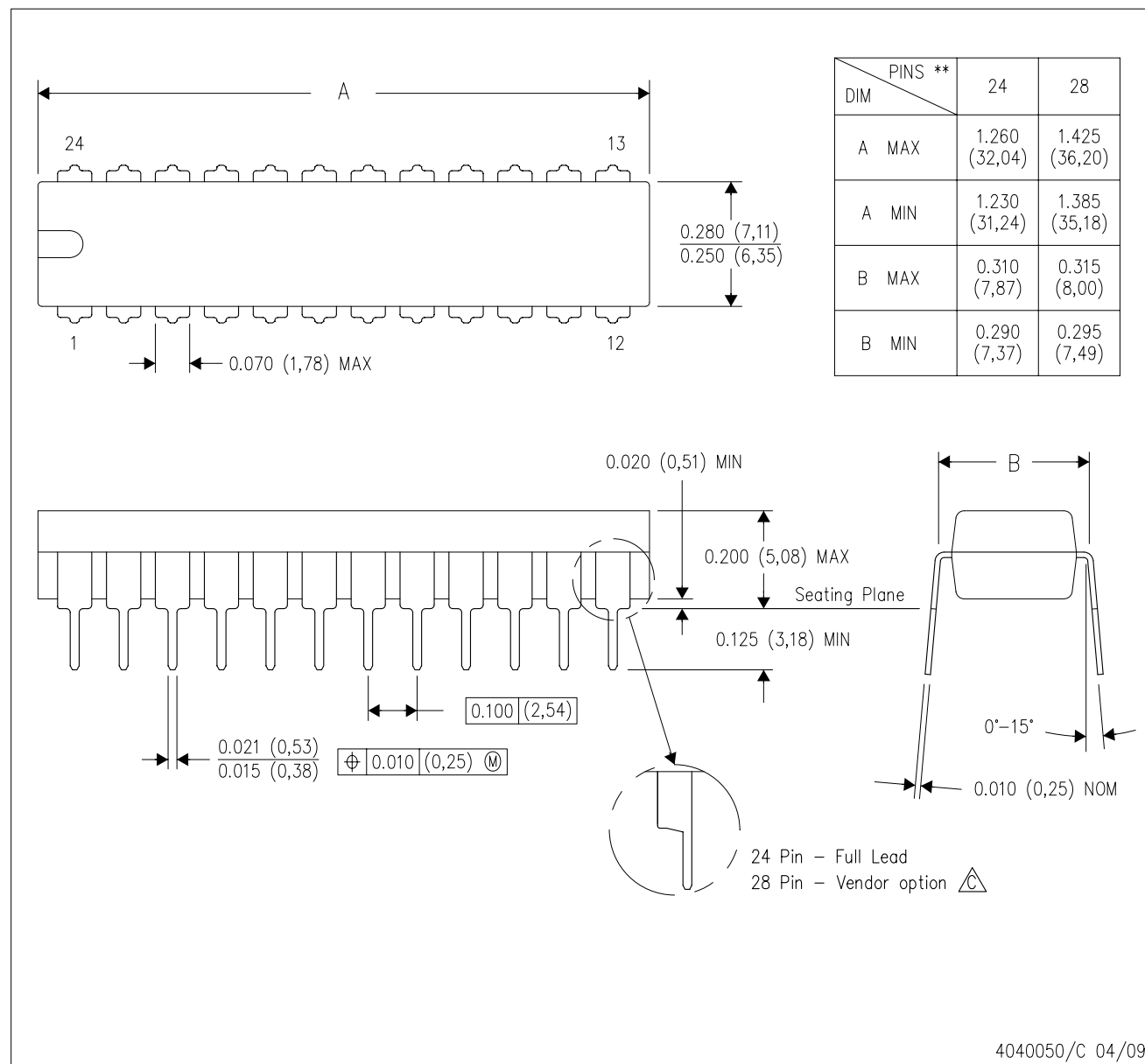
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

# MECHANICAL DATA

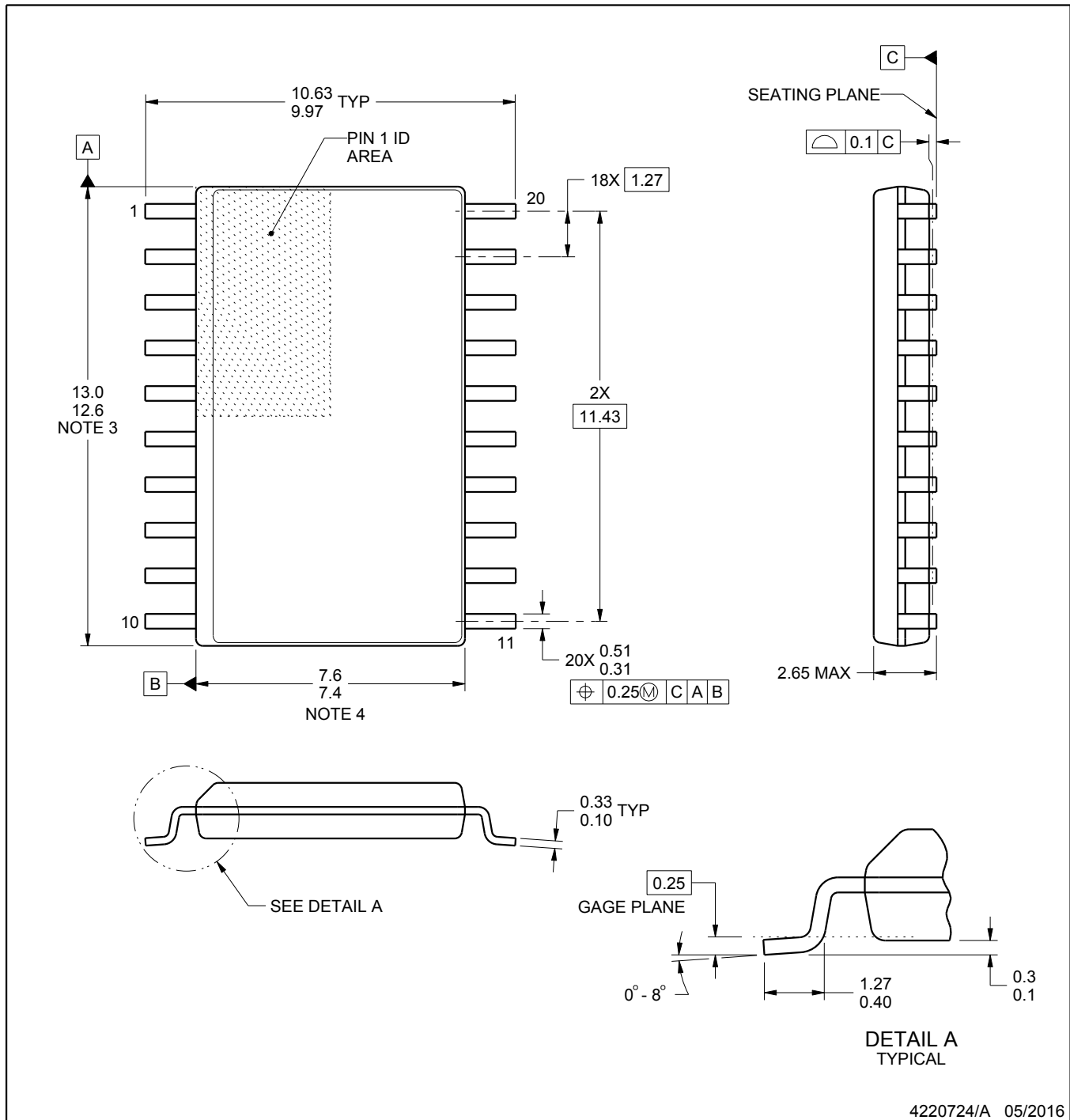
NT (R-PDIP-T\*\*)

24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - $\triangle C$  The 28 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)