

## SM72240 SolarMagic 5-Pin Microprocessor Reset Circuit

Check for Samples: [SM72240](#)

### FEATURES

- Renewable Energy Grade
- Precise monitoring of 5V supply voltages
- Fully specified over temperature
  - $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- 100 ms minimum Power-On Reset pulse width, 190 ms typical:
  - Active-Low  $\overline{\text{RESET}}$  Open Drain Output
- $\overline{\text{RESET}}$  Output valid for  $V_{\text{CC}} \geq 1\text{V}$
- Low Supply Current,  $6\mu\text{A}$  typical
- Power supply transient immunity
- Compatible with MAX811/812 applications

### APPLICATIONS

- Microprocessor Systems
- Computers
- Controllers
- Intelligent Instruments
- Portable/Battery-Powered Equipment

### DESCRIPTION

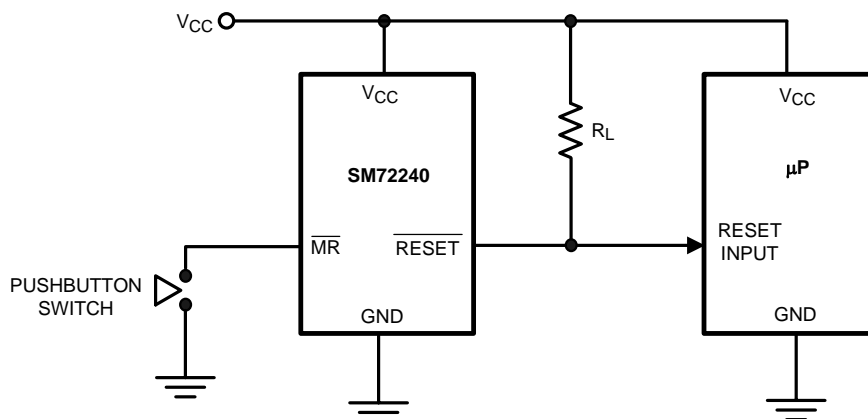
The SM72240 microprocessor supervisory circuit monitors the power supplies in microprocessor and digital systems. It provides a reset to the microprocessor during power-up, power-down, brown-out conditions, and manual reset.

The SM72240 asserts a reset signal whenever the supply decreases below the factory-programmed reset threshold. Reset will be asserted for at least 100ms even after  $V_{\text{CC}}$  rises above the reset threshold.

The SM72240 has an active-low open-drain  $\overline{\text{RESET}}$  output.

The SM72240 is suitable for monitoring 5V. With a low supply current of only  $6\mu\text{A}$ , the SM72240 is ideal for use in portable equipment. The SM72240 is available in the 5-pin SOT-23 package.

### Typical Application Circuit



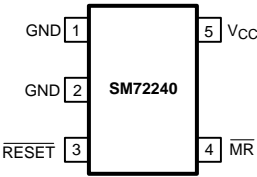
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**Connection Diagram**



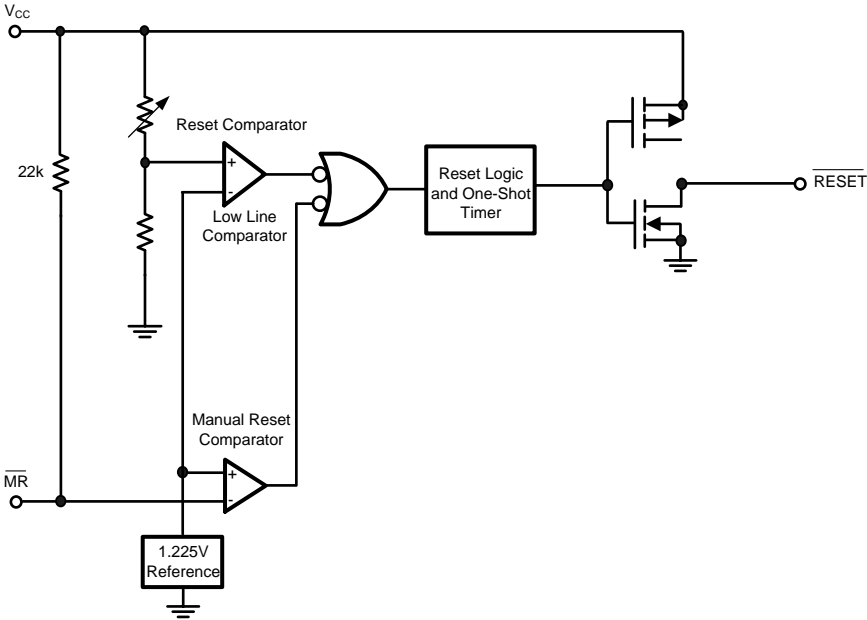
**Figure 1. 5-Pin SOT-23 Package  
See Package Number DBV**

**PIN DESCRIPTIONS**

Pin	Name	Function
1	GND	Ground reference
2	GND	Ground reference, device substrate, connect to ground.
3	$\overline{\text{RESET}}$	Active-low output. $\overline{\text{RESET}}$ remains low while $V_{\text{CC}}$ is below the reset threshold voltage, and for 190 ms after $V_{\text{CC}}$ rises above the reset threshold voltage.
4	$\overline{\text{MR}}$	Active-low input. Reset is asserted whenever this pin is pulled low and remains asserted for 190 ms after the $\overline{\text{MR}}$ pin goes high. May be left open.
5	$V_{\text{CC}}$	Supply Voltage (+5V, nominal)

**Block Diagram**

**Figure 2. SM72240 Block Diagram**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)(2)</sup>

$V_{CC}, \overline{MR}$		-0.3V to 6.0V
RESET, $\overline{RESET}$		-0.3V to ( $V_{CC} + 0.3V$ )
Input Current, $V_{CC}$ Pin		20mA
Output Current, RESET, $\overline{RESET}$ Pin		20mA
ESD Rating <sup>(3)</sup>		2kV
Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )	SOT-23 <sup>(4)</sup>	320mW
Operating Temperature Range		-40°C to +125°C
Maximum Junction Temperature		125°C
Storage Temperature Range		-65°C to +160°C
Lead Temperature (soldering, 10sec)		+300°C

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which the device operates correctly. Operating ratings do not imply specified performance limits. For performance limits and associated test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) The human body model is a 100pF capacitor discharged through a 1.5k $\Omega$  resistor into each pin.
- (4) At elevated temperatures, devices must be derated based on package thermal resistance. The device must be derated at 4.5mW/°C at ambient temperatures above 70°C. The device has internal thermal protection.

## Electrical Characteristics

Typical values are at  $T_A = +25^\circ\text{C}$ . Limits with standard typeface are for  $T_A = +25^\circ\text{C}$ , and limits in boldface type apply for the operating temperature range -40°C to +125°C, unless otherwise noted.<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{CC}$	$V_{CC}$ Range		<b>1.0</b>		<b>5.5</b>	V
$I_{CC}$	Supply Current ( $I_{LOAD} = 0A$ )	SM72240-4.63 $V_{CC} = 5.5V$		8	<b>15</b>	$\mu A$
		SM72240-3.08 $V_{CC} = 3.6V$		7	<b>10</b>	
$V_{TH}$	Reset Threshold	SM72240-4.63	4.54 <b>4.50</b>	4.63	4.72 <b>4.75</b>	V
		SM72240-3.08	3.03 <b>3.00</b>	3.08	3.14 <b>3.15</b>	
$V_{TH}$ Tempco	Reset Threshold Temperature Coefficient			30		ppm/°C
$t_{RD}$	$V_{CC}$ to Reset Delay <sup>(2)</sup>	$V_{CC} = V_{TH}$ to ( $V_{TH} - 100mV$ )		20		$\mu s$
$t_{RP}$	Reset Active Timeout Period		<b>100</b>	190	<b>560</b>	ms
$t_{MR}$	$\overline{MR}$ Minimum Pulse Width		<b>10</b>			$\mu s$
$t_{MD}$	$\overline{MR}$ to Reset Propagation Delay			2		$\mu s$
	$\overline{MR}$ Glitch Immunity <sup>(3)</sup>			100		ns
$V_{IH}$ $V_{IL}$	$\overline{MR}$ Input Threshold	$V_{CC} > V_{TH(MAX)}$	<b>2.3</b>		<b>0.8</b>	V
	$\overline{MR}$ Pull-Up Resistance			22		k $\Omega$
$V_{OL}$	$\overline{RESET}$ Output Voltage Low	$V_{CC} = V_{TH}$ min, $I_{SINK} = 3.2$ mA			<b>0.4</b>	V
		$V_{CC} > 1V$ , $I_{SINK} = 50\mu A$			<b>0.3</b>	
$I_{IN}$	$\overline{RESET}$ Output Leakage Current (SM72240)	$V_{CC} > V_{TH}$ , $\overline{RESET} = 5.5V$			<b>0.5</b>	$\mu A$

- (1) Production testing done at  $T_A = +25^\circ\text{C}$ . Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
- (2)  $\overline{RESET}$  output.
- (3) Glitches of 100 ns or less typically will not generate a reset pulse.

## Typical Performance Characteristics

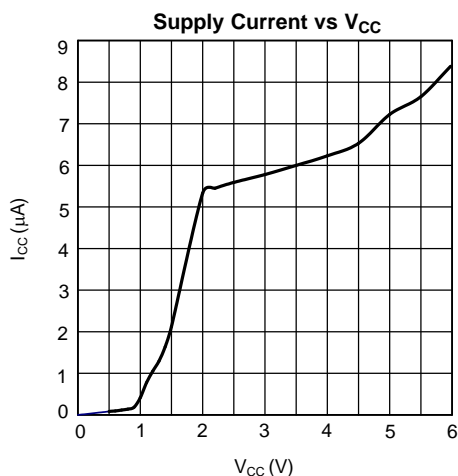


Figure 3.

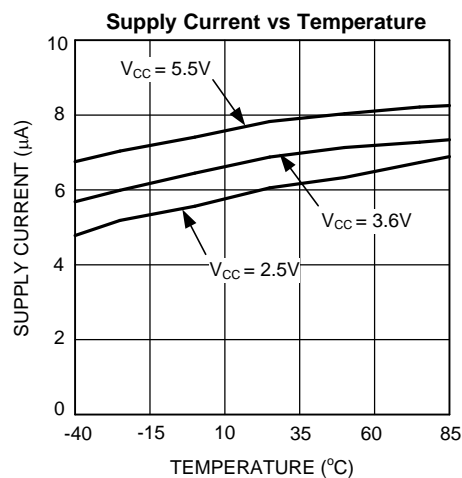


Figure 4.

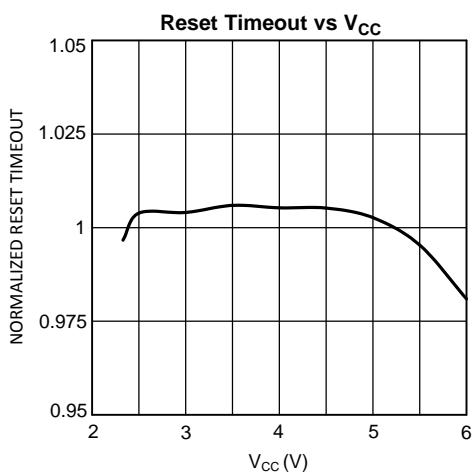


Figure 5.

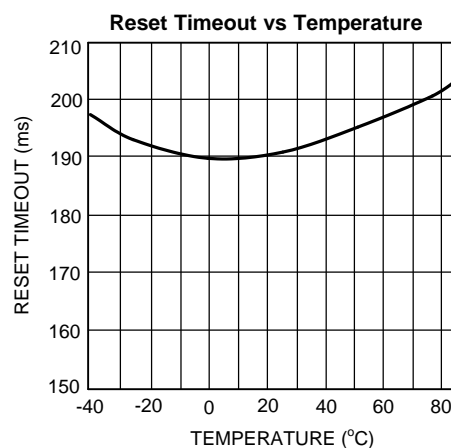


Figure 6.

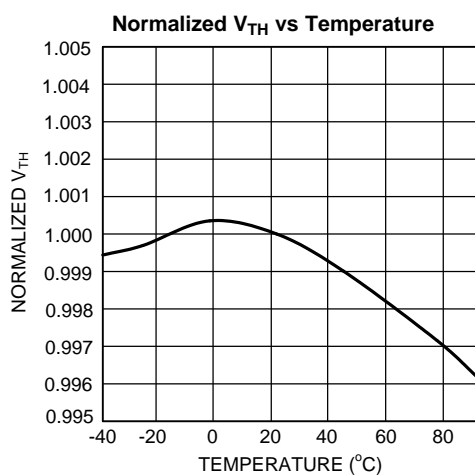


Figure 7.

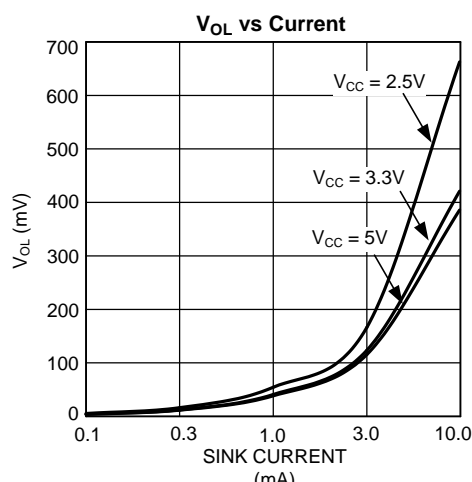


Figure 8.

## Typical Performance Characteristics (continued)

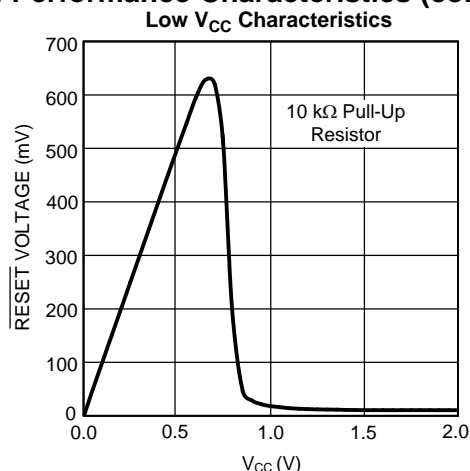


Figure 9.

## Timing Diagram

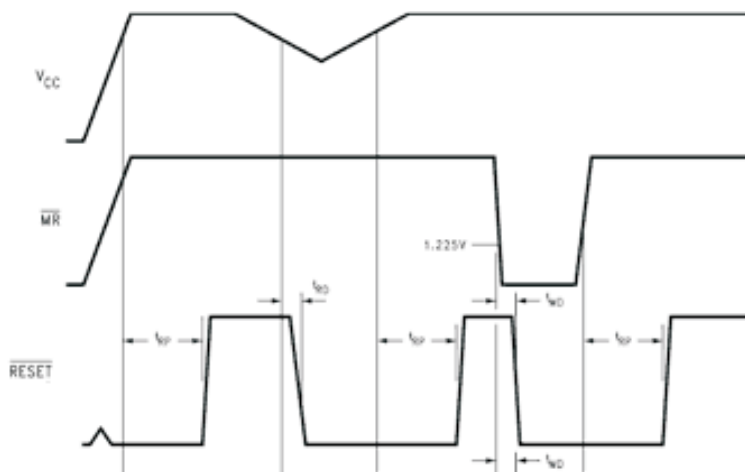


Figure 10.

## CIRCUIT INFORMATION

### RESET OUTPUT

The reset input of a  $\mu P$  initializes the device into a known state. The SM72240 microprocessor voltage monitoring circuit asserts a forced reset output to prevent code execution errors during power-up, power-down, and brownout conditions.

$\overline{RESET}$  is valid for  $V_{CC} \geq 1$  V. Once  $V_{CC}$  exceeds the reset threshold, an internal timer maintains the output for the reset timeout period. After this interval, reset goes high and the microprocessor initializes itself into a known state.  $\overline{RESET}$  is active low.

As  $V_{CC}$  drops below the reset threshold (such as during a brownout), the reset activates (see the [NEGATIVE-GOING  \$V\_{CC}\$  TRANSIENTS](#) section). When  $V_{CC}$  again rises above the reset threshold, the internal timer starts. Reset holds until  $V_{CC}$  exceeds the reset threshold for longer than the reset timeout period. After this time, reset releases.

Additionally, the Manual Reset input ( $\overline{MR}$ ) will initiate a forced reset. See the [MANUAL RESET INPUT \( \$\overline{MR}\$ \)](#) section.

The SM72240 reset output ignores short duration glitches on  $V_{CC}$  and  $\overline{MR}$ . See the [Applications Information](#) section for details.

**RESET THRESHOLD**

The SM72240 is available with a reset voltage of 4.63V or 3.08V which are suitable for monitoring 5.0V or 3.3V supplies respectively.

**MANUAL RESET INPUT ( $\overline{MR}$ )**

Many  $\mu P$ -based products require a manual reset capability, allowing the operator to initiate a reset. The  $\overline{MR}$  input is fully debounced and provides an internal 22 k $\Omega$  pull-up. When the  $\overline{MR}$  input is pulled below  $V_{IL}$  (0.25 $V_{CC}$ ) for more than 100 ns, reset is asserted after a typical delay of 2  $\mu s$ . Reset remains active as long as  $\overline{MR}$  is held low, and releases after  $\overline{MR}$  rises above  $V_{IH}$  and the reset timeout period expires. Use  $\overline{MR}$  with digital logic to assert reset or to daisy chain supervisory circuits.

**Applications Information**

**BENEFITS OF PRECISION RESET THRESHOLDS**

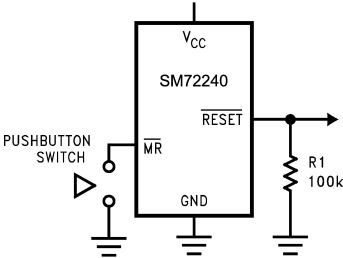
A microprocessor supply supervisor must provide a reset output within a predictable range of the supply voltage. A common threshold range is between 5% and 10% below the nominal supply voltage. The SM72240 uses highly accurate circuitry to ensure that the reset threshold occurs only within this range (for 5.0V and 3.3V supplies). [Table 1](#) shows how the standard reset threshold applies to 5.0V and 3.3V nominal supply voltages.

**Table 1. Monitored Tolerance Table**

Reset Threshold	Supply Voltage	
	3.3V	5.0V
4.63 $\pm$ %		90.8-94.4%
3.08 $\pm$ %	91.8–95.2%	

**ENSURING A VALID RESET OUTPUT DOWN TO  $V_{CC} = 0V$**

When  $V_{CC}$  falls below 1V, the SM72240  $\overline{RESET}$  output is unable to sink the rated current. A high-impedance CMOS logic input connected to  $\overline{RESET}$  can therefore drift to undetermined voltages. To prevent this situation, a 100k $\Omega$  resistor should be connected from the  $\overline{RESET}$  output to ground, as shown in [Figure 11](#).



**Figure 11. Circuit for  $\overline{RESET}$  Valid from  $V_{CC} = 0V$**

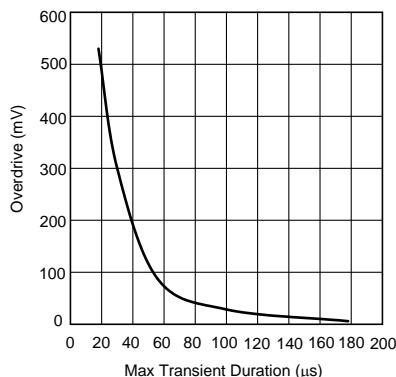
**OPEN DRAIN OUTPUT**

An open drain output allows easy paralleling of multiple microprocessor reset circuits without requiring additional logic gates. Open drain outputs also allow interfacing devices of differing logic levels or families, since the output pull-up resistor may be connected to any supply voltage up to 5.5V, regardless of  $V_{CC}$ .

The pull up resistor is calculated so that maximum current flow into  $\overline{RESET}$  is less than 10 mA when activated. The resistor must be small enough so that the leakage current of all connected devices does not create an excessive voltage drop when the output is not activated. A resistor value of 100 k $\Omega$  will generally suffice.

## NEGATIVE-GOING $V_{CC}$ TRANSIENTS

The SM72240 is relatively immune to short negative-going transients or glitches on  $V_{CC}$ . Figure 12 shows the maximum pulse width a negative-going  $V_{CC}$  transient can have without causing a reset pulse. In general, as the magnitude of the transient increases, going further below the threshold, the maximum allowable pulse width decreases. Typically, a  $V_{CC}$  transient that goes 125 mV below the reset threshold and lasts 40  $\mu$ s or less will not cause a reset pulse. A 0.1  $\mu$ F bypass capacitor mounted as close as possible to the  $V_{CC}$  pin will provide additional transient rejection.



**Figure 12. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive**

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">7</a>



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SM72240MF-3.08/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	R133	
SM72240MF-4.63/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2240	
SM72240MFE-3.08/NOPB	NRND	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	R133	
SM72240MFE-4.63/NOPB	NRND	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2240	
SM72240MFX-3.08/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	R133	
SM72240MFX-4.63/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2240	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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### Applications

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