# SN74LVC1G11 Single 3-Input Positive-AND Gate

## 1 Features

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V $V_{CC}$ Operation
- Inputs Accept Voltages to 5.5 V
- Maximum $t_{pd}$ of 4.1 ns at 3.3 V
- Low Power Consumption, 10-µA Maximum $I_{CC}$
- ±24-mA Output Drive at 3.3 V
- $I_{off}$ Supports Partial-Power-Down Mode Operation

## 2 Applications

- AV Receivers
- DLP Front Projection System
- Digital Picture Frames
- Digital Radio
- Digital Still Cameras
- Digital Video Cameras (DVC)
- Embedded PCs
- E-Books
- Ethernet Switchs
- GPS: Personal Navigation Devices
- Handset: Smartphones
- High-Speed Data Acquisition and Generation
- Military: Radar and Sonar
- Mobile Internet Devices
- Notebook PC and Netbooks
- Network-Attached Storage (NAS)
- Power Line Communication Modems
- Server PSU
- STB, DVR, and Streaming Media
- Speakers: USB
- Tablets: Enterprise
- Video Broadcasting and Infrastructure: Scalable Platform and IP-Based Multi-Format Transcoders
- Wireless Headsets, Keyboards, and Mice

## 3 Description

The SN74LVC1G11 performs the Boolean function $Y = A \bullet B \bullet C$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$ in positive logic.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

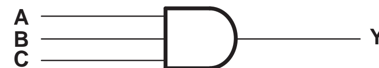
This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LVC1G11DBV | SOT-23 (6) | 2.90 mm × 1.60 mm |
| SN74LVC1G11DCK | SC70 (6) | 2.00 mm × 1.25 mm |
| SN74LVC1G11DRY | SON (6) | 1.45 mm × 1.00 mm |
| SN74LVC1G11DSF | SON (6) | 1.00 mm × 1.00 mm |
| SN74LVC1G11YZP | DSBGA (6) | 1.41 mm × 0.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram (Positive Logic)**



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision G (December 2015) to Revision H | Page |
|---|---|
| • Deleted 200-V Machine Model from *Features* | 1 |
| • Changed pinout images to improve clarity of pin names and pin numbers | 3 |
| • Added DSBGA pin numbers to *Pin Functions* table | 3 |
| • Added Operating free-air temperature, $T_A$ for BGA package | 5 |
| • Added *Receiving Notification of Documentation Updates* section | 14 |

| Changes from Revision F (December2013) to Revision G | Page |
|---|---|
| • Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. | 1 |

| Changes from Revision E (December 2011) to Revision F | Page |
|---|---|
| • Updated document to new TI data sheet format. | 1 |
| • Removed *Ordering Information* table. | 1 |
| • Updated operating temperature range | 4 |

| Changes from Revision D (January 2007) to Revision E | Page |
|---|---|
| • Added DRY and DSF packages to data sheet | 1 |


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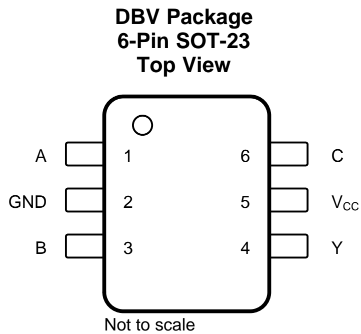
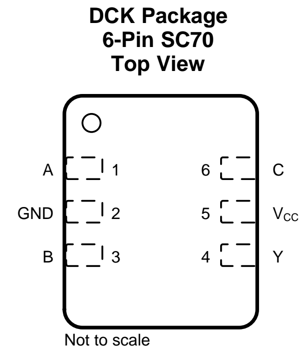
# 5 Pin Configuration and Functions

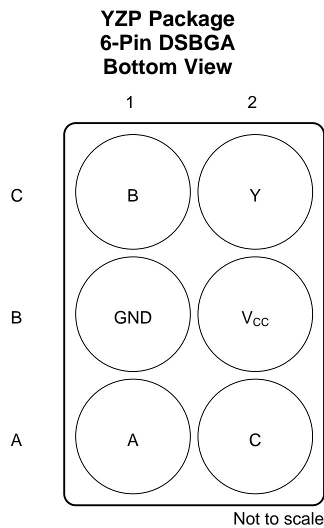
**DBV Package**
**6-Pin SOT-23**
**Top View**



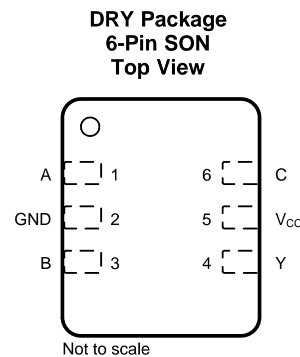

**DCK Package**
**6-Pin SC70**
**Top View**



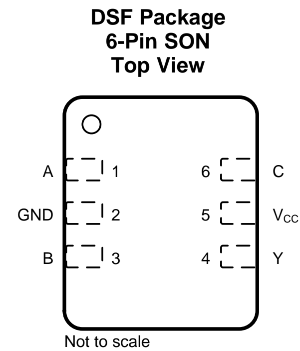

**YZP Package**
**6-Pin DSBGA**
**Bottom View**




**DRY Package**
**6-Pin SON**
**Top View**




**DSF Package**
**6-Pin SON**
**Top View**




See mechanical drawings for dimensions.

**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOT-23, SC70, SON, SON | DSBGA | | |
| A | 1 | A1 | I | A Input |
| B | 3 | C1 | I | B Input |
| C | 6 | A2 | I | C Input |
| GND | 2 | B1 | — | Ground |
| $V_{CC}$ | 5 | B2 | — | Power Supply |
| Y | 4 | C2 | O | Y Output |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage[2] | | –0.5 | 6.5 | V |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state[2] | | –0.5 | 6.5 | V |
| $V_O$ | Voltage applied to any output in the high or low state[2][3] | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the *Recommended Operating Conditions* table.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | 2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

See note[1].

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0.7 × $V_{CC}$ | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 0.3 × $V_{CC}$ | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | |
| | | $V_{CC}$ = 3 V | | –16 | |
| | | | | –24 | |
| | | $V_{CC}$ = 4.5 V | | –32 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.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## Recommended Operating Conditions (continued)

See note(1).

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 32 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 10 | |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 10 | |
| $T_A$ | Operating free-air temperature | BGA package | –40 | 85 | °C |
| | | All other packages | –40 | 125 | |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74LVC1G11 | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | DBV (SOT-23) | DCK (SC70) | DRY (SON) | YZP (DSBGA) | DSF (SON) | |
| | | 6 PINS | 6 PINS | 6 PINS | 6 PINS | 6 PINS | |
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 195.9 | 260.1 | 424.6 | 105.8 | 413.7 | °C/W |
| $R_{θJCtop}$ | Junction-to-case (top) thermal resistance | 177.4 | 98.1 | 309 | 1.6 | 226.6 | °C/W |
| $R_{θJB}$ | Junction-to-board thermal resistance | 51.7 | 63.1 | 292 | 10.8 | 317 | °C/W |
| $ψ_{JT}$ | Junction-to-top characterization parameter | 61.3 | 2.2 | 135.4 | 3.1 | 37.4 | °C/W |
| $ψ_{JB}$ | Junction-to-board characterization parameter | 51.3 | 62.4 | 292 | 10.8 | 317 | °C/W |
| $R_{θJCbot}$ | Junction-to-case (bottom) thermal resistance | — | — | — | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –100 µA | | 1.65 V to 5.5 V | $V_{CC}$ – 0.1 | | | V |
| | | $I_{OH}$ = –4 mA | | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = –8 mA | | 2.3 V | 1.9 | | | |
| | | $I_{OH}$ = –16 mA | | 3 V | 2.4 | | | |
| | | $I_{OH}$ = –24 mA | | | 2.3 | | | |
| | | $I_{OH}$ = –32 mA | | 4.5 V | 3.8 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 µA | | 1.65 V to 5.5 V | | | 0.1 | V |
| | | $I_{OL}$ = 4 mA | | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 8 mA | | 2.3 V | | | 0.3 | |
| | | $I_{OL}$ = 16 mA | | 3 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | | | | | 0.55 | |
| | | $I_{OL}$ = 32 mA | | 4.5 V | | | 0.55 | |
| $I_I$ | All inputs | $V_I$ = 5.5 V or GND | | 0 to 5.5 V | | | ±5 | µA |
| $I_{off}$ | | $V_I$ or $V_O$ = 5.5 V | | 0 | | | ±10 | µA |
| $I_{CC}$ | | $V_I$ = 5.5 V or GND, | $I_O$ = 0 | 1.65 V to 5.5 V | | | 10 | µA |
| $ΔI_{CC}$ | | One input at $V_{CC}$ – 0.6 V,<br>Other inputs at $V_{CC}$ or GND | | 3 V to 5.5 V | | | 500 | µA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 3.5 | | pF |

## 6.6 Switching Characteristics, $C_L$ = 15 pF, $T_A$ = –40°C to +85°C

over recommended operating free-air temperature range, $C_L$ = 15 pF (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | A, B, or C | Y | $V_{CC}$ = 1.8 V ± 0.15 V | 2.6 | 15.2 | ns |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.6 | 5.6 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1.2 | 4.1 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 3.1 | |

## 6.7 Switching Characteristics, $C_L$ = 30 pF or 50 pF, $T_A$ = –40°C to +85°C

over recommended operating free-air temperature range, $C_L$ = 30 pF or 50 pF (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | A, B, or C | Y | $V_{CC}$ = 1.8 V ± 0.15 V | 2.9 | 17.2 | ns |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.4 | 6.2 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1.3 | 4.9 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 3.5 | |

## 6.8 Switching Characteristics, $C_L$ = 30 pF or 50 pF, $T_A$ = –40°C to +125°C

over recommended operating free-air temperature range, $C_L$ = 30 pF or 50 pF (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | A, B, or C | Y | $V_{CC}$ = 1.8 V ± 0.15 V | 2.9 | 20 | ns |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.4 | 7.8 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1.3 | 6.2 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 4.6 | |

## 6.9 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | $V_{CC}$ = 1.8 V | 18 | pF |
| | | | $V_{CC}$ = 2.5 V | 19 | |
| | | | $V_{CC}$ = 3.3 V | 20 | |
| | | | $V_{CC}$ = 5 V | 23 | |


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## 6.10 Typical Characteristics

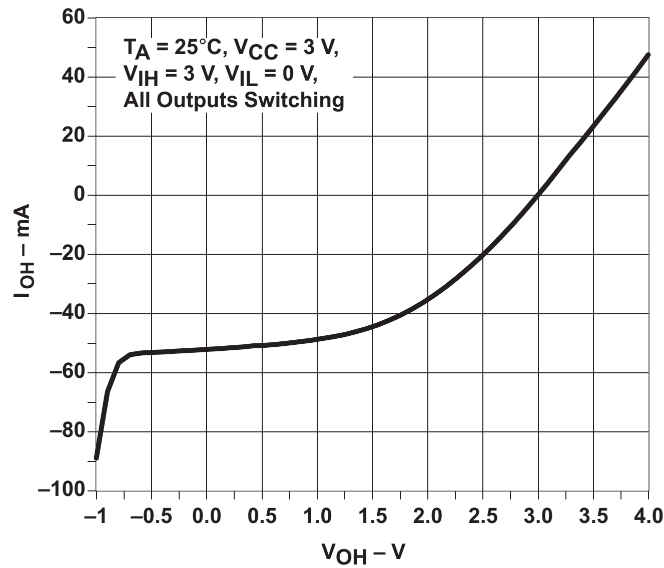
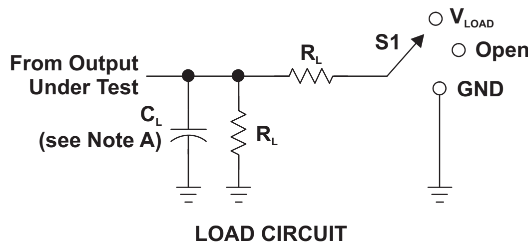


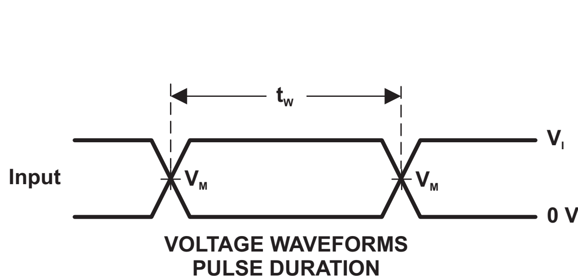

**Figure 1. Output Current Drive vs HIGH-level Output Voltage**

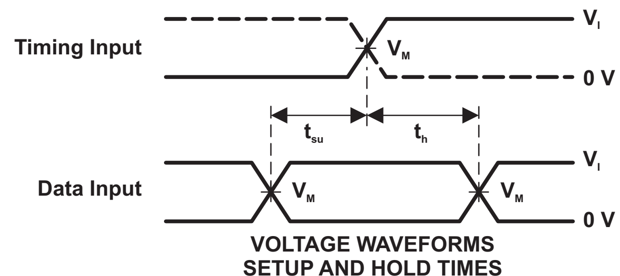
# 7 Parameter Measurement Information

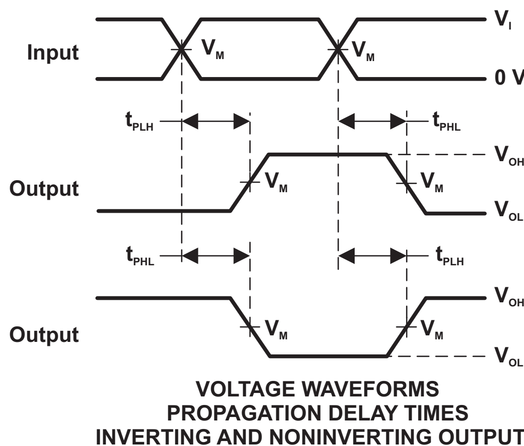


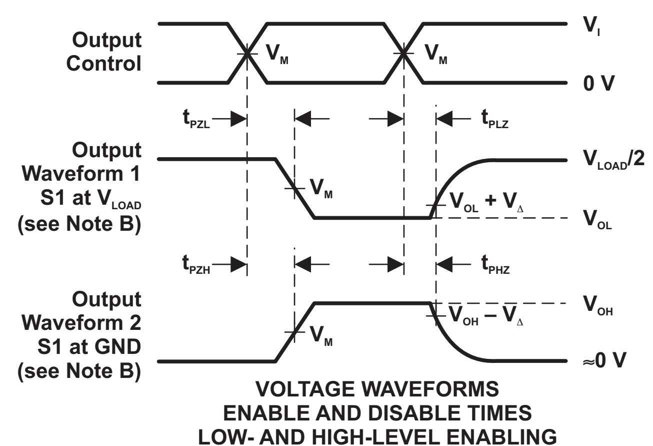

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 1 MΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 1 MΩ | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 15 pF | 1 MΩ | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 1 MΩ | 0.3 V |




NOTES:
- A. $C_L$ includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
- F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
- G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
- H. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**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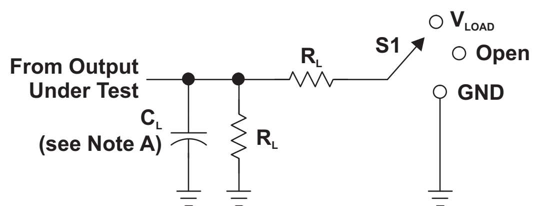
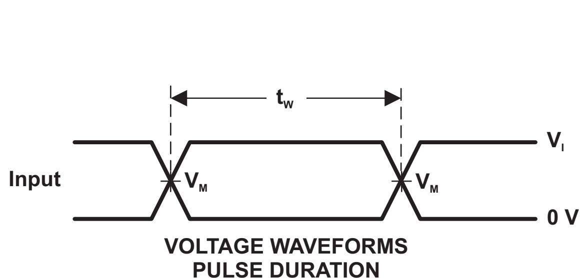
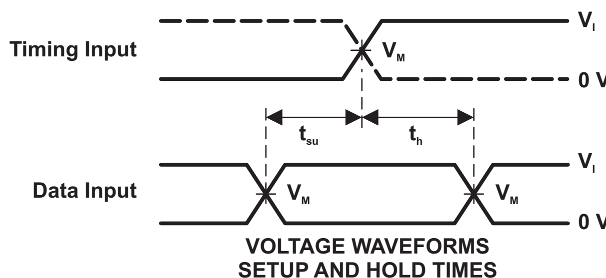
## Parameter Measurement Information (continued)

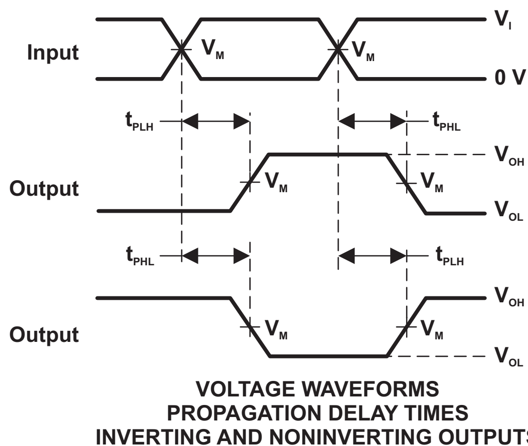


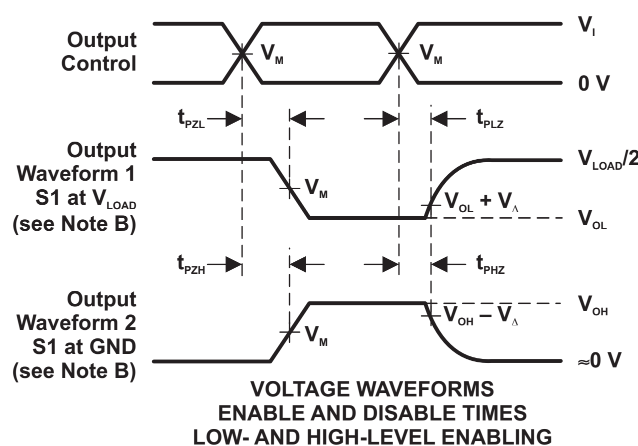

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 50 pF | 500 Ω | 0.3 V |




NOTES:
- A. $C_L$ includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
- F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
- G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
- H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

This 3-input AND gate is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

The SN74LVC1G11 device features a three-input AND gate. The output state is determined by eight patterns of 3-bit input. All inputs can be connected to $V_{CC}$ or GND.

This device is fully-specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## 8.2 Functional Block Diagram

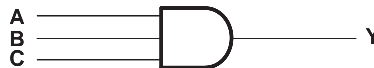



**Figure 4. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

The SN74LVC1G11 device has a wide operating $V_{CC}$ range of 1.65 V to 5.5 V, which allows use in a broad range of systems. The 5.5-V I/Os allow down translation and also allow voltages at the inputs when $V_{CC}$ = 0 V.

## 8.4 Device Functional Modes

Table 1 lists the functional modes of SN74LVC1G11.

**Table 1. Function Table**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | H | H | H |
| L | X | X | L |
| X | L | X | L |
| X | X | L | L |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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Validate and test the design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LVC1G11 device offers logical AND configuration for many design applications. This example describes basic power sequencing using the AND gate configuration. Power sequencing is often used in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning. In the application below, the power-good signals from the supplies tell the MCU to continue an operation.

## 9.2 Typical Application

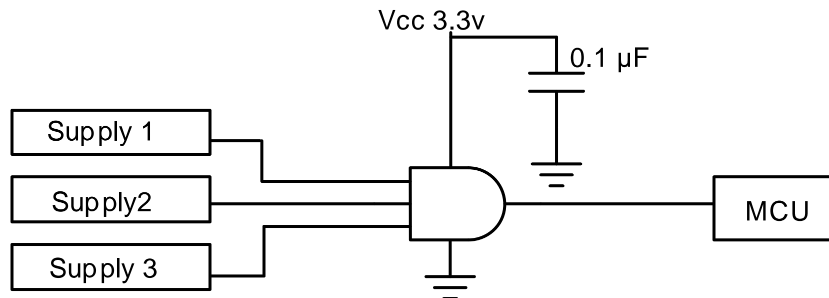



**Figure 5. Typical Application Diagram**

### 9.2.1 Design Requirements

- Recommended input conditions:
  - For rise time and fall time specifications, see Δt/Δv in the *Recommended Operating Conditions* table.
  - For specified high and low levels, see $V_{IH}$ and $V_{IL}$ in the *Recommended Operating Conditions* table.
  - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid $V_{CC}$.
- Recommended output conditions:
  - Load currents must not exceed ±50 mA.
- Frequency selection criterion:
  - Figure 6 illustrates the effects of frequency on output current.
  - Added trace resistance and capacitance can reduce maximum frequency capability. Follow the layout practices listed in the *Layout* section.

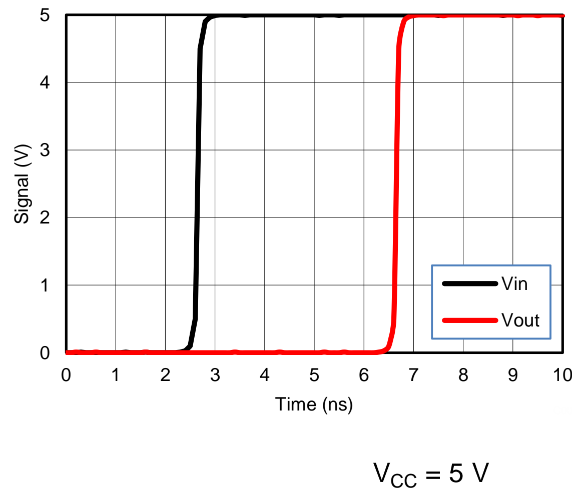
## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

The SN74LVC1G11 device uses CMOS technology and has balanced output drive. Avoid bus contentions that can drive currents that can exceed maximum limits.

The SN74LVC1G11 allows for performing the logical AND function with digital signals. Maintain input signals as close as possible to either 0 V or $V_{CC}$ for optimal operation.

### 9.2.3 Application Curve




$V_{CC}$ = 5 V

**Figure 6. Simulated Input-to-Output Voltage Response Showing Propagation Delay**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions* table.

To prevent power disturbance, ensure good bypass capacitance for each $V_{CC}$ terminal. For devices with a single-supply, a 0.1-µF bypass capacitor is recommended. If multiple pins are labeled $V_{CC}$, then a 0.01-µF or 0.022-µF capacitor is recommended for each $V_{CC}$ because the $V_{CC}$ pins are tied together internally. For devices with dual supply pins operating at different voltages, for example $V_{CC}$ and $V_{DD}$, a 0.1-µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. Place the bypass capacitor as close to the power terminal as possible for best results.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# 11 Layout

## 11.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions (or parts of functions) of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or when only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected, because the undefined voltages at the outside connections result in undefined operational states. Figure 7 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted, which does not disable the input section of the I/Os. Therefore, the I/Os cannot float when disabled.

## 11.2 Layout Example

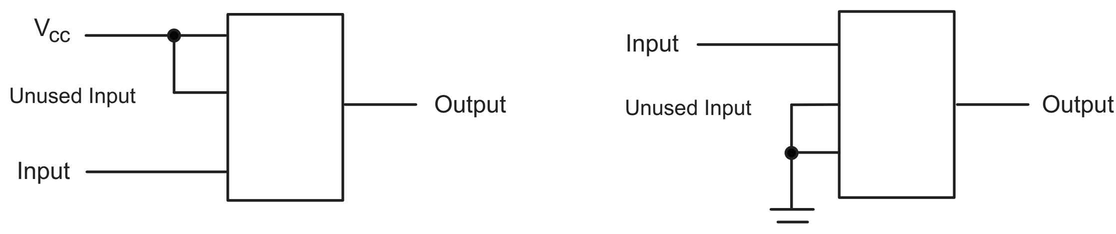


**Figure 7. Layout Diagrams**

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# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:
- *Implications of Slow or Floating CMOS Inputs*, SCBA004
- *Selecting the Right Texas Instruments Signal Switch*, SZZA030

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G11DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 125 | (C115 ~ C11F ~ C11K ~ C11R) | Samples |
| SN74LVC1G11DBVRE4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C11F | Samples |
| SN74LVC1G11DBVRG4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C11F | Samples |
| SN74LVC1G11DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C35 ~ C3F ~ C3K ~ C3R) | Samples |
| SN74LVC1G11DCKRE4 | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C35 ~ C3F ~ C3K ~ C3R) | Samples |
| SN74LVC1G11DCKRG4 | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C35 ~ C3F ~ C3K ~ C3R) | Samples |
| SN74LVC1G11DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C3 | Samples |
| SN74LVC1G11DSFR | ACTIVE | SON | DSF | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C3 | Samples |
| SN74LVC1G11YZPR | ACTIVE | DSBGA | YZP | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (C32 ~ C3N) | Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC1G11 :**

- Automotive: SN74LVC1G11-Q1

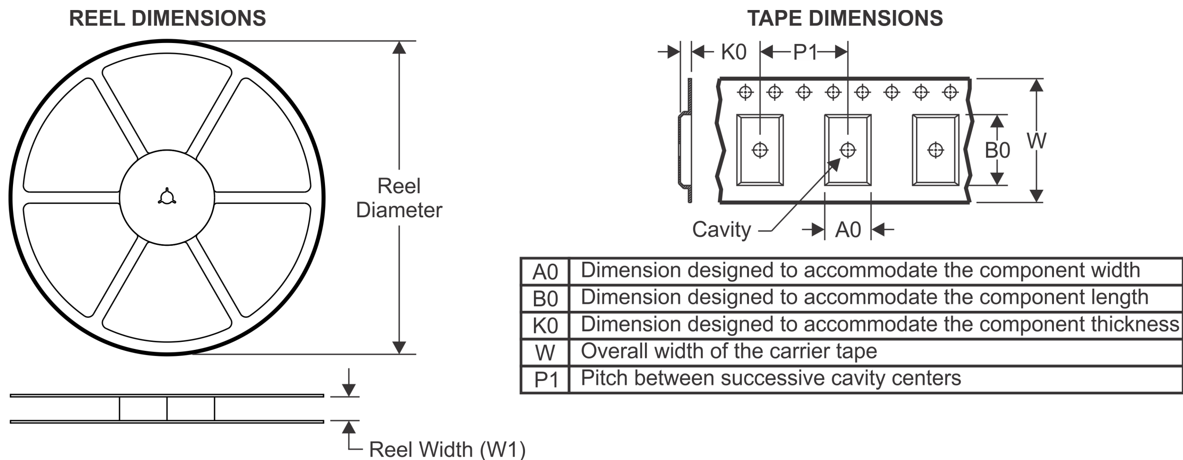
- Enhanced Product: SN74LVC1G11-EP

NOTE: Qualified Version Definitions:

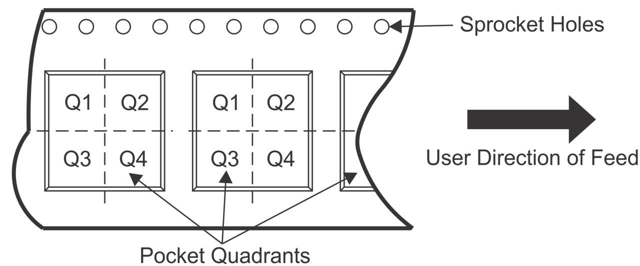
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



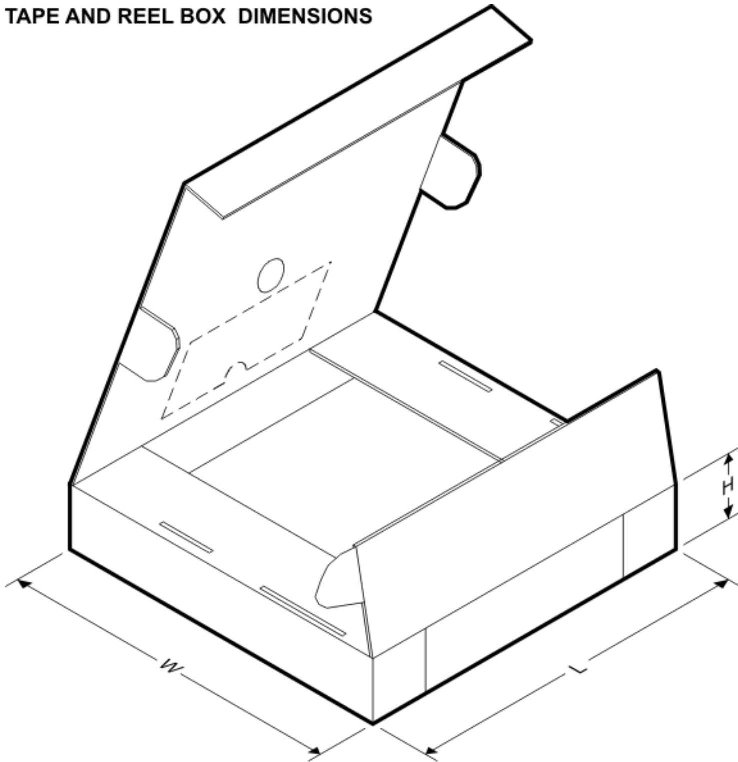

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G11DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G11DBVRG4 | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G11DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 9.2 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G11DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G11DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74LVC1G11DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1G11YZPR | DSBGA | YZP | 6 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



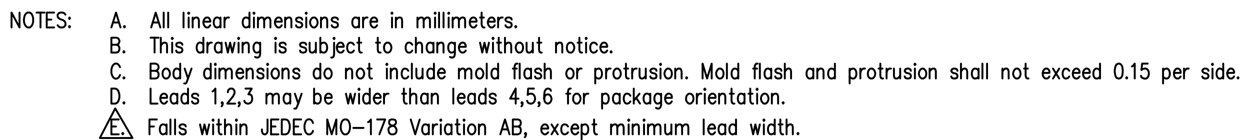

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC1G11DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G11DBVRG4 | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G11DCKR | SC70 | DCK | 6 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G11DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G11DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G11DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G11YZPR | DSBGA | YZP | 6 | 3000 | 220.0 | 220.0 | 35.0 |

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE

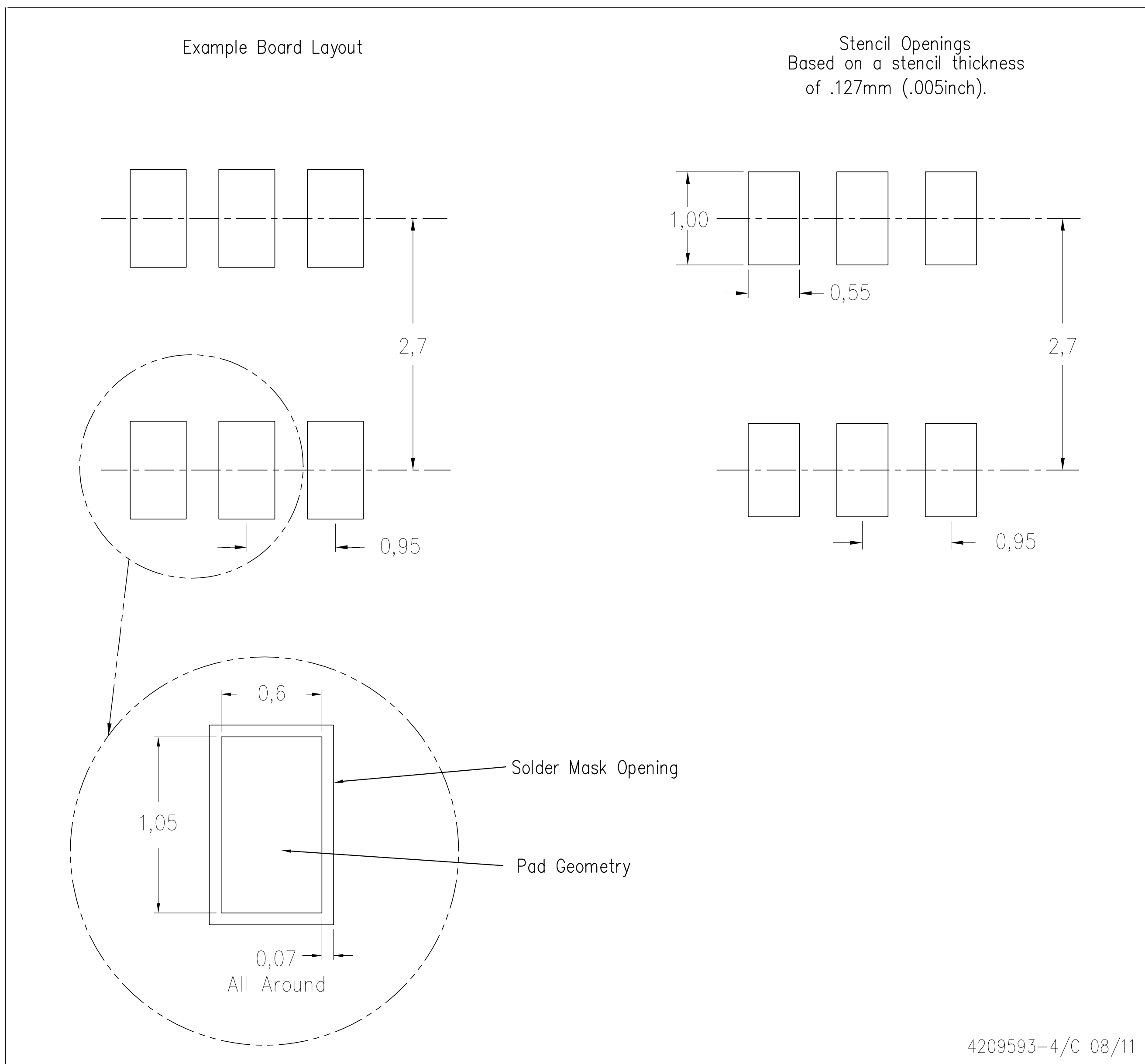
0,95
6X 0,50 / 0,25
0,20 Ⓜ
6 4
1 3
1,75 / 1,45
3,00 / 2,60
3,05 / 2,75
Pin 1 Index Area (See Detail)
Pin 1 Index Area
DETAIL: OPTIONAL ORIENTATION MARKING
0,22 / 0,08
Gage Plane
0,25
0°–8°
0,60 / 0,30
1,45 MAX
0,15 / 0,00
Seating Plane
0,10

4073253-5/N 12/14



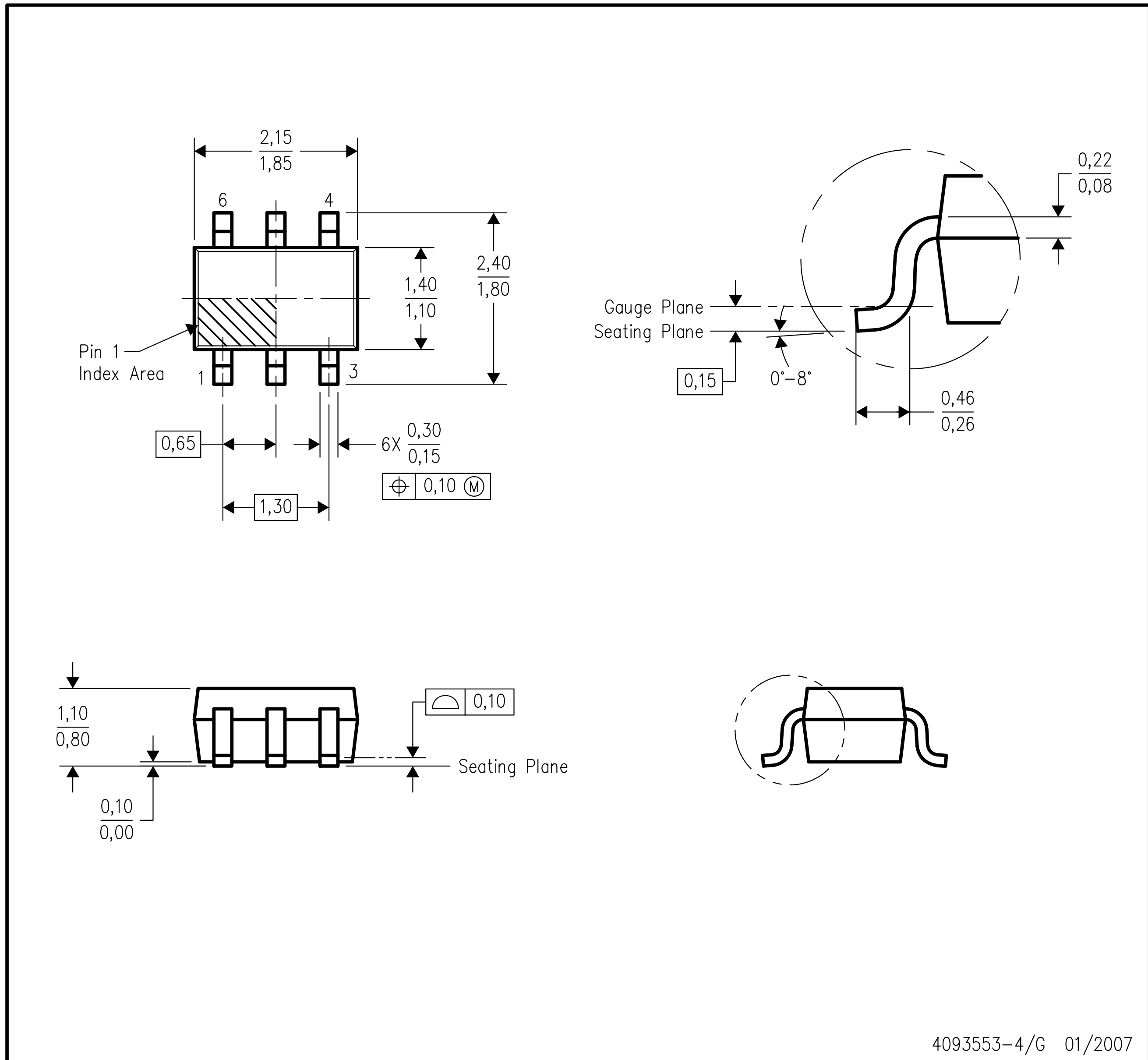
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE



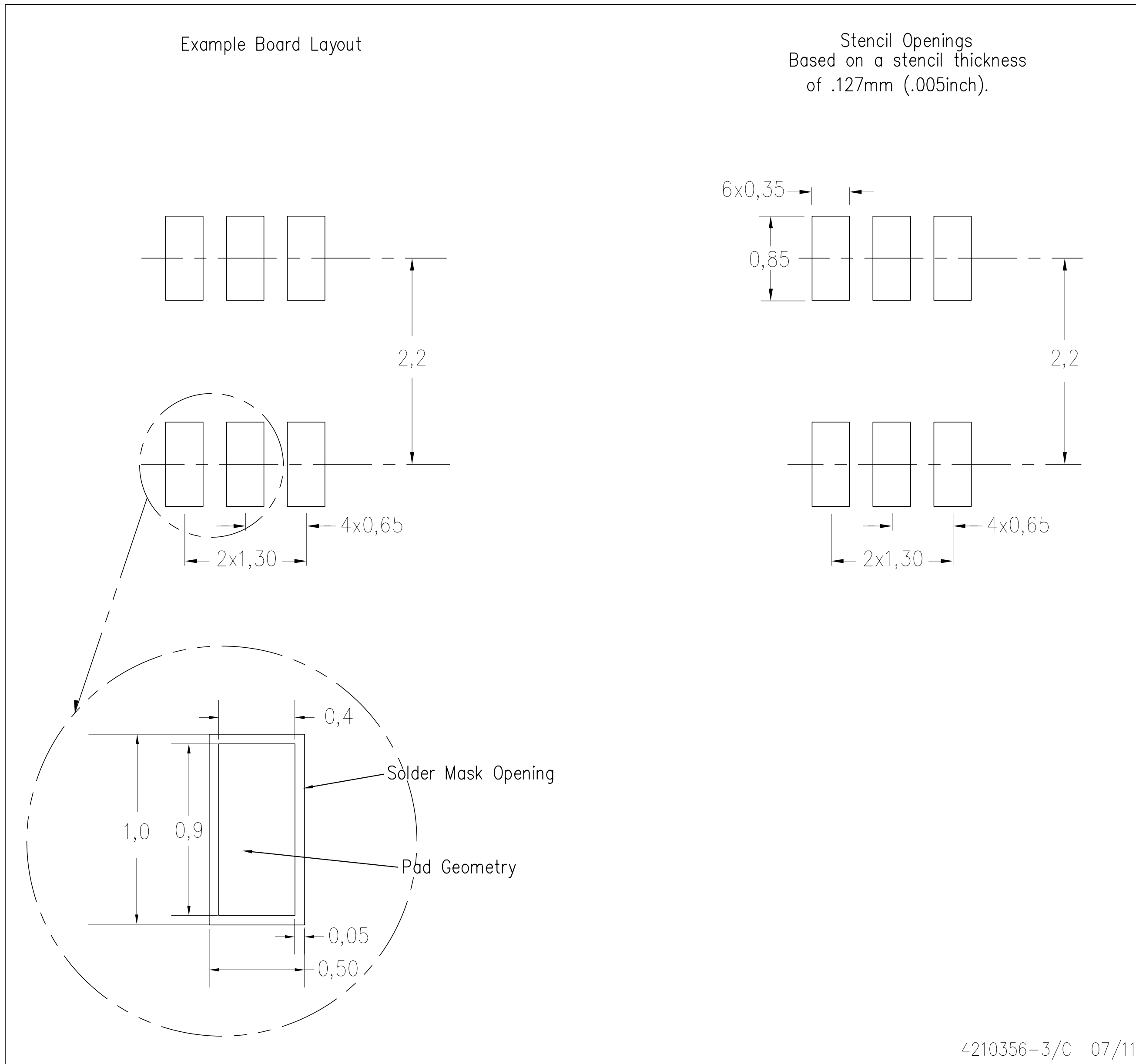

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



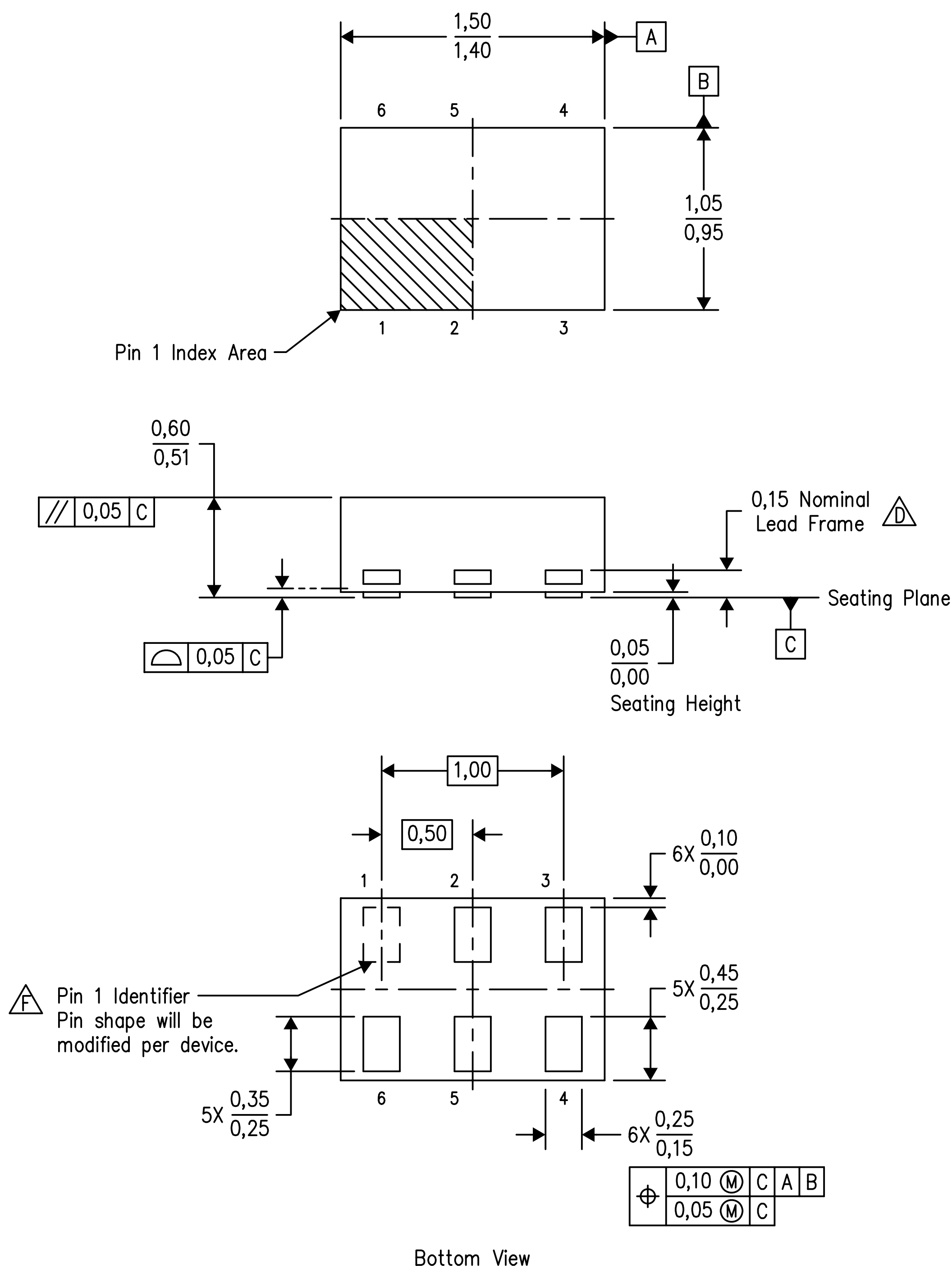

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

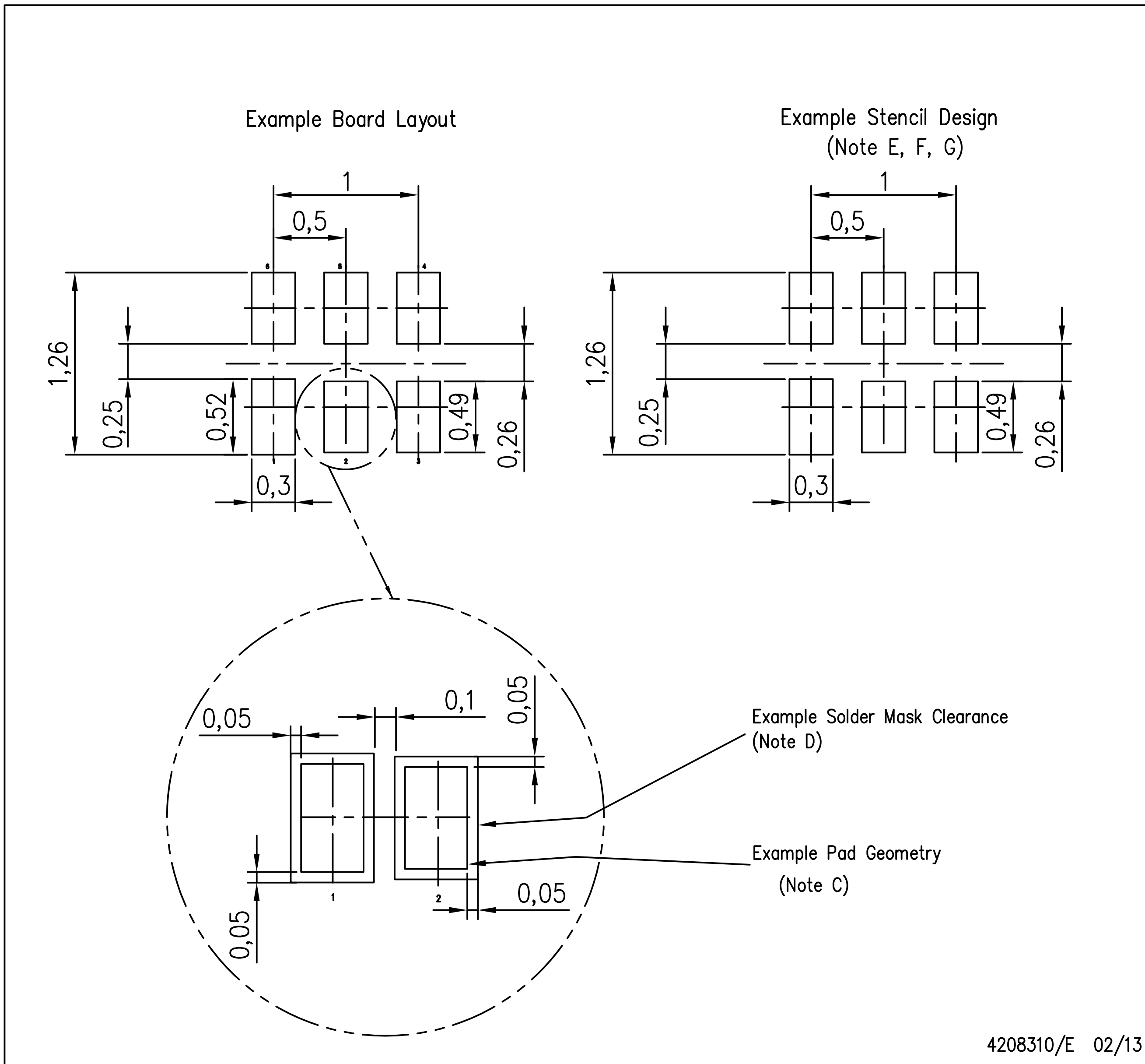
DRY (R-PUSON-N6) PLASTIC SMALL OUTLINE NO-LEAD




4207181/F 12/11

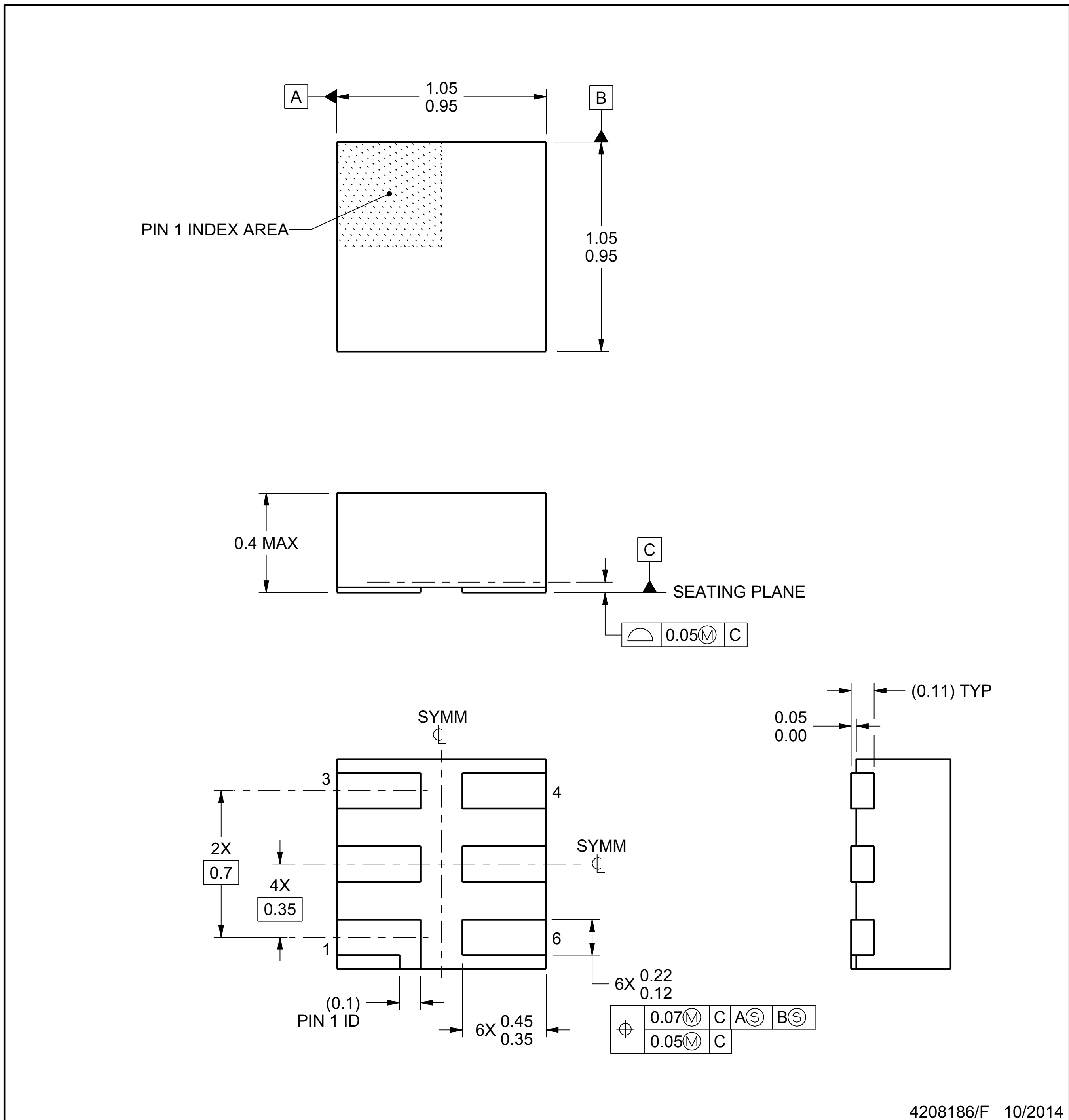
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
- E. This package complies to JEDEC MO-287 variation UFAD.
- F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



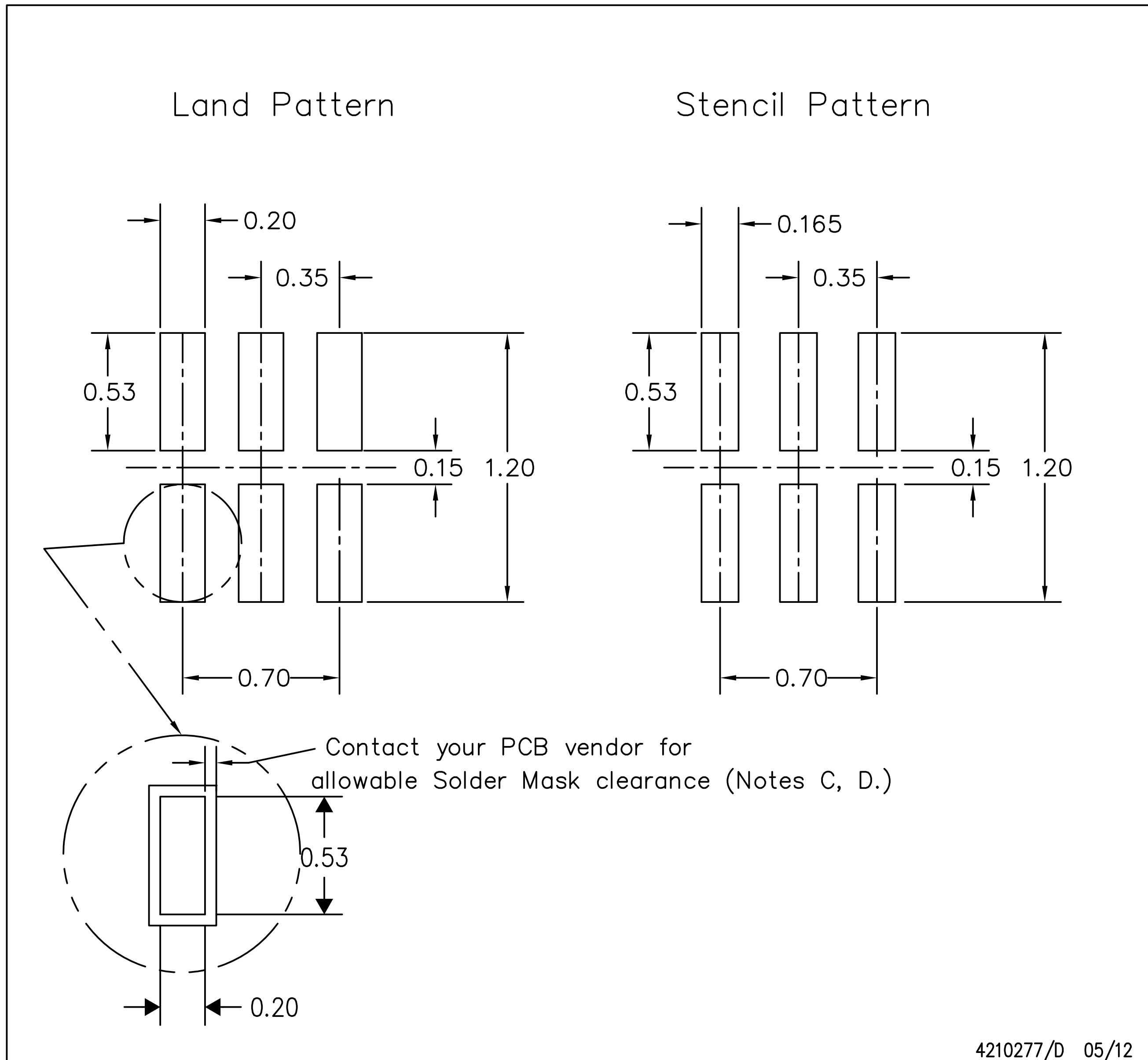

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DSF (S-PX2SON-N6) PLASTIC SMALL OUTLINE NO-LEAD

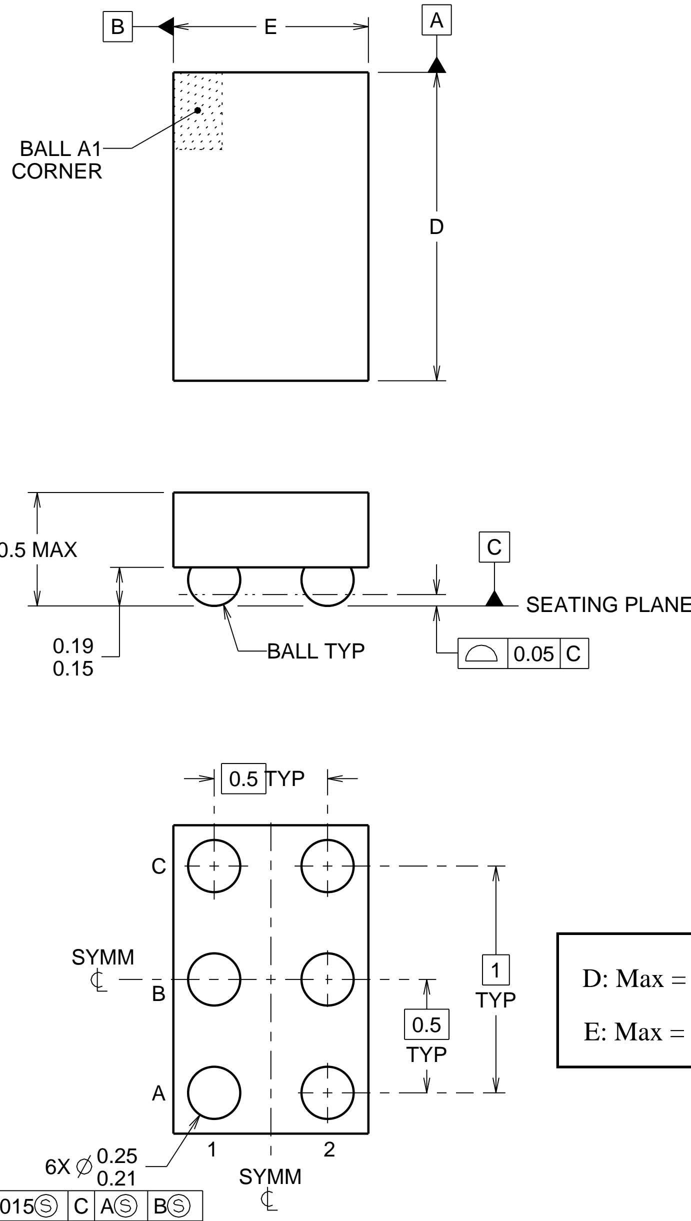



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.




NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- H. Component placement force should be minimized to prevent excessive paste block deformation.




D: Max = 1.418 mm, Min =1.358 mm

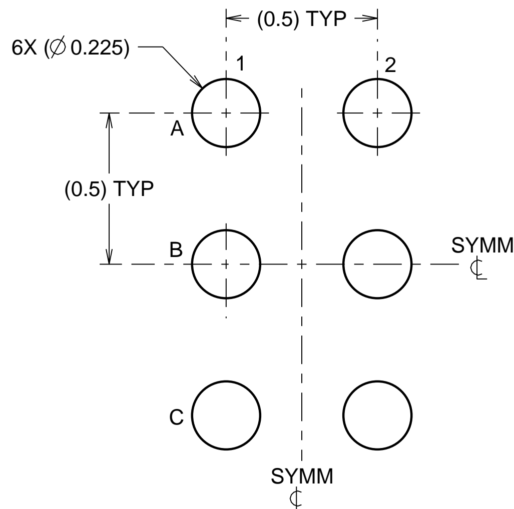
E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

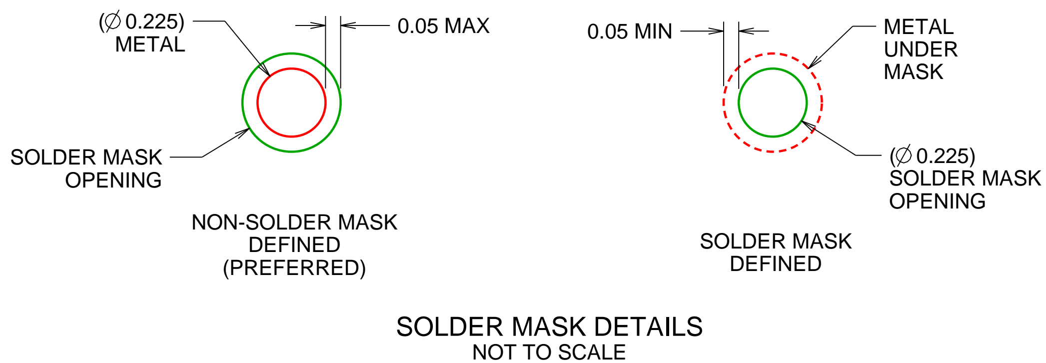
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.




LAND PATTERN EXAMPLE
SCALE:40X

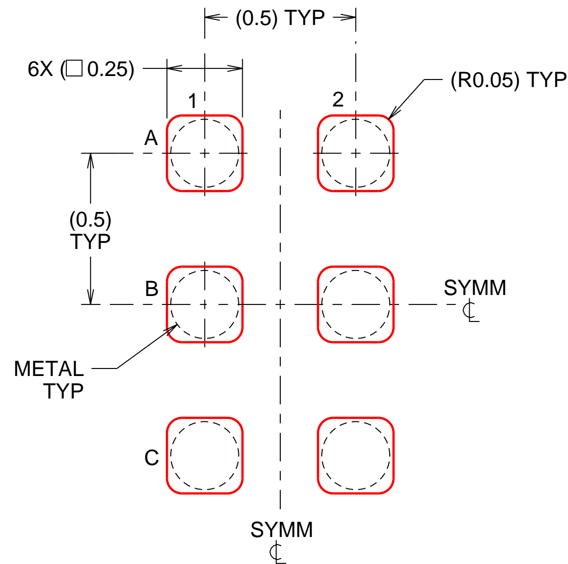



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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