1 kV Three to Six-Channel Digital Isolators

Features

- High-speed operation
  - DC to 10 Mbps
- No start-up initialization required
- Wide Operating Supply Voltage
  - 3.15 – 5.5 V
- Up to 1000 V_{RMS} isolation
- High electromagnetic immunity
- Low power consumption (typical)
  - 2.3 mA per channel at 10 Mbps
- Tri-state outputs with ENABLE
- Schmitt trigger inputs
- Default high or low output
- Precise timing (typical)
  - 40 ns propagation delay
  - 20 ns pulse width distortion
  - 100 ns minimum pulse width
- Transient Immunity 50 kV/µs
- AEC-Q100 qualification
- Wide temperature range
  - –40 to 125 °C
- RoHS-compliant packages
  - QSOP-16

Ordering Information:

See page 18.

Applications

- Industrial automation systems
- Medical electronics
- Hybrid electric vehicles
- Isolated ADC, DAC
- Power inverters
- Communication systems

Description

Silicon Lab's family of low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages over legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges and throughout device service life for ease of design and highly uniform performance. All device versions have Schmitt trigger inputs for high noise immunity and only require VDD bypass capacitors. Data rates up to 10 Mbps are supported, and all devices achieve propagation delays of less than 65 ns. Enable inputs provide a single point control for enabling and disabling output drive. Ordering options include a choice of 1kV_{RMS} isolation ratings.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	–40	25	125	ºC
Supply Voltage	V_{DD1}	3.15	—	5.5	V
	V_{DD2}	3.15	—	5.5	V

***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 2. Electrical Characteristics

(V_{DD1} = 3.15 to 5.5 V, V_{DD2} = 3.15 to 5.5 V, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	2.65	2.80	3.05	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	2.2	2.50	2.75	V
VDD Undervoltage Threshold Hysteresis	VDD_{HYS}		—	270	—	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.6	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.2	1.4	V
Input Hysteresis	V_{HYS}		—	0.40	—	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level input voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	16	—	µA
Supply Current (DC) V_{DD1} V_{DD2}		 V_I = 0, 1 C_L = 15 pF	 — —	 4.4 7.5	 7.5 10	 mA mA

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued)
(V_{DD1} = 3.15 to 5.5 V, V_{DD2} = 3.15 to 5.5 V, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current (10 Mbps) V_{DD1} V_{DD2}		V_I = 5 MHz C_L = 15 pF	— —	4.4 9.4	7.5 12	mA mA
Maximum Data Rate			0	—	10	Mbps
Minimum Pulse Width			—	—	100	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	20	40	65	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	20	30	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	20	30	ns
Channel-Channel Skew	t_{PSK}		—	20	30	ns
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V V_{CM} = 1500 V (see Figure 3)	35	50	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 1	—	10	—	ns
Enable to Data Tri-State	t_{en2}	See Figure 1	—	10	—	ns
Start-up Time[3]	t_{SU}		—	40	—	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

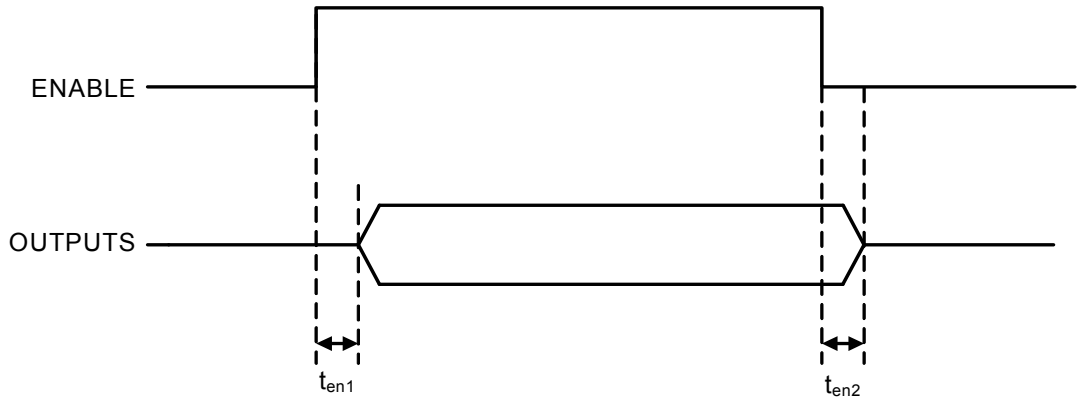


Figure 1. ENABLE Timing Diagram

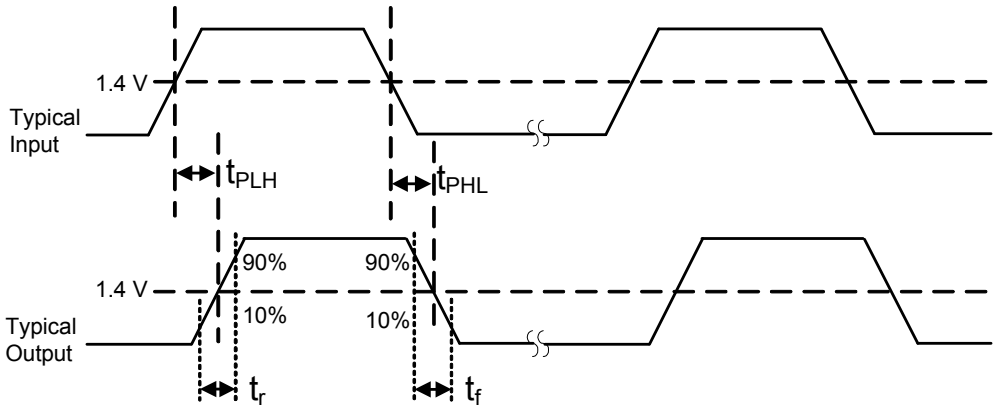


Figure 2. Propagation Delay Timing

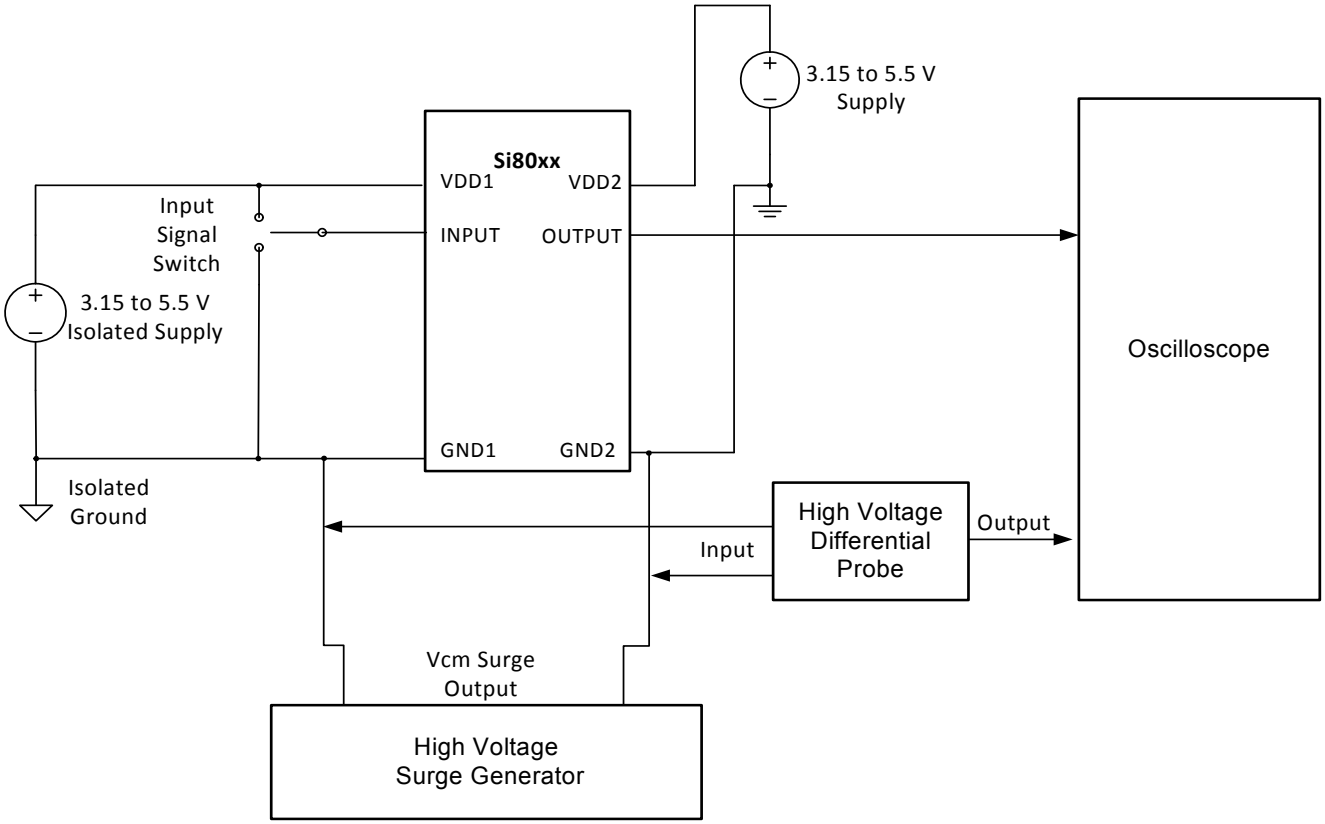


Figure 3. Common Mode Transient Immunity Test Circuit

Table 3. Thermal Characteristics

Parameter	Symbol	QSOP-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	105	ºC/W

Table 4. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	ºC
Ambient Temperature Under Bias	T_A	–40	—	125	ºC
Junction Temperature	T_J	—	—	150	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	—	7.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	—	22	mA
Latchup Immunity[3]		—	—	100	V/ns
Lead Solder Temperature (10 s)		—	—	260	ºC
Maximum Isolation (Input to Output) (1 sec) QSOP-16		—	—	1500	V_{RMS}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.
3. Latchup immunity specification is for slew rate applied across GND1 and GND2.

2. Functional Description

2.1. Theory of Operation

The Si80xx comprises a transmitter and a receiver separated by a semiconductor-based isolation barrier. The Si80xx uses a high-frequency internal oscillator on the transmitter to modulate digital input signals across the capacitive isolation barrier. On the receiver side, these signals are demodulated back to the corresponding digital output signals that are galvanically isolated from the input. This simple and elegant architecture provides a robust data path and requires no special considerations or initialization at start-up. A simplified block diagram for an Si80xx data channel is shown in Figure 4.

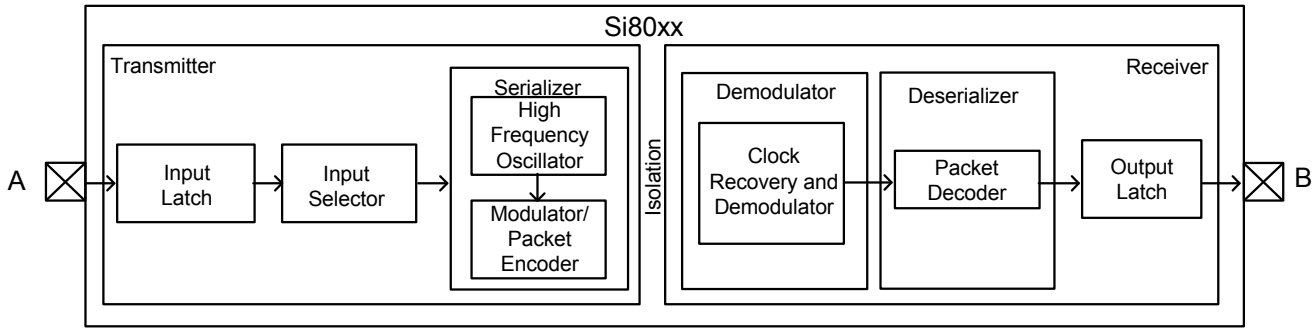


Figure 4. Simplified Channel Diagram

The transmitter consists of an input stage that latches in data from up to six asynchronous channels, followed by a serializer stage where the data is compressed into serial data packets that are then coupled across the capacitive isolation barrier. The receiver consists of a demodulator block that converts the modulated signal back into serial data packets that are then deserialized and latched to the output.

3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 5, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Refer to Table 5 to determine outputs when power supply (VDD) is not present. Additionally, refer to Table 6 for logic conditions when enable pins are used.

Table 5. Si80xx Logic Operation

V_I Input[1,2]	EN Input[1,2,3,4]	VDDI State[1,5,6]	VDDO State[1,5,6]	V_O Output[1,2]	Comments
H	H or NC	P	P	H	Enabled, normal operation.
L	H or NC	P	P	L	
X[7]	L	P	P	Hi-Z[8]	Disabled.
X[7]	H or NC	UP	P	L[9] H[9]	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I after Start-up Time, t_{SU}
X[7]	L	UP	P	Hi-Z[8]	Disabled.
X[7]	X[7]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I after Start-up Time, t_{SU}, if EN is in either the H or NC state. Upon transition of VDDO from unpowered to powered, V_O returns to Hi-Z after Start-up Time, t_{SU}, if EN is L.

Notes:

1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals. EN is the enable control input located on the same output side.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. It is recommended that the enable inputs be connected to an external logic high or low level when the Si80xx is operating in noisy environments.
4. No Connects are not internally connected and can be left floating, tied to VDD, or tied to GND.
5. “Powered” state (P) is defined as 3.15 V < VDD < 5.5 V.
6. “Unpowered” state (UP) is defined as VDD = 0 V.
7. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
8. When using the enable pin (EN) function, the output pin state is driven into a high-impedance state when the EN pin is disabled (EN = 0).
9. See "9. Ordering Guide" on page 18 for details. This is the selectable fail-safe operating mode (ordering option). Some devices have default output state = H, and some have default output state = L, depending on the ordering part number (OPN). For default high devices, the data channels have pull-ups on inputs/outputs. For default low devices, the data channels have pull-downs on inputs/outputs.

Table 6. Enable Input Truth[1]

P/N	EN2[1,2]	Operation
Si8030 Si8040 Si8050	H	Outputs B1, B2, B3, B4, B5, B6 are enabled and follow input state.
	L	Outputs B1, B2, B3, B4, B5, B6 are disabled and Logic Low or in high impedance state.[3]
Si8035 Si8045 Si8055 Si8065	—	Outputs B1, B2, B3, B4, B5, B6 are enabled and follow input state.

Notes:

1. Enable, EN, can be used for multiplexing, for clock sync, or other output control. EN is internally pulled-up to local VDD by a 16 µA current source allowing it to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to EN if it is left floating. If EN is unused, it is recommended that it be connected to an external logic level, especially if the Si80xx is operating in a noisy environment.
2. X = not applicable; H = Logic High; L = Logic Low.
3. When using the enable pin (EN) function, the output pin state is driven into a high-impedance state when the EN pin is disabled (EN = 0).

3.1. Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

3.2. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when V_{DD1} falls below $V_{DD1(UVLO–)}$ and exits UVLO when V_{DD1} rises above $V_{DD1(UVLO+)}$. Side B operates the same as Side A with respect to its V_{DD2} supply. See Figure 5 for more details.

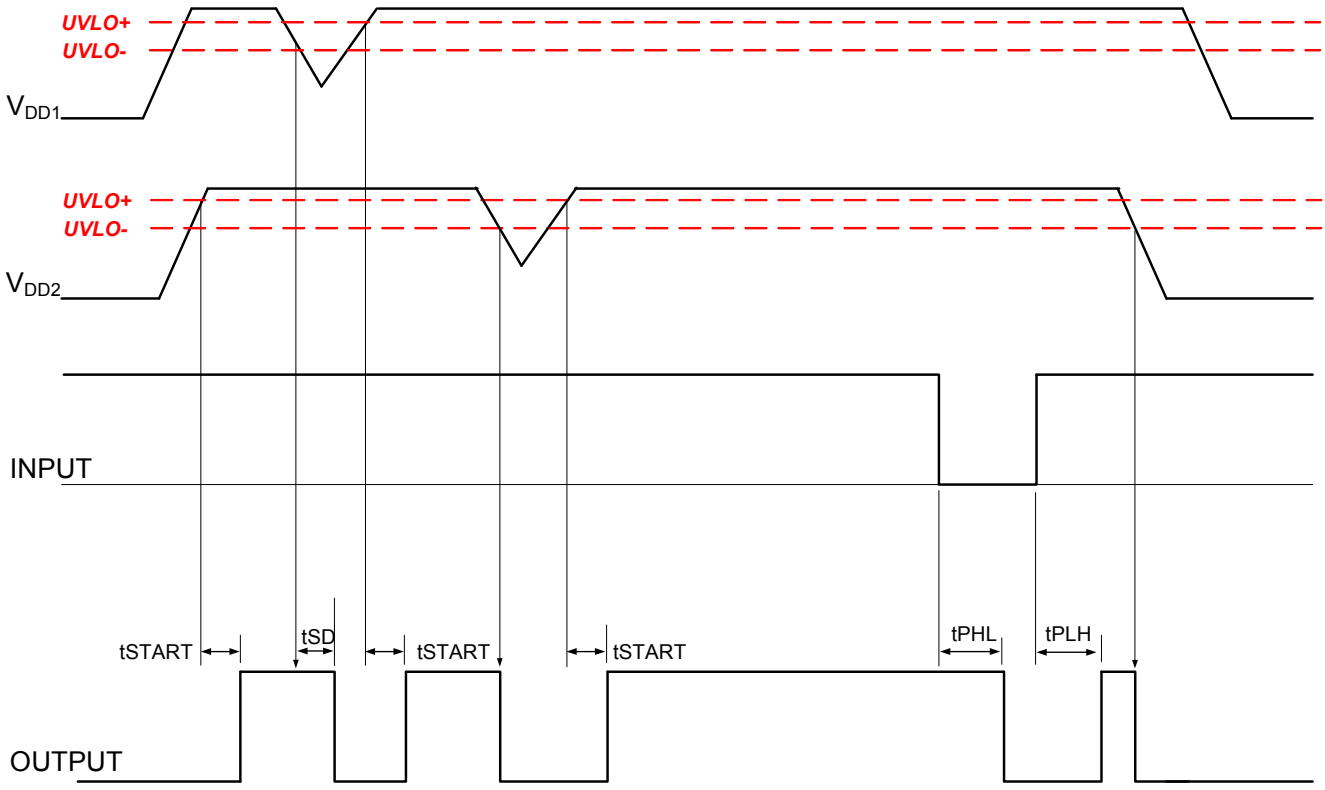


Figure 5. Device Behavior during Normal Operation

3.3. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.3.1. Supply Bypass

The Si80xx family requires a 0.1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

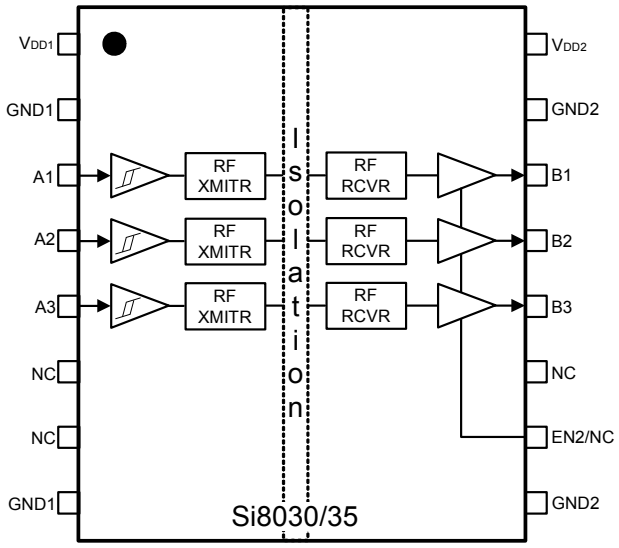
3.3.2. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

3.4. Fail-Safe Operating Mode

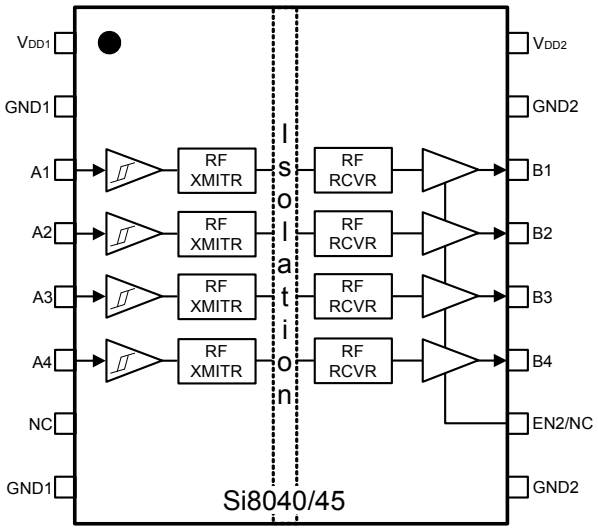
Si80xx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is not powered) can either be a logic high or logic low when the output supply is powered. See Table 5 on page 9 and "9. Ordering Guide" on page 18 for more information.

4. Pin Descriptions (Si8030/35)



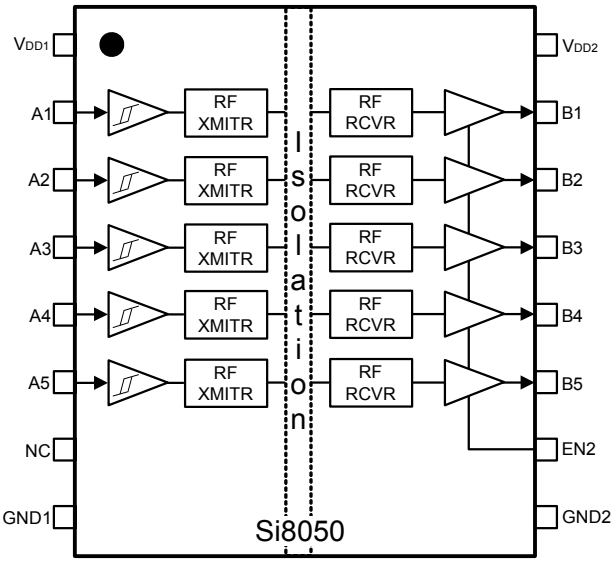
Name	Pin#	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
GND1	2	Ground	Side 1 ground.
A1	3	Digital Input	Side 1 digital input.
A2	4	Digital Input	Side 1 digital input.
A3	5	Digital Input	Side 1 digital input.
NC*	6	NA	No Connect.
NC*	7	NA	No Connect.
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
EN2/NC*	10	Digital Input	Side 2 active high enable on Si8030. NC on Si8035.
NC*	11	NA	No Connect.
B3	12	Digital Output	Side 2 digital output.
B2	13	Digital Output	Side 2 digital output.
B1	14	Digital Output	Side 2 digital output.
GND2	15	Ground	Side 2 ground.
V_{DD2}	16	Supply	Side 2 power supply.
***Note:** No Connect. These pins are not internally connected. They can be left floating, tied to V_{DD} or tied to GND.			

5. Pin Descriptions (Si8040/45)



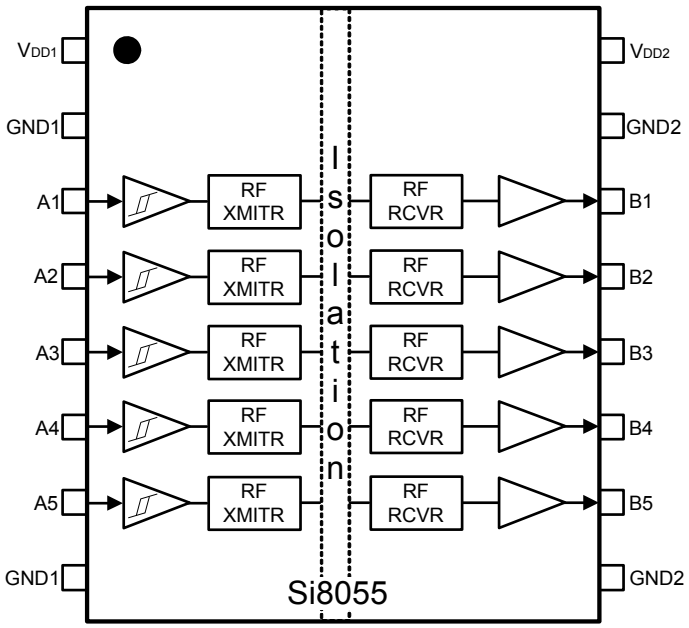
Name	Pin#	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
GND1	2	Ground	Side 1 ground.
A1	3	Digital Input	Side 1 digital input.
A2	4	Digital Input	Side 1 digital input.
A3	5	Digital Input	Side 1 digital input.
A4	6	Digital Input	Side 1 digital input.
NC*	7	NA	No Connect.
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
EN2/NC*	10	Digital Input	Side 2 active high enable on Si8040. NC on Si8045.
B4	11	Digital Output	Side 2 digital output.
B3	12	Digital Output	Side 2 digital output.
B2	13	Digital Output	Side 2 digital output.
B1	14	Digital Output	Side 2 digital output.
GND2	15	Ground	Side 2 ground.
V_{DD2}	16	Supply	Side 2 power supply.
***Note:** No Connect. These pins are not internally connected. They can be left floating, tied to V_{DD} or tied to GND.			

6. Pin Descriptions (Si8050)



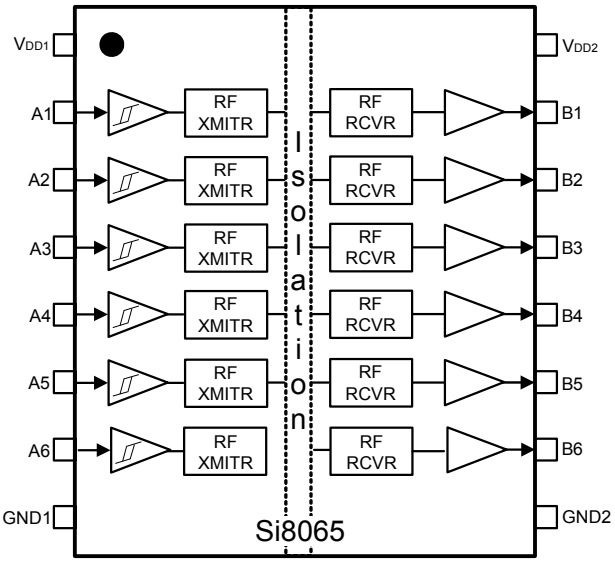
Name	Pin#	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
A1	2	Digital Input	Side 1 digital input.
A2	3	Digital Input	Side 1 digital input.
A3	4	Digital Input	Side 1 digital input.
A4	5	Digital Input	Side 1 digital input.
A5	6	Digital Input	Side 1 digital input.
NC*	7	NA	No connect.
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
EN2	10	Digital Input	Side 2 active high enable on Si8050.
B5	11	Digital Output	Side 2 digital output.
B4	12	Digital Output	Side 2 digital output.
B3	13	Digital Output	Side 2 digital output.
B2	14	Digital Output	Side 2 digital output.
B1	15	Digital Output	Side 2 digital output.
V_{DD2}	16	Supply	Side 2 power supply.
***Note:** No Connect. These pins are not internally connected. They can be left floating, tied to V_{DD} or tied to GND.			

7. Pin Descriptions (Si8055)



Name	Pin#	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
GND1	2	Ground	Side 1 ground.
A1	3	Digital Input	Side 1 digital input.
A2	4	Digital Input	Side 1 digital input.
A3	5	Digital Input	Side 1 digital input.
A4	6	Digital Input	Side 1 digital input.
A5	7	Digital Input	Side 1 digital input.
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
B5	10	Digital Output	Side 2 digital output.
B4	11	Digital Output	Side 2 digital output.
B3	12	Digital Output	Side 2 digital output.
B2	13	Digital Output	Side 2 digital output.
B1	14	Digital Output	Side 2 digital output.
GND2	15	Ground	Side 2 ground.
V_{DD2}	16	Supply	Side 2 power supply.

8. Pin Descriptions (Si8065)



Name	Pin#	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
A1	2	Digital Input	Side 1 digital input.
A2	3	Digital Input	Side 1 digital input.
A3	4	Digital Input	Side 1 digital input.
A4	5	Digital Input	Side 1 digital input.
A5	6	Digital Input	Side 1 digital input.
A6	7	Digital Input	Side 1 digital input.
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
B6	10	Digital Output	Side 2 digital output.
B5	11	Digital Output	Side 2 digital output.
B4	12	Digital Output	Side 2 digital output.
B3	13	Digital Output	Side 2 digital output.
B2	14	Digital Output	Side 2 digital output.
B1	15	Digital Output	Side 2 digital output.
V_{DD2}	16	Supply	Side 2 power supply.

9. Ordering Guide

Table 7. Ordering Guide for Valid OPNs[1,2,3]

Ordering Part Number (OPN)	Number of Inputs/Outputs	Default Output State	Output Enable Yes/No	Isolation Rating (kVrms)	Package
Si803x					
Si8030AA-B-IU	3	Low	Yes	1	QSOP-16
Si8030CA-B-IU	3	High	Yes	1	QSOP-16
Si8035AA-B-IU	3	Low	No	1	QSOP-16
Si8035CA-B-IU	3	High	No	1	QSOP-16
Si804x					
Si8040AA-B-IU	4	Low	Yes	1	QSOP-16
Si8040CA-B-IU	4	High	Yes	1	QSOP-16
Si8045AA-B-IU	4	Low	No	1	QSOP-16
Si8045CA-B-IU	4	High	No	1	QSOP-16
Si805x					
Si8050AA-B-IU	5	Low	Yes	1	QSOP-16
Si8050CA-B-IU	5	High	Yes	1	QSOP-16
Si8055AA-B-IU	5	Low	No	1	QSOP-16
Si8055CA-B-IU	5	High	No	1	QSOP-16
Si806x					
Si8065AA-B-IU	6	Low	No	1	QSOP-16
Si8065CA-B-IU	6	High	No	1	QSOP-16

Notes:
1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
   Moisture sensitivity level is MSL3 for QSOP-16 packages.
2. All devices >1 kV_{RMS} are AEC-Q100 qualified.
3. “Si” and “SI” are used interchangeably.

10. Package Outline: 16-Pin QSOP

Figure 6 illustrates the package details for the Si80xx in a 16-pin QSOP package. Table 8 lists the values for the dimensions shown in the illustration.

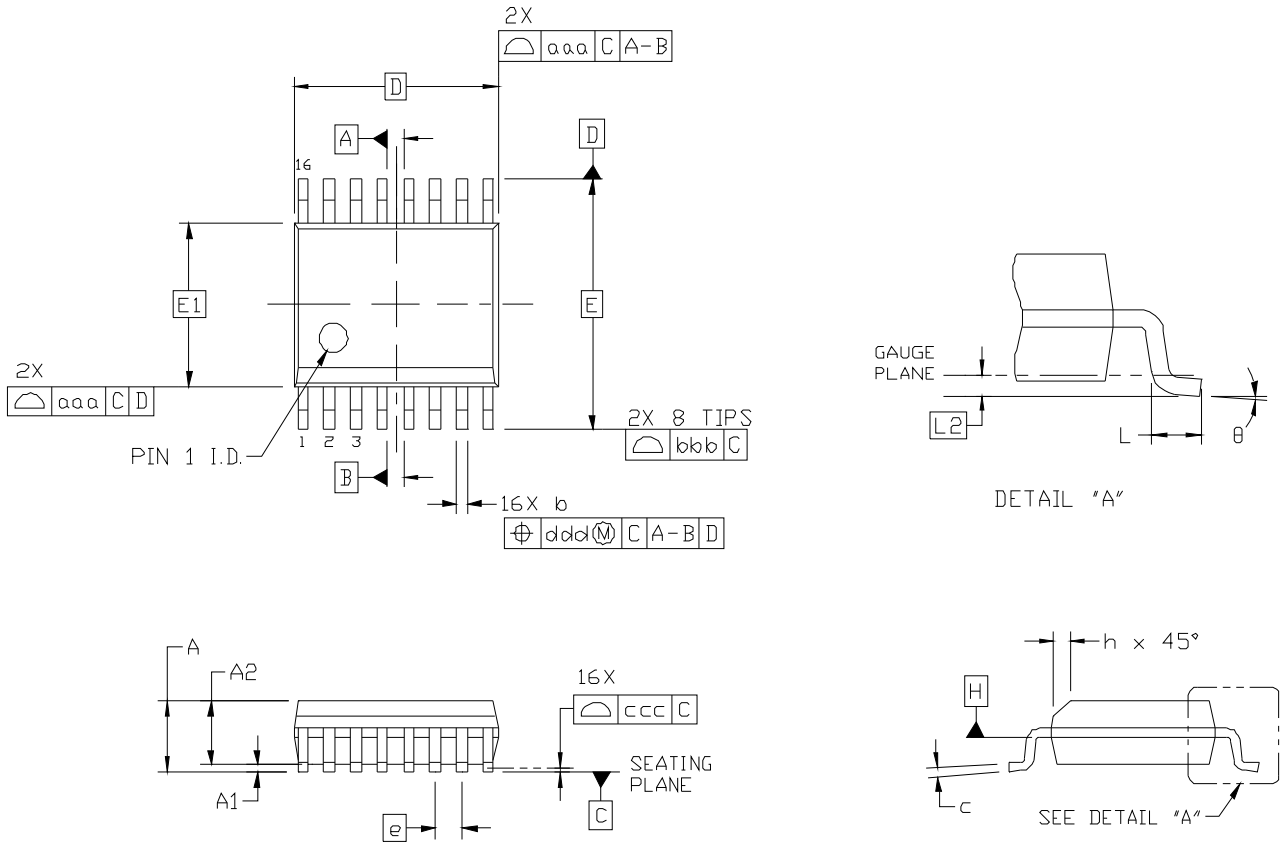


Figure 6. 16-pin QSOP Package

Table 8. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.20	0.30
c	0.17	0.25
D	4.89 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. Land Pattern: 16-Pin QSOP

Figure 7 illustrates the recommended land pattern details for the Si80xx in a 16-pin QSOP package. Table 9 lists the values for the dimensions shown in the illustration.

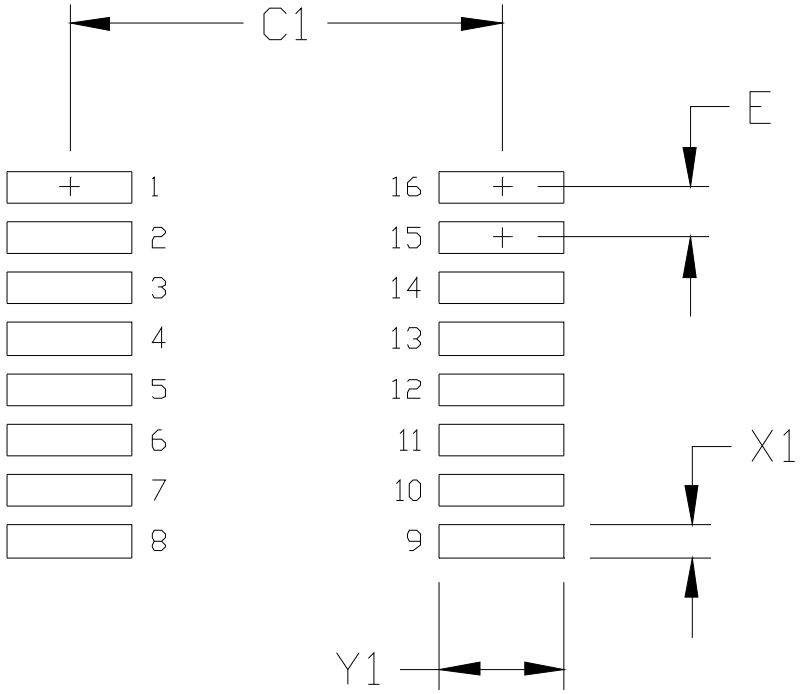


Figure 7. 16-Pin QSOP PCB Land Pattern

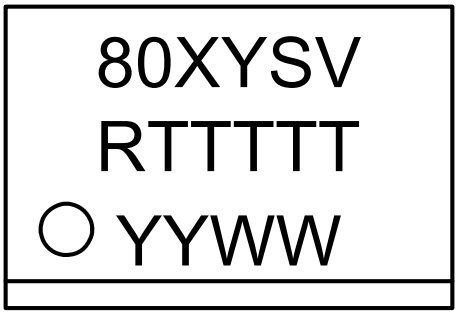
Table 9. 16-Pin QSOP Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	0.635
X1	Pad Width	0.40
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOP63P602X173-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

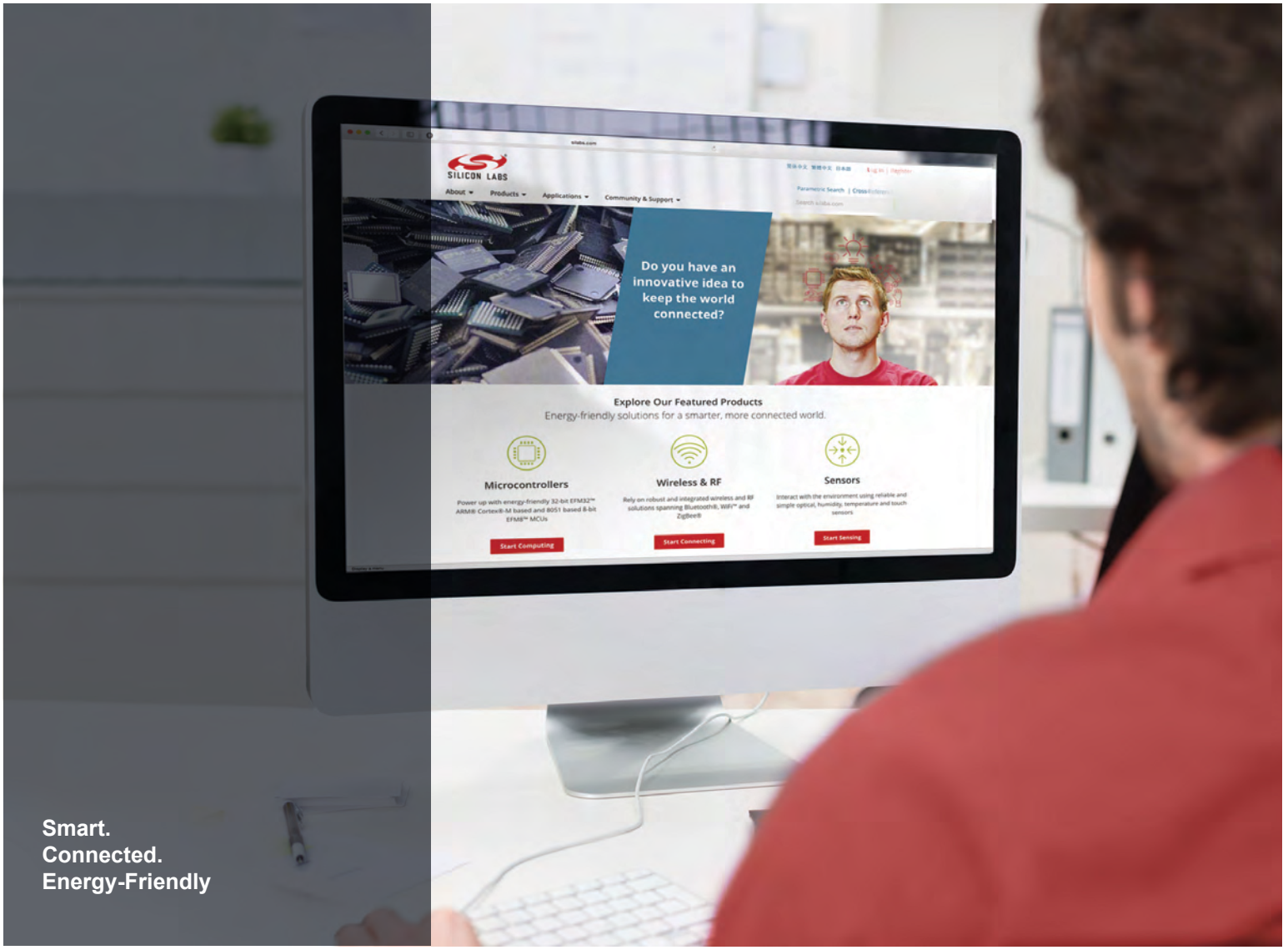
12. Top Markings

12.1. Top Marking (16-Pin QSOP)



12.2. Top Marking Explanation (16-Pin QSOP)

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	80 = Isolator product series XY = Channel Configuration X = # of data channels (6, 5, 4, 3) Y = # of reverse channels (0)* S = operating mode: A = default output = low C = default output = high V = Insulation rating A = 1 kV
Line 2 Marking:	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
Line 3 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
***Note:** Si8035/45/55/65 have 0 reverse channels.		



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