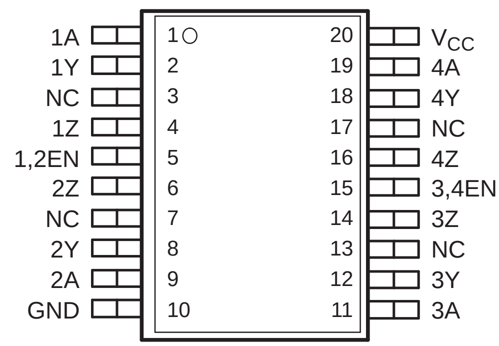
FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Designed for TIA/EIA-485, TIA/EIA-422, and ISO 8482 Applications**
- **Signaling Rates up to 30 Mbps** (2)
- **Propagation Delay Times <11 ns**
- **Low Standby Power Consumption 1.5 mA Max**
- **Output ESD Protection Exceeds 13 kV**
- **Driver Positive- and Negative-Current Limiting**
- **Power-Up and Power-Down Glitch Free for Line-Insertion Applications**
- **Thermal Shutdown Protection**
- **Industry Standard Pinout, Compatible With SN75174, MC3487, DS96174, LTC487, and MAX3042**

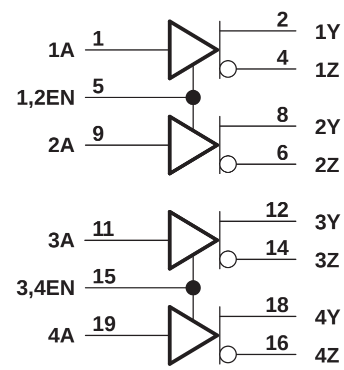
(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

(2) The signaling rate of a line is the number of voltage transitions that are made per second, expressed in the unit bits per second (bps).

20-PIN DW PACKAGE
(TOP VIEW)



logic diagram (positive logic)



DESCRIPTION/ORDERING INFORMATION

The SN65LBC174A-EP is a quadruple differential line driver with 3-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 applications.

This device is optimized for balanced multipoint bus transmission at signaling rates up to 30-million bits per second (Mbps). The transmission media may be printed-circuit-board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

Each driver features current limiting and thermal-shutdown circuitry, making it suitable for high-speed multipoint applications in noisy environments. The device is designed using LinBiCMOS™ technology, facilitating low power consumption and robustness.

The two enable (EN) inputs provide pair-wise driver enabling, or can be externally tied together to provide enable control of all four drivers with one signal. When disabled or powered off, the driver outputs present a high impedance to the bus for reduced system loading.

The SN65LBC174A-EP is characterized for operation over the temperature range of –55°C to 125°C.

ORDERING INFORMATION

T_A	PACKAGE(1)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	20-pin SOIC – DW	SN65LBC174AMDWREP	65LBC174EP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

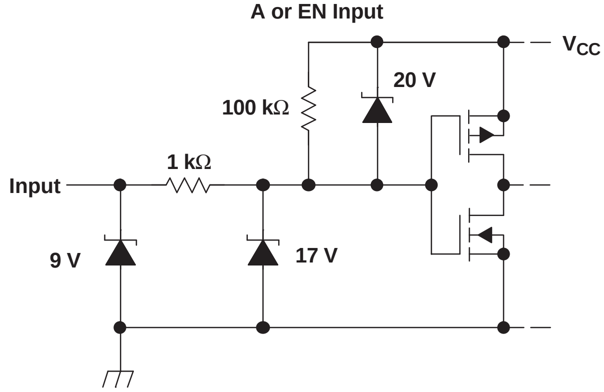
FUNCTION TABLE(1)
(each driver)

INPUT A	ENABLE G	OUTPUTS Y	OUTPUTS Z
L	H	L	H
H	H	H	L
OPEN	H	H	L
L	OPEN	L	H
H	OPEN	H	L
OPEN	OPEN	H	L
X	L	Z	Z

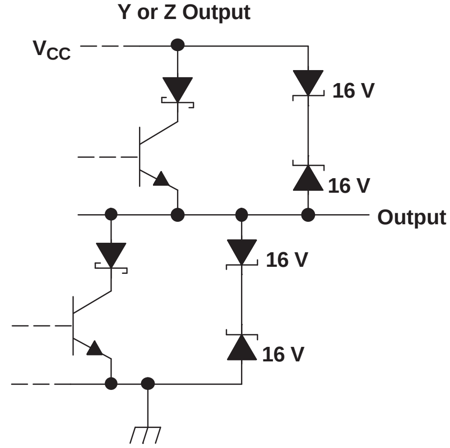
(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

A or EN Input



Y or Z Output



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)			–0.3	6	V
	Voltage range at any bus (dc)			–10	15	V
	Voltage range at any bus (transient pulse through 100 Ω, see Figure 8)			–30	30	V
V_I	Input voltage range at any A or EN terminal			–0.5	V_{CC} + 0.5	V
	Electrostatic discharge	Human-Body Model(3)	Y, Z, and GND		13	kV
			All pins		5	
		Charged-Device Model(4)	All pins		1	
T_{stg}	Storage temperature range(5)			–65	150	°C
	Continuous power dissipation			See Dissipation Rating Table		
	Lead temperature 1,6 mm (1/16 in) from case for 10 s				260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to GND.
(3) Tested in accordance with JEDEC standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC standard 22, Test Method C101.
(5) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

DISSIPATION RATING TABLE

PACKAGE	JEDEC BOARD MODEL	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
20-pin DW	Low K	1483 mW	11.86 mW/°C	949 mW	297 mW
	High K	2753 mW	22 mW/°C	1762 mW	553 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted with no air flow.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
	Voltage at any bus terminal	Y, Z	–7		12	V
V_{IH}	High-level input voltage	A, EN	2		V_{CC}	V
V_{IL}	Low-level input voltage	A, EN	0		0.8	V
	Output current		–60		60	mA
T_A	Operating free-air temperature		–55		125	°C

Electrical Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA		–1.5	–0.77		V
V_O	Open-circuit output voltage	Y or Z, No load		0		V_{CC}	V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude(2)	No load (open circuit)		3		V_{CC}	V
		R_L = 54 Ω, See Figure 1		0.8	1.6	2.5	
		With common-mode loading, See Figure 2		0.8	1.6	2.5	
$\Delta V_{OD(SS)}$	Change in steady-state differential output voltage between logic states	See Figure 1		–0.1		0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3		2	2.4	2.8	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 3		–0.04		0.04	V
I_I	Input current	A, G, $\overline{G}$		-–70		70	µA
I_{OS}	Short-circuit output current	V_{TEST} = –7 V to 12 V, See Figure 7	V_I = 0 V	–200		200	mA
			$V_I = V_{CC}$				
I_{OZ}	High-impedance-state output current		EN at 0 V	–50		50	µA
$I_{O(OFF)}$	Output current with power off		V_{CC} = 0 V	–10		10	
I_{CC}	Supply current	V_I = 0 V or V_{CC}, No load	All drivers enabled			25	mA
			All drivers disabled			1.5	

(1) All typical values are at V_{CC} = 5 V and 25°C.
(2) The minimum V_{OD} may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibility of lower output signal into account in determining the maximum signal transmission distance.

Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 54 Ω, C_L = 50 pF, See Figure 4	T_A=25°C	4.0	8	11	ns
			T_A= -55°C to 125°C	4.0		16	ns
t_{PHL}	Propagation delay time, high- to low-level output		T_A=25°C	4.0	8	11	ns
			T_A= -55°C to 125°C	4.0		16	ns
t_r	Differential output voltage rise time		T_A=25°C	3	7.5	11	ns
			T_A= -55°C to 125°C	3		24	ns
t_f	Differential output voltage fall time		T_A=25°C	3	7.5	11	ns
			T_A= -55°C to 125°C	3		24	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PLH} – t_{PHL} \rvert$				0.6		ns
					0.6		
$t_{sk(o)}$	Output skew(1)				2		ns
$t_{sk(pp)}$	Part-to-part skew(2)				3		ns
t_{PZH}	Propagation delay time, high impedance to high-level output	See Figure 5				25	ns
t_{PHZ}	Propagation delay time, high-level output to high impedance					25	ns
t_{PZL}	Propagation delay time, high impedance to low-level output	See Figure 6				30	ns
t_{PLZ}	Propagation delay time, low-level output to high impedance					20	ns

(1) Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
(2) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

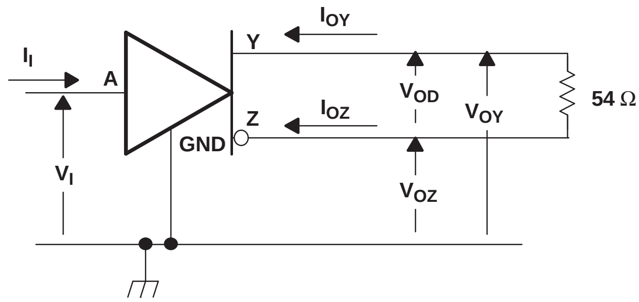


Figure 1. Test Circuit, V_{OD} Without Common-Mode Loading

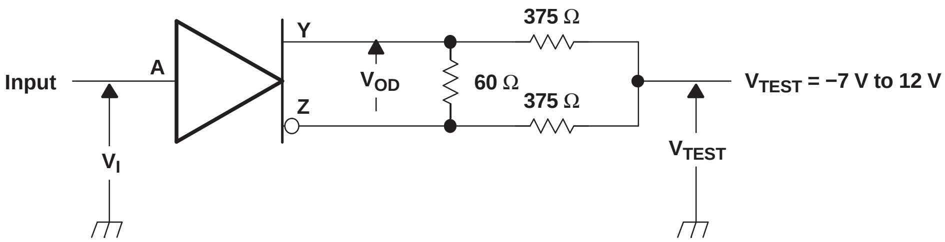
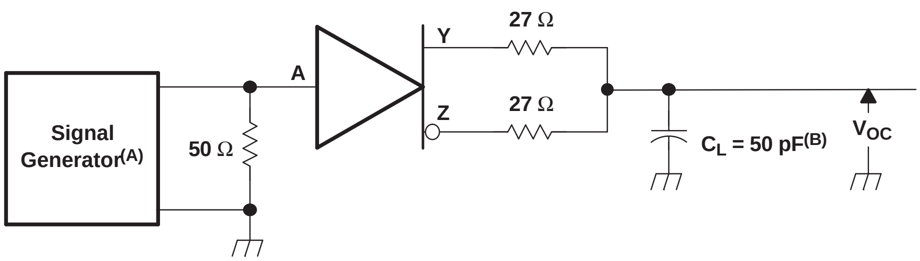


Figure 2. Test Circuit, V_{OD} With Common-Mode Loading

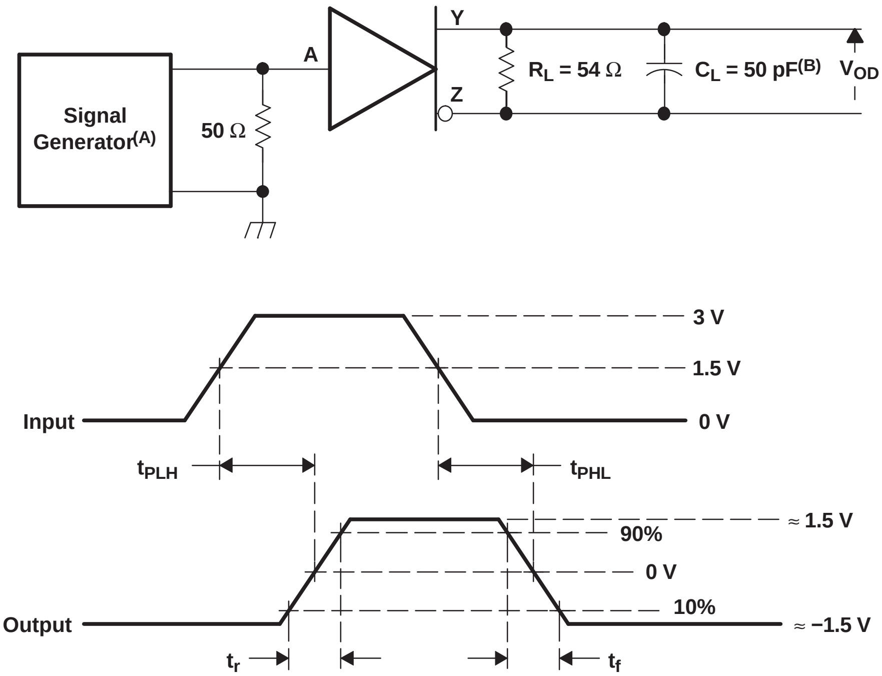


A. PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

B. Includes probe and jig capacitance

Figure 3. V_{OC} Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

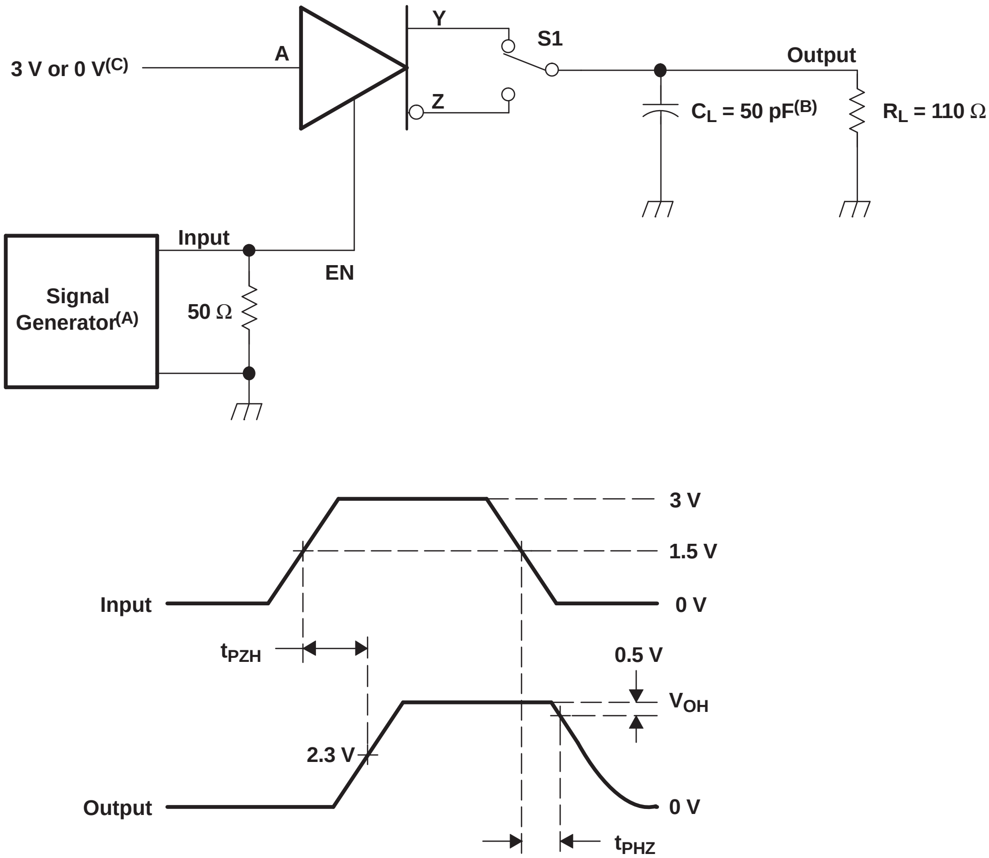


A. PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

B. Includes probe and jig capacitance

Figure 4. Output Switching Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



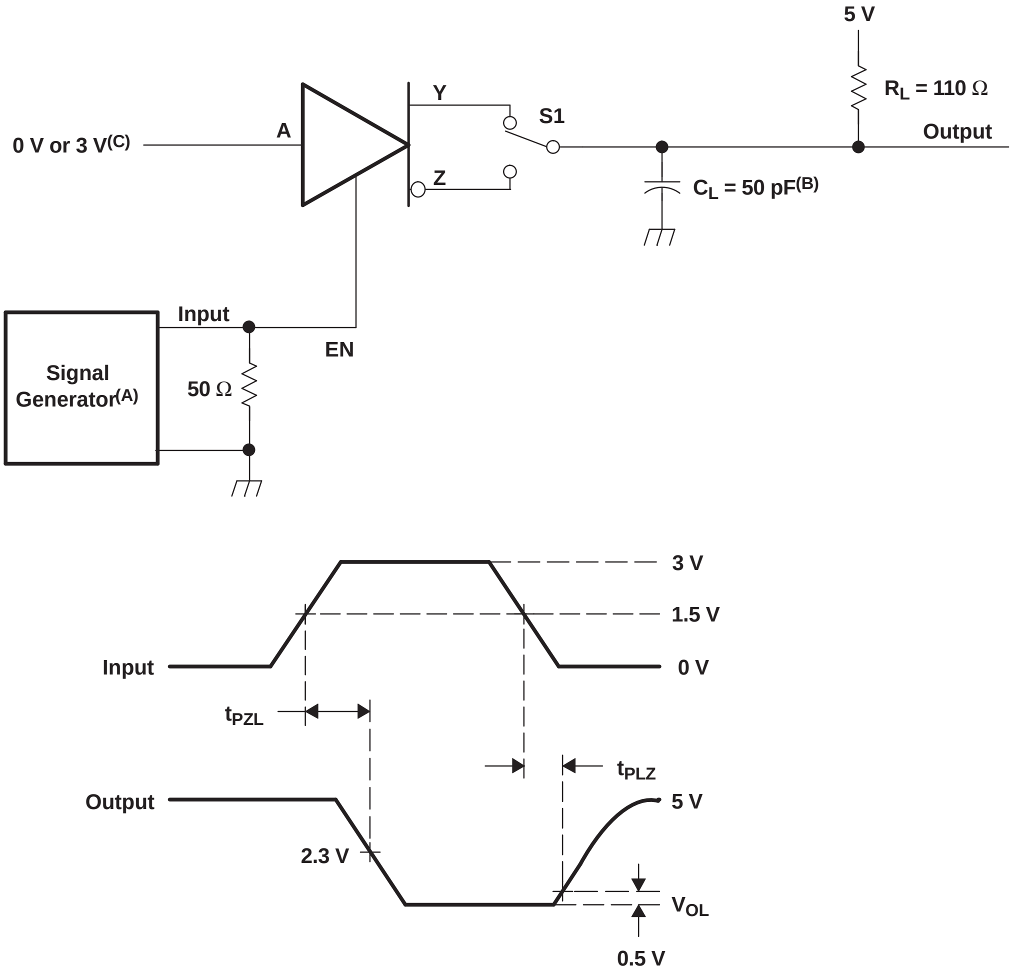
A. PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

B. Includes probe and jig capacitance

C. 3 V if testing Y output, 0 V if testing Z output

Figure 5. Enable Timing Test Circuit and Waveforms, t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION (continued)



A. PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

B. Includes probe and jig capacitance

C. 3 V if testing Y output, 0 V if testing Z output

Figure 6. Enable Timing Test Circuit and Waveforms, t_{PZL} and t_{PLZ}

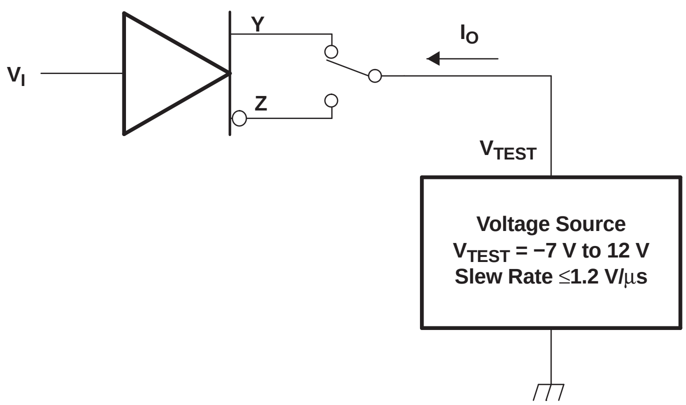


Figure 7. Test Circuit, Short-Circuit Output Current

PARAMETER MEASUREMENT INFORMATION (continued)

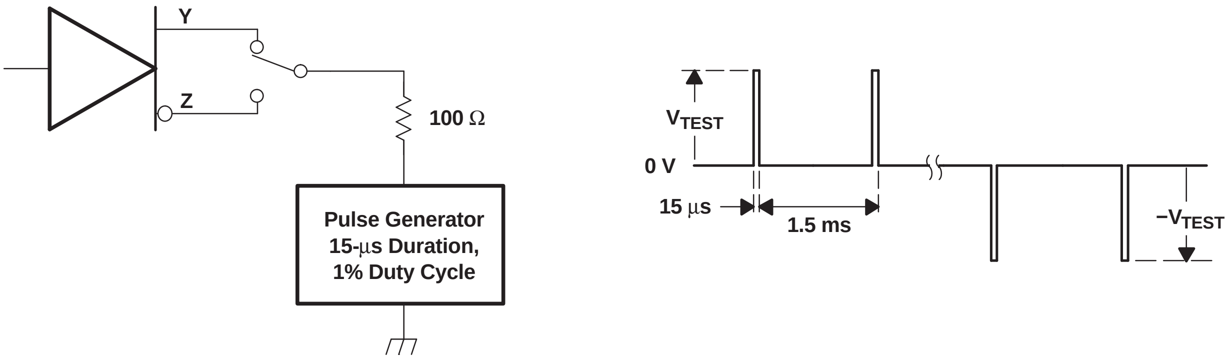


Figure 8. Test Circuit Waveform, Transient Overvoltage Test

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT

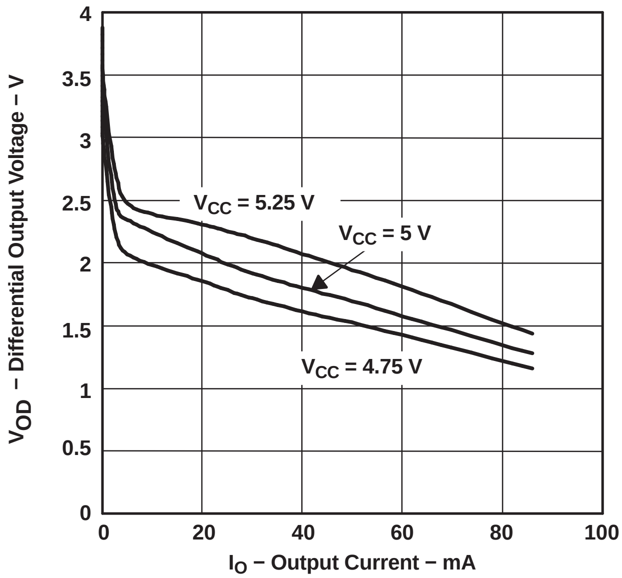


Figure 9.

DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

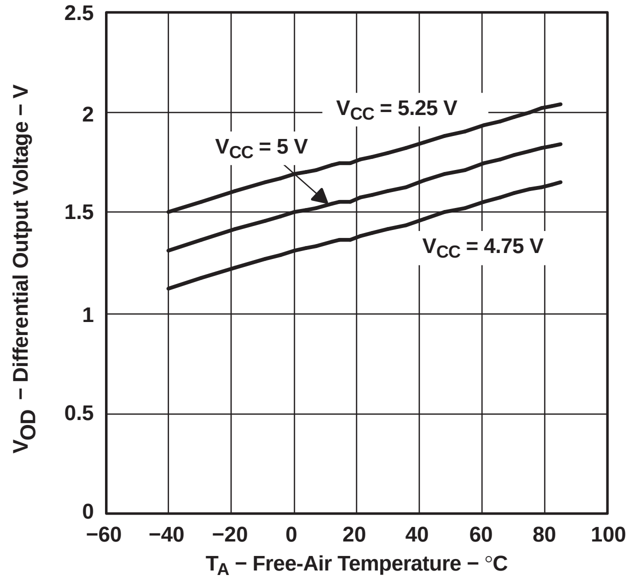


Figure 10.

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

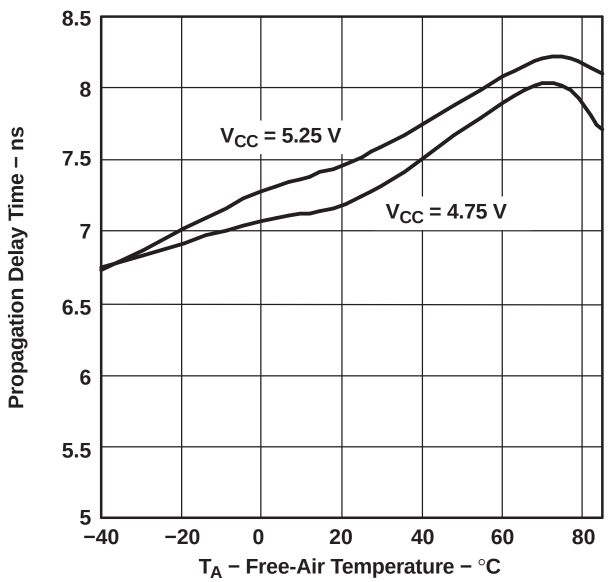


Figure 11.

SUPPLY CURRENT (FOUR CHANNELS) vs SIGNALING RATE

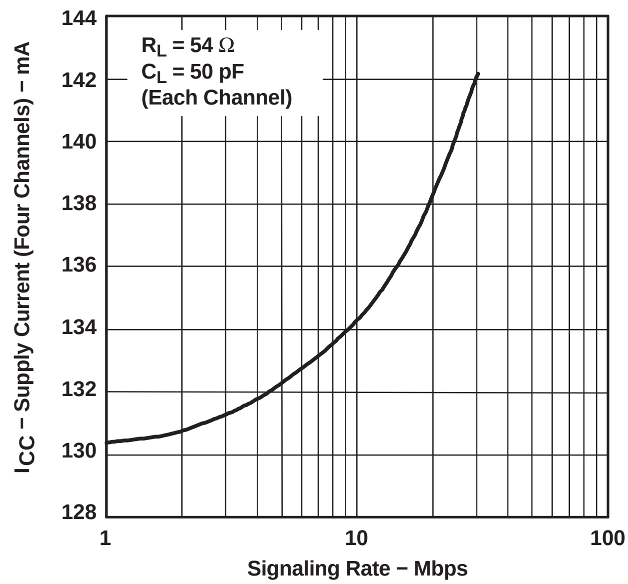


Figure 12.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

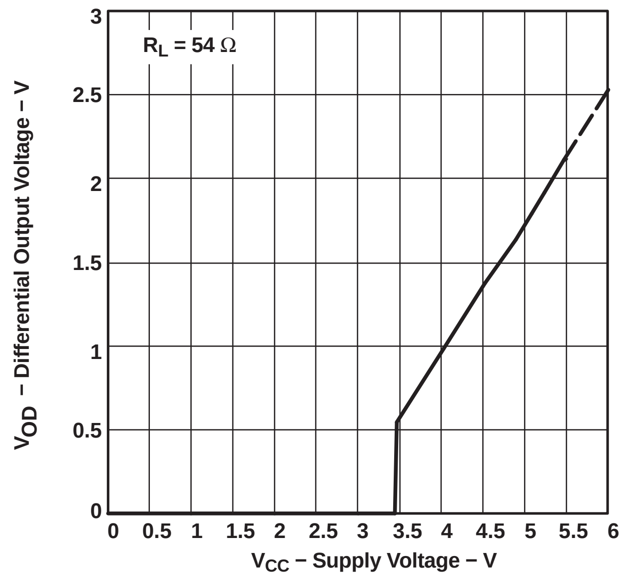


Figure 13.

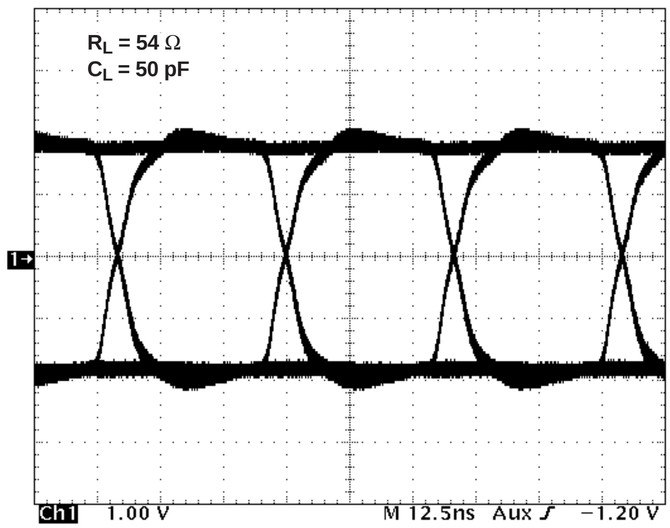


Figure 14. Eye Pattern, Pseudo-Random Data at 30 Mbps

APPLICATION INFORMATION

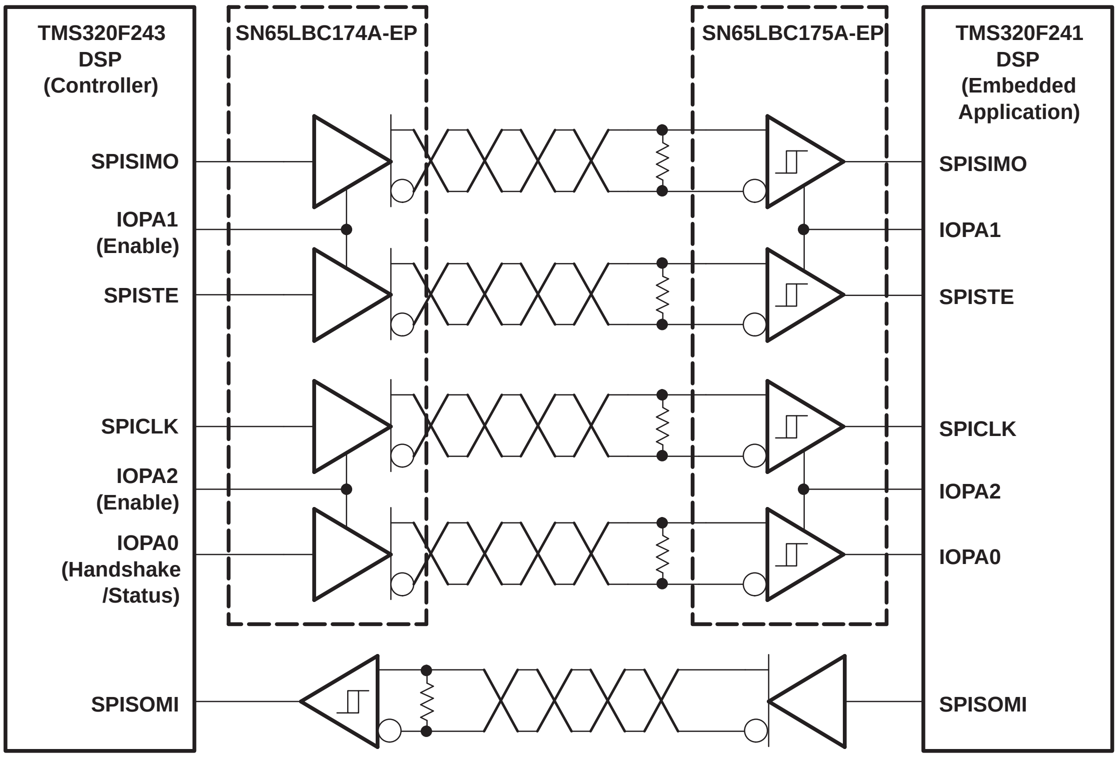


Figure 15. Typical Application Circuit, DSP-to-DSP Link Via Serial Peripheral Interface

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC174AMDWREP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	65LBC174EP	Samples
V62/07611-01XE	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	65LBC174EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN65LBC174A-EP :

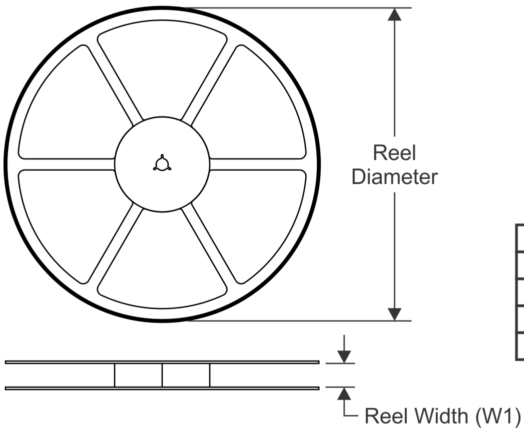
- Catalog: SN65LBC174A

NOTE: Qualified Version Definitions:

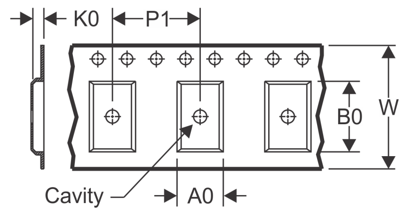
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

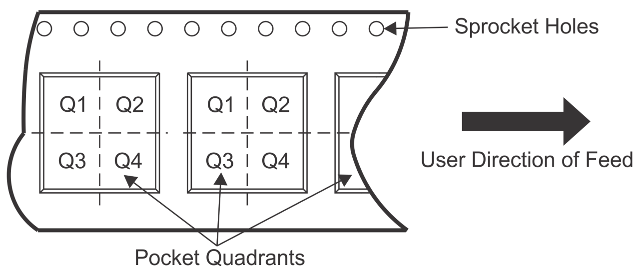


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

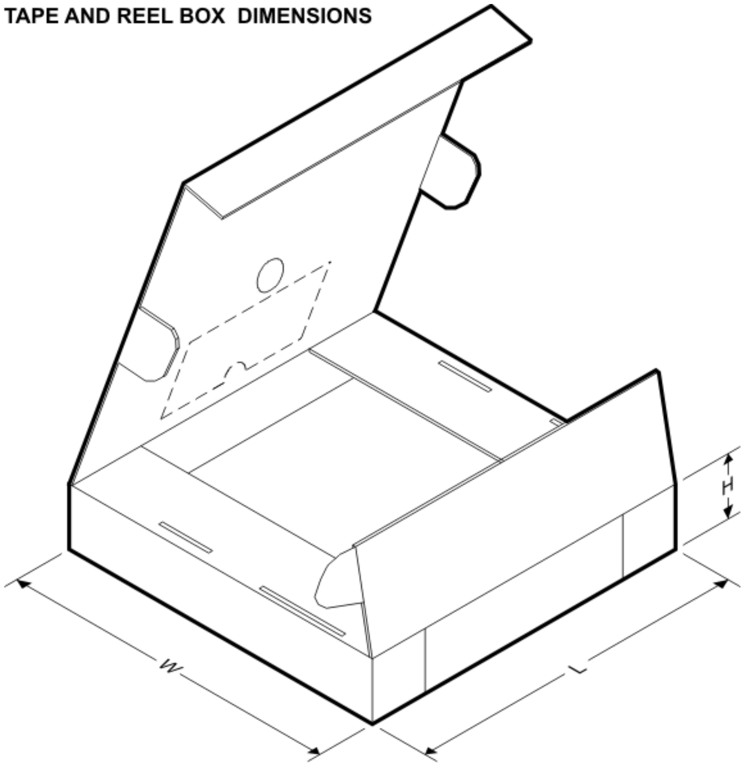
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

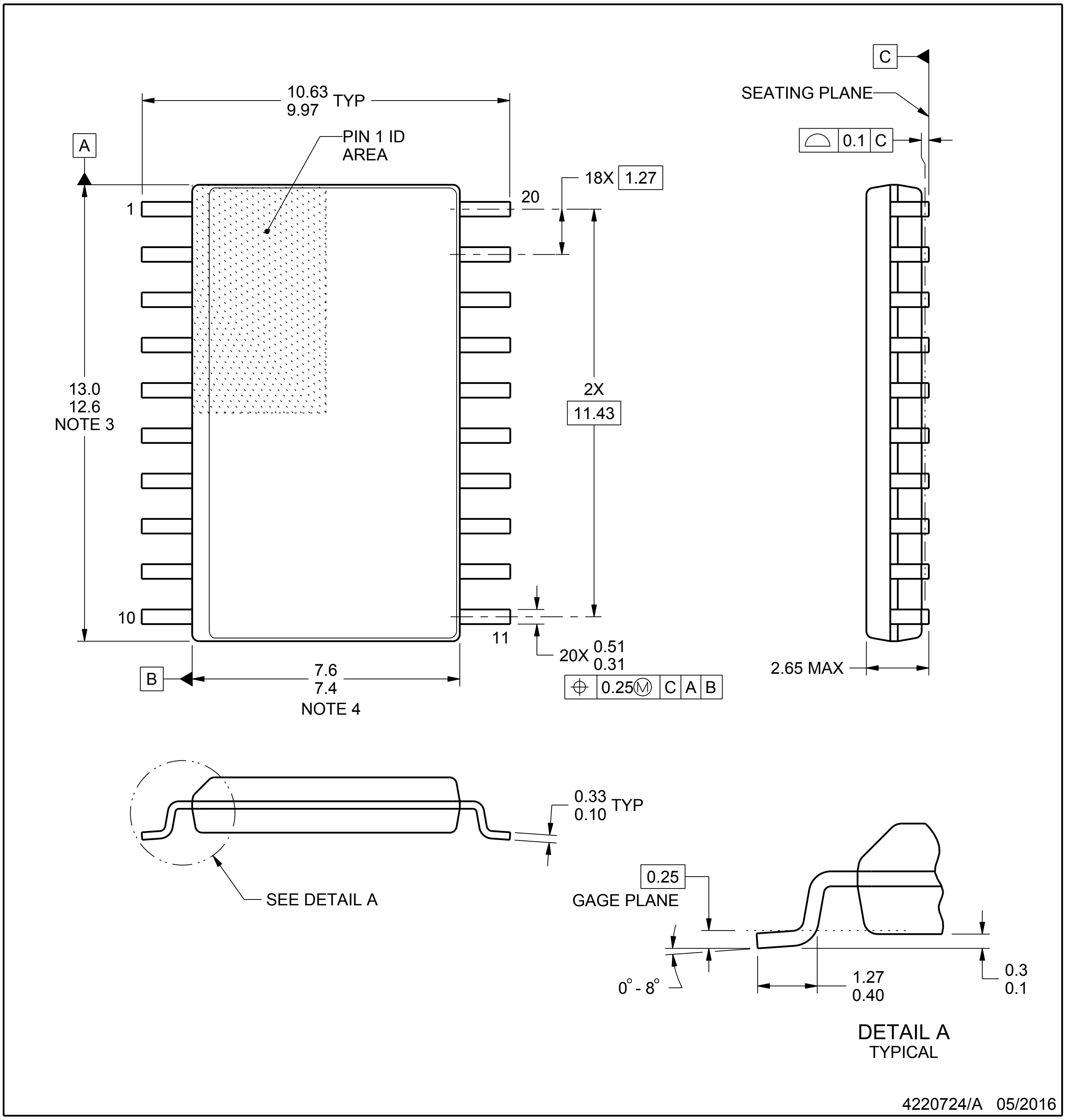
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC174AMDWREP	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



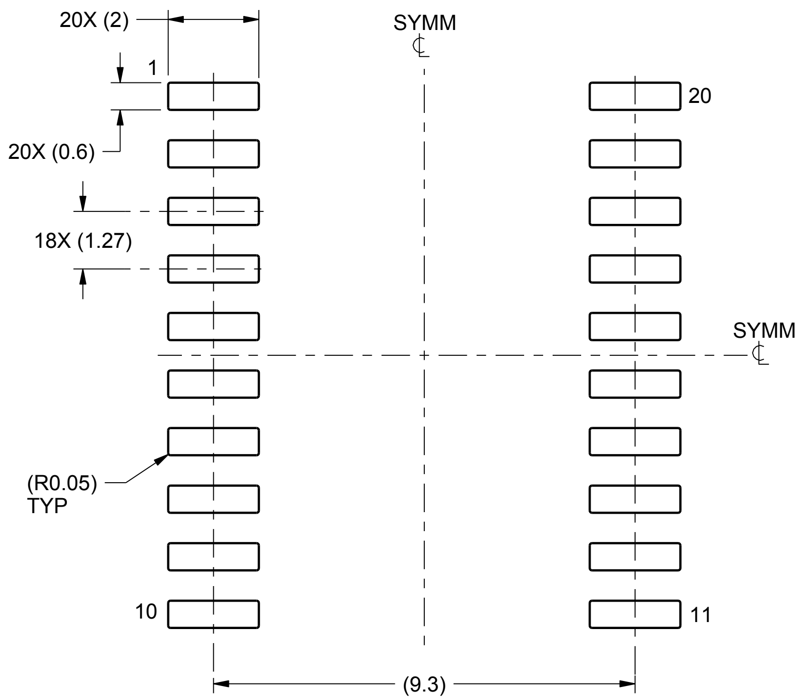
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC174AMDWREP	SOIC	DW	20	2000	367.0	367.0	45.0

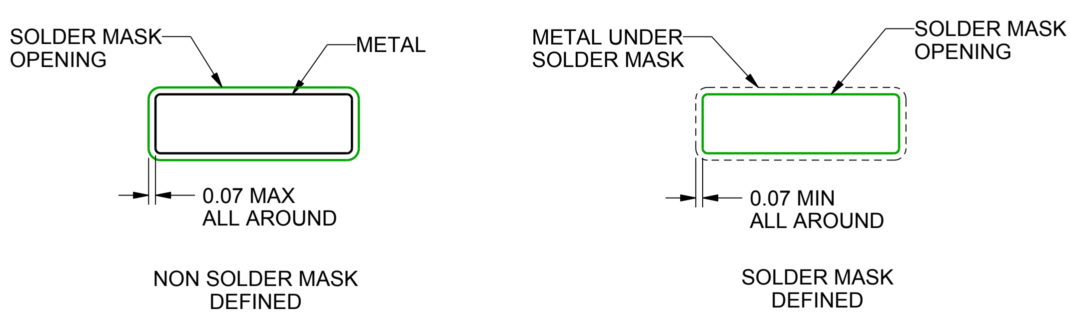


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

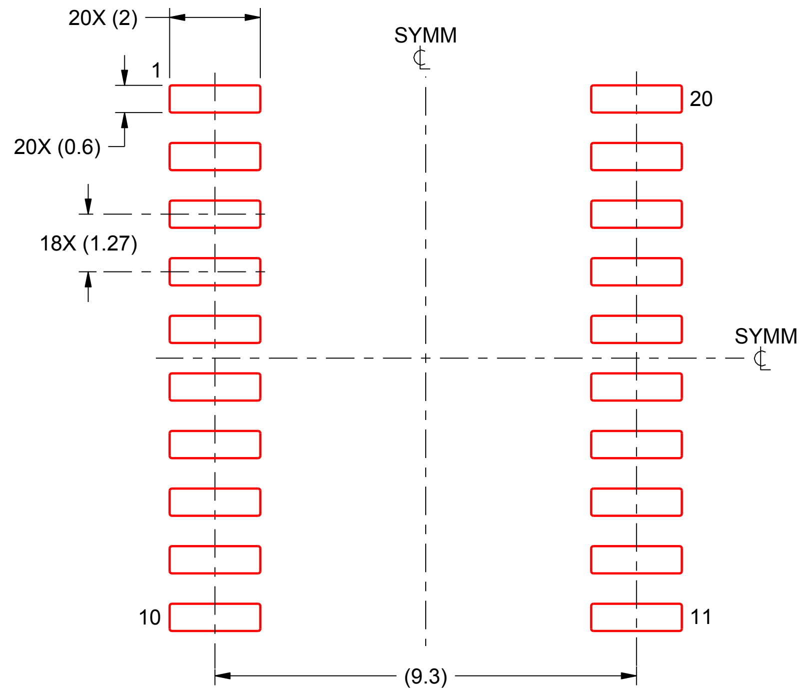


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.