

FEATURES

- Member of the Texas Instruments Widebus+™ Family
- Optimized for 1.8-V Operation and Is 3.6-V I/O **Tolerant to Support Mixed-Mode Signal** Operation
- Ioff Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable

- Max t_{pd} of 2 ns at 1.8 V
- Low Power Consumption, 40-µA Max Icc
- ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 32-bit noninverting bus transceiver is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC32245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as four 8-bit transceivers, two 16-bit transceivers, or one 32-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T _A	PACK	AGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Tape and reel	SN74AUC32245GKER	MM245

Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



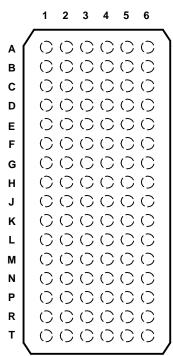
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SN74AUC32245 32-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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GKE PACKAGE (TOP VIEW)



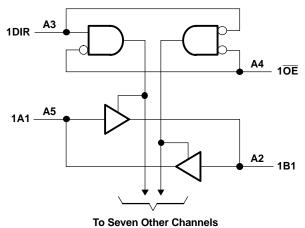
TERMINAL ASSIGNMENTS

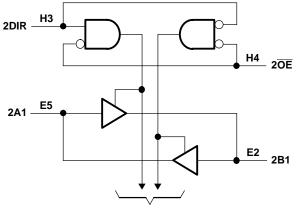
	1	2	3	4	5	6
Α	1B2	1B1	1DIR	1 0E	1A1	1A2
В	1B4	1B3	GND	GND	1A3	1A4
С	1B6	1B5	V _{CC}	V _{CC}	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
Е	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	V _{CC}	V _{CC}	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
н	2B7	2B8	2DIR	2 0E	2A8	2A7
J	3B2	3B1	3DIR	3 0E	3A1	3A2
к	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	V _{CC}	V _{CC}	3A5	3A6
м	3B8	3B7	GND	GND	3A7	3A8
Ν	4B2	4B1	GND	GND	4A1	4A2
Р	4B4	4B3	V _{CC}	V _{CC}	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
т	4B7	4B8	4DIR	4 0E	4A8	4A7

FUNCTION TABLE (EACH 8-BIT SECTION)

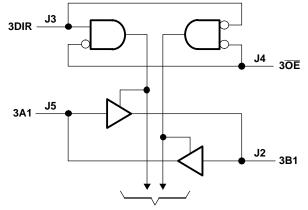
INP	UTS	OPERATION
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
н х		Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)

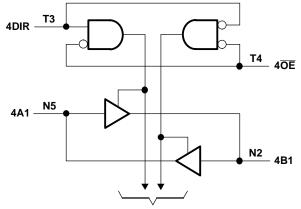




To Seven Other Channels



To Seven Other Channels



To Seven Other Channels

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT		
V_{CC}	Supply voltage range	Supply voltage range						
VI	Input voltage range ⁽²⁾	Input voltage range ⁽²⁾						
Vo	Voltage range applied to a	-off state ⁽²⁾	-0.5	3.6	V			
Vo	Output voltage range ⁽²⁾			-0.5	V _{CC} + 0.5	V		
I _{IK}	Input clamp current	V ₁ < 0			-50	mA		
I _{OK}	Output clamp current	V _O < 0			-50	mA		
I _O	Continuous output current				±20	mA		
	Continuous current through	V _{CC} or GND			±100	mA		
θ_{JA}	Package thermal impedant		40	°C/W				
T _{stg}	Storage temperature range			-65	150	°C		

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	2.7	V
		V _{CC} = 0.8 V	V _{CC}		
VIH	High-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	$0.65 imes V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 0.8 V		0	
V _{IL}	Low-level input voltage	V _{CC} = 1.1 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
VI	Input voltage		0	3.6	V
V	Output veltage	Active state	0	V _{CC}	V
Vo	Output voltage	3-state	0	3.6	v
		V _{CC} = 0.8 V		-0.7	
	High-level output current	V _{CC} = 1.1 V		-3	
I _{OH}		V _{CC} = 1.4 V		-5	mA
		V _{CC} = 1.65 V		-8	
		V _{CC} = 2.3 V		-9	
		V _{CC} = 0.8 V		0.7	
		V _{CC} = 1.1 V		3	
I _{OL}	Low-level output current	V _{CC} = 1.4 V		5	mA
		V _{CC} = 1.65 V		8	
		V _{CC} = 2.3 V		9	
$\Delta t / \Delta v$	Input transition rise or fall rate			5	ns/V
T _A	Operating free-air temperature		-40	85	°C

 All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	ΜΙΝ ΤΥ	'P ⁽¹⁾ MAX	UNIT
	I _{OH} = -100 μA	0.8 V to 2.7 V	V _{CC} - 0.1		
	$I_{OH} = -0.7 \text{ mA}$	0.8 V		0.55	
M	$I_{OH} = -3 \text{ mA}$	1.1 V	0.8		V
V _{OH}	$I_{OH} = -5 \text{ mA}$	1.4 V	1		v
	$I_{OH} = -8 \text{ mA}$	1.65 V	1.2		
	$I_{OH} = -9 \text{ mA}$	2.3 V	1.8		
	I _{OL} = 100 μA	0.8 V to 2.7 V		0.2	
	I _{OL} = 0.7 mA	0.8 V		0.25	
M	I _{OL} = 3 mA	1.1 V		0.3	V
V _{OL}	I _{OL} = 5 mA	1.4 V		0.4	v
	I _{OL} = 8 mA	1.65 V		0.45	
	I _{OL} = 9 mA	2.3 V		0.6	
I _I All inputs	$V_1 = V_{CC}$ or GND	0 to 2.7 V		±5	μΑ
l _{off}	$V_1 \text{ or } V_0 = 2.7 \text{ V}$	0		±10	μΑ
I _{OZ} ⁽²⁾	$V_{O} = V_{CC}$ or GND	2.7 V		±10	μΑ
I _{CC}	$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	0.8 V to 2.7 V		40	μΑ
C _i	$V_1 = V_{CC}$ or GND	2.5 V		pF	
C _{io}	$V_0 = V_{CC}$ or GND	2.5 V		7	pF

(1) (2)

All typical values are at $T_A = 25^{\circ}C$. For I/O ports, the parameter I_{OZ} includes the input leakage current.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = ± 0.		V _{CC} = ± 0.			_c = 1.8 0.15 V		V _{CC} = ± 0.		UNIT
	(INFOT)	(001F01)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	B or A	5.6	0.5	3.1	0.5	2	0.5	1.5	2	0.4	1.9	ns
t _{en}	OE	A or B	10	0.7	4.6	0.7	3.1	0.7	2.1	3.1	0.7	2.6	ns
t _{dis}	OE	A or B	12.8	0.8	6.8	0.8	5	0.8	3.4	4.8	0.5	2.9	ns

Operating Characteristics

 $T_A = 25^{\circ}C$

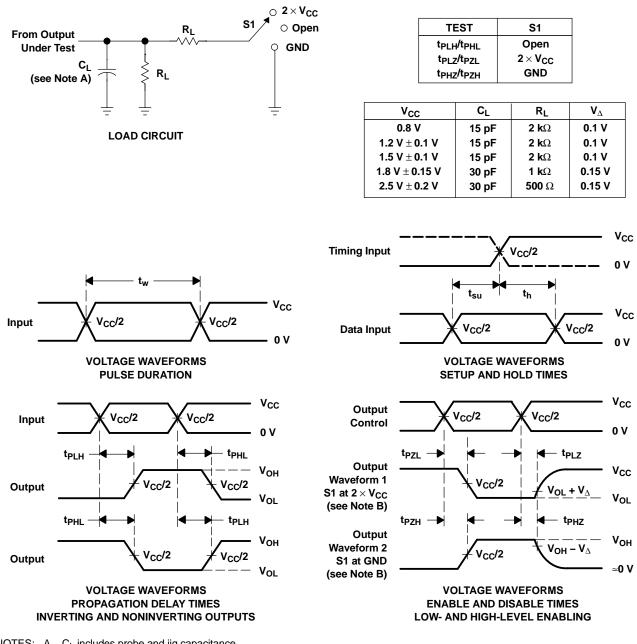
	PARAMETER		TEST CONDITIONS	V _{CC} = 0.8 V TYP	V _{CC} = 1.2 V TYP	V _{CC} = 1.5 V TYP	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	UNIT
C	Power	Outputs enabled	f = 10 MHz	22	23	24	25	29	pF
C _{pd} dissipation capacitance	capacitance	Outputs disabled		1	1	1	1	1	μr

SN74AUC32245 **32-BIT BUS TRANSCEIVER** WITH 3-STATE OUTPUTS

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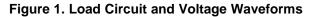


PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , slew rate \geq 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.





2-Oct-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
SN74AUC32245ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	MM245	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

2-Oct-2014

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC32245ZKER	LFBGA	ZKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

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PACKAGE MATERIALS INFORMATION

18-Aug-2014



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC32245ZKER	LFBGA	ZKE	96	1000	336.6	336.6	41.3

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Falls within JEDEC MO-205 variation CC.

D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).



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