SN74AUP1G34 Low-Power Single Buffer Gate

1 Features

- Available in the Ultra Small 0.64 mm^2 Package (DPW) with 0.5-mm Pitch
- Low Static-Power Consumption; I_{CC} = 0.9 μA Max
- Low Dynamic-Power Consumption; C_{pd} = 4.1 pF Typ at 3.3 V
- Low Input Capacitance; C_i = 1.5 pF Typ
- Low Noise - Overshoot and Undershoot < 10% of V_{CC}
- I_{off} Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input (V_{hys} = 250 mV Typ at 3.3 V)
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- t_{pd} = 4.1 ns Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- ATCA Solutions
- Active Noise Cancellation (ANC)
- Barcode Scanner
- Blood Pressure Monitor
- CPAP Machine
- Cable Solutions
- DLP 3D Machine Vision, Hyperspectral Imaging, Optical Networking, and Spectroscopy
- E-Book
- Embedded PC
- Field Transmitter: Temperature or Pressure Sensor
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radio (SDR)
- TV: High-Definition (HDTV), LCD, and Digital
- Video Communications System
- Wireless Data Access Card, Headset, Keyboard, Mouse, and LAN Card
- X-ray: Baggage Scanner, Medical, and Dental

3 Description

This single buffer gate performs the Boolean function Y = A in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1G34	SOT (5)	1.60 mm × 1.20 mm
	USON (6)	1.45 mm × 1.00 mm
	X2SON (4)	0.80 mm × 0.80 mm
	DSBGA (4)	0.79 mm × 0.79 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplifed Schematic

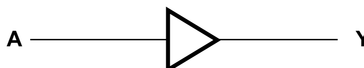

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Table of Contents

1 **Features** ... 1
2 **Applications** ... 1
3 **Description** ... 1
4 **Simplifed Schematic** ... 1
5 **Revision History** ... 2
6 **Pin Configuration and Function** ... 3
7 **Specifications** ... 3
  7.1 Absolute Maximum Ratings ... 3
  7.2 Handling Ratings ... 4
  7.3 Recommended Operating Conditions ... 4
  7.4 Thermal Information ... 4
  7.5 Electrical Characteristics ... 5
  7.6 Switching Characteristics, C_L = 5 pF ... 5
  7.7 Switching Characteristics, C_L = 10 pF ... 6
  7.8 Switching Characteristics, C_L = 15 pF ... 6
  7.9 Switching Characteristics, C_L = 30 pF ... 6
  7.10 Operating Characteristics ... 6
  7.11 Typical Characteristics ... 7
8 **Parameter Measurement Information** ... 8
  8.1 Propagation Delays, Setup and Hold Times, and Pulse Width ... 8
  8.2 Enable and Disable Times ... 9
9 **Detailed Description** ... 10
  9.1 Overview ... 10
  9.2 Functional Block Diagram ... 10
  9.3 Feature Description ... 10
  9.4 Device Functional Modes ... 10
10 **Application and Implementation** ... 11
  10.1 Application Information ... 11
  10.2 Typical Application ... 11
11 **Power Supply Recommendations** ... 12
12 **Layout** ... 12
  12.1 Layout Guidelines ... 12
  12.2 Layout Example ... 12
13 **Device and Documentation Support** ... 13
  13.1 Trademarks ... 13
  13.2 Electrostatic Discharge Caution ... 13
  13.3 Glossary ... 13
14 **Mechanical, Packaging, and Orderable Information** ... 13

5 Revision History

Changes from Revision J (June 2014) to Revision K — **Page**

- Updated Device Information table. ... 1

Changes from Revision I (November 2012) to Revision J — **Page**

- Updated document to new TI data sheet format. ... 1
- Deleted Ordering Information table. ... 1
- Updated Description. ... 1
- Added Device Information table. ... 1
- Added Handling Ratings table. ... 4
- Added Thermal Information table. ... 4
- Added Typical Characteristics. ... 7

Changes from Revision H (October 2012) to Revision I — **Page**

- Changed DPW package pinout ... 3

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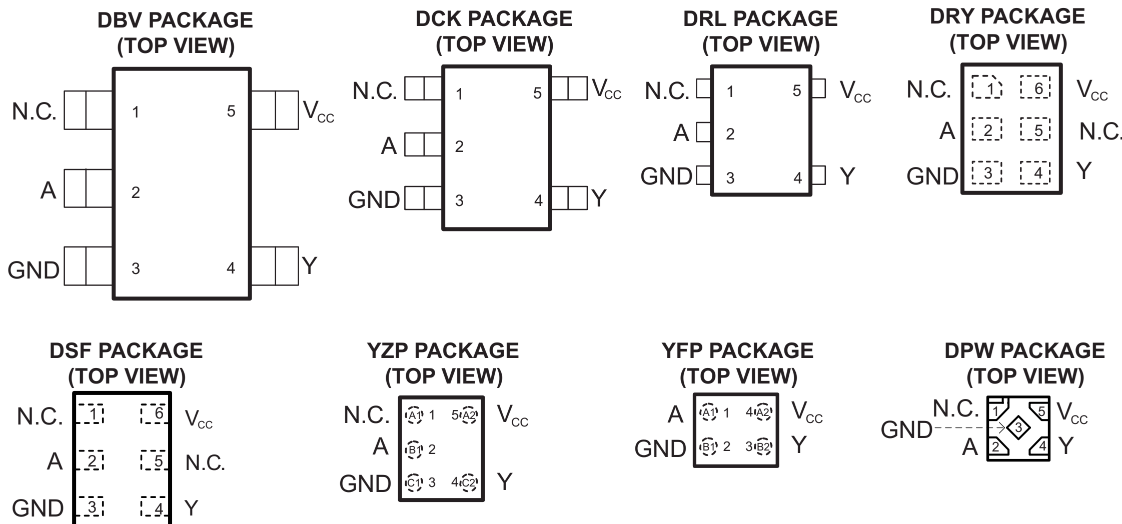
6 Pin Configuration and Function



N.C. – No internal connection

See mechanical drawings for dimensions.

Pin Functions

PIN						I/O	DESCRIPTION
NAME	DBV, DCK, DRL	DSF, DRY	YFP	DPW	YFP		
NC	1	1, 5	–	1		–	No connect
A	2	2	A1	2	A1	I	Input A
GNY	3	3	B1	3	B1	–	Ground
Y	4	4	B2	4	B2	O	Output Y
V_{CC}	5	6	A2	5	A2	–	Power Pin

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
V_O	Output voltage range in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH} [2]	High-level output current	V_{CC} = 0.8 V		–20	μA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65 V		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		-4	
I_{OL} [2]	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs,* literature number SCBA004.
(2) Defined by the signal integrity requirements and design goal priorities

7.4 Thermal Information

THERMAL METRIC[1]		DBV	DCK	DRL	DSF	DRY	UNIT
		5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	271.4	338.4	349.7	407.1	554.9	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	213.5	110.6	120.5	232.0	385.4	
$R_{θJB}$	Junction-to-board thermal resistance	108.2	118.8	171.4	306.9	388.2	
$ψ_{JT}$	Junction-to-top characterization parameter	89.3	3.0	10.8	40.3	159.0	
$ψ_{JB}$	Junction-to-board characterization parameter	107.6	117.8	169.4	306.0	384.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –20 µA		0.8 V to 3.6 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_{OH} = –1.1 mA		1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
		I_{OH} = –1.7 mA		1.4 V	1.11			1.03		
		I_{OH} = –1.9 mA		1.65 V	1.32			1.3		
		I_{OH} = –2.3 mA		2.3 V	2.05			1.97		
		I_{OH} = –3.1 mA			1.9			1.85		
		I_{OH} = –2.7 mA		3 V	2.72			2.67		
		I_{OH} = –4 mA			2.6			2.55		
V_{OL}		I_{OL} = 20 µA		0.8 V to 3.6 V			0.1		0.1	V
		I_{OL} = 1.1 mA		1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
		I_{OL} = 1.7 mA		1.4 V			0.31		0.37	
		I_{OL} = 1.9 mA		1.65 V			0.31		0.35	
		I_{OL} = 2.3 mA		2.3 V			0.31		0.33	
		I_{OL} = 3.1 mA					0.44		0.45	
		I_{OL} = 2.7 mA		3 V			0.31		0.33	
		I_{OL} = 4 mA					0.44		0.45	
I_I	A input	V_I = GND to 3.6 V		0 V to 3.6 V			0.1		0.5	µA
I_{off}		V_I or V_O = 0 V to 3.6 V		0 V			0.2		0.6	µA
ΔI_{off}		V_I or V_O = 0 V to 3.6 V		0 V to 0.2 V			0.2		0.6	µA
I_{CC}		V_I = GND or (V_{CC} to 3.6 V)	I_O = 0	0.8 V to 3.6 V			0.5		0.9	µA
ΔI_{CC}		V_I = V_{CC} – 0.6 V	I_O = 0	3.3 V			40		50	µA
C_i		V_I = V_{CC} or GND		0 V		1.5				pF
				3.6 V		1.5				
C_o		V_O = GND		0 V		2.5				pF

7.6 Switching Characteristics, C_L = 5 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V	1.8	14.5	27.4			ns
			1.2 V ± 0.1 V	3	5.6	11.2	0.4	13.9	
			1.5 V ± 0.1 V	2.5	4	7.2	0.7	9.2	
			1.8 V ± 0.15 V	2.2	3.2	6	0.8	7.3	
			2.5 V ± 0.2 V	1.8	2.4	3.9	0.6	5.1	
			3.3 V ± 0.3 V	1.4	2	3.2	0.6	4.1	

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7.7 Switching Characteristics, C_L = 10 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3 and Figure 4

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V	2.7	16.6	28.2			ns
			1.2 V ± 0.1 V	3.6	6.6	12.7	0.3	15.4	
			1.5 V ± 0.1 V	3	4.8	8.3	1.2	10.3	
			1.8 V ± 0.15 V	2.7	3.9	6.9	1.3	8.3	
			2.5 V ± 0.2 V	2.3	2.9	4.5	1.2	5.8	
			3.3 V ± 0.3 V	2	2.4	3.8	1.1	4.8	

7.8 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3 and Figure 4

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V	5.1	18.6	30.2			ns
			1.2 V ± 0.1 V	4.3	7.5	13.6	1.3	16.5	
			1.5 V ± 0.1 V	3.6	5.5	9	1.9	11.2	
			1.8 V ± 0.15 V	3.2	4.5	7.5	1.9	8.9	
			2.5 V ± 0.2 V	2.6	3.4	5.2	1.7	6.5	
			3.3 V ± 0.3 V	2.3	2.9	4.2	1.5	5	

7.9 Switching Characteristics, C_L = 30 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3 and Figure 4

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V	9.9	24.2	36.3			ns
			1.2 V ± 0.1 V	6.3	10.1	16.3	3.6	18.9	
			1.5 V ± 0.1 V	5.1	7.4	11	3.4	13	
			1.8 V ± 0.15 V	4.5	6.1	9.3	3.2	10.6	
			2.5 V ± 0.2 V	3.7	4.7	6.4	2.7	7.8	
			3.3 V ± 0.3 V	3.3	4	5.3	2.5	6.5	

7.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	3.8	pF
			1.2 V ± 0.1 V	3.8	
			1.5 V ± 0.1 V	3.8	
			1.8 V ± 0.15 V	3.8	
			2.5 V ± 0.2 V	3.9	
			3.3 V ± 0.3 V	4.1	

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7.11 Typical Characteristics

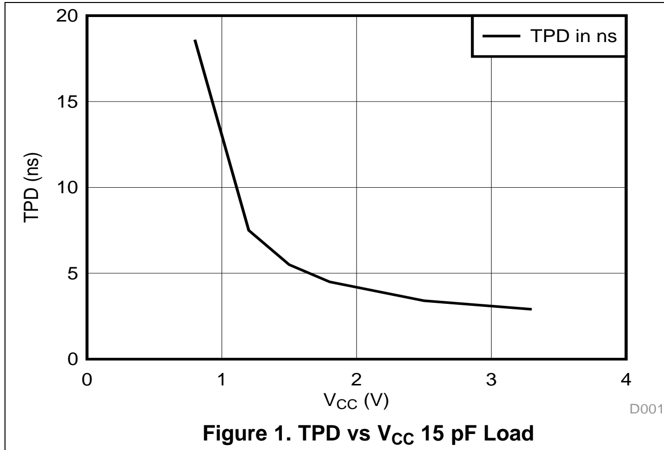

Figure 1. TPD vs V_{CC} 15 pF Load

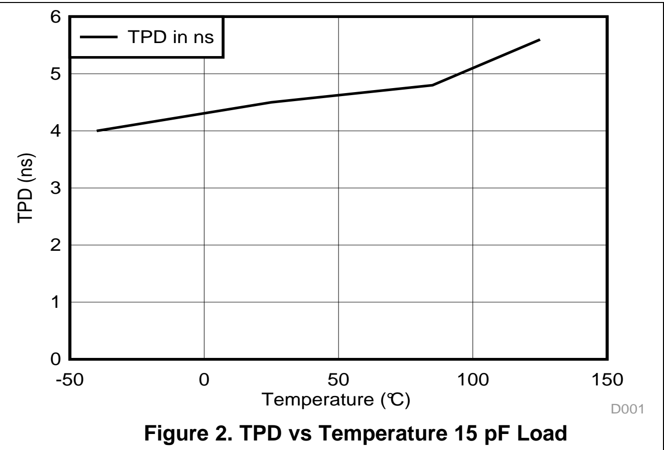

Figure 2. TPD vs Temperature 15 pF Load

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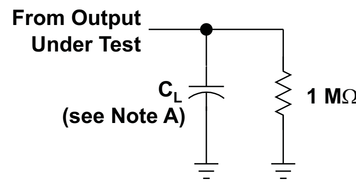
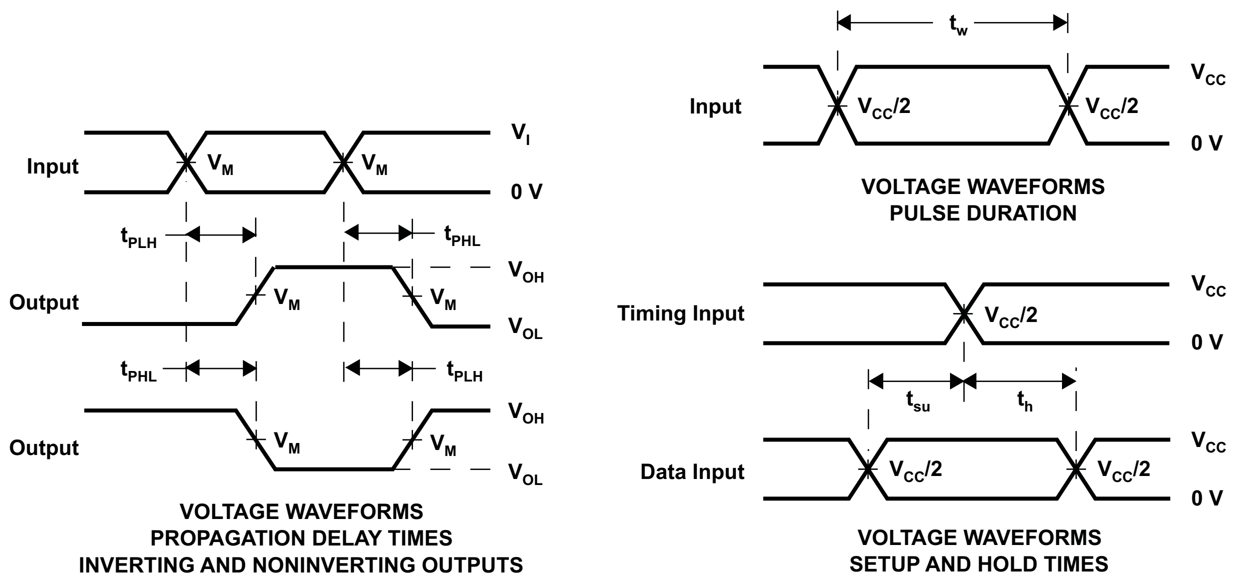
8 Parameter Measurement Information

8.1 Propagation Delays, Setup and Hold Times, and Pulse Width



LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



NOTES:
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 Mhz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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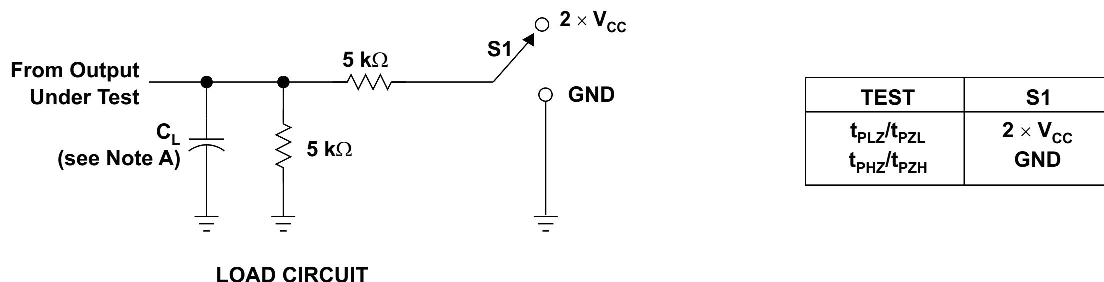
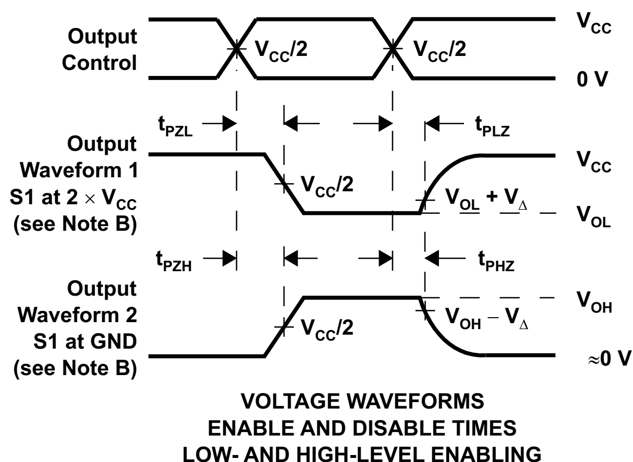
8.2 Enable and Disable Times



TEST	S1
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



NOTES:
- A. CL includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

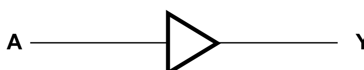
9 Detailed Description

9.1 Overview

This single buffer gate operates from 0.8 V to 3.6 V and performs the Boolean function Y = A in positive logic. The AUP family of devices has quiescent power consumption less than 1 µA and comes in the ultra small DPW package. The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current back-flow through the device when it is powered. The I_{off} feature also allows for live insertion.

9.2 Functional Block Diagram



9.3 Feature Description

- Wide operating V_{CC} range of 0.8 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- Input hysteresis allows slow input transition and better switching noise immunity at the input
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V
- Low noise due to slower edge rates

9.4 Device Functional Modes

Table 1. Function Table

INPUT A	OUTPUT Y
H	H
L	L

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10 Application and Implementation

10.1 Application Information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

The AUP family of single gate logic makes excellent translators for the new lower voltage Micro- processors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the new uC power levels.

10.2 Typical Application

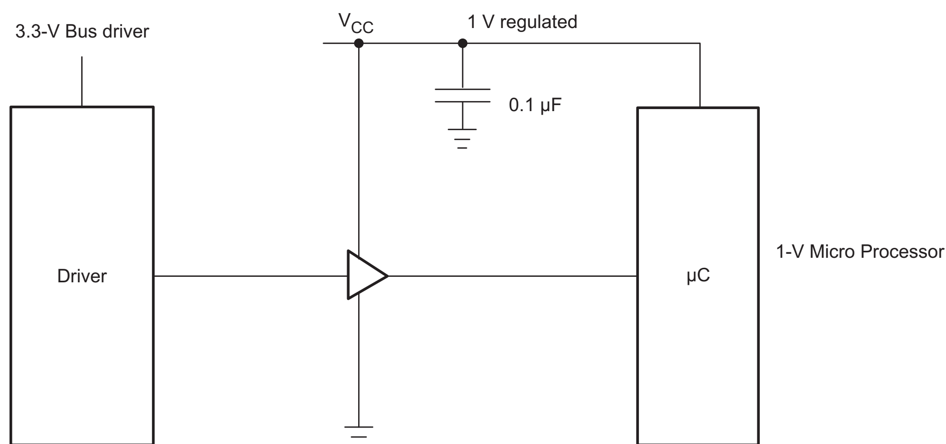

Figure 5. Typical Application

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

10.2.2 Detailed Design Procedure

1. Recommended Input conditions
   - Rise time and fall time specifications. See (Δt/ΔV) in *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid V_{CC}
2. Recommend output conditions
   - Load currents should not exceed 20 mA on the output and 50 mA total for the part
   - Outputs should not be pulled above V_{CC}

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Typical Application (continued)

10.2.3 Application Curves

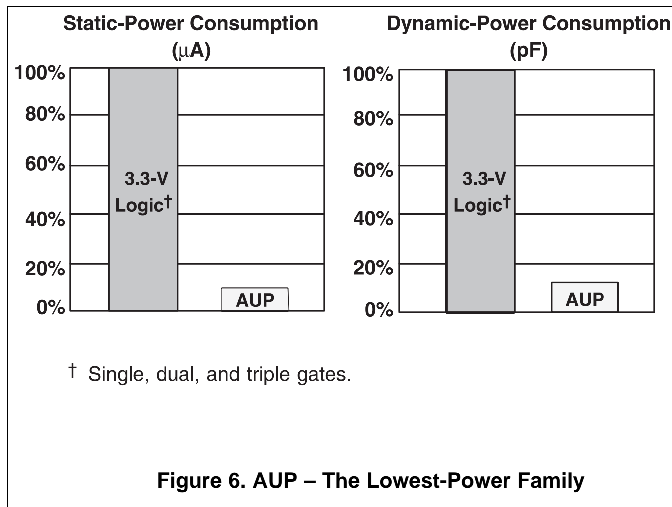


Figure 6. AUP – The Lowest-Power Family

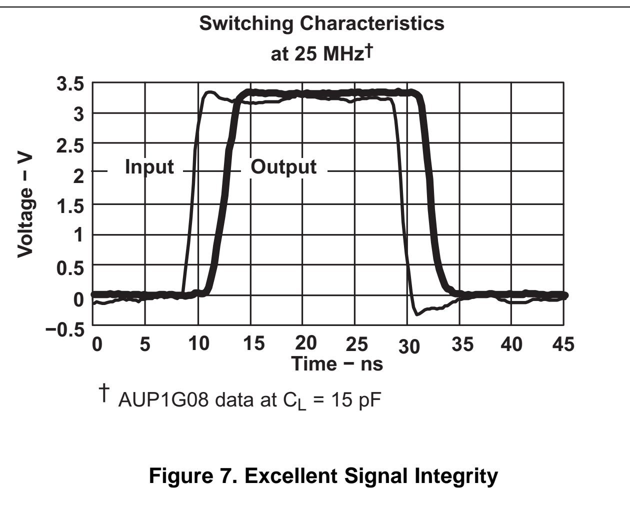


Figure 7. Excellent Signal Integrity

11 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended and if there are multiple V_{CC} terminals then .01 μF or .022 μF is recommended for each power terminal. It is ok to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

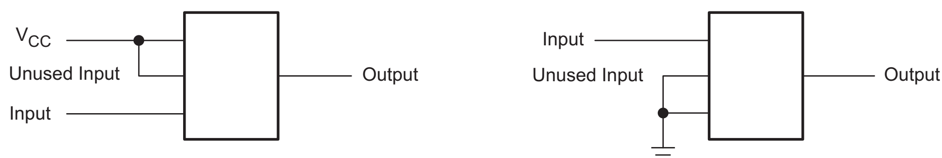
12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally OK to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

12.2 Layout Example



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13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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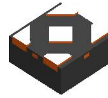
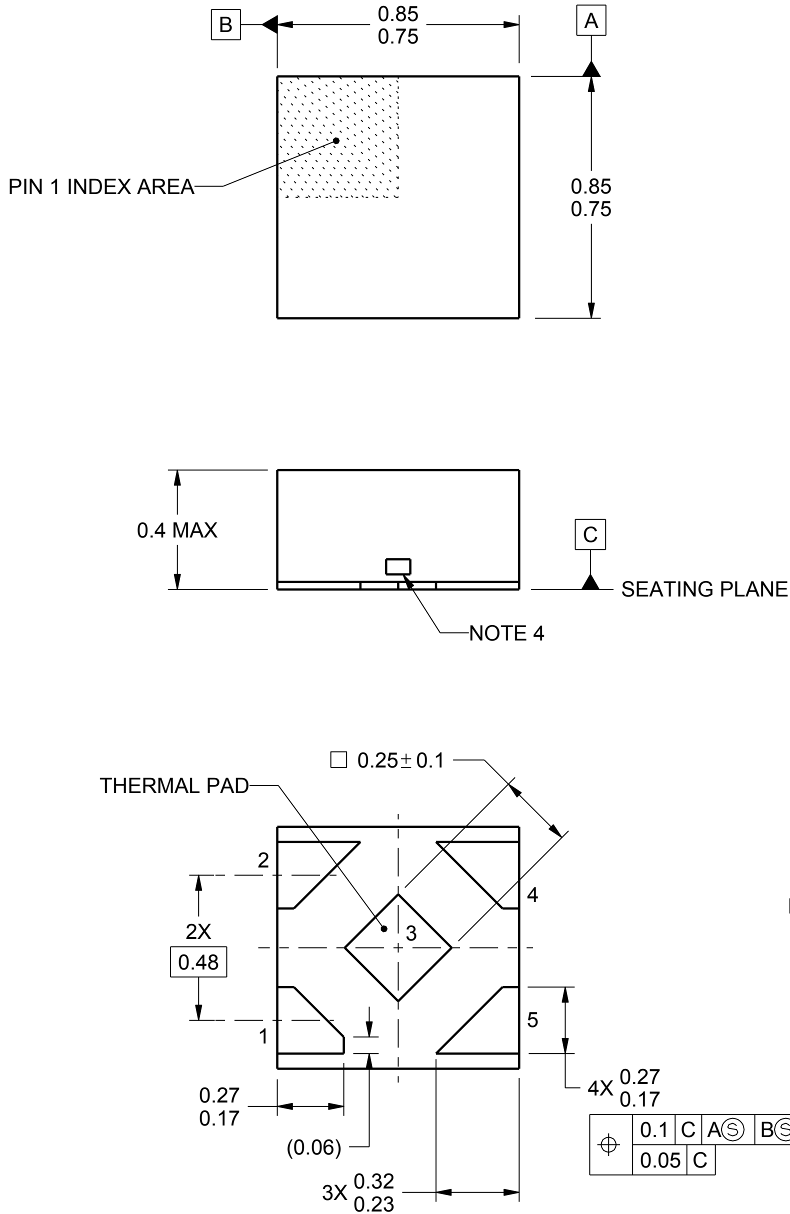


PACKAGE OUTLINE

X2SON - 0.4 mm max height

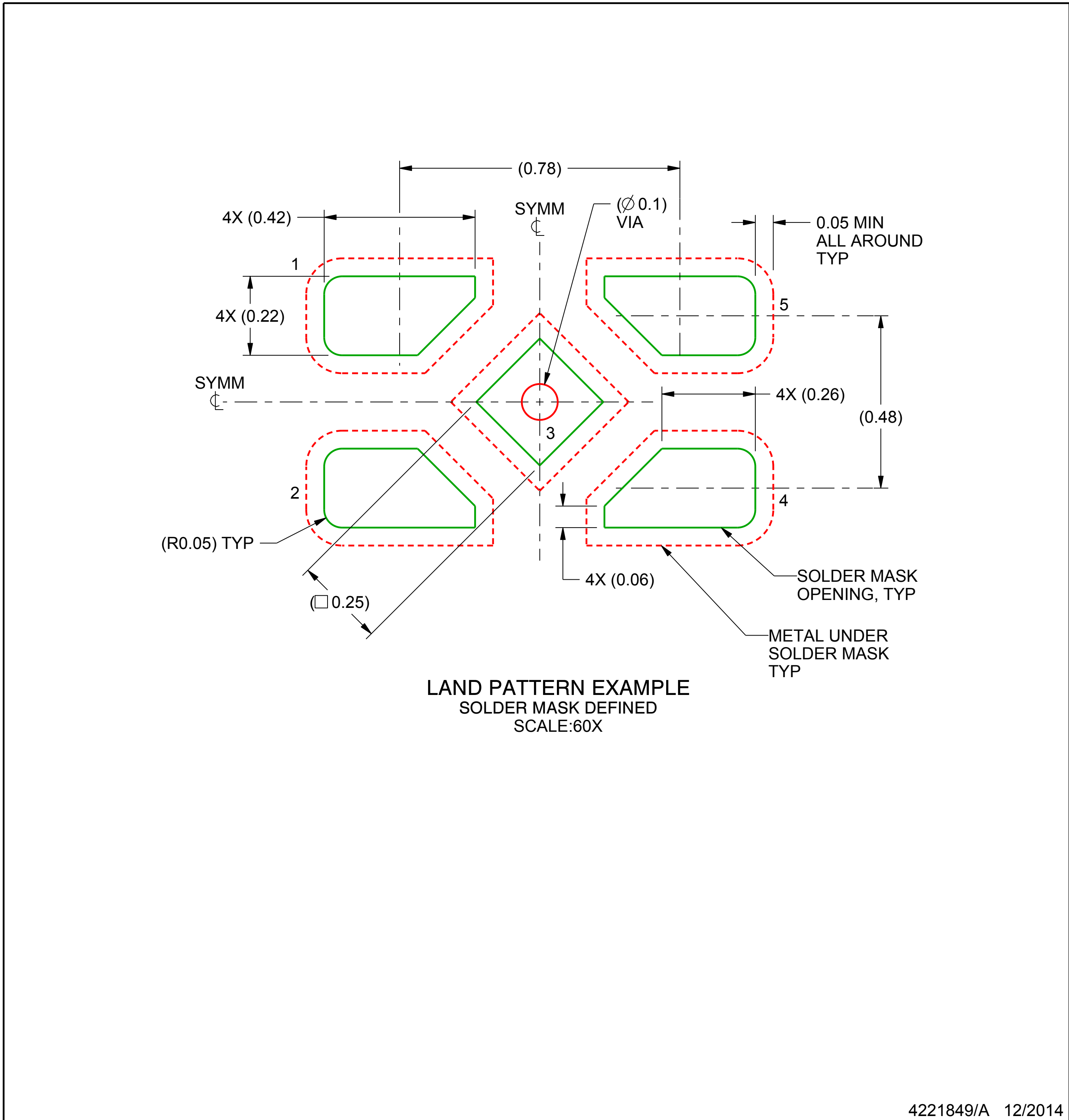
PLASTIC SMALL OUTLINE - NO LEAD



4221849/A 12/2014

NOTES:

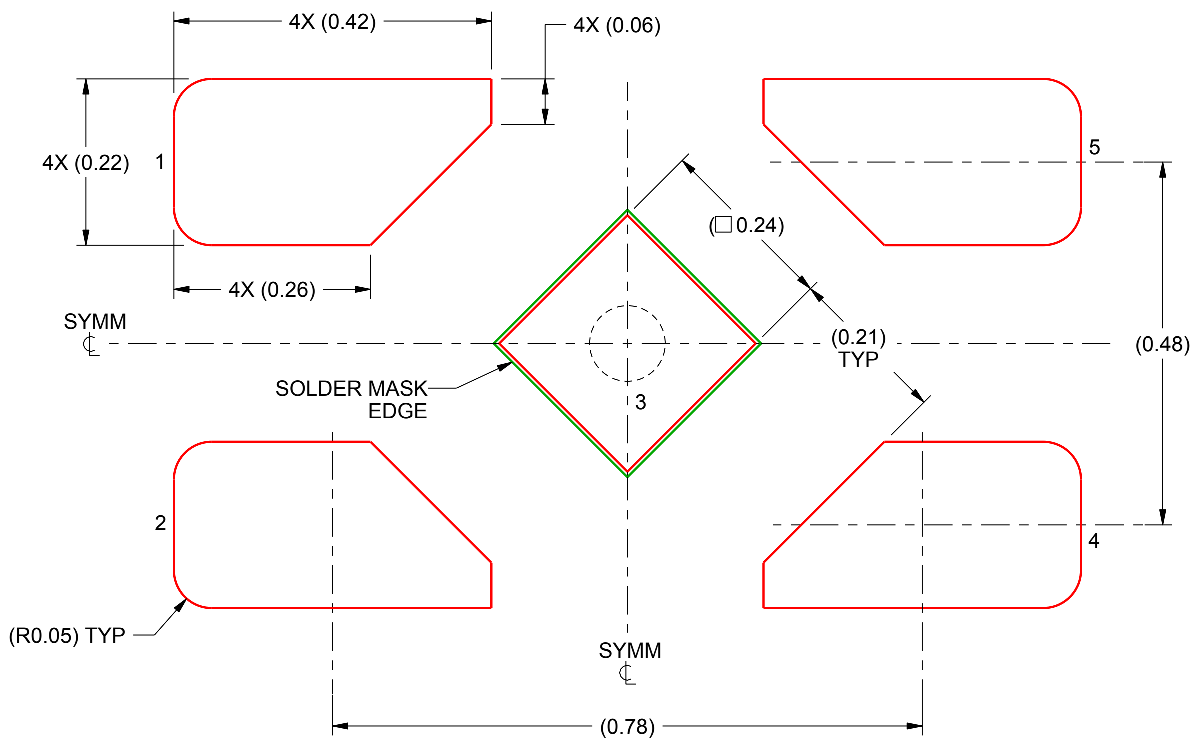
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

4221849/A 12/2014

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G34DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H34R	Samples
SN74AUP1G34DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H34R	Samples
SN74AUP1G34DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H95 ~ H9F ~ H9K ~ H9R)	Samples
SN74AUP1G34DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H95 ~ H9R)	Samples
SN74AUP1G34DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H95 ~ H9R)	Samples
SN74AUP1G34DPWR	ACTIVE	X2SON	DPW	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	G4	Samples
SN74AUP1G34DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H97 ~ H9R)	Samples
SN74AUP1G34DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H9	Samples
SN74AUP1G34DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM		H9	Samples
SN74AUP1G34YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		H9 N	Samples
SN74AUP1G34YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	H9N	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

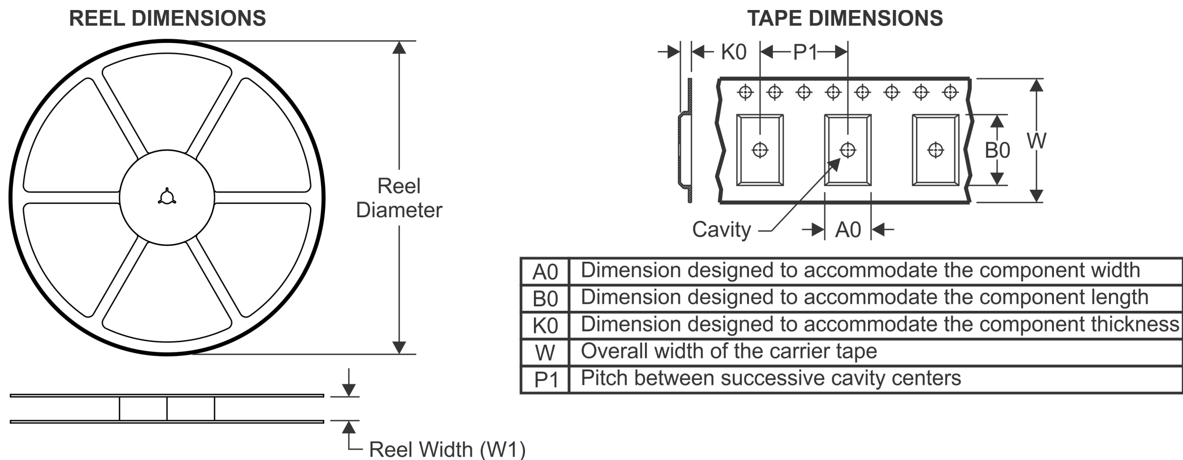
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

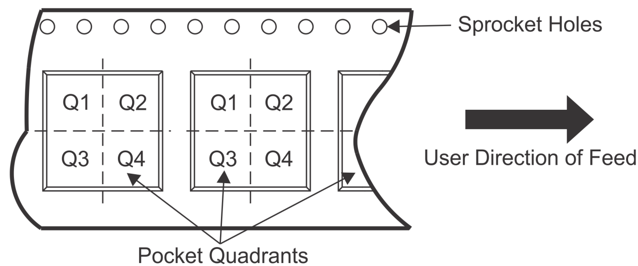
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

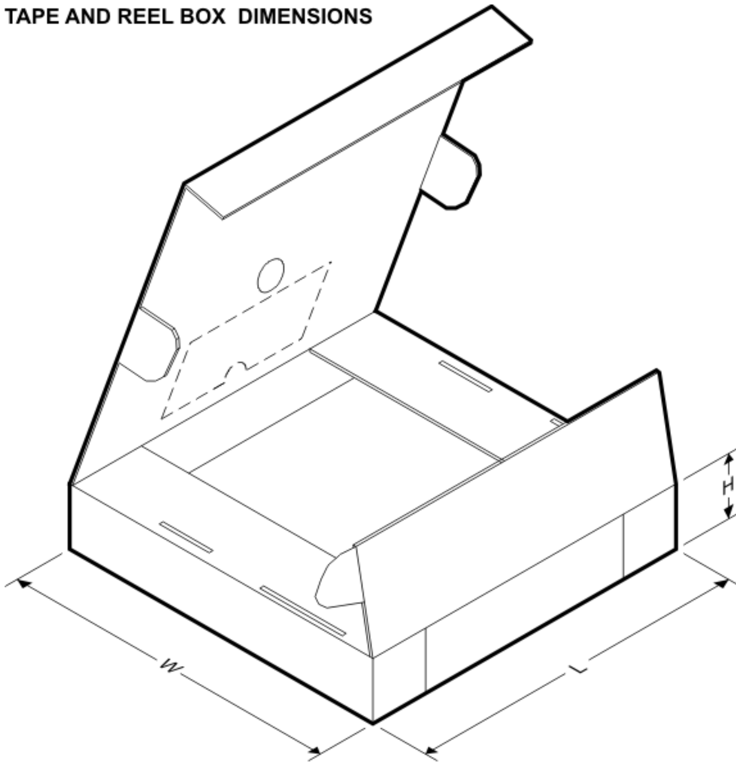
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G34DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G34DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G34DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G34DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G34DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G34DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74AUP1G34DRLR	SOT	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G34DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G34DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G34DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G34YFPR	DSBGA	YFP	4	3000	178.0	9.2	0.89	0.89	0.58	4.0	8.0	Q1
SN74AUP1G34YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

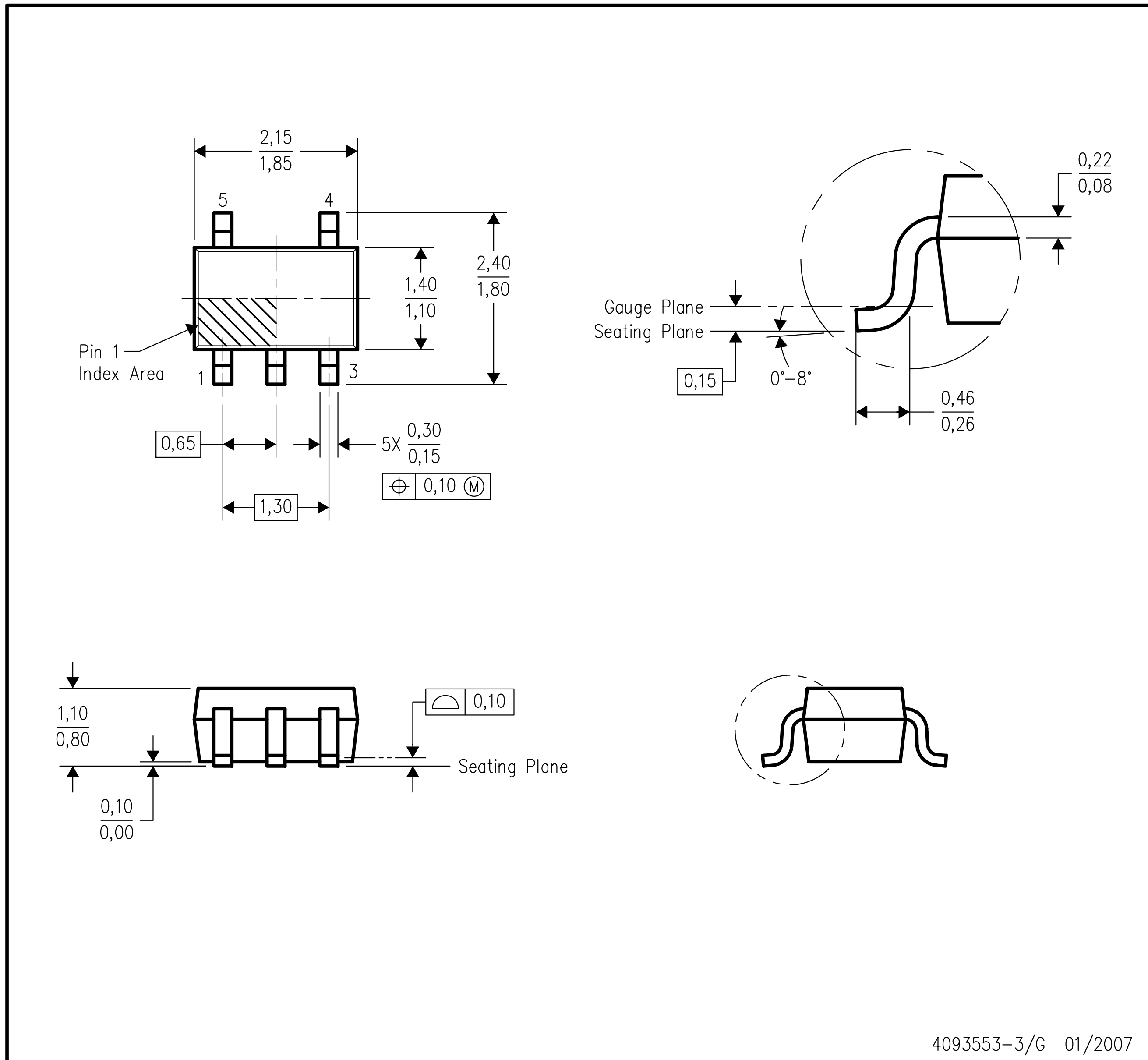
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

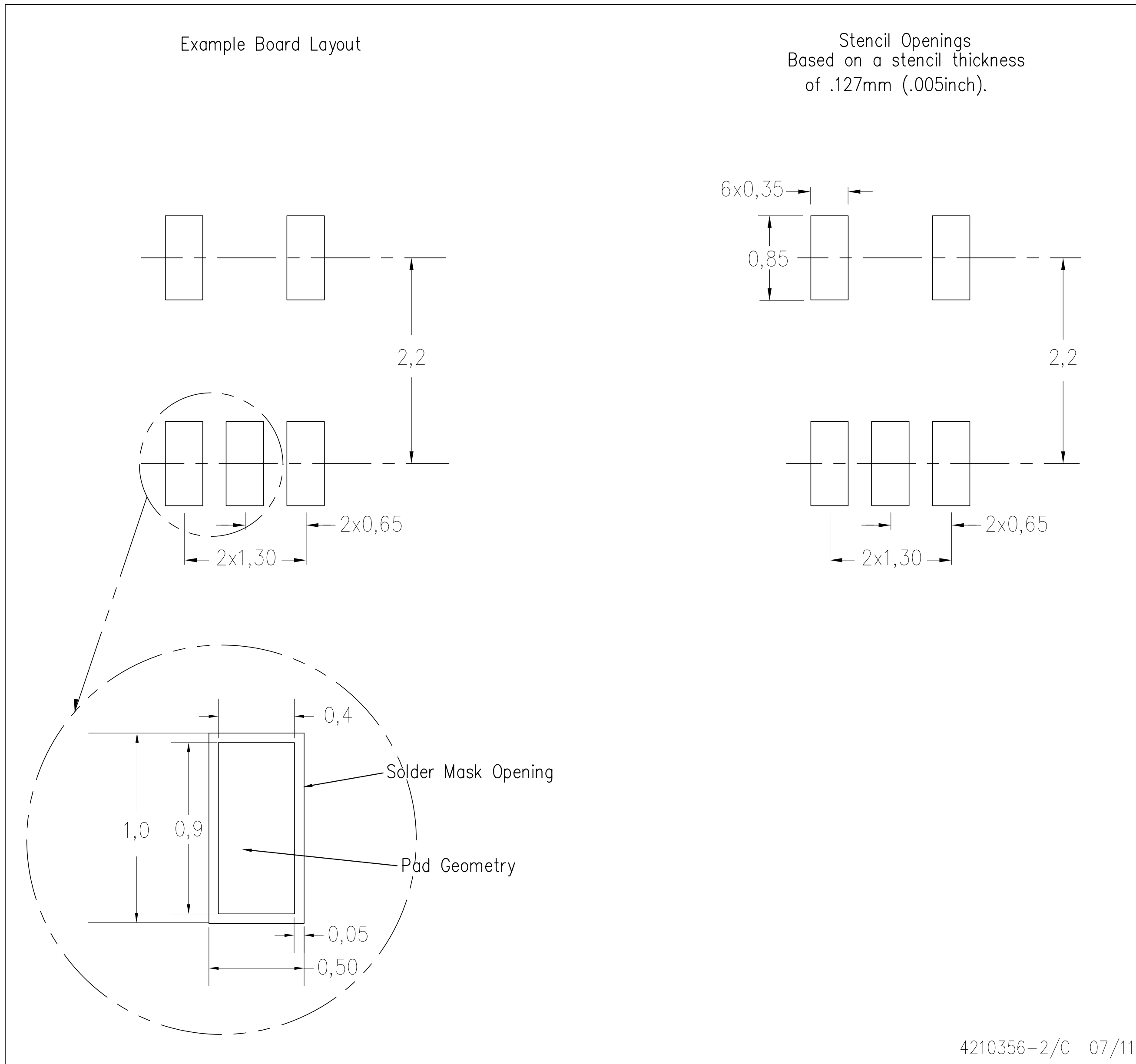
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G34DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G34DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G34DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUP1G34DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G34DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G34DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74AUP1G34DRLR	SOT	DRL	5	4000	184.0	184.0	19.0
SN74AUP1G34DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G34DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G34DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G34YFPR	DSBGA	YFP	4	3000	220.0	220.0	35.0
SN74AUP1G34YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



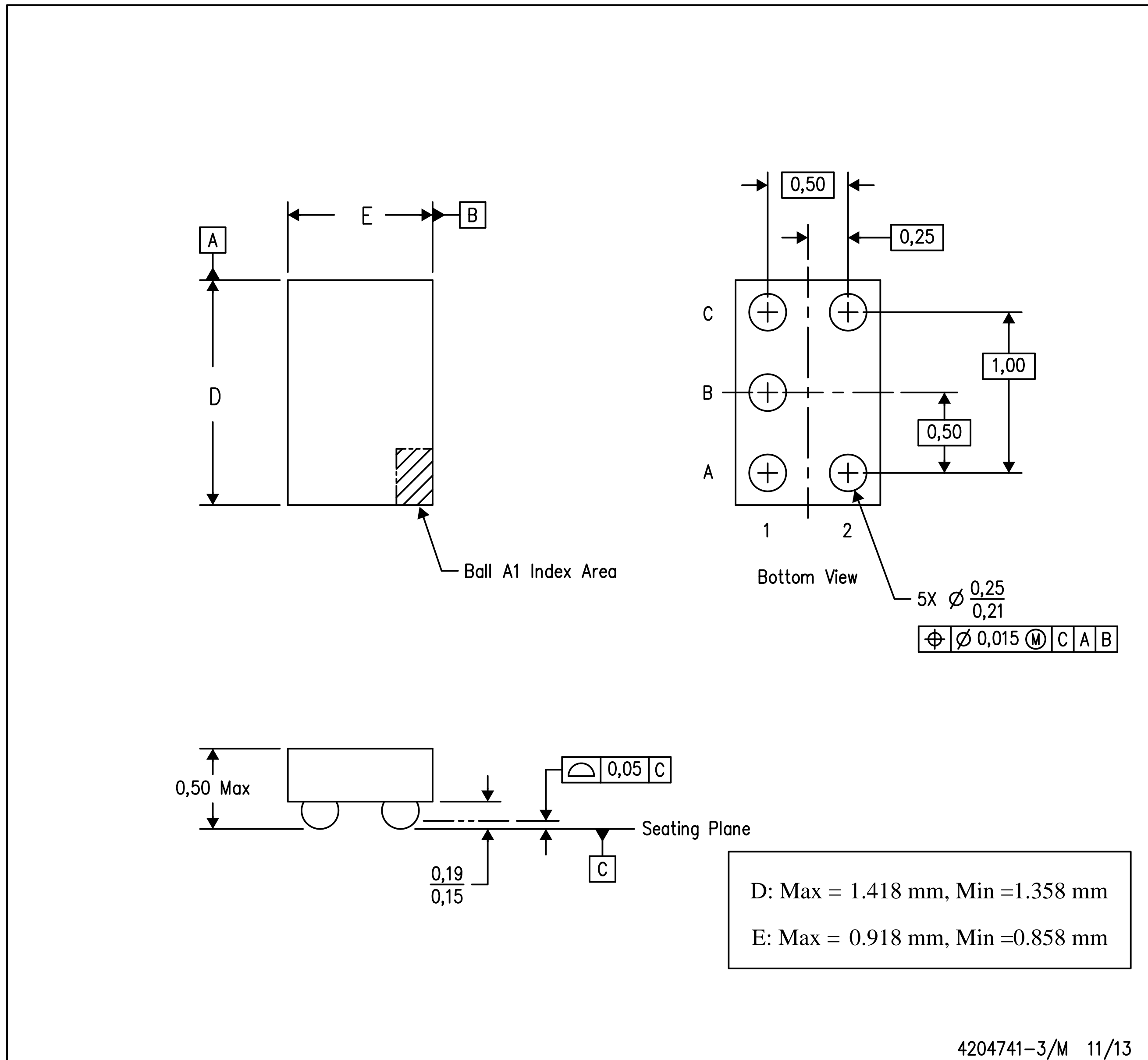
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

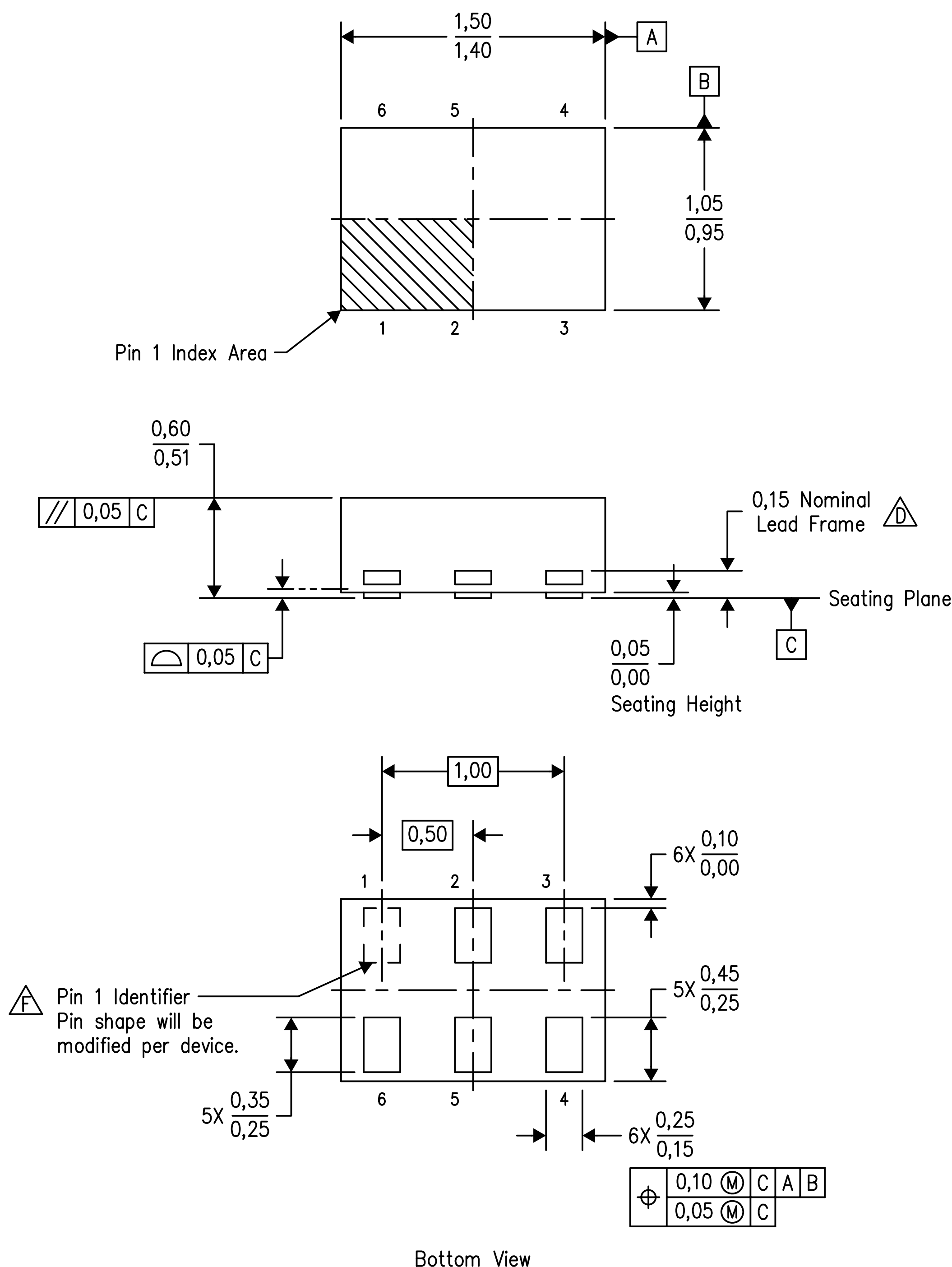
YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to change without notice.

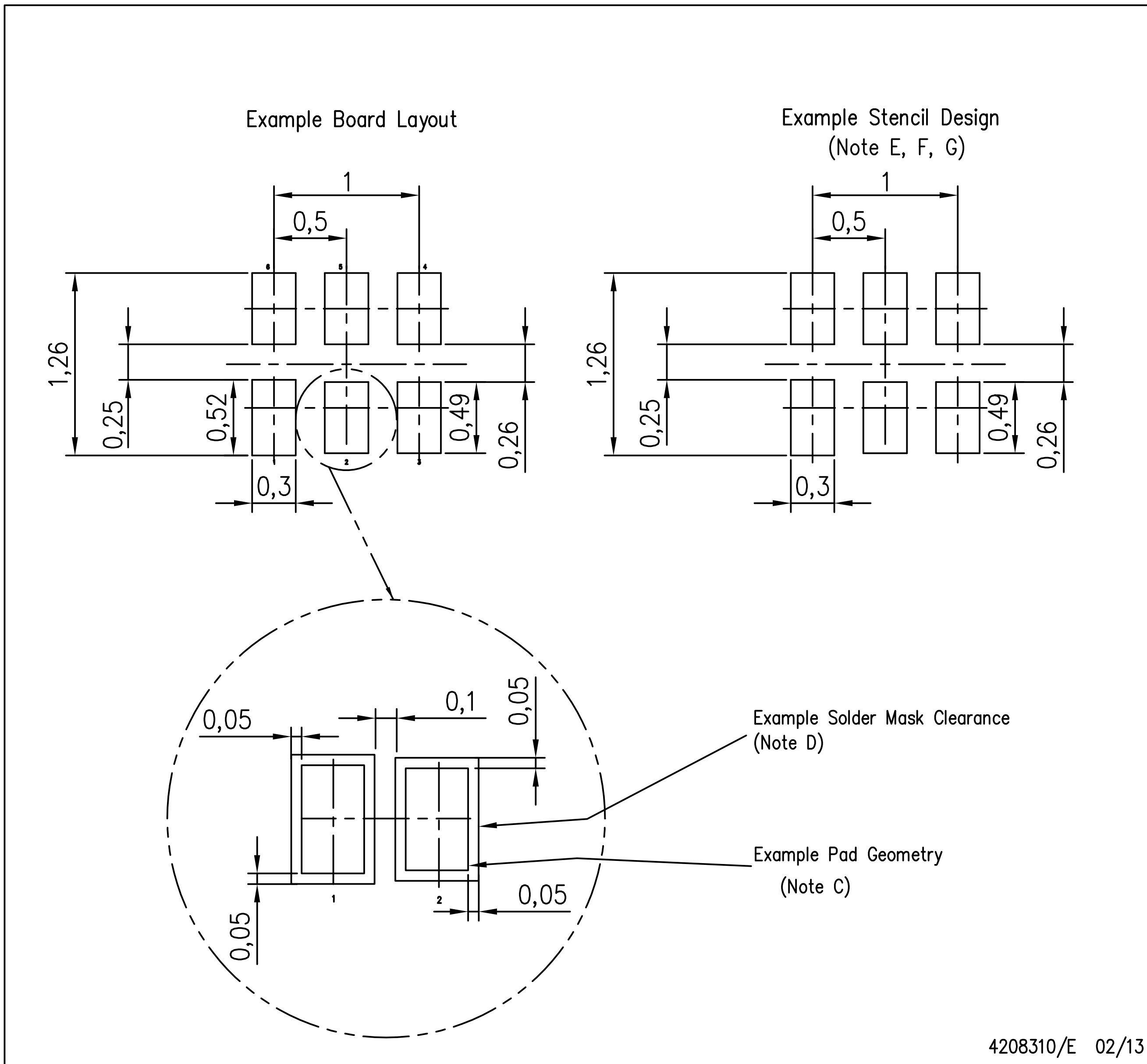
C. SON (Small Outline No–Lead) package configuration.

D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.

E. This package complies to JEDEC MO–287 variation UFAD.

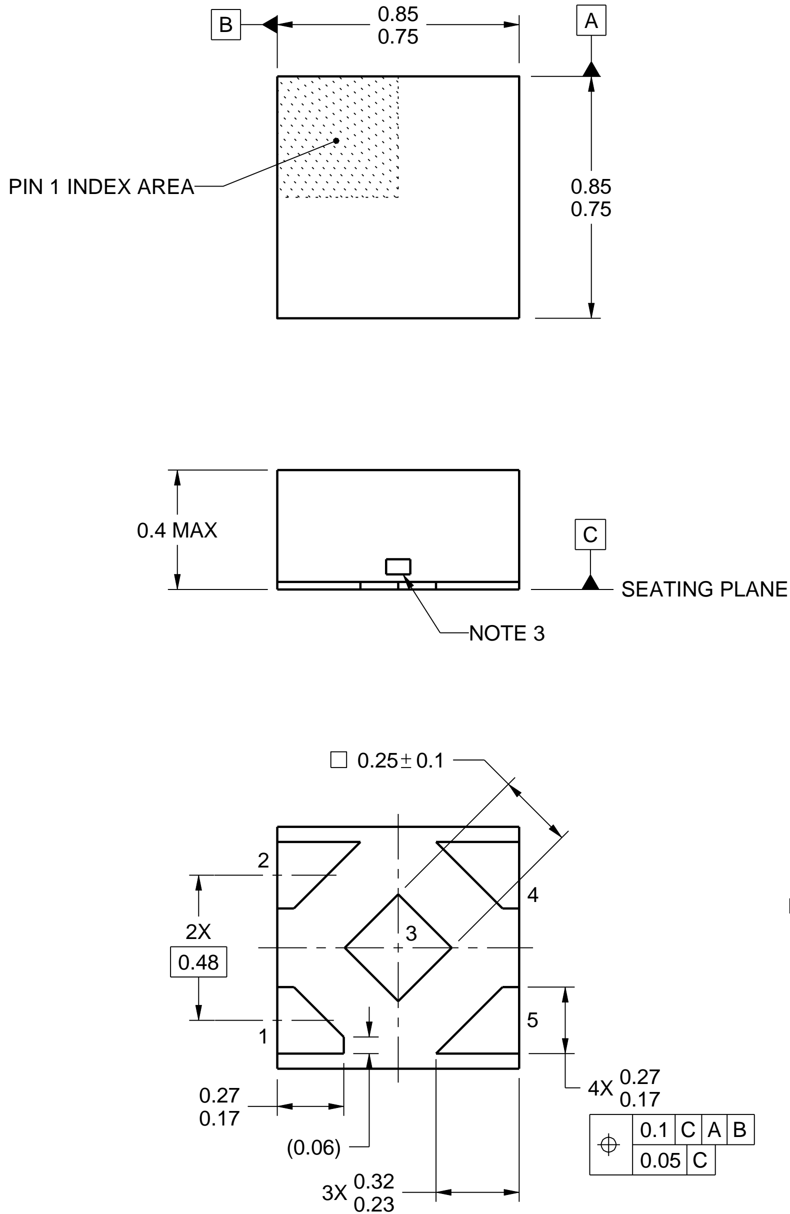
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4223102/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

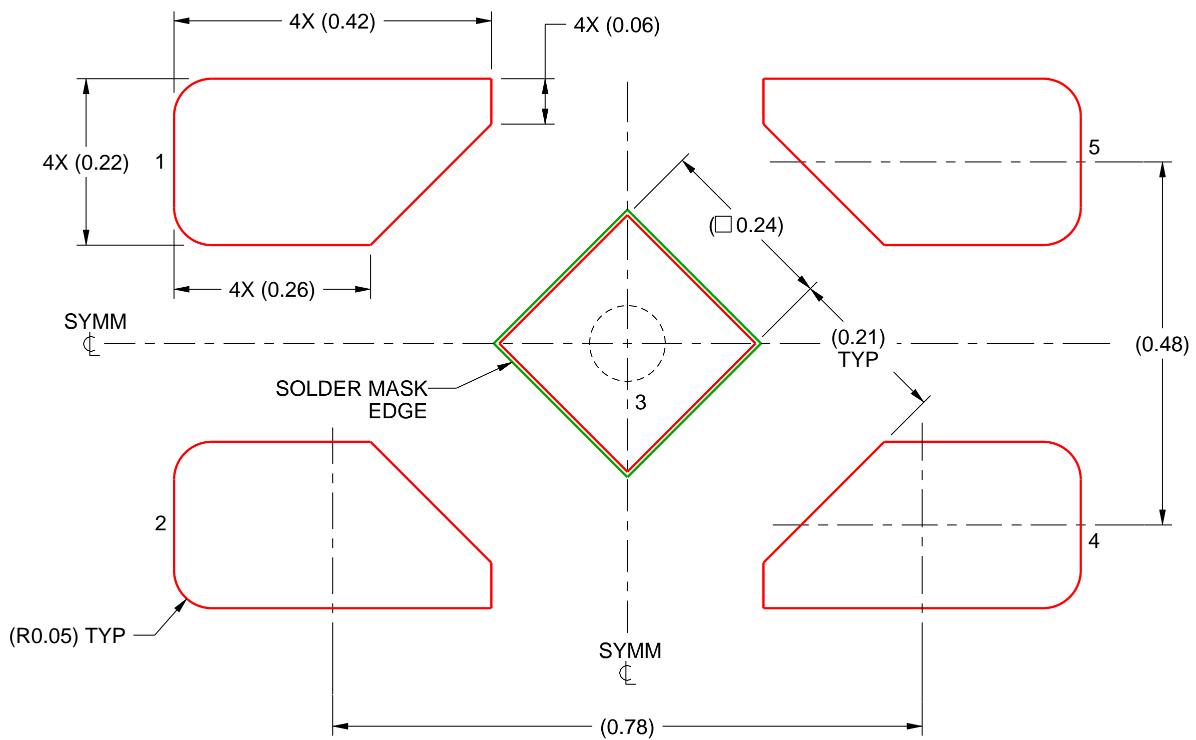
(0.78)
4X (0.42)
SYMM
(Ø0.1) VIA
0.05 MIN ALL AROUND TYP
1
4X (0.22)
5
SYMM
4X (0.26)
(0.48)
3
2
4
(R0.05) TYP
4X (0.06)
SOLDER MASK OPENING, TYP
(□0.25)
(0.21) TYP EXPOSED METAL CLEARANCE
METAL UNDER SOLDER MASK TYP

LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/A 07/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



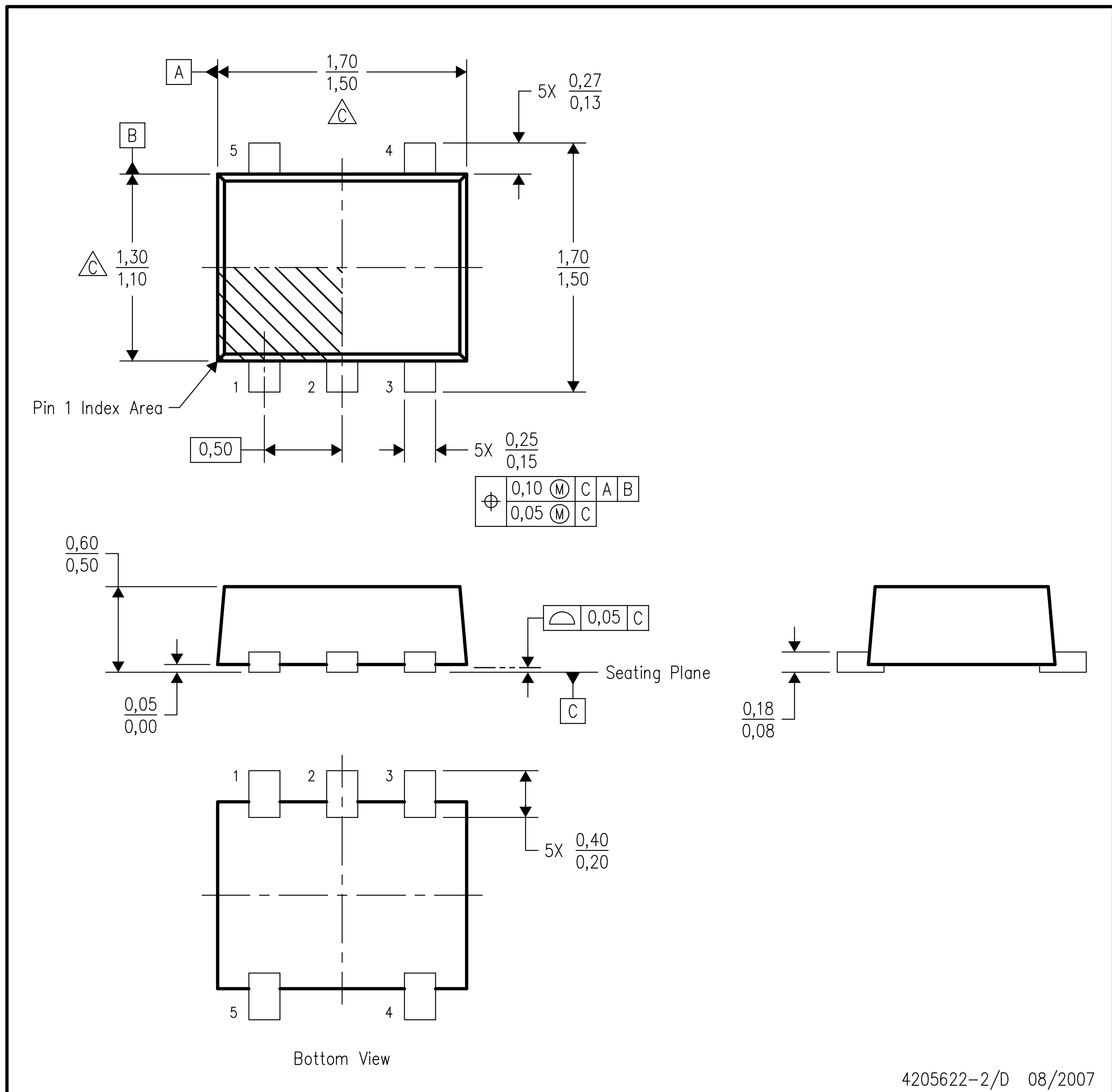
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

4223102/A 07/2016

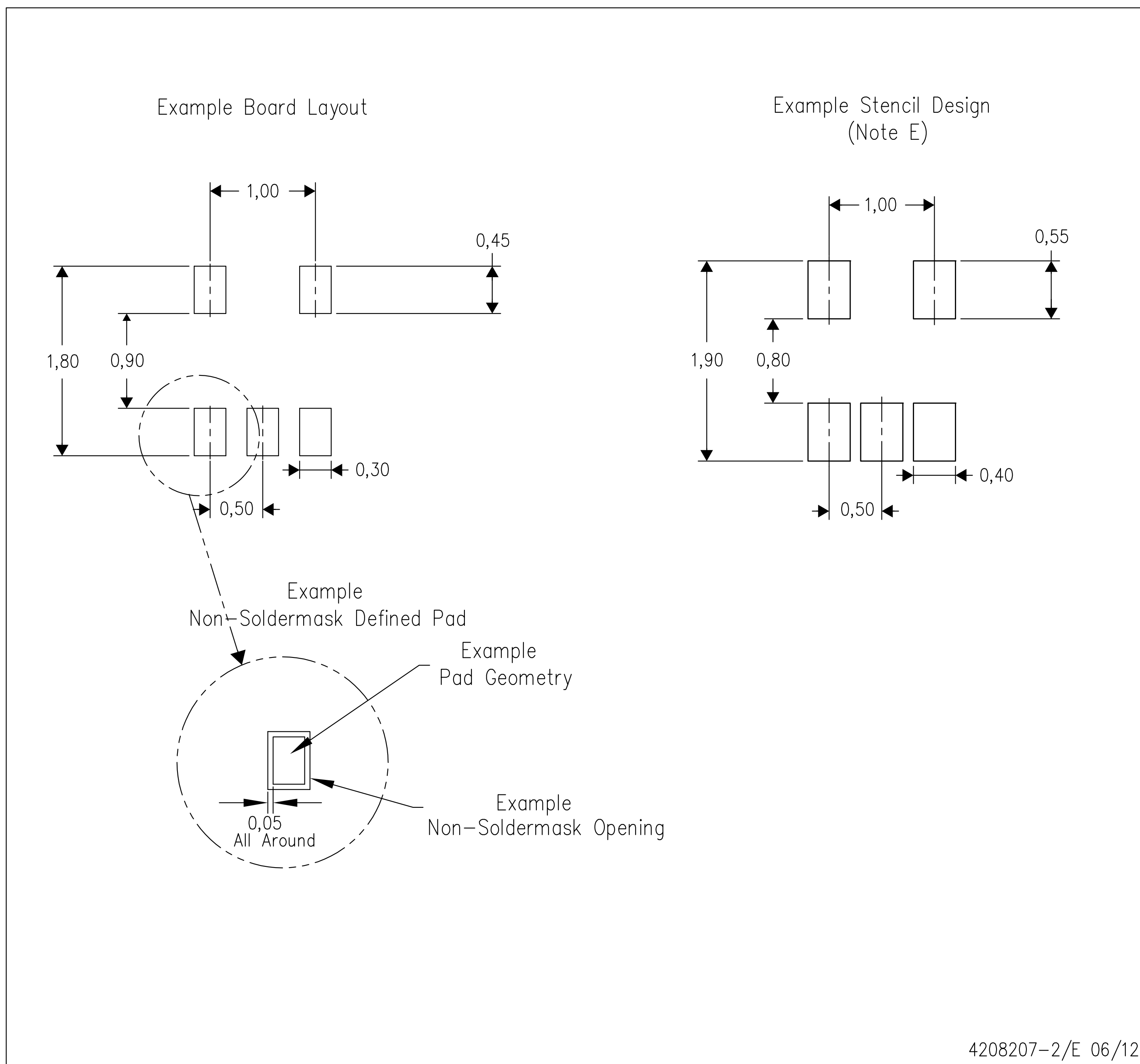
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



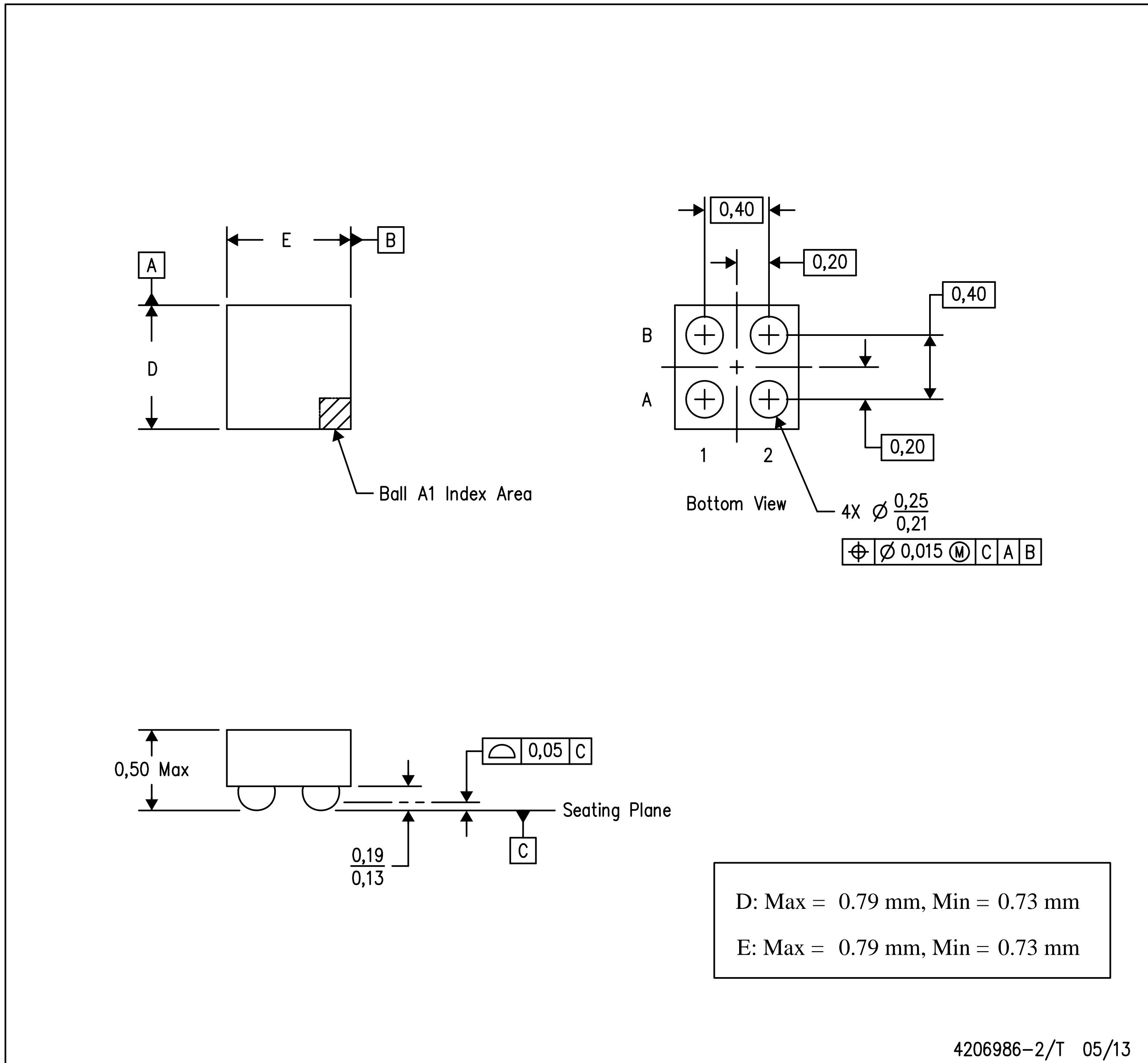
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

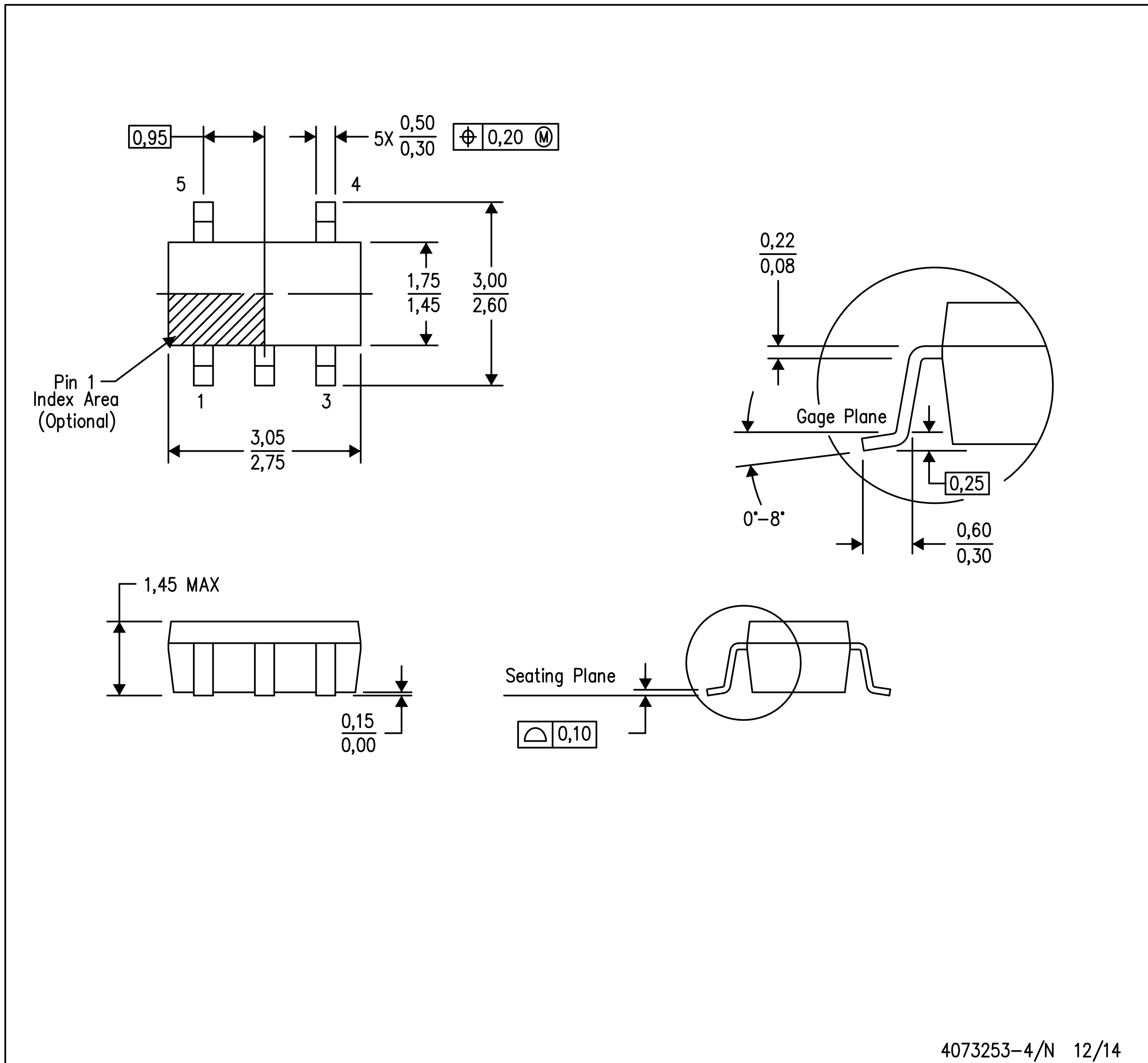
YFP (S-XBGA-N4) DIE-SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

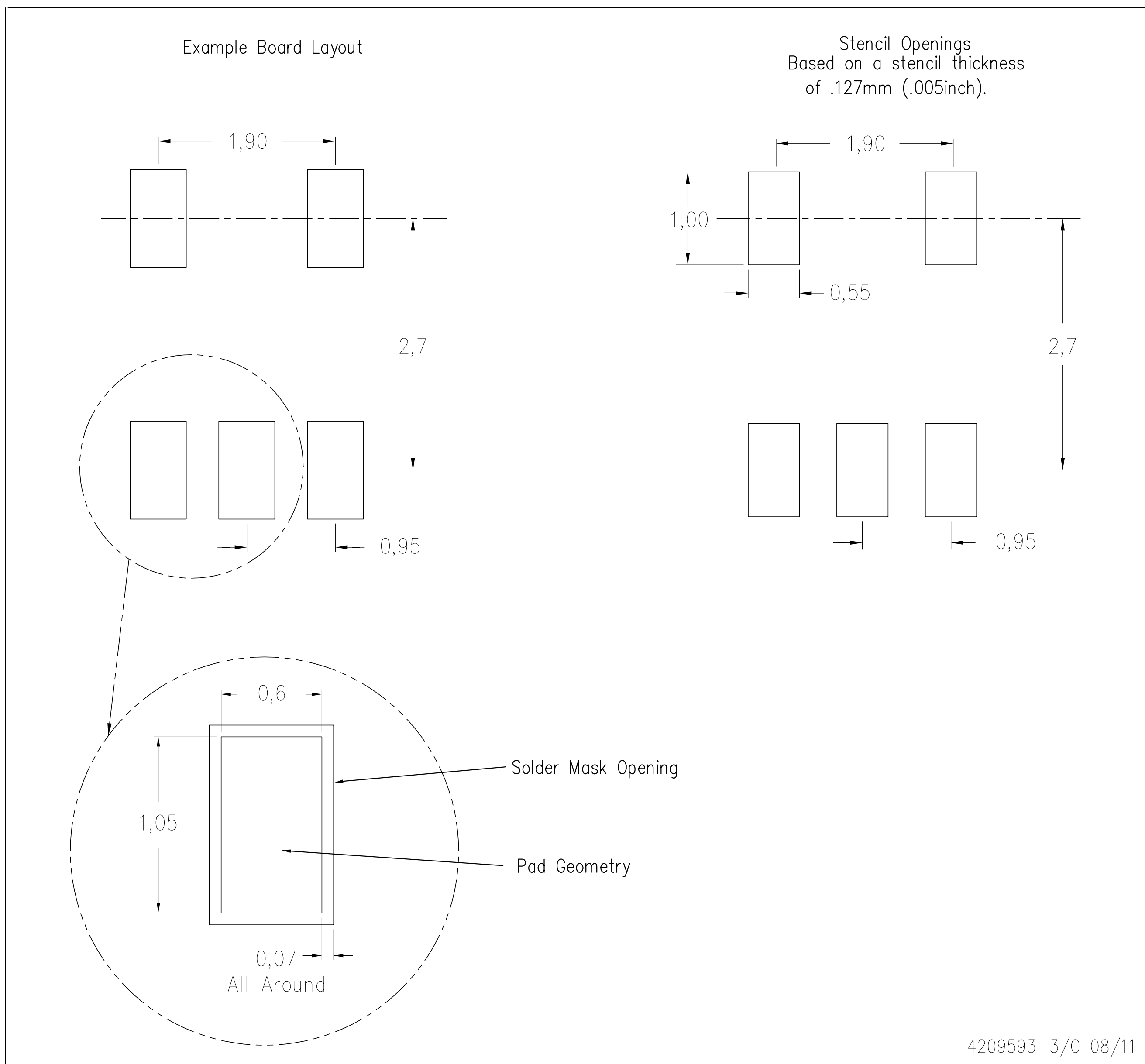
NanoFree is a trademark of Texas Instruments

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

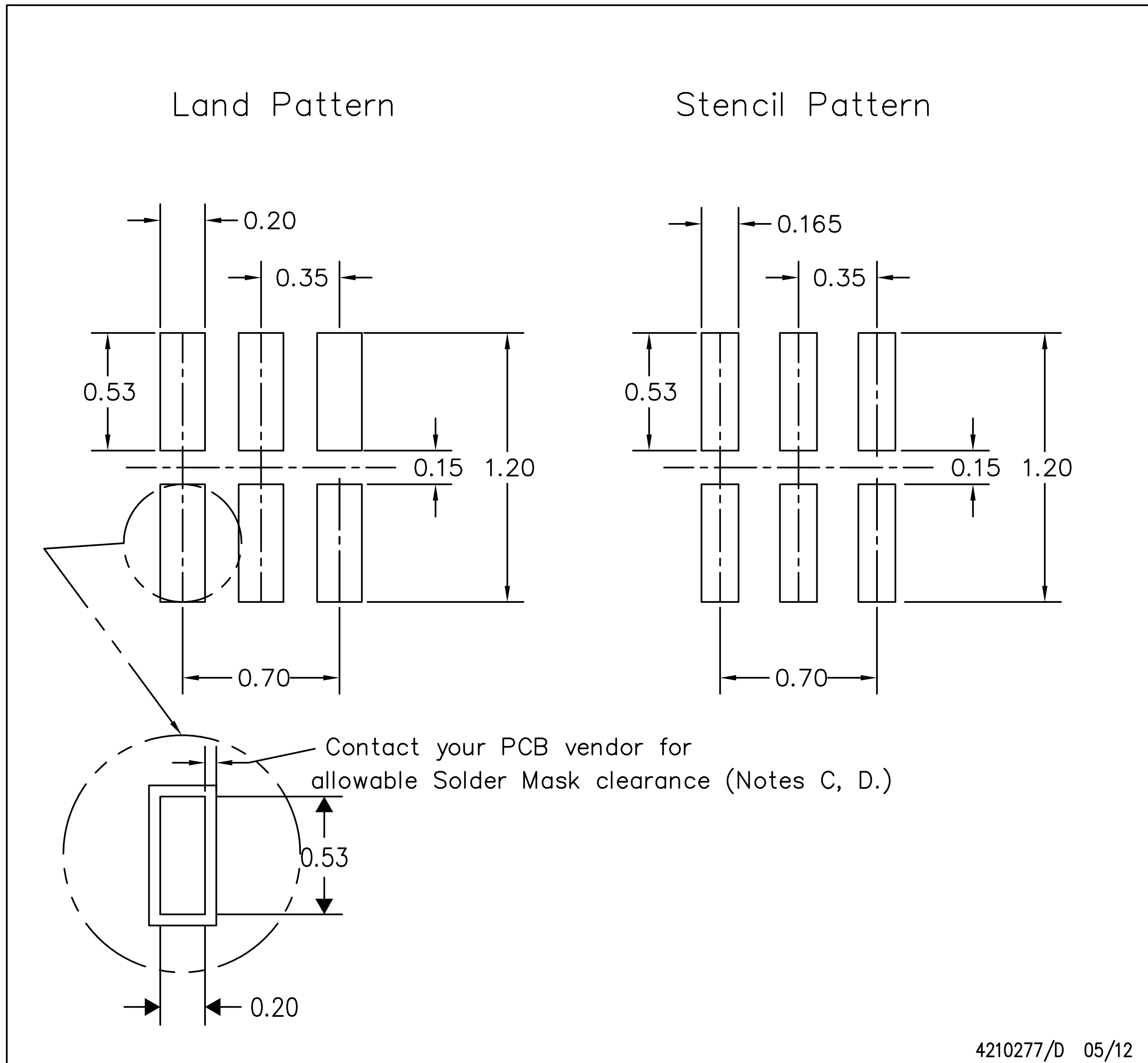
DSF (S-PX2SON-N6) PLASTIC SMALL OUTLINE NO-LEAD

4208186/F 10/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

DSF (S-PX2SON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
H. Component placement force should be minimized to prevent excessive paste block deformation.

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