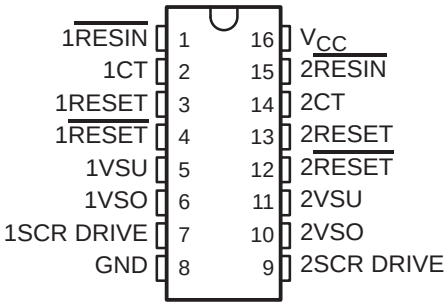
SLVS019F – OCTOBER 1987 – REVISED JULY 1999

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **$\overline{\text{RESET}}$ Defined When V_{CC} Exceeds 1 V**
- **Wide Supply-Voltage Range . . . 3.5 V to 18 V**
- **Precision Overvoltage and Undervoltage Sensing**
- **250-mA Peak Output Current for Driving SCR Gates**
- **2-mA Active-Low SCR Gate Drive for False-Trigger Protection**
- **Temperature-Compensated Voltage Reference**
- **True and Complementary Reset Outputs**
- **Externally Adjustable Output Pulse Duration**

DW OR N PACKAGE
(TOP VIEW)



description

The TL7770 is an integrated-circuit system supervisor designed for use as a reset controller in microcomputer and microprocessor power-supply systems. This device contains two independent supply-voltage supervisors that monitor the supplies for overvoltage and undervoltage conditions at the VSO and VSU terminals, respectively. When V_{CC} attains the minimum voltage of 1 V during power up, the $\overline{\text{RESET}}$ output becomes active (low). As V_{CC} approaches 3.5 V, the time-delay function activates, latching RESET and $\overline{\text{RESET}}$ active (high and low, respectively) for a time delay (t_d) after system voltages have achieved normal levels. Above V_{CC} = 3.5 V, taking $\overline{\text{RESIN}}$ low activates the time-delay function during normal system-voltage levels. To ensure that the microcomputer system has reset, the outputs remain active until the voltage at VSU exceeds the threshold value, V_{IT+}, for a time delay, which is determined by an external timing capacitor such that:

$$t_d \approx 20 \times 10^3 \times \text{capacitance}$$

where t_d is in seconds and capacitance is in farads.

The overvoltage-detection circuit is programmable for a wide range of designs. During an overvoltage condition, an internal silicon-controlled rectifier (SCR) is triggered, providing 250-mA peak instantaneous current and 25-mA continuous current to the SCR gate drive terminal, which can drive an external high-current SCR gate or an overvoltage-warning circuit.

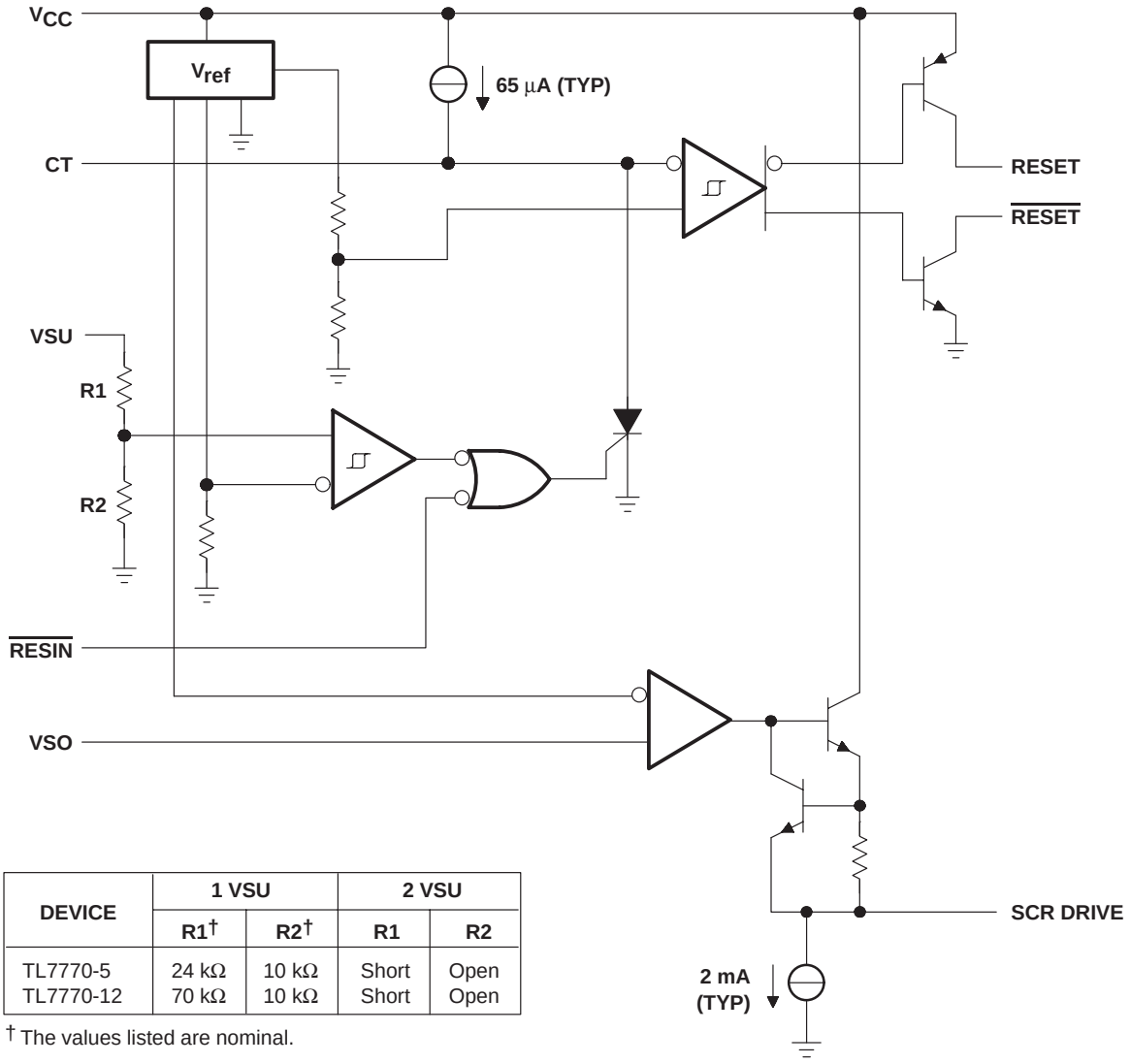
The TL7770C series is characterized for operation from 0°C to 70°C. The TL7770I series is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (DW)	PLASTIC DIP (N)	
0°C to 70°C	TL7770-5CDW TL7770-12CDW	TL7770-5CN TL7770-12CN	TL7770-5Y TL7770-12Y
–40°C to 85°C	TL7770-5IDW	TL7770-5IN	—

DW package is available taped and reeled. Add the suffix R to the device type (e.g., TL7770-5CDWR). Chip forms are tested at 25°C.

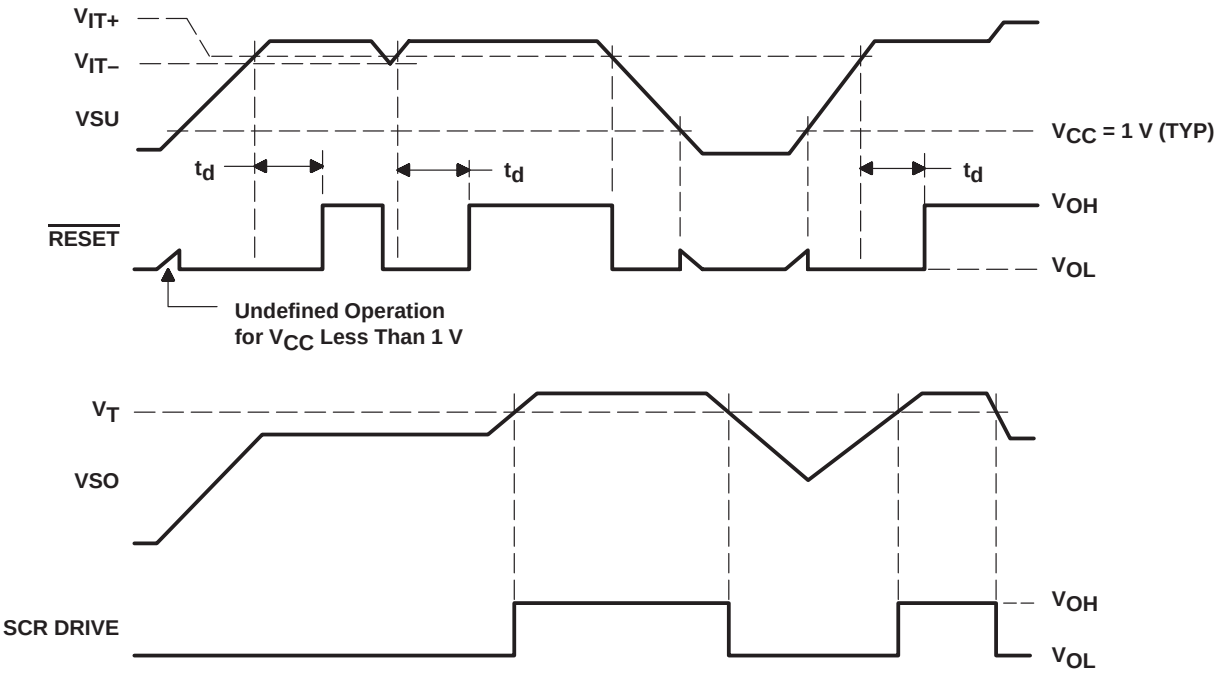
functional block diagram (each channel)



DEVICE	1 VSU		2 VSU	
	R1†	R2†	R1	R2
TL7770-5	24 kΩ	10 kΩ	Short	Open
TL7770-12	70 kΩ	10 kΩ	Short	Open

† The values listed are nominal.

timing requirements



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 20 V
Input voltage range, V_I: 1VSU, 2VSU, 1VSO, and 2VSO (see Note 1) . . . . . –0.3 V to 18 V
Low-level output current (1$\overline{\text{RESET}}$ and 2$\overline{\text{RESET}}$), I_{OL} . . . . . 20 mA
High-level output current (1RESET and 2RESET), I_{OH} . . . . . –20 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DW package . . . . . 57°C/W
N package . . . . . 88°C/W
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: DW or N package . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	18	V
Input voltage range, V_I (see Note 4)	1VSU, 2VSU, 2VSO, 1VSO	0	18	V
Output voltage, V_O (1CT, 2CT)			5	V
High-level input voltage range, V_{IH} (1$\overline{\text{RESIN}}$, 2$\overline{\text{RESIN}}$)		2	18	V
Low-level input voltage range, V_{IL} (1$\overline{\text{RESIN}}$, 2$\overline{\text{RESIN}}$)		0	0.8	V
Output sink current, I_O (1CT, 2CT)			50	μA
High-level output current, I_{OH} (1RESET, 2RESET)			–16	mA
Low-level output current, I_{OL} (1$\overline{\text{RESET}}$, 2$\overline{\text{RESET}}$)			16	mA
Continuous output current, I_O (1SCR DRIVE, 2SCR DRIVE)			25	mA
Timing capacitor, C_T			10	μF
Operating free-air temperature, T_A	TL7770C series	0	70	°C
	TL7770I series	–40	85	°C

NOTE 4: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating conditions (unless otherwise noted)

supply supervisor section

PARAMETER			TEST CONDITIONS†	TL7770-5C TL7770-12C TL7770-5I			UNIT
				MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	RESET	I_{OH} = –15 mA	V_{CC}–1.5			V
		SCR DRIVE	I_{OH} = –20 mA	V_{CC}–1.5			
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	I_{OL} = 15 mA			0.4	V
$V_{IT–}$	Undervoltage input threshold at VSU (negative-going)	TL7770-5 (5-V sense, 1VSU)	T_A = MIN to MAX	4.46		4.64	V
		TL7770-12 (12-V sense, 1VSU)		10.68		11.12	
		TL7770-5, TL7770-12 (programmable sense, 2VSU)		1.47		1.53	
V_{hys}	Hysteresis at VSU ($V_{IT+} – V_{IT–}$)	TL7770-5 (5-V sense, 1VSU)	T_A = MIN to MAX		15		mV
		TL7770-12 (12-V sense, 1VSU)			36		
		TL7770-5, TL7770-12 (programmable sense, 2VSU)			5		
V_T	Overvoltage threshold at VSO	TL7770-5, TL7770-12 (VSO)	T_A = MIN to MAX	2.48		2.68	V
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 5.5 V or 0.4 V			–10	µA
		VSO	V_I = 2.4 V		0.5	2	
I_{OH}	High-level output current	$\overline{\text{RESET}}$	V_O = 18 V			50	µA
I_{OL}	Low-level output current	RESET	V_O = 0			–50	µA
I_{OH}	Peak output current	SCR DRIVE	Duration = 1 ms	250			mA

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

total device

PARAMETER		TEST CONDITIONS†		TL7770-5C TL7770-12C TL7770-5I			UNIT
				MIN	TYP‡	MAX	
V_{res}§	Power-up reset voltage	V_{CC} = VSU			0.8	1	V
I_{CC}	Supply current	1$\overline{\text{VSU}}$ = 18 V, 2$\overline{\text{VSU}}$ = 2 V, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC}, 1VSO and 2VSO at 0 V	T_A = 25°C			5	mA
			T_A = MIN to MAX			6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

electrical characteristics over recommended operating conditions (unless otherwise noted)

supply supervisor section

PARAMETER			TEST CONDITIONS	TL7770-5Y TL7770-12Y			UNIT
				MIN	TYP†	MAX	
V_{IT-}	Undervoltage input threshold at VSU (negative-going)	TL7770-5 (5-V sense, 1VSU)	T_A = MIN to MAX	4.46		4.64	V
		TL7770-12 (12-V sense, 1VSU)		10.68		11.12	
		TL7770-5, TL7770-12 (programmable sense, 2VSU)		1.47		1.53	
V_{hys}	Hysteresis at VSU ($V_{IT+} - V_{IT-}$)	TL7770-5 (5-V sense, 1VSU)	T_A = MIN to MAX		15		mV
		TL7770-12 (12-V sense, 1VSU)			36		
		TL7770-5, TL7770-12 (programmable sense, 2VSU)			5		
V_T	Overvoltage threshold at VSO	TL7770-5, TL7770-12 (VSO)	T_A = MIN to MAX	2.48		2.68	V
I_I	Input current	VSO	V_I = 2.4 V		0.5		µA

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

total device

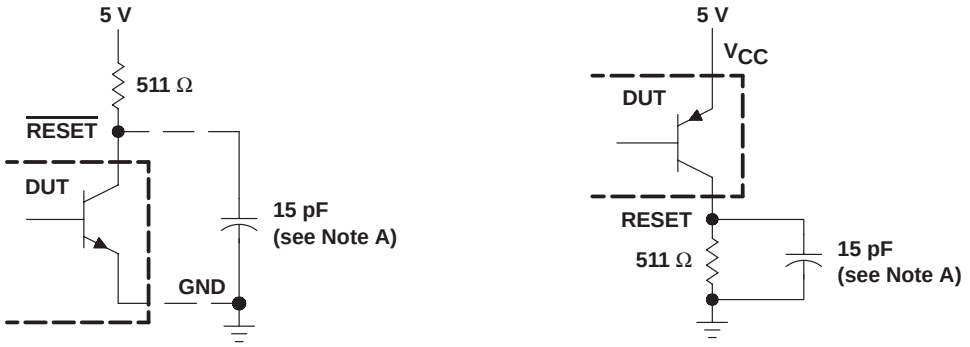
PARAMETER		TEST CONDITIONS		TL7770-5Y TL7770-12Y			UNIT
				MIN	TYP†	MAX	
V_{res}‡	Power-up reset voltage	V_{CC} = VSU,	V_{OL} = 0.4 V, I_{OL} = 1 mA		0.8		V
I_{CC}	Supply current	1VSU = 18 V, 2VSU = 2 V, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC}, 1VSO and 2VSO at 0 V	T_A = 25°C			5	mA

† Typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics, V_{CC} = 5 V, C_T open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	RESET	See Figures 1 and 3		270	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$			270	500	ns
t_r	Rise time		RESET				75	ns
t_f	Fall time					150		
t_r	Rise time		$\overline{\text{RESET}}$			75		ns
t_f	Fall time						50	
$t_{w(min)}$	Minimum effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2a		150		ns
		VSU		See Figure 2b		100		

PARAMETER MEASUREMENT INFORMATION

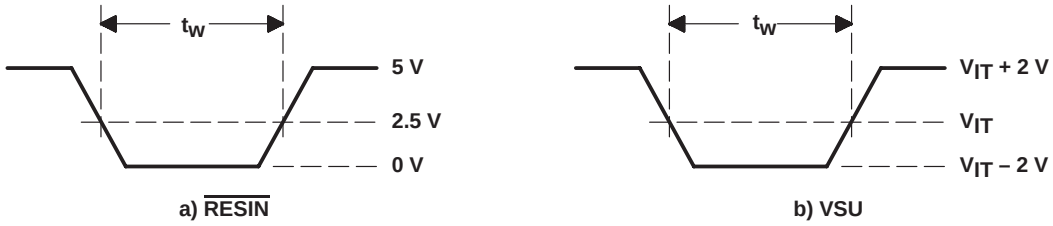


RESET OUTPUT CONFIGURATION

RESET OUTPUT CONFIGURATION

NOTE A: This includes jig and probe capacitance.

Figure 1. RESET and RESET Output Configurations



a) RESIN

b) VSU

WAVEFORMS

Figure 2. Input Pulse Definition

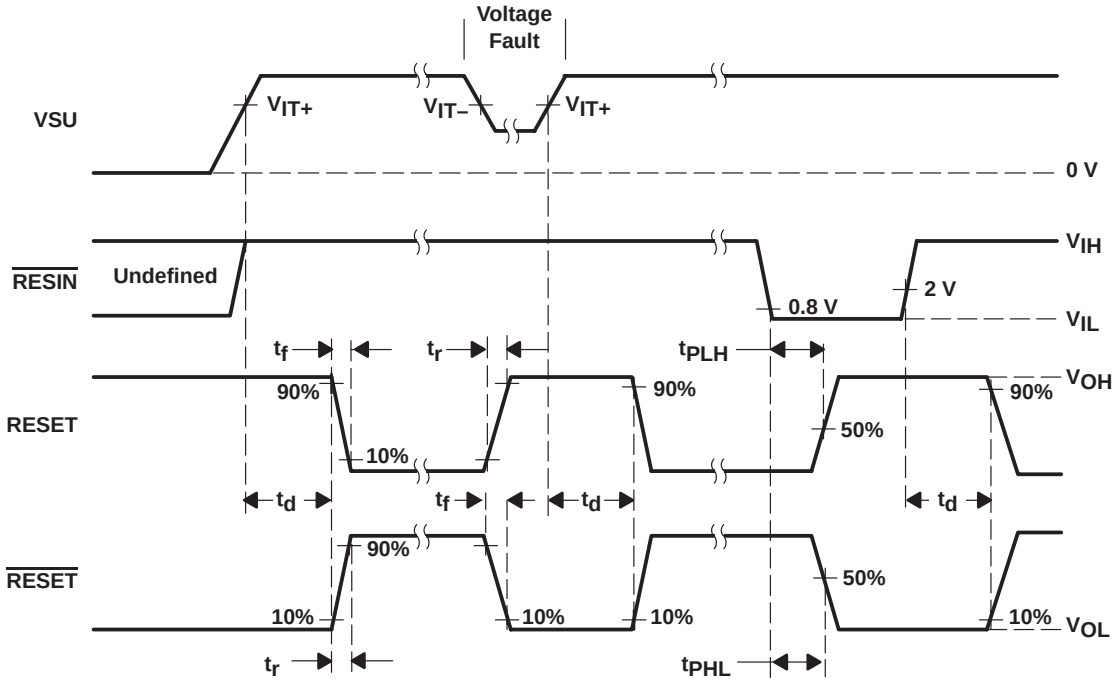
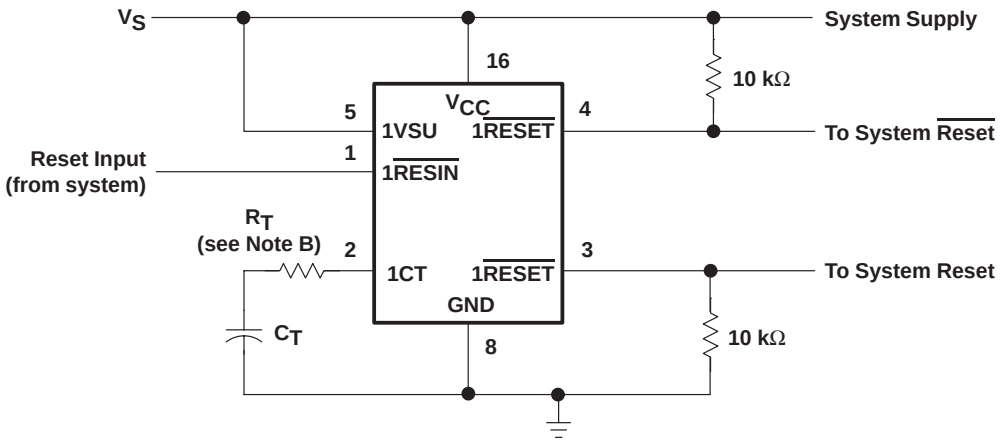


Figure 3. Voltage Waveforms

APPLICATION INFORMATION



NOTE B: When V_{CC} and 1VSU are connected to the same point, it is recommended that series resistance (R_T) be added between the time-delay programming capacitor (C_T) and the voltage-supervisor device terminal (1CT). The suggested R_T value is given by:

$$R_T > \frac{V_I - V_{IT-}}{1 \times 10^{-3}}, \text{ where } V_I = \left(\text{the lesser of 7.1 V or } V_S\right)$$

When this series resistor is used, the t_d calculation is as follows:

$$t_d = \frac{1.3 - \left[\left((6.5E - 5) \times 10^{-5}\right) \times R_T\right]}{6.5 \times 10^{-5}} \times C_T$$

Figure 4. System Reset Controller With Undervoltage Sensing

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9093201MEA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
5962-9093202M2A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
5962-9093202MEA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
TL7770-12CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7770-12C	Samples
TL7770-12CN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
TL7770-12MJB	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
TL7770-5CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL7770-5C	Samples
TL7770-5CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL7770-5C	Samples
TL7770-5CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7770-5CN	Samples
TL7770-5CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7770-5CN	Samples
TL7770-5IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL7770-5I	Samples
TL7770-5IDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL7770-5I	Samples
TL7770-5IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL7770-5I	Samples
TL7770-5IDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL7770-5I	Samples
TL7770-5IDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL7770-5I	Samples
TL7770-5MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
TL7770-5MJB	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
TL7770-5QDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125		
TL7770-5QDWR	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125		
TL7770-5QN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

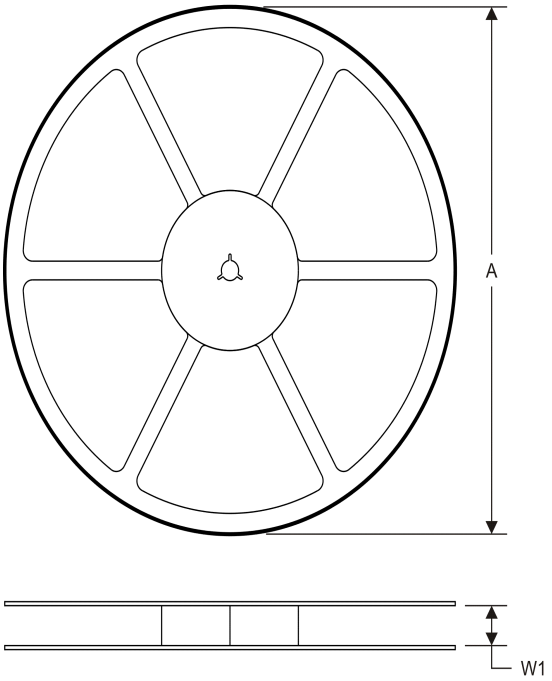
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

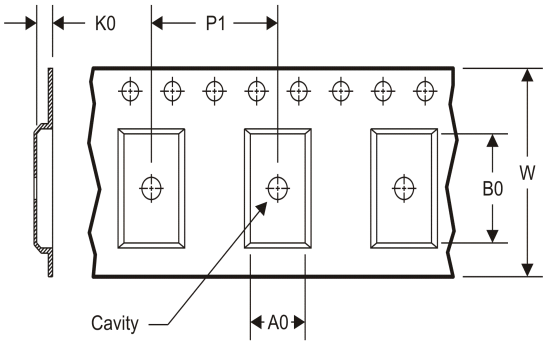
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



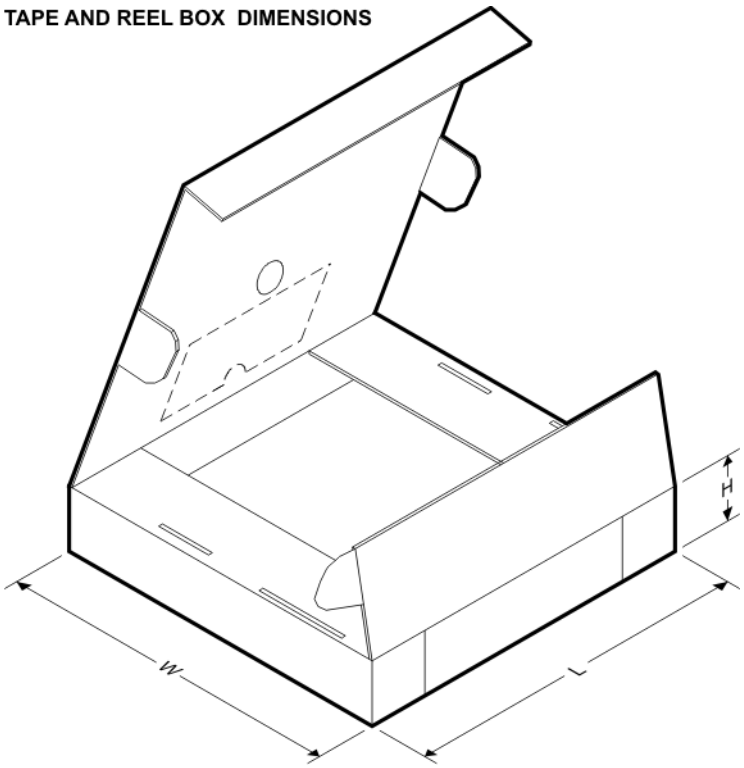
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7770-12CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TL7770-5CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TL7770-5IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



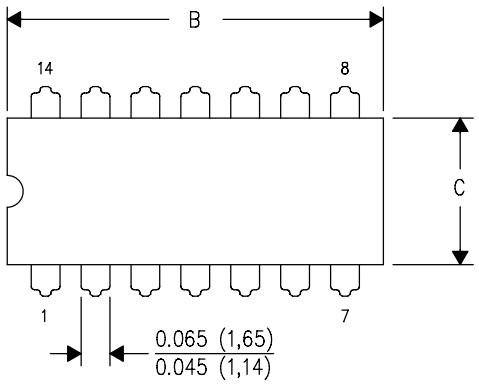
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7770-12CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
TL7770-5CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
TL7770-5IDWR	SOIC	DW	16	2000	367.0	367.0	38.0

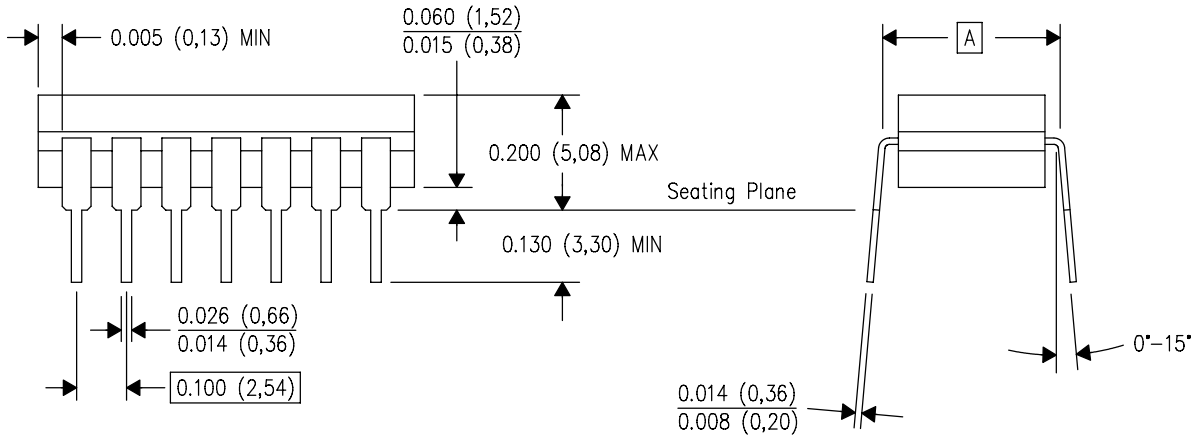
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



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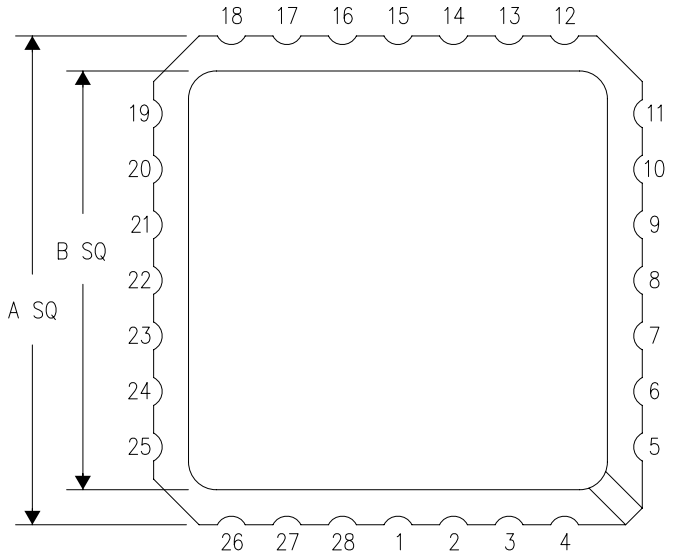
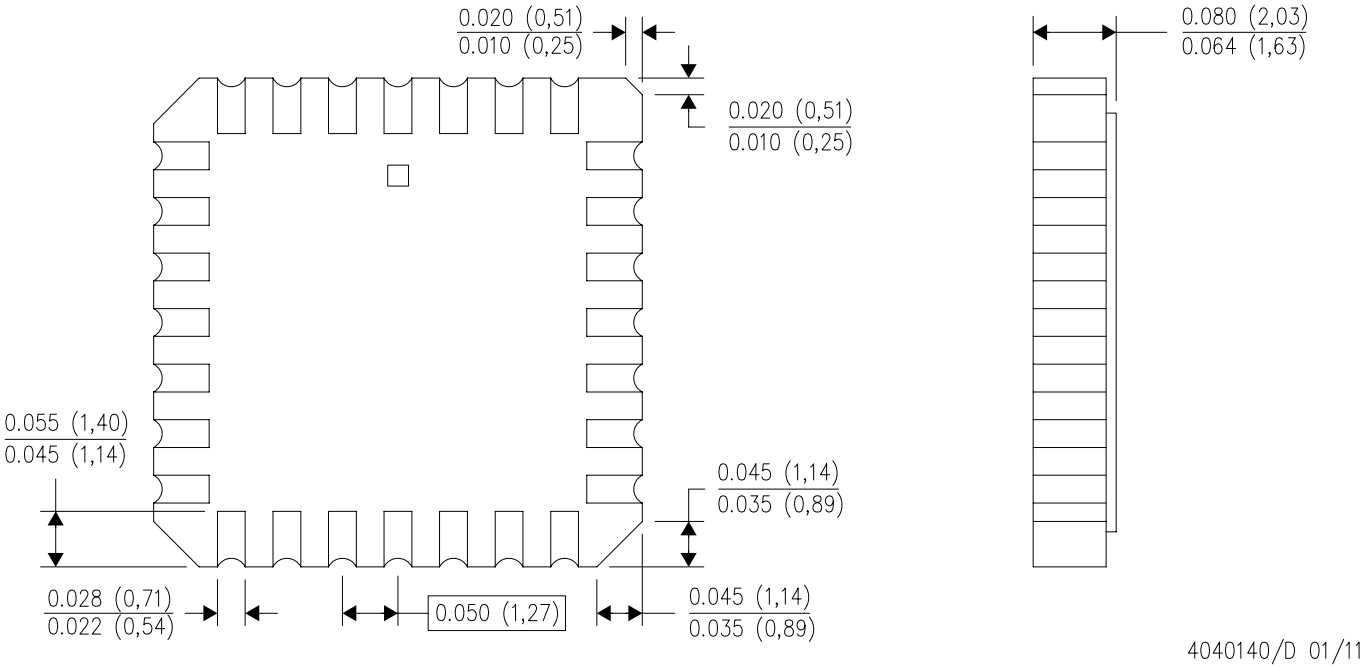
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



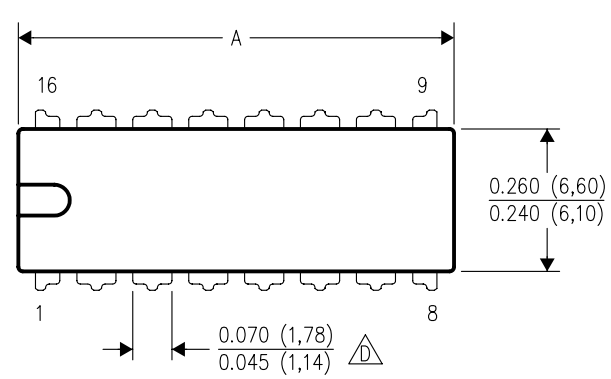
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

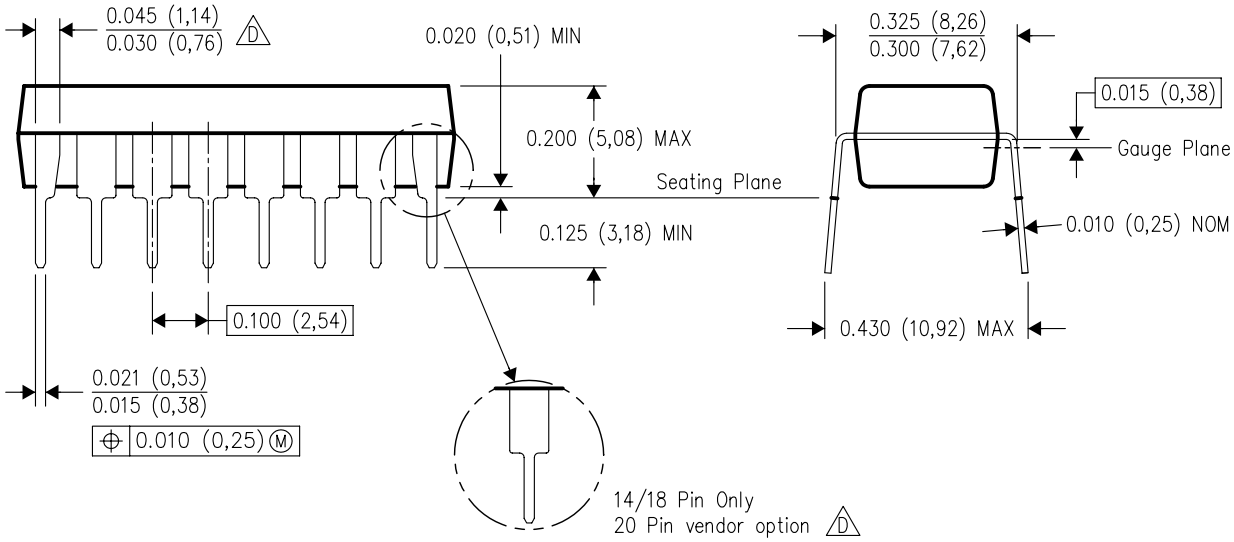
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



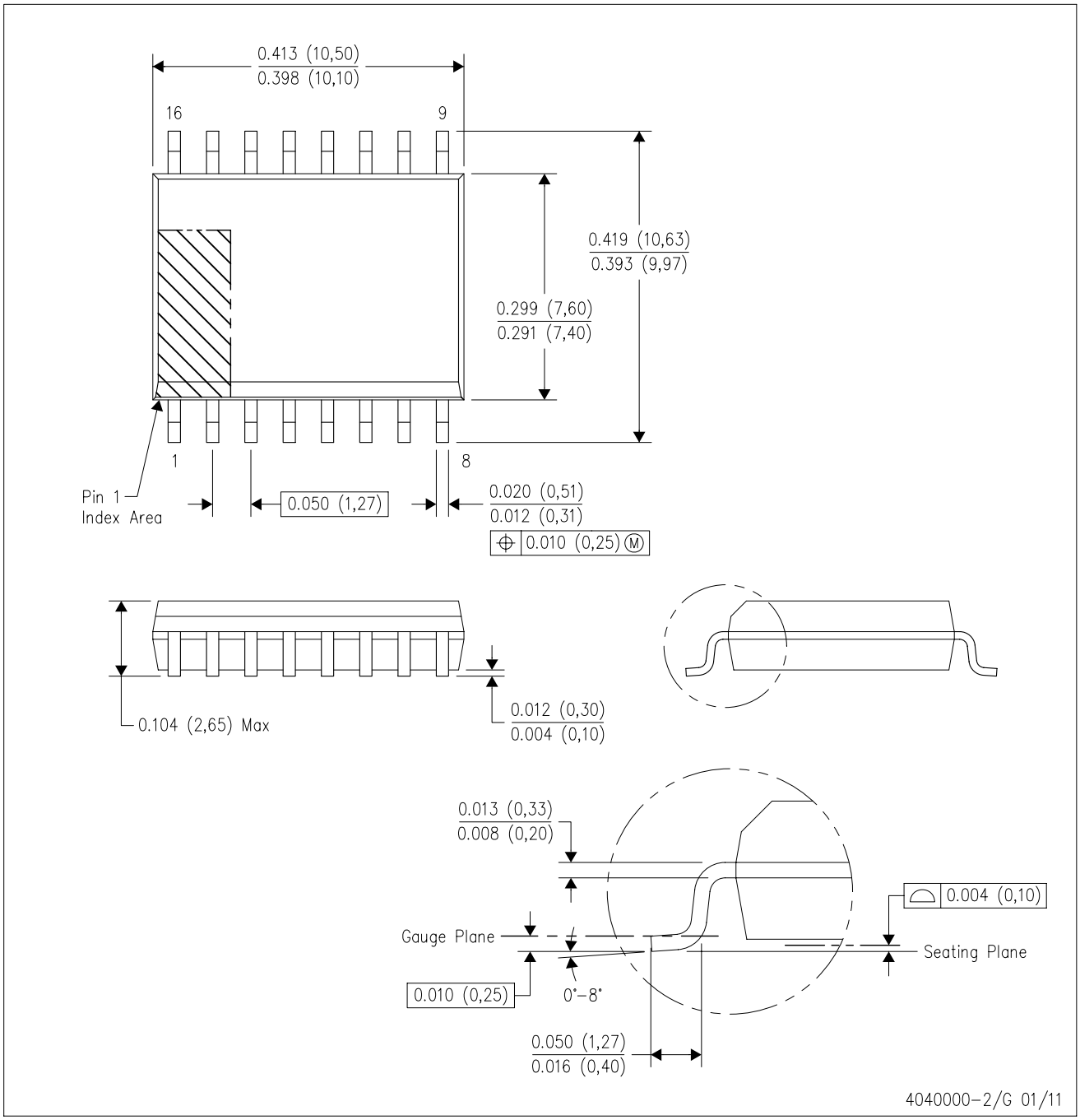
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

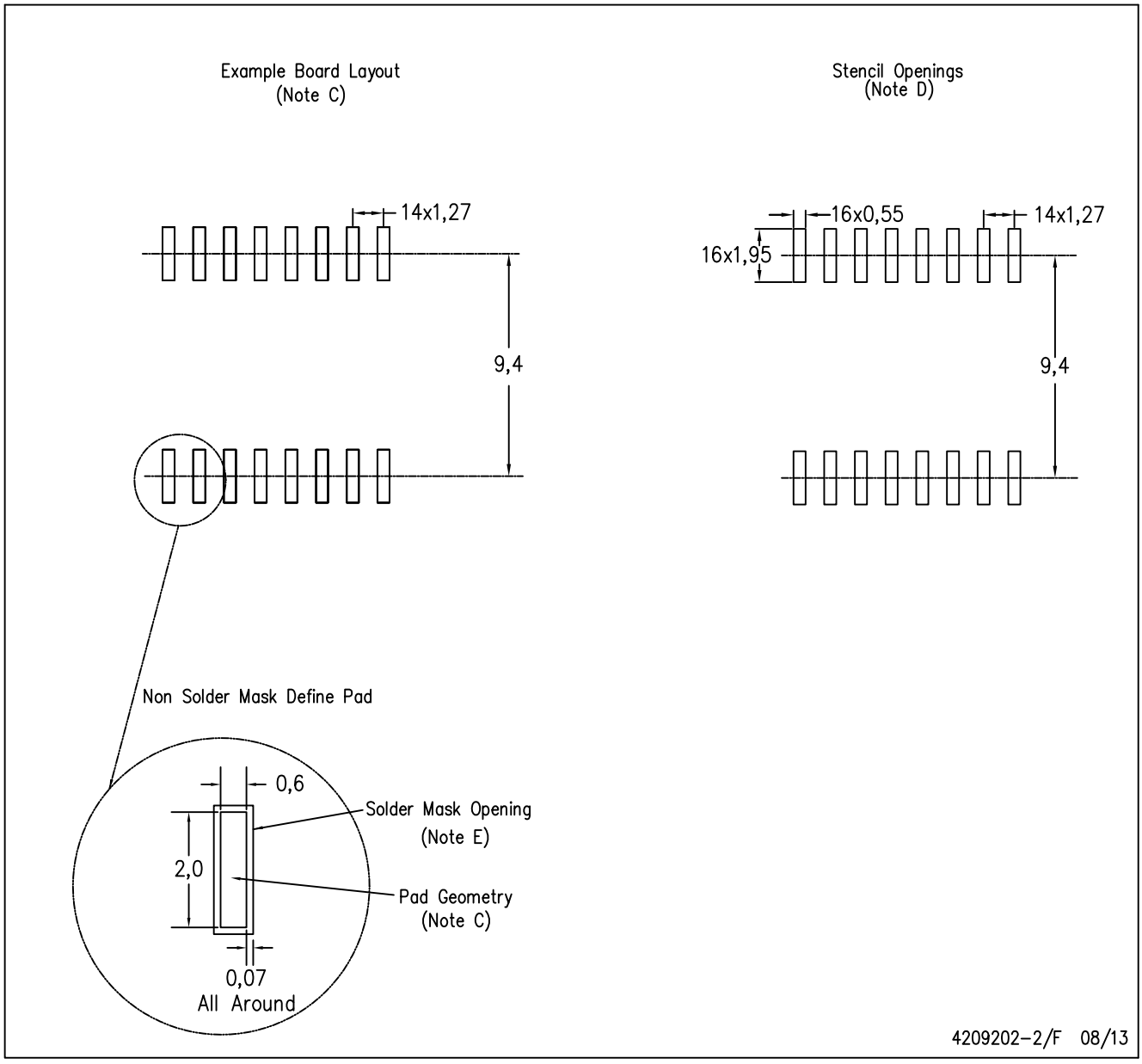
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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