#### TPA6102A2 50-mW ULTRALOW-VOLTAGE, FIXED-GAIN STEREO HEADPHONE AUDIO POWER AMPLIFIER

BYPASS

SHUTDOWN I

GND □

IN2- □

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8 III IN1-

7 Ⅲ V<sub>O</sub>1

6 DD VDD

₩ V<sub>O</sub>2

D or DGK PACKAGE (TOP VIEW)

3

- 50-mW Stereo Output
- Low Supply Current . . . 0.75 mA
- Low Shutdown Current . . . 50 nA
- Minimal External Components Required
- Gain Set Internally to 14 dB
- Pop Reduction Circuitry
- Internal Mid-Rail Generation
- Thermal and Short-Circuit Protection
- Surface-Mount Packaging
  - MSOP
  - SOIC
- 1.6-V to 3.6-V Supply Voltage Range

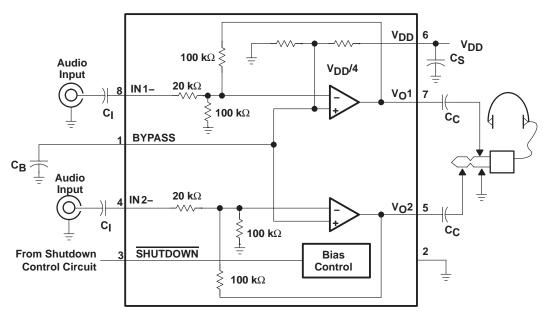
#### description

The TPA6102A2 is a stereo audio power amplifier packaged in either an 8-pin SOIC package or an 8-pin MOSP package capable of delivering 50 mW of continuous RMS power per channel into 16- $\Omega$  loads. Amplifier gain is internally set to 14 dB (inverting) to save board space by eliminating six external resistors.

The TPA6102A2 is optimized for battery applications because of its low-supply current, shutdown current, and THD+N. To obtain the low-supply voltage range, the TPA6102A2 biases BYPASS to V<sub>DD</sub>/4.

When driving a  $16-\Omega$  load with 40-mW output power from 3.3 V, THD+N is 0.08% at 1 kHz, and less than 0.2% across the audio band of 20 Hz to 20 kHz. For 30 mW into 32- $\Omega$  loads, the THD+N is reduced to less than 0.06% at 1 kHz, and is less than 0.3% across the audio band of 20 Hz to 20 kHz.

#### typical application circuit





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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#### **AVAILABLE OPTIONS**

-	PACKAGED DEVICE			
IA.	SMALL OUTLINE (D)	MSOP (DGK)	SYMBOLIZATION	
-40°C to 85°C	TPA6102A2D	TPA6102A2DGK	AJN	

#### **Terminal Functions**

TERMINA	AL.		
NAME	NO.	1/0	DESCRIPTION
BYPASS	1	I	Tap to voltage divider for internal mid-supply bias supply. BYPASS is set at $V_{DD}/4$ . Connect to a 0.1- $\mu$ F to 1- $\mu$ F low ESR capacitor for best performance.
GND	2	I	GND is the ground connection.
IN1-	8	ı	IN1– is the inverting input for channel 1.
IN2-	4	I	IN2– is the inverting input for channel 2.
SHUTDOWN	3	I	Active-low input. When held low, the device is placed in a low supply current mode.
$V_{DD}$	6	- 1	V <sub>DD</sub> is the supply voltage terminal.
V <sub>O</sub> 1	7	0	V <sub>O</sub> 1 is the audio output for channel 1.
V <sub>O</sub> 2	5	0	V <sub>O</sub> 2 is the audio output for channel 2.

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V <sub>DD</sub>	4 V
Input voltage, V <sub>I</sub>	
Continuous total power dissipation	Internally Limited
Operating junction temperature range, T <sub>J</sub>	–40°C to 150°C
Storage temperature range, T <sub>stq</sub>	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### **DISSIPATION RATING TABLE**

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
D	710 mW	5.68 mW/°C	454 mW	369 mW
DGK	469 mW	3.75 mW/°C	300 mW	244 mW

#### recommended operating conditions

	МІ	N MAX	UNIT
Supply voltage, V <sub>DD</sub>	1.	6 3.6	V
High-level input voltage, V <sub>IH</sub> (SHUTDOWN)	60% x V <sub>D</sub>	)	V
Low-level input voltage, V <sub>IL</sub> (SHUTDOWN)		25% x V <sub>DD</sub>	V
Operating free-air temperature, T <sub>A</sub>	-4	0 85	°C



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## dc electrical characteristics at $T_A$ = 25°C, $V_{DD}$ = 3.6 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voo	Output offset voltage	A <sub>V</sub> = 14 dB		5	40	mV
PSRR	Power supply rejection ratio	V <sub>DD</sub> = 3 V to 3.6 V		72		dB
I <sub>DD</sub>	Supply current	SHUTDOWN = 3.6 V		0.75	1.5	mA
I <sub>DD(SD)</sub>	Supply current in SHUTDOWN mode	SHUTDOWN = 0 V		50	250	nA
I <sub>IH</sub>	High-level input current (SHUTDOWN)	$V_{DD} = 3.6 \text{ V},  V_{I} = V_{DD}$			1	μΑ
I <sub>IL</sub>	Low-level input current (SHUTDOWN)	$V_{DD} = 3.6 \text{ V},  V_{I} = 0 \text{ V}$			1	μΑ
Z <sub>I</sub>	Input impedance			20		kΩ

## ac operating characteristics, $\rm V_{DD}$ = 3.3 V, $\rm T_A$ = 25°C, $\rm R_L$ = 16 $\Omega$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
G	Gain			14		dB
PO	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		50		mW
THD+N	Total harmonic distortion + noise	$P_0 = 45 \text{ mW},  20-20 \text{ kHz}$		0.4%		
ВОМ	Maximum output power BW	THD < 0.5%		> 20		kHz
ksvr	Supply ripple rejection ratio	f = 1 kHz		47		dB
SNR	Signal-to-noise ratio	P <sub>O</sub> = 50 mW		86		dB
Vn	Noise output voltage (no noise weighting filter)			45		μV(rms)

## ac operating characteristics, $\rm V_{DD}$ = 3.3 V, $\rm T_A$ = 25°C, $\rm R_L$ = 32 $\rm \Omega$

	PARAMETER	TEST CONDITIONS	MIN TYP MAX	UNIT
G	Gain		14	dB
PO	Output power (each channel)	THD $\leq$ 0.1%, f = 1 kHz	35	mW
THD+N	Total harmonic distortion + noise	$P_0 = 30 \text{ mW},  20-20 \text{ kHz}$	0.4%	
ВОМ	Maximum output power BW	THD < 0.4%	>20	kHz
ksvr	Supply ripple rejection ratio	f = 1 kHz	47	dB
SNR	Signal-to-noise ratio	$P_O = 30 \text{ mW}$	86	dB
Vn	Noise output voltage (no noise weighting filter)		50	μV(rms)

# **TPA6102A2** 50-mW ULTRALOW-VOLTAGE, FIXED-GAIN STEREO HEADPHONE AUDIO POWER AMPLIFIER SLOS324B – JUNE 2000 – REVISED SEPTEMBER 2004

# dc electrical characteristics at $T_A$ = 25°C, $V_{DD}$ = 1.6 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voo	Output offset voltage	A <sub>V</sub> = 14 dB		5	40	mV
PSRR	Power supply rejection ratio	V <sub>DD</sub> = 1.4 V to 1.8 V		80		dB
I <sub>DD</sub>	Supply current	SHUTDOWN = 1.6 V		0.65	1.2	mA
IDD(SD)	Supply current in SHUTDOWN mode	SHUTDOWN = 0 V		50	250	nA
I <sub>IH</sub>	High-level input current (SHUTDOWN)	$V_{DD} = 1.6 \text{ V},  V_I = V_{DD}$			1	μΑ
I <sub>IL</sub>	Low-level input current (SHUTDOWN)	$V_{DD} = 1.6 \text{ V},  V_{I} = 0 \text{ V}$			1	μΑ
Z <sub>I</sub>	Input impedance			20		kΩ

## ac operating characteristics, $\rm V_{DD}$ = 1.6 V, $\rm T_A$ = 25°C, $\rm R_L$ = 16 $\Omega$

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
G	Gain		14		dB
Po	Output power (each channel)	THD $\leq$ 0.5%, f = 1 kHz	10		mW
THD+N	Total harmonic distortion + noise	$P_0 = 9.5 \text{ mW},  20-20 \text{ kHz}$	0.06%		
Вом	Maximum output power BW	THD < 1%	> 20		kHz
ksvr	Supply ripple rejection ratio	f = 1 kHz	47		dB
SNR	Signal-to-noise ratio	P <sub>O</sub> = 10 mW	82		dB
Vn	Noise output voltage (no noise weighting filter)		32	μ	ιV(rms)

## ac operating characteristics, V<sub>DD</sub> = 1.6 V, T<sub>A</sub> = 25°C, R<sub>L</sub> = 32 $\Omega$

	PARAMETER	TEST CONDITIONS	MIN TYP MAX	UNIT
G	Gain		14	dB
PO	Output power (each channel)	THD $\leq$ 0.5%, f = 1 kHz	7.5	mW
THD+N	Total harmonic distortion + noise	$P_O = 6.5 \text{ mW},  20-20 \text{ kHz}$	0.05%	
Вом	Maximum output power BW	THD < 1%	>20	kHz
ksvr	Supply ripple rejection ratio	f = 1 kHz	47	dB
SNR	Signal-to-noise ratio	P <sub>O</sub> = 7.5 mW	84	dB
V <sub>n</sub>	Noise output voltage (no noise weighting filter)		32	μV(rms)

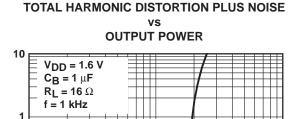
#### TYPICAL CHARACTERISTICS

#### **Table of Graphs**

			FIGURE
		vs Frequency	1, 3, 5, 7, 9, 11
THD+N	Total harmonic distortion plus noise	vs Output power	2, 4, 6, 8, 10, 12
		vs Output voltage	13, 14
Po	Output power	vs Load resistance	15, 16
ksvr	Supply ripple rejection ratio	vs Frequency	17, 18
Vn	Output noise voltage	vs Frequency	19, 20
	Crosstalk	vs Frequency	21, 22
	Closed-loop gain and phase	vs Frequency	23, 24, 25, 26
$I_{DD}$	Supply current	vs Supply voltage	27
$P_{D}$	Power dissipation	vs Output power	28



### **TOTAL HARMONIC DISTORTION PLUS NOISE FREQUENCY** THD+N - Total Harmonic Distortion Plus Noise - % 10 $V_{DD} = 1.6 V$ $P_0 = 9.5 \text{ mW}$ $C_B = 1 \mu F$ $R_L = 16 \Omega$ 0.1 0.01 0.001 0.0001 20 100 1 k 10 k 20 k f - Frequency - Hz



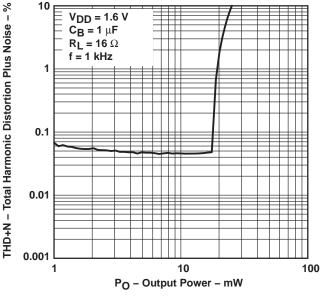
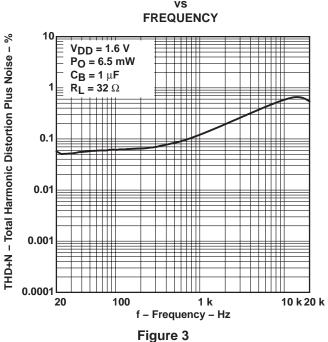


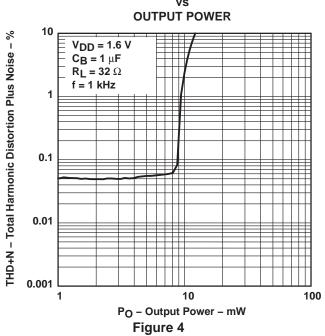
Figure 2

# TOTAL HARMONIC DISTORTION PLUS NOISE

Figure 1



# TOTAL HARMONIC DISTORTION PLUS NOISE

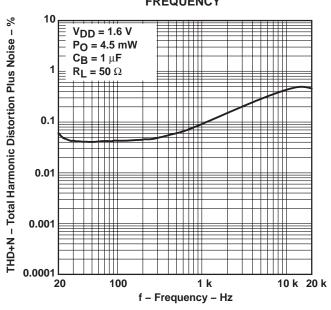




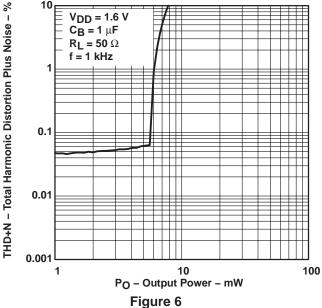
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#### TYPICAL CHARACTERISTICS

# TOTAL HARMONIC DISTORTION PLUS NOISE **FREQUENCY**



 $V_{DD} = 1.6 V$  $C_B = 1 \mu F$  $R_L = 50 \Omega$ f = 1 kHz



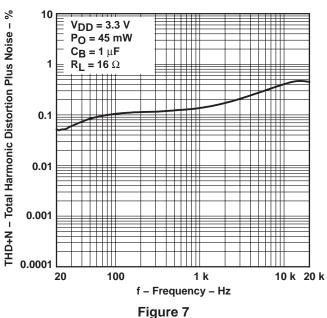
TOTAL HARMONIC DISTORTION PLUS NOISE

**OUTPUT POWER** 

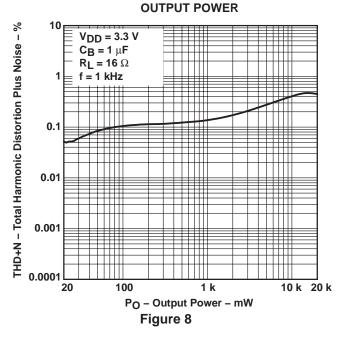
## TOTAL HARMONIC DISTORTION PLUS NOISE

Figure 5



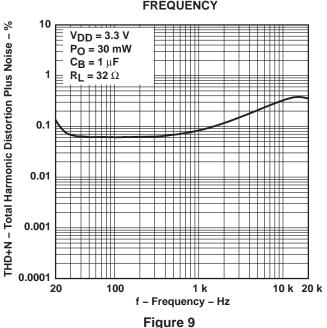


#### TOTAL HARMONIC DISTORTION PLUS NOISE vs

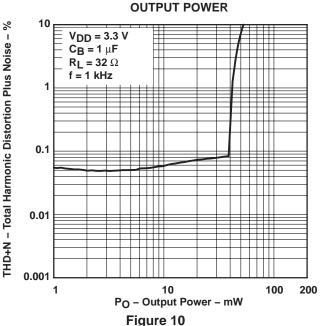




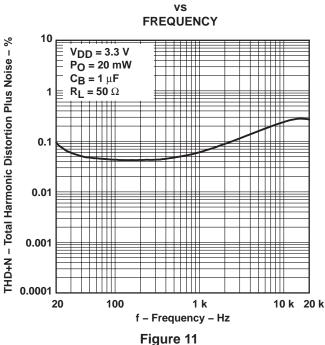
# TOTAL HARMONIC DISTORTION PLUS NOISE **FREQUENCY**



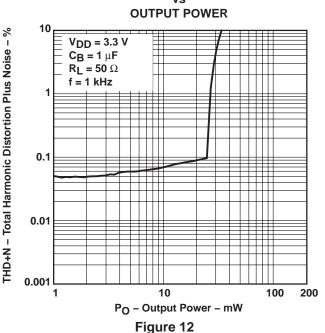
# TOTAL HARMONIC DISTORTION PLUS NOISE



# TOTAL HARMONIC DISTORTION PLUS NOISE



# TOTAL HARMONIC DISTORTION PLUS NOISE





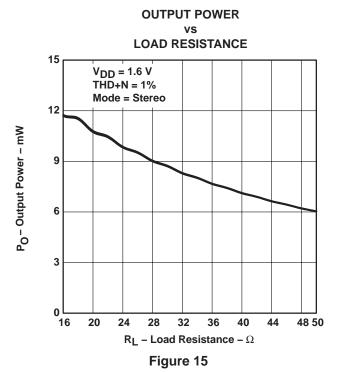
# 

Figure 13

0.2 0.3 0.4 0.5 0.6 0.7

VO - Output Voltage - V

0.8 0.9



# TOTAL HARMONIC DISTORTION PLUS NOISE vs

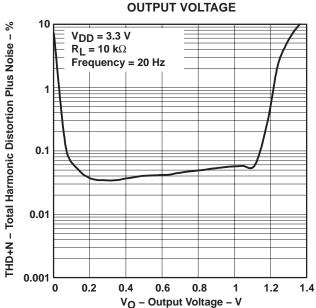


Figure 14

# OUTPUT POWER vs LOAD RESISTANCE

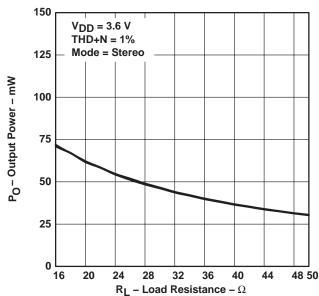


Figure 16



THD+N - Total Harmonic Distortion Plus Noise - %

0.001

0.1

#### SUPPLY RIPPLE REJECTION RATIO **FREQUENCY** 0 V<sub>DD</sub> = 1.6 V -10 k<sub>SVR</sub>- Supply Ripple Rejection Ratio - dB $C_B = 1 \mu F$ -20 $R_L = 32 \Omega$ -30 -40 -50 -60 -70 -80 -90 -100 -110 -120 100 1 k 10 k 20 k 10 f - Frequency - Hz

Figure 17

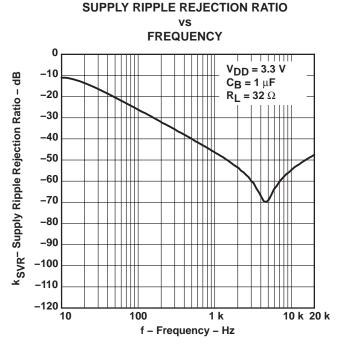
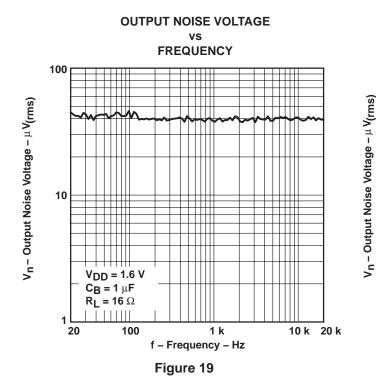


Figure 18

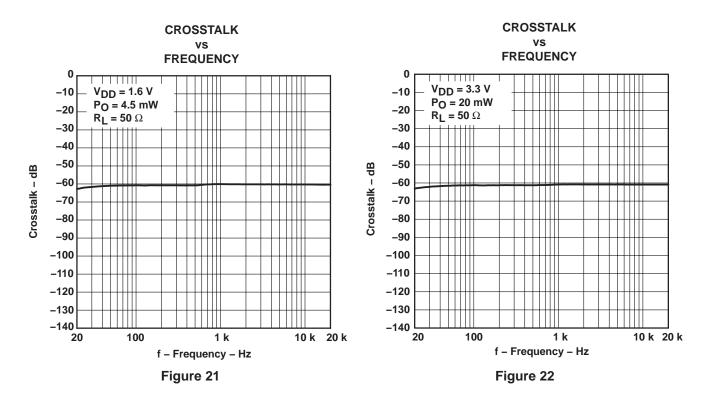
**OUTPUT NOISE VOLTAGE** 



10  $V_{DD} = 3.3 V$  $C_B = 1 \mu F$  $R_L = 16 \Omega$ 

**FREQUENCY** 100 20 100 10 k 20 k 1 k f - Frequency - Hz

Figure 20



#### **CLOSED-LOOP GAIN AND PHASE**

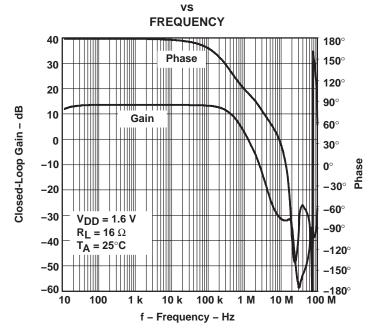


Figure 23



### **CLOSED-LOOP GAIN AND PHASE**

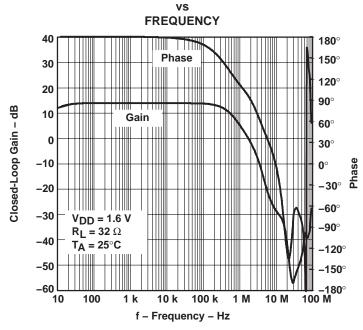


Figure 24

#### **CLOSED-LOOP GAIN AND PHASE**

vs **FREQUENCY** 40 180° **Phase** 150° 30 120° 20 90° Closed-Loop Gain - dB 10 Gain 60° 0 30° -30° Bhase -10 -20 **-60**° -30  $V_{DD} = 3.3 V$ **-90**°  $R_L = 16 \Omega$ -40 T<sub>A</sub> = 25°C –120° -50 –150° —180° 100 M -60 10 100 1 k 10 k 100 k 1 M 10 M f - Frequency - Hz

Figure 25



# CLOSED-LOOP GAIN AND PHASE vs

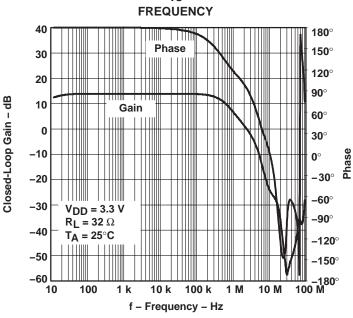
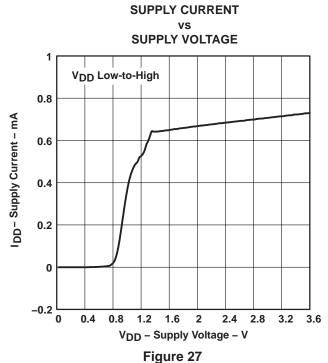


Figure 26

## riguie



OUTPUT POWER

40

VDD = 3.3 V

35

VDD = 3.3 V

30

15

0

10

20

30

40

50

60

70

PO - Output Power - mW

Figure 28

**POWER DISSIPATION** 

TEXAS INSTRUMENTS

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#### APPLICATION INFORMATION

#### input capacitor, CI

In the typical application, an input capacitor ( $C_I$ ) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case,  $C_I$  and  $R_I$  form a high-pass filter with the corner frequency determined in equation 1.  $R_I$  is set internally and is fixed at 20 k $\Omega$ .

$$f_{C} = \frac{1}{2\pi R_{I}C_{I}} \tag{1}$$

The value of  $C_l$  is important to consider, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where the specification calls for a flat bass response down to 20 Hz. Equation 1 is reconfigured as equation 2.

$$C_{l} = \frac{1}{2\pi R_{l} f_{c}} \tag{2}$$

In this example,  $C_I$  is 0.40  $\mu$ F, so one would likely choose a value in the range of 0.47  $\mu$ F to 1  $\mu$ F. A further consideration for this capacitor is the leakage path from the input source through the input network ( $R_I$ ,  $C_I$ ) and the feedback resistor ( $R_F$ ) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at  $V_{DD}/4$ , which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

#### power supply decoupling, CS

The TPA6102A2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1  $\mu$ F, placed as close as possible to the device  $V_{DD}$  lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10  $\mu$ F or greater placed near the power amplifier is recommended.

#### midrail bypass capacitor, CB

The midrail bypass capacitor ( $C_B$ ) serves several important functions. During start-up,  $C_B$  determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 55-k $\Omega$  source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 3 should be maintained.

$$\frac{1}{\left(C_{\mathsf{B}} \times 55 \,\mathrm{k}\Omega\right)} \le \frac{1}{\left(C_{\mathsf{I}} R_{\mathsf{I}}\right)} \tag{3}$$

As an example, consider a circuit where  $C_B$  is 1  $\mu$ F,  $C_I$  is 1  $\mu$ F, and  $R_I$  is 20  $k\Omega$ . Inserting these values into the equation 3 results in: 18.18  $\leq$  50 which satisfies the rule. Bypass capacitor ( $C_B$ ) with values of 0.47- $\mu$ F to 1- $\mu$ F ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.



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# 50-mW ULTRALOW-VOLTAGE, FIXED-GAIN STEREO HEADPHONE AUDIO POWER AMPLIFIER

#### APPLICATION INFORMATION

#### output coupling capacitor, CC

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (CC) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{C} = \frac{1}{2\pi R_{I} C_{C}} \tag{4}$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of C<sub>C</sub> are required to pass low-frequencies into the load. Consider the example where a  $C_C$  of 68  $\mu F$  is chosen and loads vary from 32  $\Omega$  to 47  $k\Omega$ . Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common-Load Impedances vs Low-Frequency Output Characteristics in SE Mode

RL	CC	Lowest Frequency
32 Ω	68 μF	73 Hz
10,000 Ω	68 μF	0.23 Hz
47,000 Ω	68 μF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

The output-coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{\left(C_{\mathsf{B}} \times 55 \,\mathsf{k}\Omega\right)} \le \frac{1}{\left(C_{\mathsf{I}}\mathsf{R}_{\mathsf{I}}\right)} \ll \frac{1}{\mathsf{R}_{\mathsf{L}}\mathsf{C}_{\mathsf{C}}} \tag{5}$$

#### using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

#### 3.3-V versus 1.6-V operation

The TPA6102A2 was designed for operation over a supply range of 1.6 V to 3.6 V. There are no special considerations for 1.6-V versus 3.3-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 0.75 mA (typical) to 0.65 mA (typical). The most important consideration is that of output power. Each amplifier can produce a maxium output voltage swing within a few hundred millivolts of the rails with a 10-k $\Omega$  load. However, this voltage swing decreases as the load resistance decreases and the  $r_{DS(on)}$  as the output stage transistors becomes more significant. For example, for a 32- $\Omega$  load, the maximum peak output voltage with V<sub>DD</sub> = 1.6 V is approximately 0.7 V with no clipping distortion. This reduced voltage swing effectively reduces the maximum undistorted output power.







10-Jun-2014

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6102A2D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6102A2	Samples
TPA6102A2DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6102A2	Samples
TPA6102A2DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJN	Samples
TPA6102A2DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJN	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



#### PACKAGE OPTION ADDENDUM

10-Jun-2014

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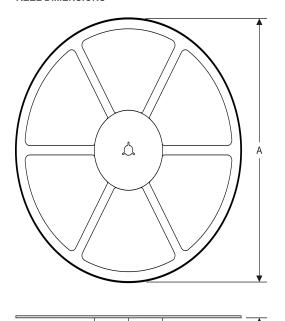
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### PACKAGE MATERIALS INFORMATION

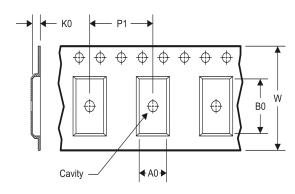
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#### TAPE AND REEL INFORMATION

#### **REEL DIMENSIONS**



#### **TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### TAPE AND REEL INFORMATION

#### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6102A2DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6102A2DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0

# DGK (S-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



## D (R-PDSO-G8)

#### PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



# D (R-PDSO-G8)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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