











TLV2217

SLVS067M-MARCH 1992-REVISED NOVEMBER 2016

TLV2217 Low-Dropout Fixed-Voltage Regulators

Features

- Fixed 1.8-V, 2.5-V, and 3.3-V Outputs
- ±1% Maximum Output Voltage Tolerance at $T_J = 25^{\circ}C$
- 500-mV Maximum Dropout Voltage at 500 mA (3.3-V Option)
- ±2% Output Voltage Variation Across Load and Temperature
- Internal Overcurrent Limiting
- Internal Thermal-Overload Protection
- Internal Overvoltage Protection

Applications

- Electronic Points of Sale
- Medical, Health, and Fitness Applications
- **Printers**
- Appliances and White Goods
- TV Set-Top Boxes

3 Description

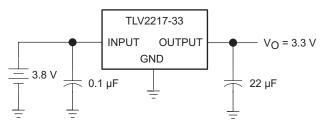
The TLV2217 family of low-dropout regulators offers a variety of fixed-voltage options that offer a maximum continuous input voltage of 16 V, making them more versatile than CMOS regulators. Utilizing a PNP pass element, these regulators are capable of sourcing 500 mA of current, with a specified maximum dropout of 500 mV (3.3-V and 2.5-V options), making these regulators ideal for lowvoltage applications. Additionally, the TLV2217 regulators offer very tight output accuracy of ±2% across operating load and temperature ranges. Other convenient features the regulators provide are overcurrent limiting, thermal-overload internal protection, and overvoltage protection. The TLV2217 family of regulators is available in fixed voltages of 1.8 V, 2.5 V, and 3.3 V.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
TLV2217-xxPW	TSSOP (20)	6.50 mm × 4.40 mm		
TLV2217-xxKVU	TO-252 (2)	6.04 mm × 6.15 mm		
TLV2217-xxKCS	TO-220 (3)	10.16 mm × 9.15 mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

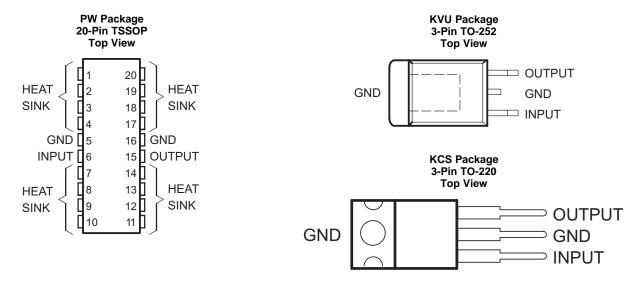
Changes from Revision L (April 2005) to Revision M

Page

•	Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
•	Deleted Ordering Information table; see Package Ordering Addendum at the end of the data sheet	1
•	Changed Junction-to-ambient thermal resistance, R _{θJA} , values in <i>Thermal Information</i> table From: 83°C/W To: 81.6°C/W (PW), From: 28°C/W To: 31°C/W (KVU), and From: 19°C/W To: 22.5°C/W (KCS)	4
•	Changed Junction-to-case (top) thermal resistance, R _{θJC(top)} , values in <i>Thermal Information</i> table From: 32°C/W To: 22.1°C/W (PW), From: 19°C/W To: 37.5°C/W (KVU), and From: 17°C/W To: 34.6°C/W (KCS)	4
•	Changed Junction-to-case (bottom) thermal resistance, R _{θJC(bot)} , values in <i>Thermal Information</i> table From: 1.4°C/W To: 0.6°C/W (KVU) and From: 3°C/W To: 0.8°C/W (KCS)	4



5 Pin Configuration and Functions



Pin Functions

	PIN			1/0	DESCRIPTION			
NAME	PW	KVU	KCS	I/O	DESCRIPTION			
INPUT	6	1	1	I	Voltage input			
OUTPUT	15	3	3	0	Voltage output			
GND	5, 16	2	2	_	Ground			
HEAT SINK	1, 2, 3, 4, 7, 8, 9, 10, 11, 12, 13, 14 17, 18, 19, 20	_	_	_	Connection for improved thermal dissipation. These terminals have an internal resistive connection to ground and must be grounded or electrically isolated.			



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

1 0 1			
	MIN	MAX	UNIT
Continuous input voltage, V _I		16	V
Operating virtual junction temperature, T _J		150	°C
Storage temperature, T _{stg}	-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
\/	Floatroatatio dia abarra	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	\/
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _I	Input voltage	3 ⁽¹⁾	12	V
Io	Output current	0	500	mA
TJ	Operating virtual junction temperature	0	125	င့

⁽¹⁾ Minimum V_I is equal to 3.0 V or $V_O(max)$ + 0.5 V, whichever is greater.

6.4 Thermal Information

			TLV2217				
	THERMAL METRIC ⁽¹⁾⁽²⁾	PW (TSSOP)	KVU (TO-252)	KCS (TO-220)	UNIT		
		20 PINS	3 PINS	3 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.6	31	22.5	°C/W		
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.1	37.5	34.6	°C/W		
$R_{\theta JB}$	Junction-to-board thermal resistance	32	11.3	8.8	°C/W		
ΨЈТ	Junction-to-top characterization parameter	0.9	1.9	3	°C/W		
ΨЈВ	Junction-to-board characterization parameter	31.5	11.2	7.8	°C/W		
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	_	0.6	8.0	°C/W		

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

⁽²⁾ Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.



6.5 Electrical Characteristics: TLV2217-33

 $V_1 = 4.5 \text{ V}$, $I_0 = 500 \text{ mA}$, $T_1 = 25^{\circ}\text{C}$, and over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CON	TEST CONDITIONS ⁽¹⁾				UNIT
On touch and the same	$I_0 = 20 \text{ mA to } 500 \text{ mA},$	$T_J = 25^{\circ}C$	3.267	3.3	3.333	V
Output voltage	$V_1 = 3.8 \text{ V to } 5.5 \text{ V}$	$T_J = 0$ °C to 125°C	3.234		3.336	V
Input voltage regulation	V _I = 3.8 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz, V _{ripple} = 1 V _{PP} V _I	= 4.5 V		-62		dB
Output voltage regulation	I _O = 20 mA to 500 mA	I _O = 20 mA to 500 mA				mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dranaut valtage	I _O = 250 mA	I _O = 250 mA			400	mV
Dropout voltage	I _O = 500 mA				500	IIIV
B:	I _O = 0 mA	I _O = 0 mA			5	A
Bias current	I _O = 500 mA	I _O = 500 mA				mA

⁽¹⁾ Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor, with equivalent series resistance of 1.5 Ω, on the output.

6.6 Electrical Characteristics: TLV2217-25

 $V_1 = 3.3 \text{ V}$, $I_0 = 500 \text{ mA}$, $T_1 = 25 ^{\circ}\text{C}$, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CON	TEST CONDITIONS ⁽¹⁾			MAX	UNIT
	$I_{O} = 20 \text{ mA to } 500 \text{ mA},$	$T_J = 25^{\circ}C$	2.475	2.4	2.525	V
Output voltage	$V_1 = 3.8 \text{ V to } 5.5 \text{ V}$	$T_J = 0$ °C to 125°C	2.45		2.55	V
Input voltage regulation	V _I = 3.8 V to 5.5 V			4	12	mV
Ripple rejection	f = 120 Hz, V _{ripple} = 1 V _{PP} V	f = 120 Hz, V _{ripple} = 1 V _{PP} V _I = 4.5 V				dB
Output voltage regulation	I _O = 20 mA to 500 mA			4	23	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I _O = 250 mA	I _O = 250 mA			400	m\/
Dropout voltage	I _O = 500 mA	I _O = 500 mA				mV
Diagram of	I _O = 0 mA	$I_O = 0 \text{ mA}$			5	
Bias current	I _O = 500 mA			19	49	mA

⁽¹⁾ Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor, with equivalent series resistance of 1.5 Ω, on the output.

6.7 Electrical Characteristics: TLV2217-18

 $V_{L} = 3.3 \text{ V}$, $I_{C} = 500 \text{ mA}$, $T_{L} = 25 ^{\circ}\text{C}$, and over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CON	TEST CONDITIONS ⁽¹⁾			MAX	UNIT
Output voltage	$I_0 = 20 \text{ mA to } 500 \text{ mA},$	$T_J = 25^{\circ}C$	1.782	1.8	1.818	18 V
Output voltage	$V_1 = 3.8 \text{ V to } 5.5 \text{ V}$	$T_J = 0$ °C to 125°C	1.764		1.836	V
Input voltage regulation	$V_1 = 3.8 \text{ V to } 5.5 \text{ V}$	•		3	9	mV
Ripple rejection	f = 120 Hz, V _{ripple} = 1 V _{PP}	f = 120 Hz, V _{ripple} = 1 V _{PP} V _I = 4.5 V				dB
Output voltage regulation	I _O = 20 mA to 500 mA	I _O = 20 mA to 500 mA			17	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Drangut voltage	$I_0 = 250 \text{ mA}$	I _O = 250 mA				m\/
Dropout voltage	$I_O = 500 \text{ mA}$	I _O = 500 mA				mV
	$I_O = 0 \text{ mA}$	I _O = 0 mA			5	A
Bias current	I _O = 500 mA	I _O = 500 mA				mA

⁽¹⁾ Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor, with equivalent series resistance of 1.5 Ω, on the output.

²⁾ Dropout voltage is limited by the input voltage range, with minimum $V_1 = 3 \text{ V}$.



6.8 Typical Characteristics

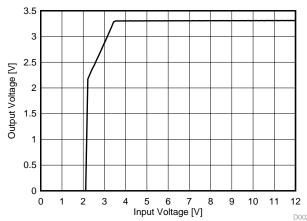


Figure 1. TLV2217-33 Output Voltage vs Input Voltage



7 Detailed Description

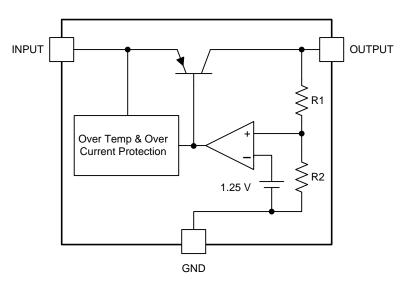
7.1 Overview

The TLV2217 device is a positive low-dropout voltage regulator designed to provide up to 500 mA of output current. The device is available in 1.8-V, 2.5-V, and 3.3-V options. All internal circuitry is designed to operate down to 0.5-V input-to-output differential, with the minimum input voltage of 3 V for all voltage options.

The TLV2217 device is designed to be stable with tantalum and aluminum electrolytic output capacitors having an ESR between 0.4 Ω and 2 Ω .

The TLV2217 device is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Overload Block

Current limiting and overtemperature shutdown protects against overload by turning off the PNP pass element.

7.4 Device Functional Modes

7.4.1 Operation With Low Input Voltage

The TLV2217 device requires 0.5-V headroom $(V_I - V_O)$ to operate in regulation. With less headroom, the device may drop out and OUTPUT voltage is INPUT voltage minus dropout voltage.

7.4.2 Operation at Light Loads

The load or feedback must consume the minimum bias current defined in *Electrical Characteristics: TLV2217-33* for regulation, or the output may be too high.

7.4.3 Operation in Self Protection

When an overload occurs, the device shuts down the output stage or reduce the output current to prevent device damage. The device automatically resets from the overload. The output may be reduced or alternate between on and off until the overload is removed.



8 Application and Implementation

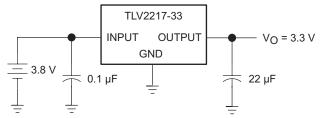
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV2217 is a low-dropout linear regulator and can be used as a fixed output voltage supply for a wide variety of applications up to 500 mA. The TLV2217 has multiple output voltage options including 1.8 V, 2.5 V, and 3.3 V. The TLV2217 requires a minimum of 3 V or $(V_{O(max)} + 0.5 \text{ V})$ input to ensure regulation and is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

8.2 Typical Application



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Figure 2. Typical Application Schematic

8.2.1 Design Requirements

The input voltage must be high enough so that there is enough headroom for the output to regulate. This specification is defined as the dropout voltage in the *Electrical Characteristics: TLV2217-33*.

A 0.1-µF capacitor must be place on the input to stabilize the input supply, especially if the TLV2217 is not placed near the source of supply.

Output capacitor selection is critical for regulator stability. Larger C_{OUT} values benefit the regulator by improving transient response and loop stability. This device is designed to be stable with tantalum and aluminum electrolytic output capacitors having an ESR between 0.4 Ω and 2 Ω . See *Compensation-Capacitor Selection Information* for additional details regarding capacitor selection.

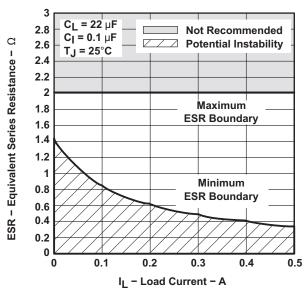
8.2.2 Detailed Design Procedure

8.2.2.1 Compensation-Capacitor Selection Information

The TLV2217 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figure 3 and Figure 4 can be used to establish the capacitance value and ESR range for the best regulator performance.



Typical Application (continued)



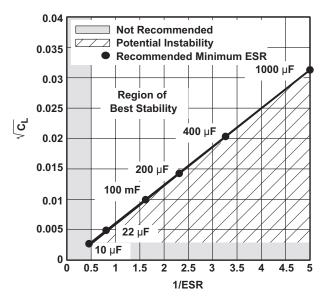


Figure 3. TLV2217 ESR of Output Capacitor vs Load Current

Figure 4. TLV2217 Stability vs ESR

8.2.2.2 High Start-up Current

Due to the structure of the TLV2217, a high peak current is required on start-up. See Figure 5 for the input current characteristic.

NOTE

When the TLV2217 is starting up, it has to overcome the peak current to start regulating at the output. Due to the peak current required for the TLV2217, a resistor connected in series with the input is not recommended, as the I*R drop across the resistor may cause the input voltage to drop below the required headroom for the device.

8.2.3 Application Curves

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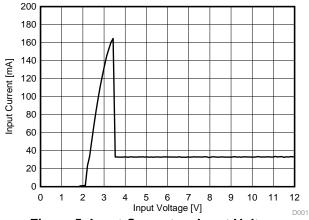


Figure 5. Input Current vs Input Voltage



9 Power Supply Recommendations

See Recommended Operating Conditions for the recommended supply voltage range.

10 Layout

10.1 Layout Guidelines

See Figure 6 for an example layout for the TLV2217 using the TO-220 package. Input and output bypass capacitors must be placed as close to the device pins as possible. The output capacitor must have a specified ESR in the range defined by Figure 4. Additionally, the ground pin and thermal tab must be well connected to a ground plane to aid in thermal dissipation.

10.2 Layout Example

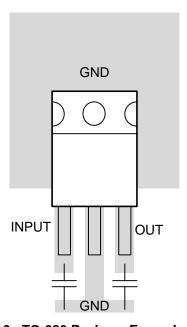


Figure 6. TO-220 Package Example Layout

Submit Documentation Feedback



11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.





18-Mar-2016

PACKAGING INFORMATION

Orderable Device	Status	Package Type		Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TLV2217-18KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TLV2217-18	Samples
TLV2217-18KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TLV2217-18	Samples
TLV2217-18KTPR	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI	0 to 125	2217-18	
TLV2217-18KTPRG3	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI	0 to 125		
TLV2217-18KVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	2217-18	Samples
TLV2217-25KC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	0 to 125	TLV2217-25	
TLV2217-25KCE3	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	0 to 125	TLV2217-25	
TLV2217-25KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TLV2217-25	Samples
TLV2217-25KTPR	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI	0 to 125	2217-25	
TLV2217-25KTPRG3	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI	0 to 125		
TLV2217-25KVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	2217-25	Samples
TLV2217-25PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	2217-25	Samples
TLV2217-33KC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	0 to 125	TLV2217-33	
TLV2217-33KCE3	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	0 to 125	TLV2217-33	
TLV2217-33KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TLV2217-33	Samples
TLV2217-33KTPR	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI	0 to 125	2217-33	
TLV2217-33KTPRG3	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI	0 to 125		
TLV2217-33KVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	2217-33	Samples
TLV2217-33PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	2217-33	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.



PACKAGE OPTION ADDENDUM

18-Mar-2016

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

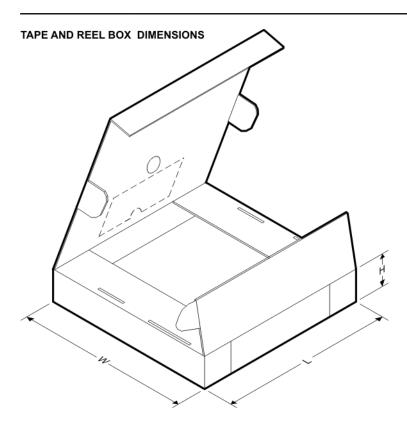
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2217-18KVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV2217-25KVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV2217-25PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLV2217-33KVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV2217-33PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

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*All dimensions are nominal

All differentiates are normal										
Device	Package Type	Package Drawing	Pins SPQ		Length (mm)	Width (mm)	Height (mm)			
TLV2217-18KVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0			
TLV2217-25KVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0			
TLV2217-25PWR	TSSOP	PW	20	2000	367.0	367.0	38.0			
TLV2217-33KVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0			
TLV2217-33PWR	TSSOP	PW	20	2000	367.0	367.0	38.0			

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



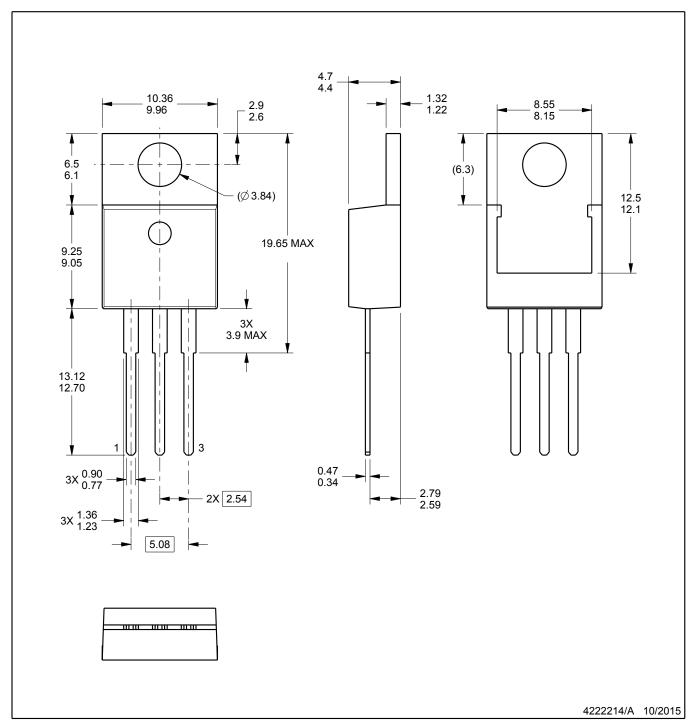
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153





TO-220

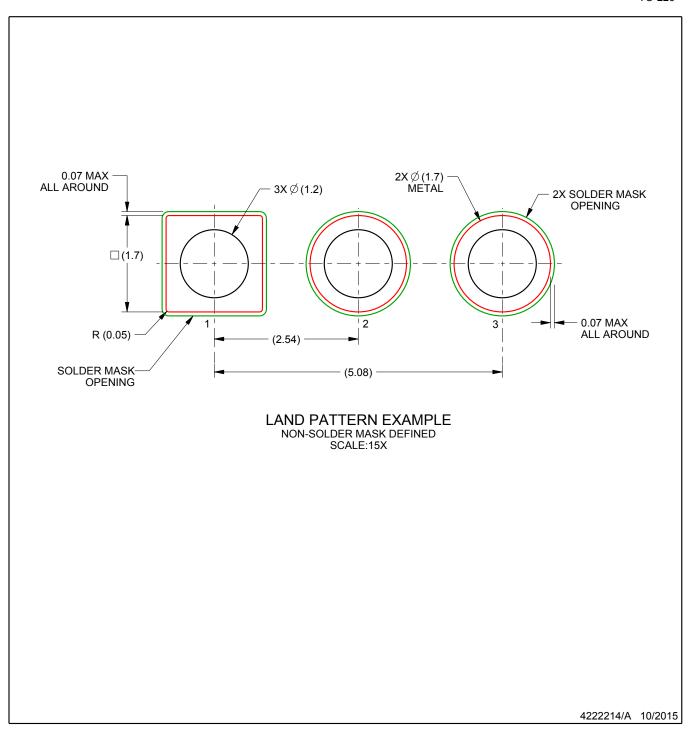


NOTES:

- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 Reference JEDEC registration TO-220.

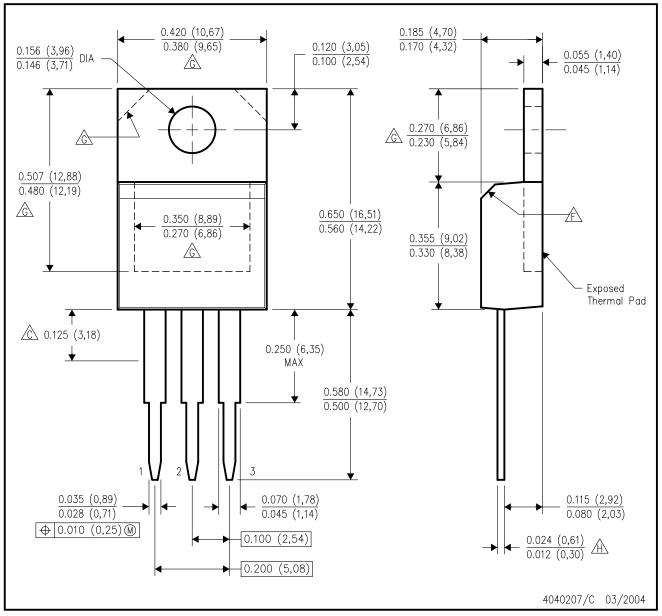


TO-220



KC (R-PSFM-T3)

PLASTIC FLANGE-MOUNT PACKAGE



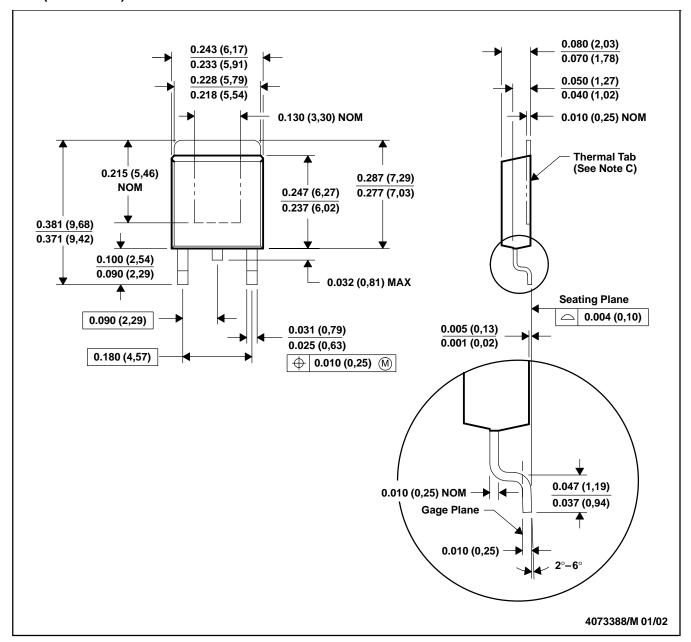
NOTES: A. All linear

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- The chamfer is optional.
- Thermal pad contour optional within these dimensions.
- Falls within JEDEC TO-220 variation AB, except minimum lead thickness.



KTP (R-PSFM-G2)

PowerFLEX™ PLASTIC FLANGE-MOUNT PACKAGE



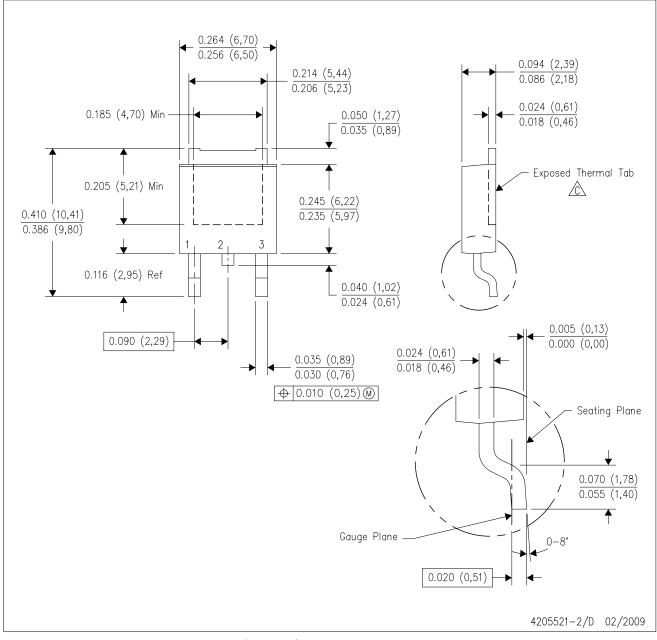
- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. The center lead is in electrical contact with the thermal tab.
 - D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
 - E. Falls within JEDEC TO-252 variation AC.

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KVU (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- The center lead is in electrical contact with the exposed thermal tab.
- D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
- E. Falls within JEDEC TO-252 variation AA.



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