Three-Port HDMI Switch

Check for Samples: TMDS361B

FEATURES

- **3:1 Sink-side switch Supporting DVI Above 1920 × 1200 and HDMI HDTV Resolutions up to 1080p With 16-Bit Color Depth**
- **Designed for Signaling Rates up to 3 Gbps**
- **Supports HDMI 1.3a Specification**
- **Adaptive Equalization on inputs to support up to 20-m HDMI Cable at 2.25 Gbps for 1080p 12-Bit Color Depth**
- **TMDS Input Clock-Detect Circuit**
- **DDC Repeater Function**
- **<2-mW Low-Power Mode**
- **Local I^2C or GPIO Configurable**
- **Enhanced ESD. HBM: 10 kV on All Input TMDS, DDC I^2C, HPD Pins**
- **3.3-Volt Power Supply**
- **Temperature Range: 0°C to 70°C**
- **64-Pin TQFP Package: Pin-Compatible With TMDS351**
- **Robust TMDS Receive Stage That Can Work With Non-Compliant Input Common-Mode HDMI Signal**

APPLICATIONS

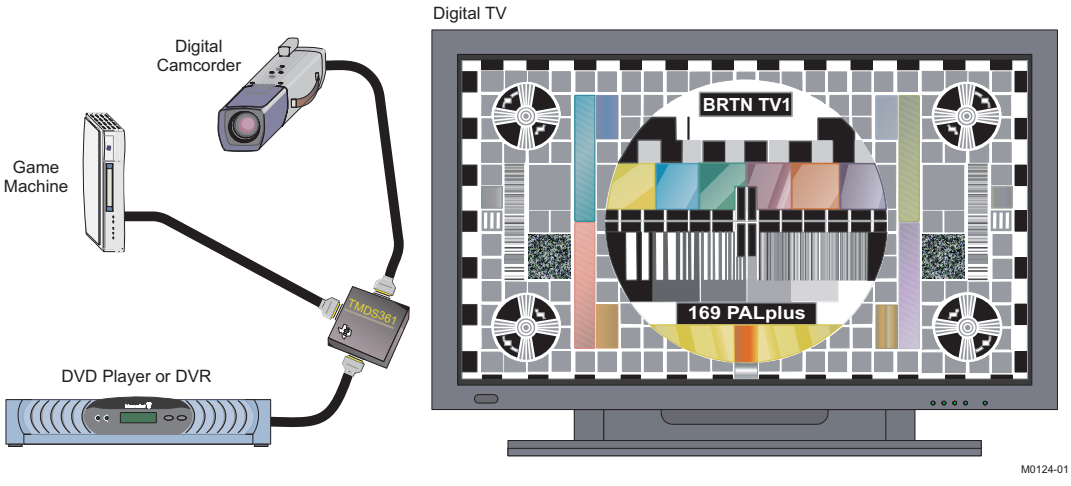
- **High-Definition Digital TV**
  - **LCD**
  - **Plasma**
  - **DLP®**

DESCRIPTION

The TMDS361B is a three-port digital video interface (DVI) or high-definition multimedia interface (HDMI) switch that allows up to three DVI or HDMI ports to be switched to a single display terminal. Four TMDS channels, one hot-plug detector, and a digital display control (DDC) interface are supported on each port. Each TMDS channel supports signaling rates up to 3 Gbps to allow 1080p resolution in 16-bit color depth. TMDS361B is not intended for source side applications such as external switch boxes.

The TMDS361B provides an adaptive equalizer for different ranges of cable lengths. The equalizer automatically compensates for intersymbol interference [ISI] loss of an HDMI/DVI cable for up to 20 dB at 3 Gbps. (see Figure 15).

TYPICAL APPLICATION



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DLP is a registered trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

When any of the input ports are selected, the integrated terminations (50-Ω termination resistors pulled up to VCC) are switched on for the TMDS clock channel, the TMDS clock-detection circuit is enabled, and the DDC repeater is enabled. After a valid TMDS clock is detected, the integrated termination resistors for the data lines are enabled, and the output TMDS lines are enabled. When an input port is not selected, the integrated terminations are switched off, the TMDS receivers are disabled, and the DDC repeater is disabled. Clock-detection circuitry provides an automatic power-management feature, because if no valid TMDS clock is detected, the terminations on the input TMDS data lines are disconnected and the TMDS outputs are placed in a high-impedance state.

The TMDS361B is designed to be controlled via a local I^2C interface or GPIO interface based on the status of the I2C_SEL pin. The local I^2C interface in TMDS361B is a slave-only I^2C interface. (See the I2C INTERFACE NOTES section.)

I^2C Mode: When the I2C_SEL pin is set low, the device is in I^2C mode. With local I^2C, the interface port status can be read and the advanced configurations of the device such as TMDS output edge rate control, DDC I^2C buffer output-voltage-select (OVS) settings (See the DDC I2C Function Description for detailed description on DDC I^2C buffer description and OVS description), device power management, TMDS clock-detect feature, and TMDS input-port selection can be set. See Table 8 through Table 11.

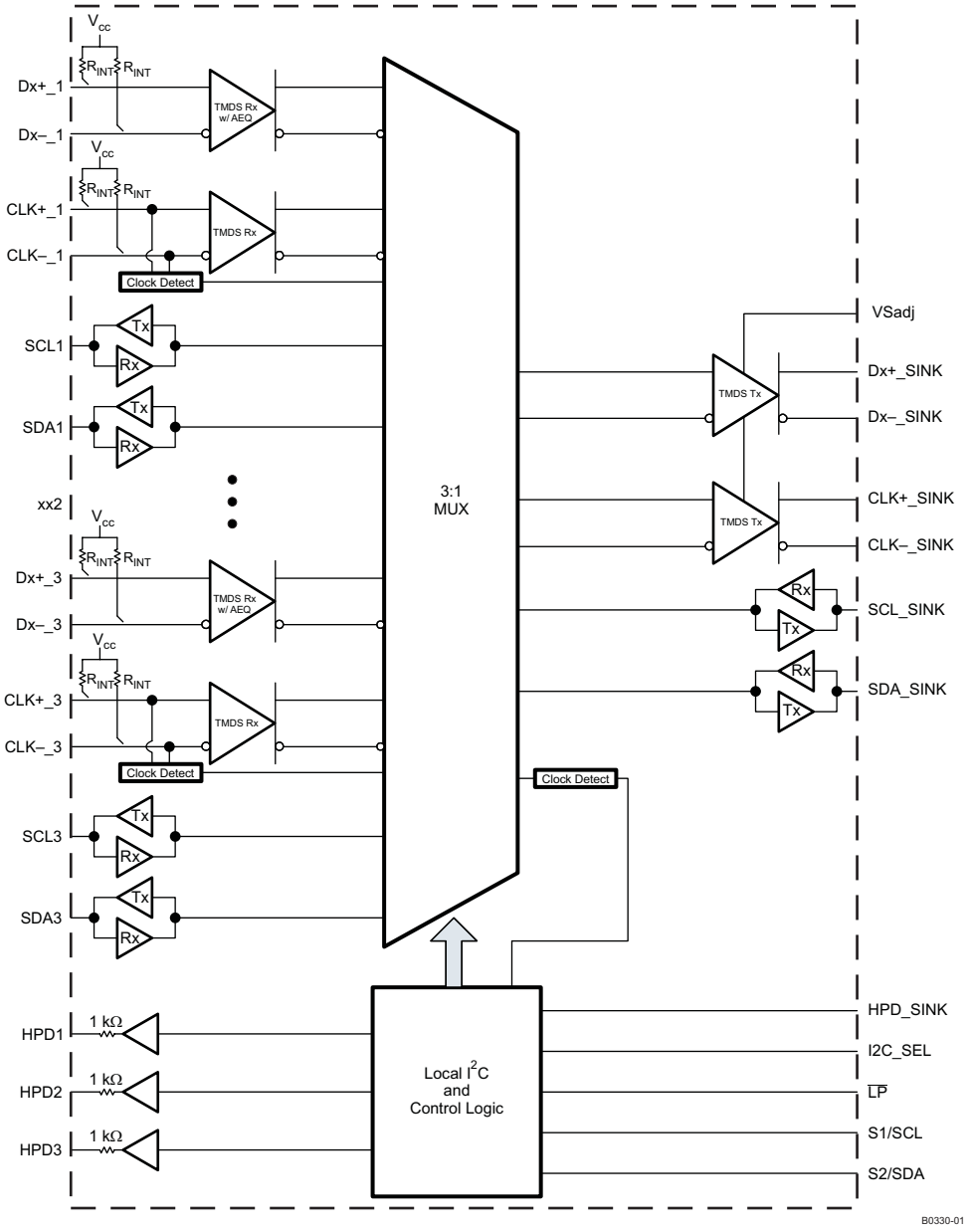
GPIO mode: When the I2C_SEL pin is set high, the device is in GPIO control mode. The port selection is controlled with source selectors, S1 and S2. The power-saving mode is controlled through the $\overline{LP}$ pin. In GPIO mode, the default TMDS output edge rate that is the fastest setting of rise and fall time is set, and the default DDC I^2C buffer OVS setting (OVS3) is set. See Table 8 and the DDC I2C Function Description for a detailed description of the DDC I^2C buffer.

Following are some of the key features (advantages) that TMDS361B provides to the overall sink-side system (HDTV).

- 3×1 switch that supports TMDS data rates up to 3 Gbps on all three input ports
- ESD: Built-in support for high ESD protection (up to 10 kV on the HDMI source side). The HDMI source-side pins on the TMDS361B are connected via the HDMI/DVI exterior connectors and cable to the HDMI/DVI sources (e.g., DVD player). In TV applications, it can be expected that the source side may be subjected to higher ESD stresses compared to the sink side that is connected internally to the HDMI receiver.
- Adaptive equalization: The built-in adaptive equalization support compensates for intersymbol interference [ISI] loss of up to 20 dB, which represents a typical 20-m HDMI/DVI cable at 3 Gbps. Adaptive equalization adjusts the equalization gain **automatically**, based on the cable length and the incoming TMDS data rate.
- TMDS clock-detect circuitry: This feature provides an automatic power-management feature and also ensures that the TMDS output port is turned on only if there is a valid TMDS input signal. TMDS clock-detect feature can be bypassed in I^2C mode; see Table 10 and Table 11. It is recommended to enable the TMDS clock-detect circuitry during normal operation. However, for HDMI compliance testing (TMDS termination-voltage test), the clock-detect feature should be disabled by using the I^2C mode control. If the customer requires passing the TMDS termination-voltage test in GPIO mode with the default TMDS clock-detect circuitry enabled, then a valid TMDS clock should be provided for this compliace test, so that the terminations on the TMDS data pair can be connected, and thus customer can pass the TMDS termination-voltage test.
- DDC I^2C buffer: This feature provides isolation on the source side and sink side DDC I^2C capacitance, thus helping the sink system to pass system-level compliance.
- Robust TMDS receive stage: This feature ensures that the TMDS361B can work with TMDS input signals having common-mode voltage levels that can be either compliant or non-compliant with HDMI/DVI specifications.
- VSadj: This feature adjusts the TMDS output swing and can help the sink system to tune the output TMDS swing of the TMDS361B (if needed) based on the system requirements.
- GPIO or local I^2C interface to control the device features
- TMDS output edge-rate control: This feature adjusts the TMDS361B TMDS output rise and fall times. There

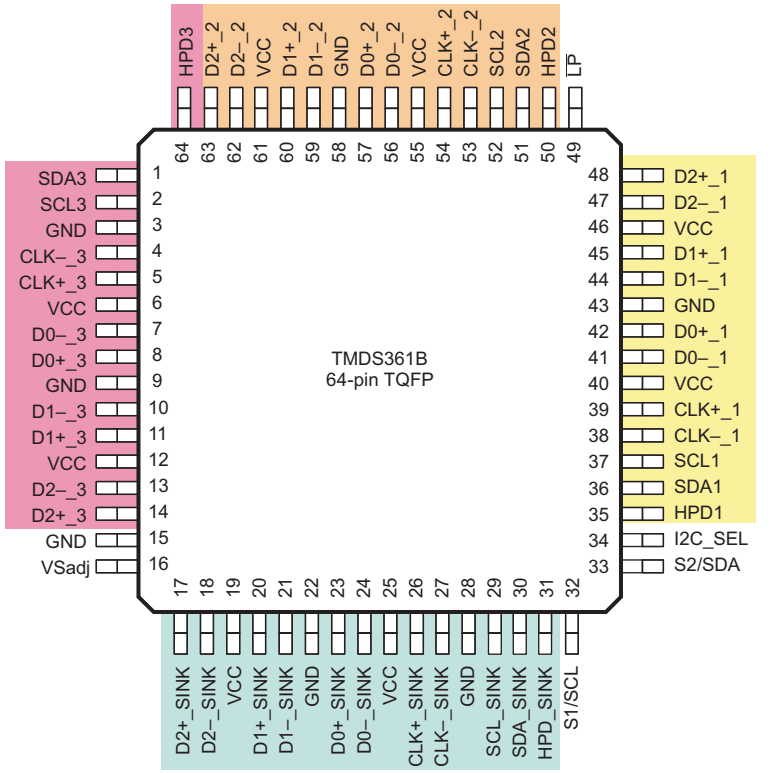
are four settings of the rise and fall times that can be chosen. The default setting is the fastest rise and fall time; the other three settings are slower. Slower edge transitions can potentially help the sink system (HDTV) in passing regulatory EMI compliance.

FUNCTIONAL BLOCK DIAGRAM



PAG PACKAGE

PAG-64
(Top View)



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PIN FUNCTIONS

PIN		I/O	DESCRIPTION
SIGNAL	NO.		
TMDS INPUT PINS			
CLK+_1 CLK–_1	39 38	I	Port-1 TMDS differential clock
D[0:2]+_1 D[0:2]–_1	42, 45, 48 41, 44, 47	I	Port-1 TMDS differential data inputs
CLK+_2 CLK–_2	54 53	I	Port-2 TMDS differential clock
D[0:2]+_2 D[0:2]–_2	57, 60, 63 56, 59, 62	I	Port-2 TMDS differential data inputs
CLK+_3 CLK–_3	5 4	I	Port-3 TMDS differential clock
D[0:2]+_3 D[0:2]–_3	8, 11, 14 7, 10, 13	I	Port-3 TMDS differential data inputs
TMDS OUTPUT PINS			
CLK+_SINK CLK–_SINK	26 27	O	TMDS sink differential clock
D[0:2]+_SINK D[0:2]–_SINK	23, 20, 17 24, 21, 18	O	TMDS sink differential data outputs
HOT-PLUG-DETECT STATUS PINS			
HPD[1:3]	35, 50, 64	O	Source port hot-plug-detect output
HPD_SINK	31	I	Sink hot-plug-detect input
DDC PINS			
SCL[1:3]	37, 52, 2	I/O	TMDS port bidirectional DDC clock
SDA[1:3]	36, 51, 1	I/O	TMDS port bidirectional DDC data
SCL_SINK	29	I/O	TMDS sink-side bidirectional DDC clock
SDA_SINK	30	I/O	TMDS sink-side bidirectional DDC data
CONTROL PINS			
$\overline{LP}$	49	I	Low-power select bar
I2C_SEL	34	I	GPIO/local I^2C control select
S1/SCL	32	I	Source select 1(GPIO) / local I^2C clock (I2C)
S2/SDA	33	I/O	Source select 2 (GPIO) / local I^2C data (I2C)
VSadj	16	I	TMDS-compliant voltage swing control
SUPPLY AND GROUND PINS			
VCC	6, 12, 19, 25, 40, 46, 55, 61		3.3-V supply
GND	3, 9, 15, 22, 28, 43, 58		Ground

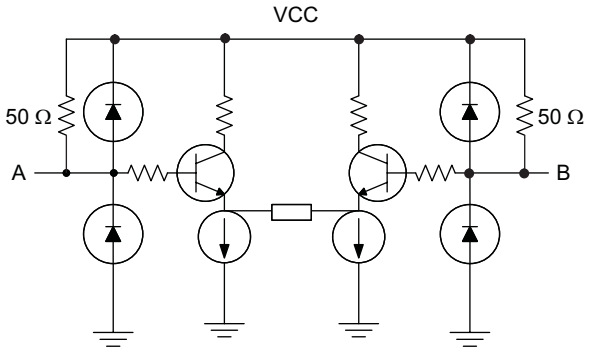
Table 1. Source Selection Lookup(1)

CONTROL PINS		I/O SELECTED		HOT-PLUG DETECT STATUS			Power Mode
S2	S1	Port Selected	SCL_SINK SDA_SINK	HPD1	HPD2	HPD3	
H	H	Port 1 Terminations of port 2 and port 3 are disconnected.	SCL1 SDA1	HPD_SINK	L	L	Normal mode
H	L	Port 2 Terminations of port 1 and port 3 are disconnected.	SCL2 SDA2	L	HPD_SINK	L	Normal mode
L	L	Port 3 Terminations of port 1 and port 2 are disconnected.	SCL3 SDA3	L	L	HPD_SINK	Normal mode
L	H	None (Z) All terminations are disconnected.	None (Z) Are pulled HIGH by external pullup termination	HPD_SINK	HPD_SINK	HPD_SINK	Standby mode

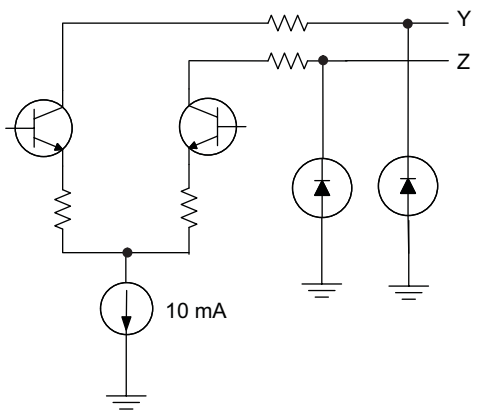
(1) H: Logic high; L: Logic low; X: Don't care; Z: High impedance

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

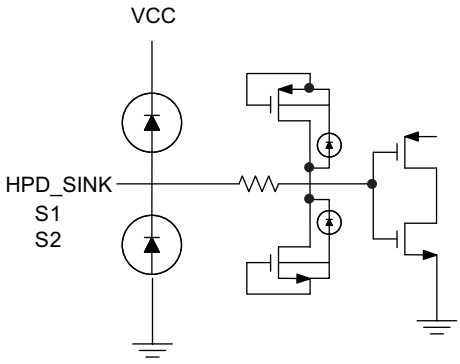
TMDS Input Stage



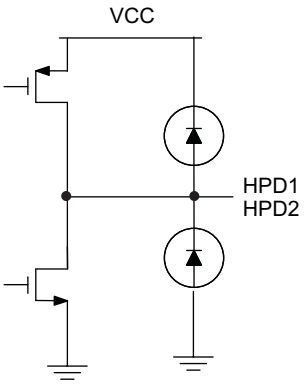
TMDS Output Stage



Status and Source Selector



HPD Output Stage



DDC Buffer

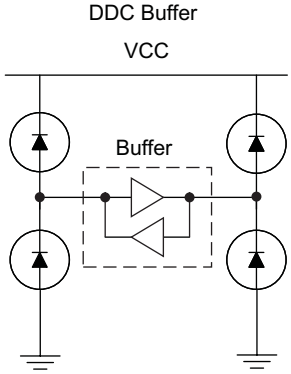


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Table 2. Control-Pin Lookup Table(1)

SIGNAL	LEVEL		STATE	DESCRIPTION
$\overline{LP}$	H		Normal mode	Normal operational mode for device. If $\overline{LP}$ is left floating, then a weak internal pullup to VCC pulls it to VCC.
	L		Low-power mode	Device is forced into a low-power state, causing the inputs and outputs to go to a high-impedance state. All other inputs are ignored.
S[2:1] GPIO mode	**S2**	**S1**		
	H	H	Port 1	Port 1 is selected as the active port; all other ports are low.
	H	L	Port 2	Port 2 is selected as the active port; all other ports are low.
	L	L	Port 3	Port 3 is selected as the active port; all other ports are low.
	L	H	HPD[1:3] follow HPD_SINK	Standby mode: HPD[1:3] follow HPD_sink.
I2C_SEL	L		I^2C	Device is configured by I^2C logic.
	H		GPIO	Device is configured by GPIO. If the I2C_SEL pin is left floating, then a weak internal pullup to VCC pulls the I2C_SEL pin high.
VSadj	4.02 kΩ		Compliant voltage	Driver output voltage swing precision control to aid with system compliance. The VSadj resistor value can be selected to be 4.02 kΩ ±10% based on the system requirement to pass HDMI compliance.

(1) (H) Logic high; (L) Logic low

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
TMDS361BPAGR	TMDS361B	64-pin TQFP reel (large)
TMDS361BPAG	TMDS361B	64-pin TQFP tray

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage range(2)	VCC	–0.3 to 3.6	V
Voltage range	TMDS I/O	–0.3 to 4	V
	HPD and DDC I/O	–0.3 to 5.5	
	Control and status I/O	–0.3 to 5.5	
Electrostatic discharge	Human body model(3) on SCL[1:3], SDA[1:3], HPD[1:3], D[0:2]+_[1:3], D[0:2]–_[1:3], CLK+_[1:3], CLK–_[1:3] pins	±10,000	V
	Human body model(3) on all other pins	±9,000	
	Charged-device model(4)	±1500	
	Machine model(5)	±200	
	IEC 61000-4-2(6), contact discharge	±8,000	
	IEC 61000-4-2(6), air discharge	±15,000	
Continuous power dissipation		See Dissipation Ratings table	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A
(6) Tested in accordance with IEC EN 61000-4-2

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \le 25°C$	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
64-pin TQFP (PAG)	Low-K	1066 mW	10.66 mW/°C	586 mW
	High-K	1481 mW	14.8 mW/°C	814 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance			37.13		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			15.3		°C/W
$P_{D(1)}$	Device power dissipation in normal mode	$\overline{LP}$ = HIGH, TMDS: $V_{ID(pp)}$ = 1200 mV, 3 Gbps TMDS data pattern; HPD_SINK = HIGH, S1/S2 = LOW/LOW, LOW/HIGH, HIGH/HIGH		560	780	mW
$P_{D(2)}$	Device power dissipation in standby mode	$\overline{LP}$ = HIGH, TMDS: $V_{ID(pp)}$ = 1200 mV, 3 Gbps TMDS data pattern; HPD_SINK = HIGH, S1 = HIGH, S2 = LOW		10	20	mW
P_{SD}	Device power dissipation in low-power mode	$\overline{LP}$ = LOW		1	2	mW
P_{NCLK}	Device power dissipation in normal mode with no active TMDS input clock	$\overline{LP}$ = HIGH, no TMDS input clock, HPD_SINK =HIGH, S1/S2 = LOW/LOW, LOW/HIGH, HIGH/HIGH		40	65	mW
T_J	Junction Temperature		0		125	°C

(1) The maximum rating is simulated under 3.6-V VCC across worst-case temperature and process variation. Typical conditions are simulated at 3.3-V VCC, 25°C with nominal process material.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	0		70	°C
TMDS DIFFERENTIAL OUTPUT AND INPUT PINS					
$V_{ID(pp)}$	Peak-to-peak input differential voltage	0.15		1.56	V
V_{IC}	Input common-mode voltage	VCC – 0.4		VCC + 0.01	V
$t_{IN\_Rise\_Fall}$	TMDS input rise and fall time	75			ps
V_{IN_PRE}	Acceptable pre-emphasis on TMDS input signals. Note that an input signal into TMDS361B with longer pre-emphasis duration and/or larger pre-emphasis amplitude could result in over-equalization.	See (Figure 26)			
AVCC	TMDS output termination voltage	3	3.3	3.6	V
d_R	Data rate			3	Gbps
R_{VSadj}	Resistor for TMDS-compliant voltage output swing	3.66	4.02	4.47	kΩ
R_T	Termination resistance	45	50	55	Ω
DDC PINS					
V_I	Input voltage	0		5.5	V
$d_{R(I2C)}$	I^2C data rate			100	Kbps
HPD AND CONTROL PINS					
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V

DEVICE POWER

The TMDS361B is designed to operate from a single 3.3-V supply voltage. The TMDS361B has three power modes of operation. These three modes are referred to as normal mode, standby mode, and low-power mode.

Normal mode is designed to be used during typical operating conditions. In normal mode, the device is fully functional and consumes the greatest amount of power.

Standby mode is designed to be used when reduced power is desired, but DDC and HPD communication must be maintained. Standby mode can be enabled via the I^2C interface (See Table 8 through Table 11) or GPIO interface (See Table 1). In standby mode, the high-speed TMDS data and clock channels are disabled to reduce power consumption. The internal I^2C logic and DDC function normally. HPD[1:3] follow HPD_SINK.

Low-power mode is designed to consume the least possible amount of power while still applying 3.3 V to the device. Low-power mode can be enabled by either the $\overline{LP}$ pin or by local I^2C (See Table 8 through Table 11). In low-power mode, all of the inputs and outputs are disabled with the exception of the internal I^2C logic and $\overline{LP}$ pin.

The clock-detect feature in the TMDS361B provides an automatic power-management feature in normal mode. If no valid TMDS clock is detected, the terminations on the input TMDS data lines are disconnected, and the TMDS outputs are high-Z. As soon as a valid TMDS clock is detected, the terminations on the TMDS data lines are connected, the TMDS outputs come out of high-Z, and the device is fully functional and consumes the greatest amount of power.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Normal-mode supply current	$\overline{LP}$ = HIGH, TMDS: $V_{ID(pp)}$ = 1200 mV, 3 Gbps TMDS data pattern; HPD_SINK = HIGH, S1/S2 = LOW/LOW, LOW/HIGH, HIGH/HIGH		170	216	mA
I_{STBY}	Standby supply current	$\overline{LP}$ = HIGH, TMDS: $V_{ID(pp)}$ = 1200 mV, 3 Gbps TMDS data pattern; HPD_SINK = HIGH, S1 = HIGH, S2 = LOW		3	5.5	mA
I_{SD}	Shutdown current	$\overline{LP}$ = LOW		300	555	µA
I_{NCLK}	Normal-mode supply current, with no active TMDS input clock	$\overline{LP}$ = HIGH, no TMDS input clock, HPD_SINK = HIGH, S1/S2 = LOW/LOW, LOW/HIGH, HIGH/HIGH		12	18	mA

HOT-PLUG DETECT

The TMDS361B is designed to support the hot-plug indication to the input ports (HDMI/DVI sources connected to the TMDS361B) via the HPD[1:3] output pins. The state of the hot-plug output of the selected source follows the state of the hot-plug input (HPD_SINK input pin) from the sink side. The state of the hot-plug output for the non-selected source goes low (See Table 1).

The maximum V_{OH} of the HPD depends on VCC. It is recommended that if V_{OH} greater than 3.6 V is needed on HPD, then an external circuit can be used to drive V_{OH} from the 5 V of the HDMI source (connected as shown in Figure 45).

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(HPD)}$	High-level output voltage	I_{OH} = 100 µA	2		VCC	V
$V_{OL(HPD)}$	Low-level output voltage	I_{OL} = 100 µA	0		0.4	V
I_H	High-level input current	V_{IH} = 2 V, VCC = 3.6 V	–10		10	µA
I_L	Low-level input current	V_{IL} = 0.8 V, VCC = 3.6 V	–10		10	µA
R_L	Output source impedance		800	1000	1200	Ω

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD1(HPD)}$	HPD_SINK propagation delay	HPD_SINK to HPD[1:3]		12	20	ns
$t_{S1(HPD)}$	Selecting port HPD switch time	S[1:2] to HPD[1:3]		17	30	ns
$t_{S2(HPD)}$	Deselecting port HPD switch time	S[1:2] to HPD[1:3]		14	22	ns
$t_{Z(HPD)}$	Low-power to high-level propagation delay	$\overline{LP}$ to HPD[1:3]		13	20	ns

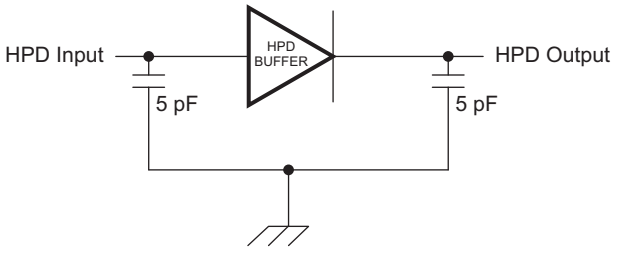


Figure 1. HPD Test Circuit

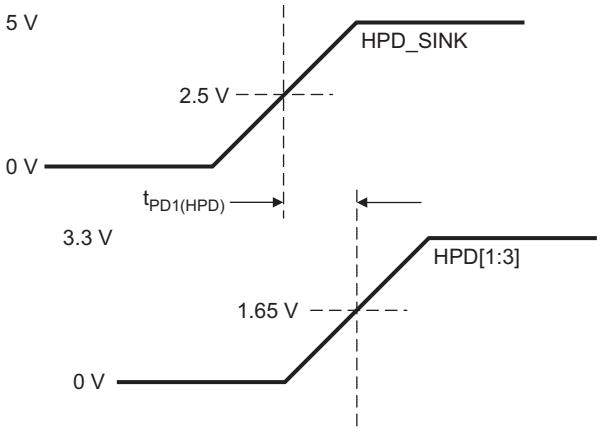


Figure 2. HPD Timing Diagram #1

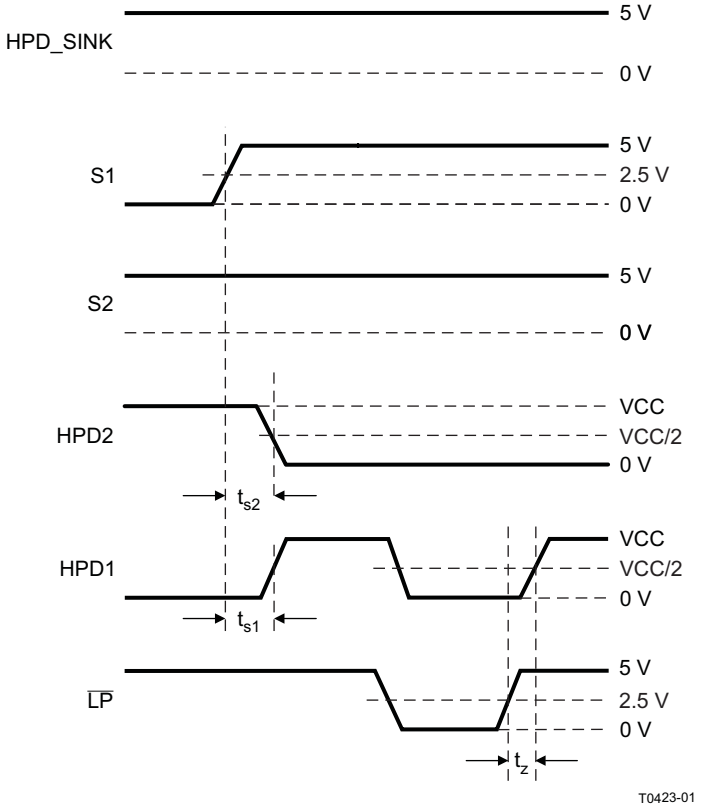


Figure 3. HPD Timing Diagram #2

TMDS DDC and Local I²C Pins

DDC I²C Buffer or Repeater: The TMDS361B provides buffering on the DDC I²C interface for each of the input ports connected. This feature isolates the capacitance on the source side from the sink side and thus helps in passing system-level compliance. See the DDC I2C Function Description section for a detailed description on how the DDC I²C buffer operates. Note that a key requirement on the sink side is that the $V_{IL(Sink)}$ (input to TMDS361B) should be less than 0.4 V. This requirement should be met for the DDC I²C buffer to function properly. There are three settings of $V_{IL(Sink)}$ and $V_{OL(Sink)}$ that can be chosen based on OVS settings (See Table 8 through Table 11).

Local I²C Interface: The TMDS361B includes a slave I²C interface to control device features like TMDS input port selection, TMDS output edge-rate control, power management, DDC buffer OVS settings, etc. See Table 8 through Table 11.

The TMDS361B is designed to be controlled via a local I²C interface or GPIO interface, based on the status of the I2C_SEL pin. The local I²C interface in the TMDS361B is only a slave I²C interface. See the I2C INTERFACE NOTES section for a detailed description of I²C functionality.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_L	Low-level input current		VCC = 3.6 V, V_I = 0 V	–10		10	µA
$I_{lkg(Sink)}$	Input leakage current	Sink pins	VCC = 3.6 V, V_I = 4.95 V	–10		10	µA
$C_{IO(Sink)}$	Input/output capacitance	Sink pins	DC bias = 2.5 V, ac = 3.5 Vp-p, f = 100 kHz			15	pF
$V_{IH(Sink)}$	High-level input voltage	Sink pins		2.1		5.5	V
$V_{IL1(Sink)}$	Low-level input voltage	Sink pins	OVS 1	–0.2		0.4	V
$V_{OL1(Sink)}$	Low-level output voltage	Sink pins	I_O = 3 mA, OVS = HIGH	0.6		0.7	V
$V_{IL2(Sink)}$	Low-level input voltage	Sink pins	OVS 2	–0.2		0.4	V
$V_{OL2(Sink)}$	Low-level output voltage	Sink pins	I_O = 3 mA, OVS = LOW	0.5		0.6	V
$V_{IL3(Sink)}$	Low-level input voltage	Sink pins	OVS 3	–0.2		0.3	V
$V_{OL3(Sink)}$	Low-level output voltage	Sink pins	I_O = 3 mA, OVS = high-Z	0.4		0.5	V
$I_{lkg(I2C)}$	Input leakage current	Port[1:3] pins	VCC = 3.6 V, V_I = 4.95 V	–10		10	µA
$C_{IO(I2C)}$	Input/output capacitance	Port[1:3] pins	DC bias = 2.5 V, ac = 3.5 Vp-p, f = 100 kHz			15	pF
$V_{IH(I2C)}$	High-level input voltage	Port[1:3] pins		2.1		5.5	V
$V_{IL(I2C)}$	Low-level input voltage	Port[1:3] pins		–0.2		1.5	V
$V_{OL(I2C)}$	Low-level output voltage	Port[1:3] pins	I_O = 3 mA			0.2	V

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Propagation delay time, low to high	Source to sink	80		251	ns
t_{PHL1}	Propagation delay time, high to low	Source to sink	35		200	ns
t_{PLH2}	Propagation delay time, low to high	Sink to source	204		459	ns
t_{PHL2}	Propagation delay time, high to low	Sink to source	35		200	ns
t_{f1}	Output signal fall time	Sink side	20		72	ns
t_{f2}	Output-signal fall time	Source side	20		72	ns
f_{SCL}	SCL clock frequency for internal register	Local I^2C			100	kHz
$t_{W(L)}$	Clock LOW period for I^2C register	Local I^2C	4.7			µs
$t_{W(H)}$	Clock HIGH period for internal register	Local I^2C	4			µs
t_{SU1}	Internal register setup time, SDA to SCL	Local I^2C	250			ns
$t_{h(1)}$ *1	Internal register hold time, SCL to SDA	Local I^2C	0			µs
$t_{(buf)}$	Internal register bus free time between STOP and START	Local I^2C	4.7			µs
$t_{su(2)}$	Internal register setup time, SCL to START	Local I^2C	4.7			µs
$t_{h(2)}$	Internal register hold time, START to SCL	Local I^2C	4			µs
$t_{su(3)}$	Internal register hold time, SCL to STOP	Local I^2C	4			µs

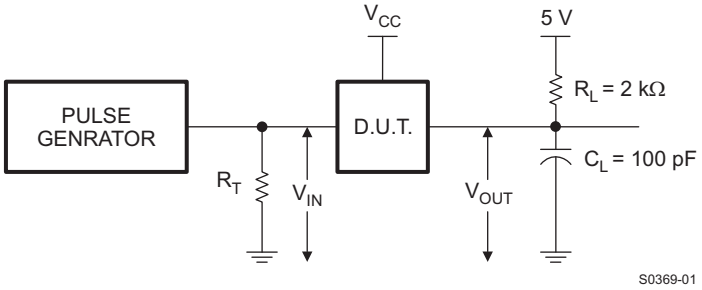


Figure 4. Sink-Side Test Circuit

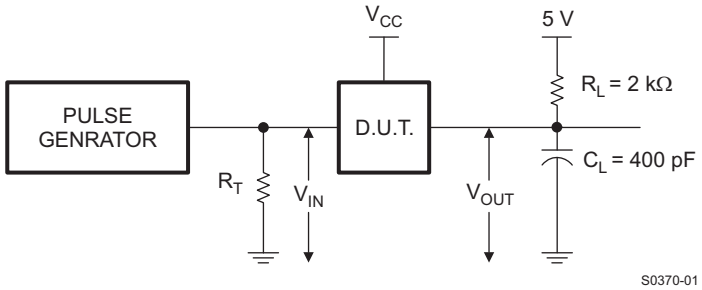


Figure 5. Source-Side Test Circuit

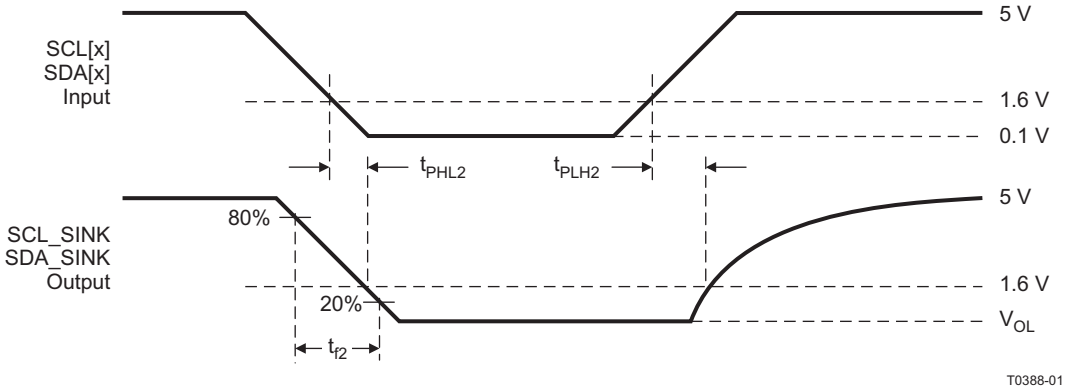


Figure 6. Source-Side Output AC Measurements

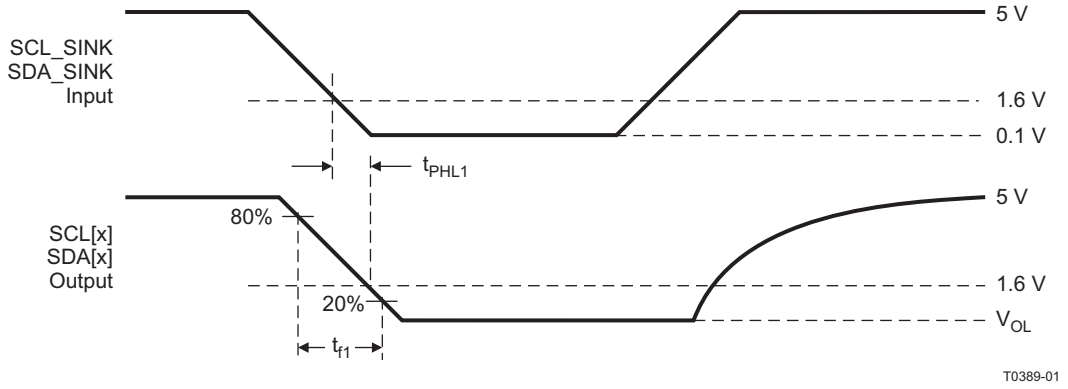


Figure 7. Sink-Side Output AC Measurements

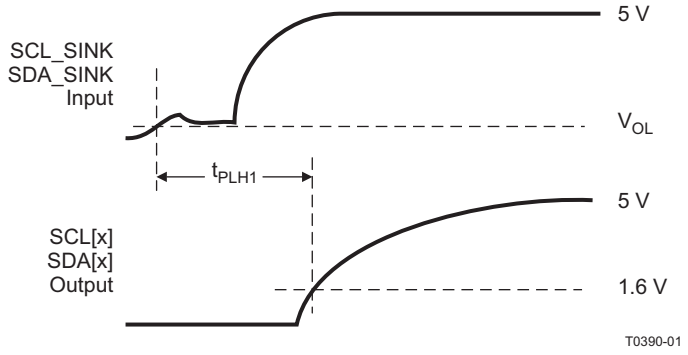


Figure 8. Source-Side Output AC Measurements (Continued)

TMDS Main Link Pins

The TMDS port of the TMDS361B is designed to support the Digital Video Interface (DVI) 1.0 and High Definition Multimedia Interface (HDMI) 1.3 specifications. The differential output voltage swing can be fine-tuned with the VSadj resistor.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Single-ended HIGH-level output voltage	AVCC = 3.3 V, R_T = 50 Ω	AVCC – 10		AVCC + 10	mV
V_{OL}	Single-ended LOW-level output voltage		AVCC – 600		AVCC – 400	mV
V_{SWING}	Single-ended output voltage swing		400		600	mV
$V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states				5	mV
$V_{OD(pp)}$	Peak-to-peak output differential voltage		800		1200	mV
$V_{(O)SBY}$	Single-ended standby output voltage		AVCC – 10		AVCC + 10	mV
$I_{(O)OFF}$	Single-ended power-down output current	0 V ≤ VCC ≤ 1.5 V, AVCC = 3.3 V, R_T = 50 Ω	–10		10	µA
I_{OS}	Short-circuit output current	See Figure 16	-15	12	15	mA
$V_{CD(pp)}$	Minimum valid clock differential voltage (peak-to-peak)	Input TMDS clock frequency = 300 MHz	100			mV

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time	AVCC = 3.3 V, R_T = 50 Ω. See Figure 9 and Figure 10.	250		800	ps
t_{PHL}	Propagation delay time		250		800	ps
t_{R1}	Rise time, fastest mode (default setting): fastest setting		84	110	140	ps
t_{F1}	Fall time, fastest mode (default setting): fastest setting		84	110	140	ps
t_{R2}	Rise time, fastest mode + 50 ps (approximately)		142	160	190	ps
t_{F2}	Fall time, fastest mode + 50 ps (approximately)		142	160	190	ps
t_{R3}	Rise time, fastest mode + 100 ps (approximately)		187	210	230	ps
t_{F3}	Fall time, fastest mode + 100 ps (approximately)		187	210	230	ps
t_{R4}	Rise time, fastest mode + 120 ps (approximately): slowest setting		216	230	260	ps
t_{F4}	Fall time, fastest mode + 120 ps (approximately): slowest setting		216	230	260	ps
$t_{SK(P)}$	Pulse skew (see (2))			8	15	ps
$t_{SK(D)}$	Intra-pair skew	AVCC = 3.3 V, R_T = 50 Ω. See Figure 11.		10	30	ps
$t_{SK(O)}$	Inter-pair skew (see (3))				100	ps
$t_{JITD(PP)}$	Peak-to-peak output residual data jitter	AVCC = 3.3 V, R_T = 50 Ω, dR = 2.25 Gbps. See Figure 14 for measurement setup; residual jitter is the total jitter measured at TTP4 minus the jitter measured at TTP1. See Figure 15 for the loss profile of the cable used for $t_{JITD(PP)}$ measurement. Also see Typical Curves for $t_{JITD(PP)}$ across cable length and input TMDS data rate.		125	198	ps

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between t_{PLH} and t_{PHL} of a specified terminal.
(3) $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of a sink-port bank when inputs of the active source port are tied together.

SWITCHING CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{JITC(PP)}$	Peak-to-peak output residual clock jitter	AVCC = 3.3 V, R_T = 50 Ω, input TMDS clock frequency = 225 MHz. See Figure 14for measurement setup; residual jitter is the total jitter measured at TTP4 minus the jitter measured at TTP1. See Figure 15 for the loss profile of the cable used for $t_{JITC(PP)}$ measurement. $t_{JITC(PP)}$ is measured at TMDS differential clock signal crossing.		54	84	ps
t_{CLK1}	Valid clock-detect enable time	AVCC = 3.3 V, R_T = 50 Ω, input TMDS clock frequency = 300 MHz. See Figure 13.		300	500	ns
t_{CLK2}	Invalid clock-detect disable time	AVCC = 3.3 V, R_T = 50 Ω, input TMDS clock frequency = 1 MHz. See Figure 13.		500	800	ns
t_{SEL1}	Port selection time (see (4)	AVCC = 3.3 V, R_T = 50 Ω		300	500	ns
t_{SEL2}	Port deselection time (see (5))	AVCC = 3.3 V, R_T = 50 Ω		40	50	ns
f_{CD}	Clock-detect frequency	AVCC = 3.3 V, R_T = 50 Ω. See Figure 13.	25		300	MHz

(4) t_{SEL1} includes the time for the valid clock-detect enable time and $t_{S1(HPD)}$, because the $t_{S1(HPD)}$ event happens in parallel with t_{SEL1}; thus, the t_{SEL1} time is primarily the t_{CLK1} time.
(5) t_{SEL2} is primarily the $t_{S2(HPD)}$ time.

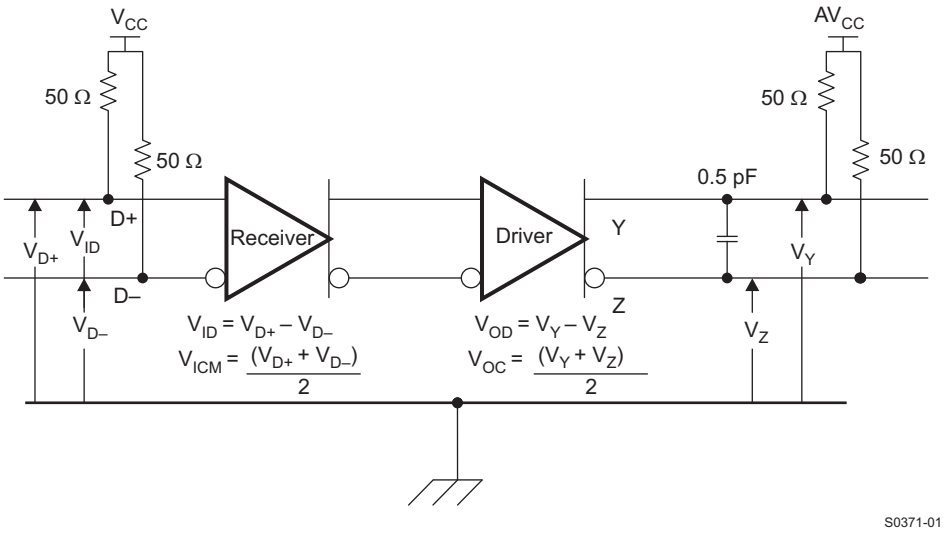


Figure 9. TMDS Main-Link Test Circuit

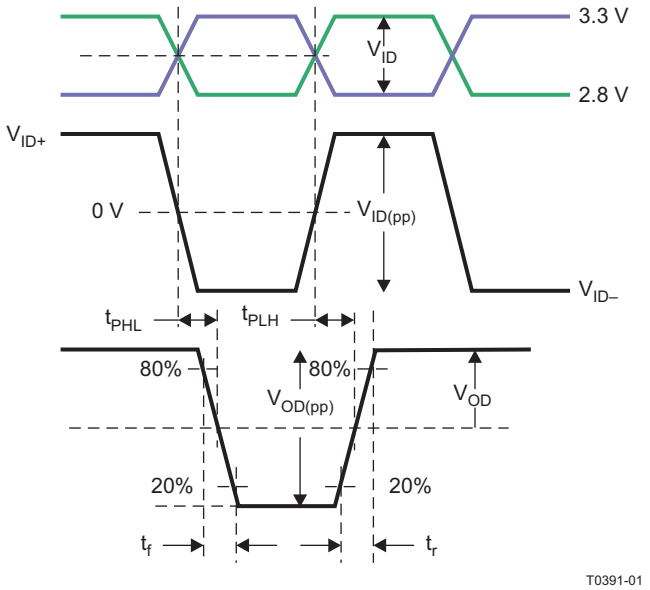


Figure 10. TMDS Main-Link Timing Measurements

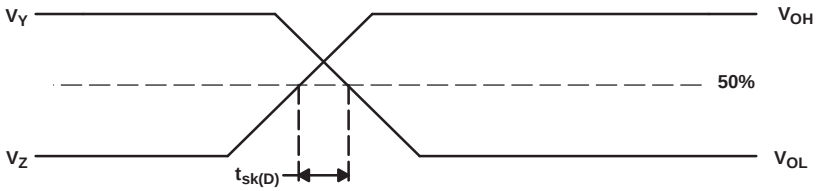


Figure 11. Definition of Intra-Pair Differential Skew

Figure 12. TMDS Main-Link Common-Mode Measurements

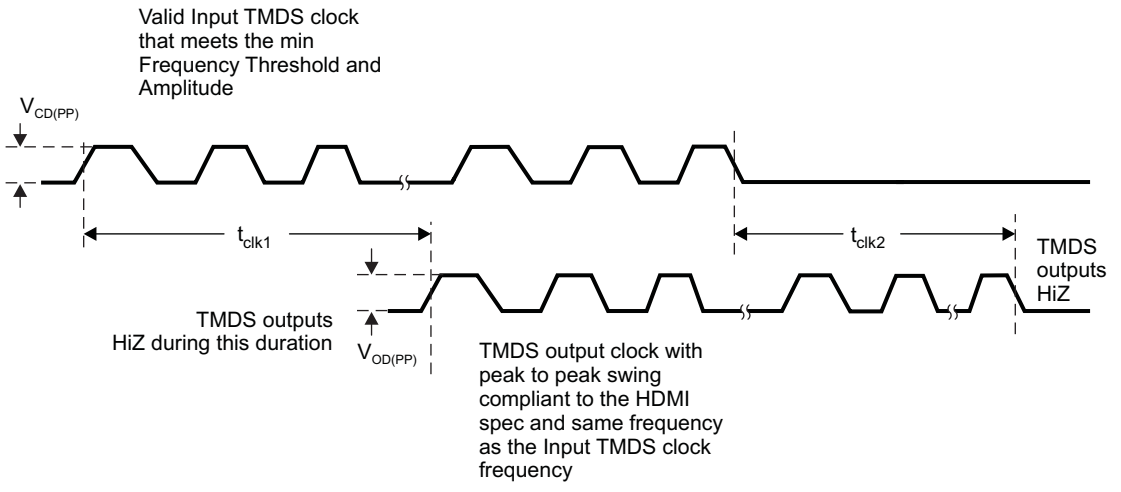
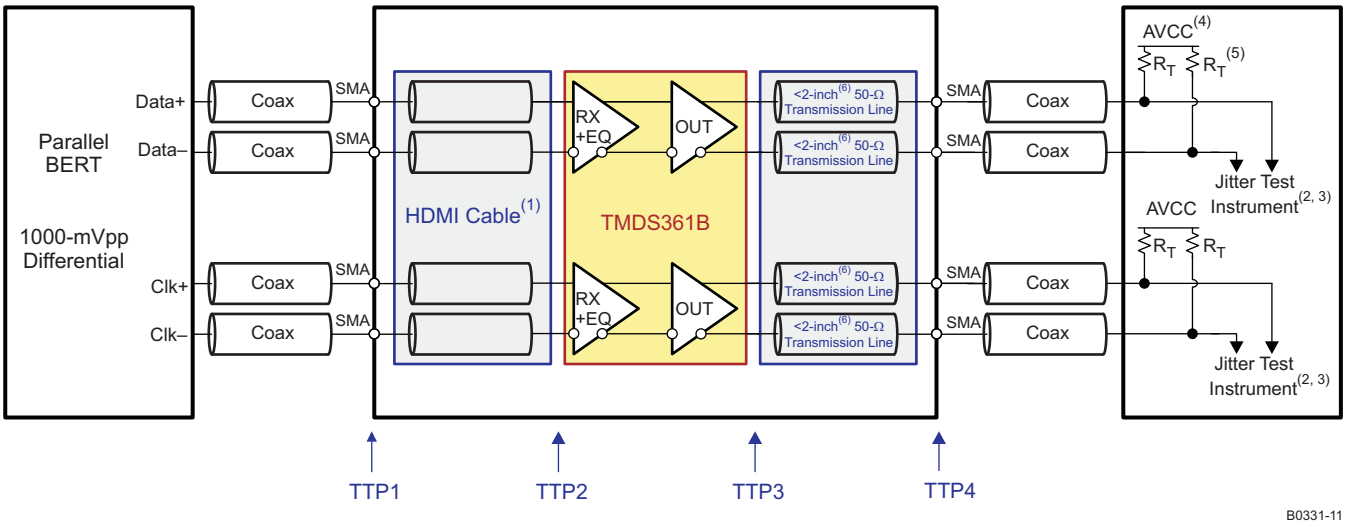


Figure 13. Clock-Detect Timing Diagram



(1) The HDMI cable between TTP1 and TTP2 is 0 m (no loss) case and 20 m case. See Figure 15 for the loss profile of the cable.

(2) All jitter is measured at a BER of 10^{-9}.

(3) Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP1.

(4) AVCC = 3.3 V; VSadj = 4.02 kΩ.

(5) R_T = 50 Ω.

(6) 2 inches = 5,08 cm.

NOTES: Output edge rate default (fastest): input edge rate from the parallel BERT greater than 75 ps (20%–80%). The input signal from the parallel BERT has no pre-emphasis.

Figure 14. Jitter Measurement Setup

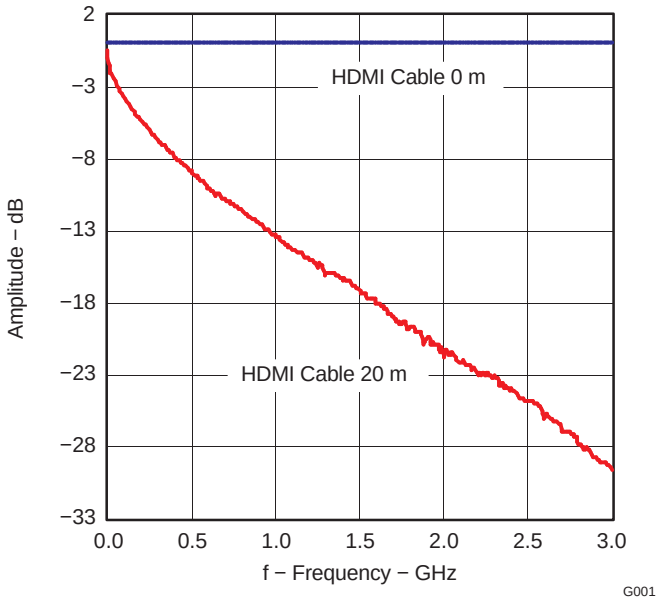


Figure 15. Loss Profile of 20-m HDMI Cable

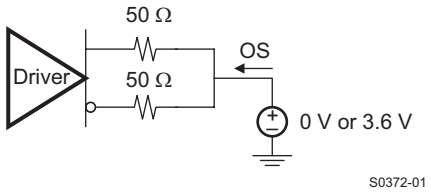


Figure 16. TMDS Main Link Short-Circuit Output Circuit

TYPICAL CHARACTERISTICS

AVCC = 3.3 V, R_T = 50 Ω

POWER vs AMBIENT TEMPERATURE

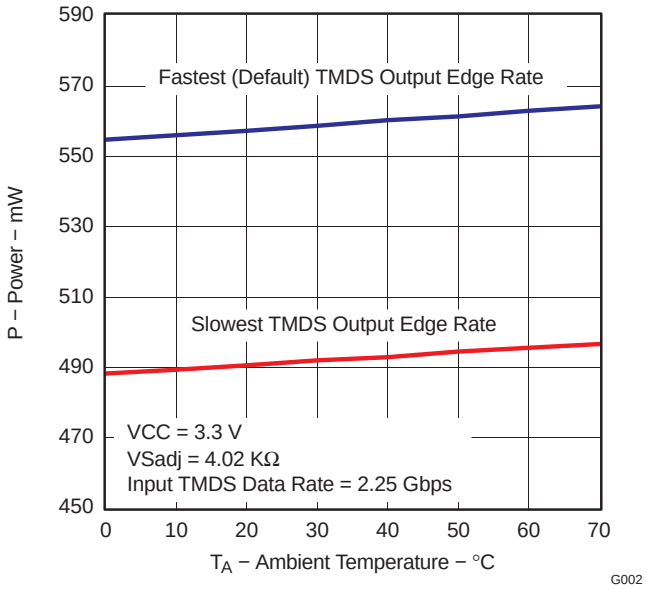


Figure 17.

POWER vs INPUT TMDS DATA RATE

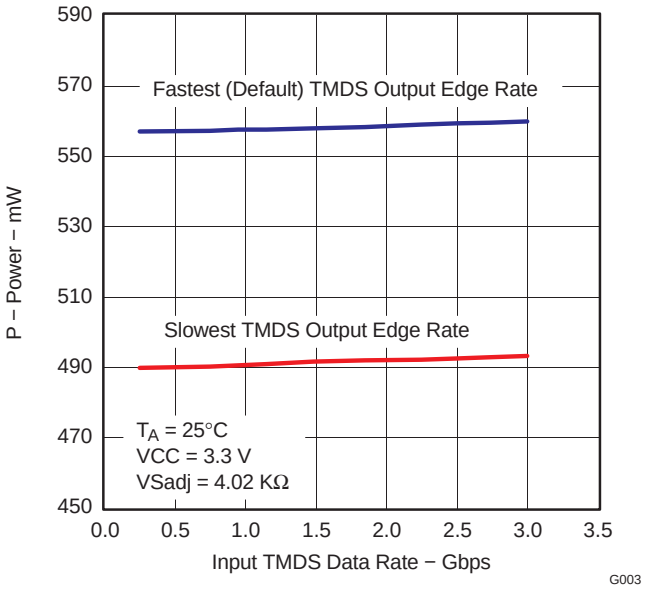


Figure 18.

TYPICAL CHARACTERISTICS (continued)

AVCC = 3.3 V, R_T = 50 Ω

PEAK-to-PEAK RESIDUAL CLOCK JITTER vs INPUT TMDS DATA RATE

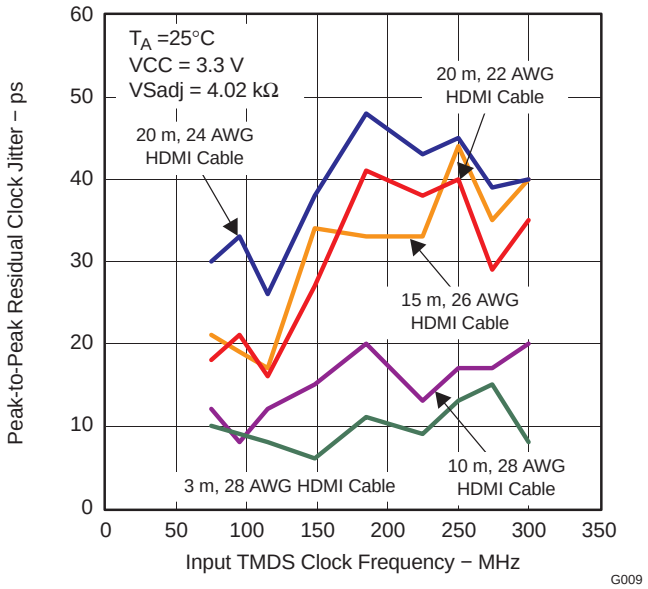


Figure 19.

PEAK-to-PEAK RESIDUAL DATA JITTER vs INPUT TMDS DATA RATE

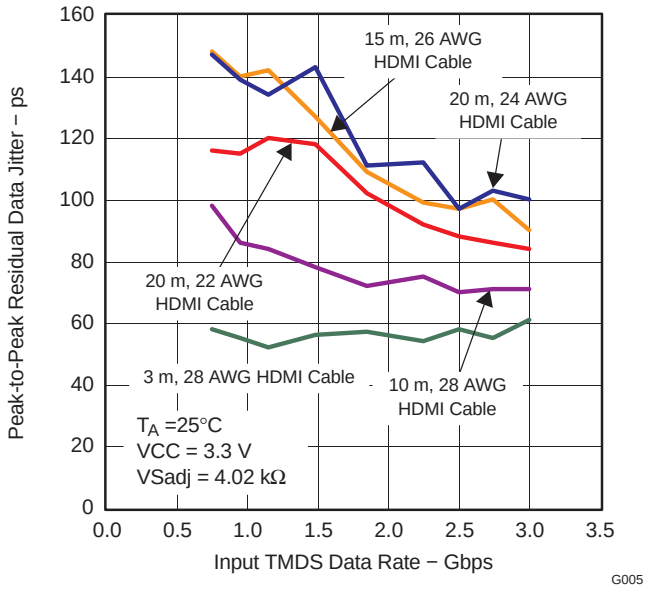


Figure 20.

PEAK-to-PEAK RESIDUAL CLOCK JITTER vs HDMI CABLE LENGTH

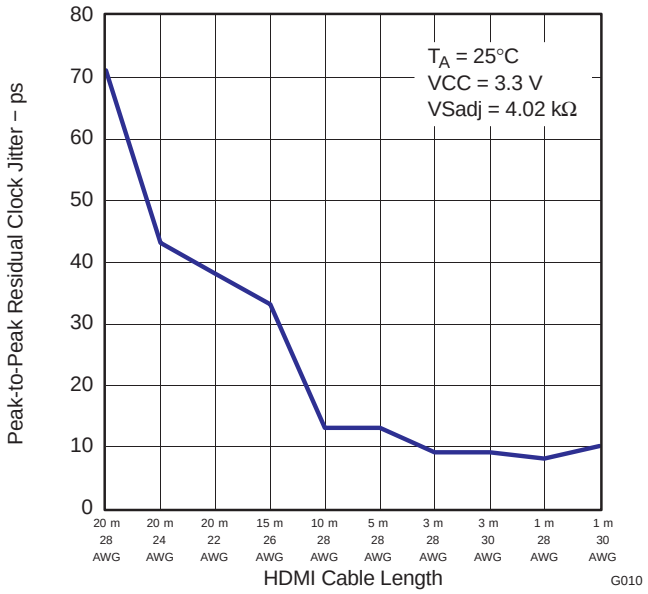


Figure 21.

PEAK-to-PEAK RESIDUAL DATA JITTER vs HDMI CABLE LENGTH

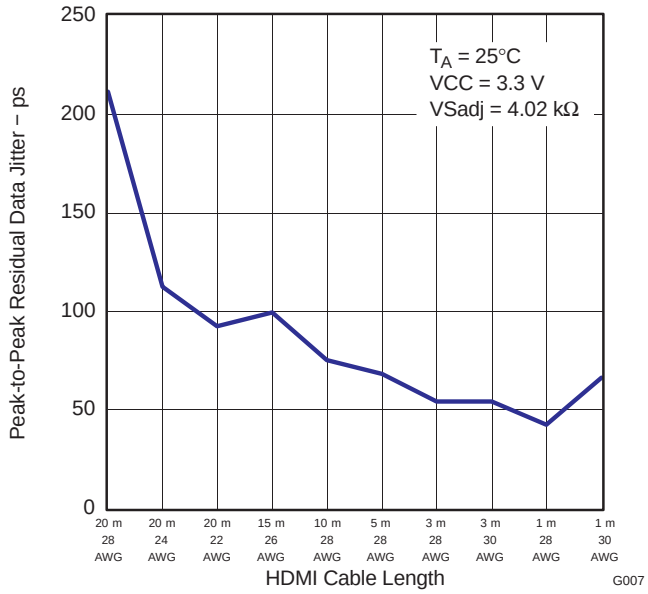


Figure 22.

TYPICAL CHARACTERISTICS (continued)

AVCC = 3.3 V, R_T = 50 Ω

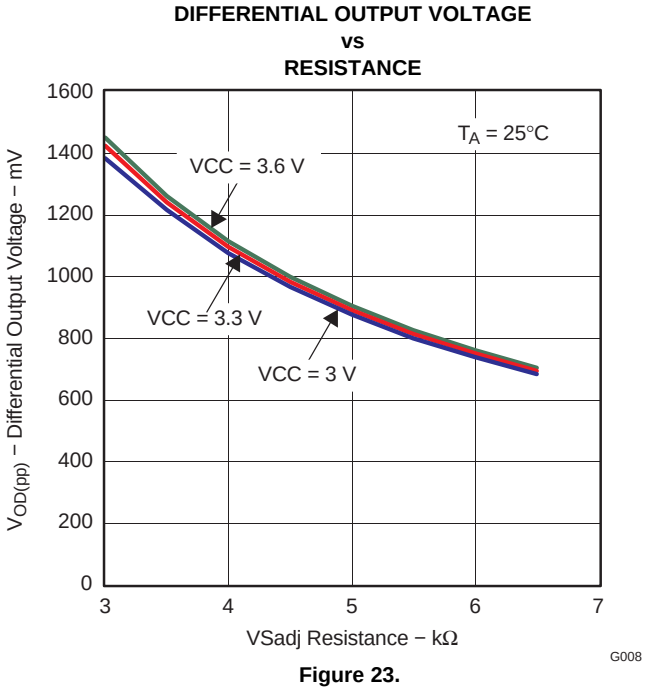


Figure 23.

(1) The HDMI cable between TTP1 and TTP2 is 0 m (no loss) case. See Figure 15 for the loss profile of the cable.

(2) Eye data is measured using an 8-GHz bandwith oscilloscope (Agilent).

(3) Eye data is taken at TTP4.

(4) AVCC = 3.3 V; VSadj = 4.02 kΩ.

(5) R_T = 50 Ω.

(6) 2 inches = 5,08 cm.

NOTES: Output edge rate default (fastest): input edge rate from the video pattern generator greater than 75 ps (20%–80%). The input signal from the parallel BERT has pre-emphasis. See Figure 26 for acceptable input pre-emphasis duration and amplitude.

Pass/fail criterion: output eye at TTP4 should comply with output eye mask (See Figure 25). The input TMDS clock frequencies tested: 25 MHz, 30.24 MHz, 36 MHz, 54 MHz, 65 MHz, 74.25 MHz, 84.75 MHz, 108 MHz, 135 MHz, 148.5 MHz, 185.625 MHz, 222.75 MHz, 297 MHz.

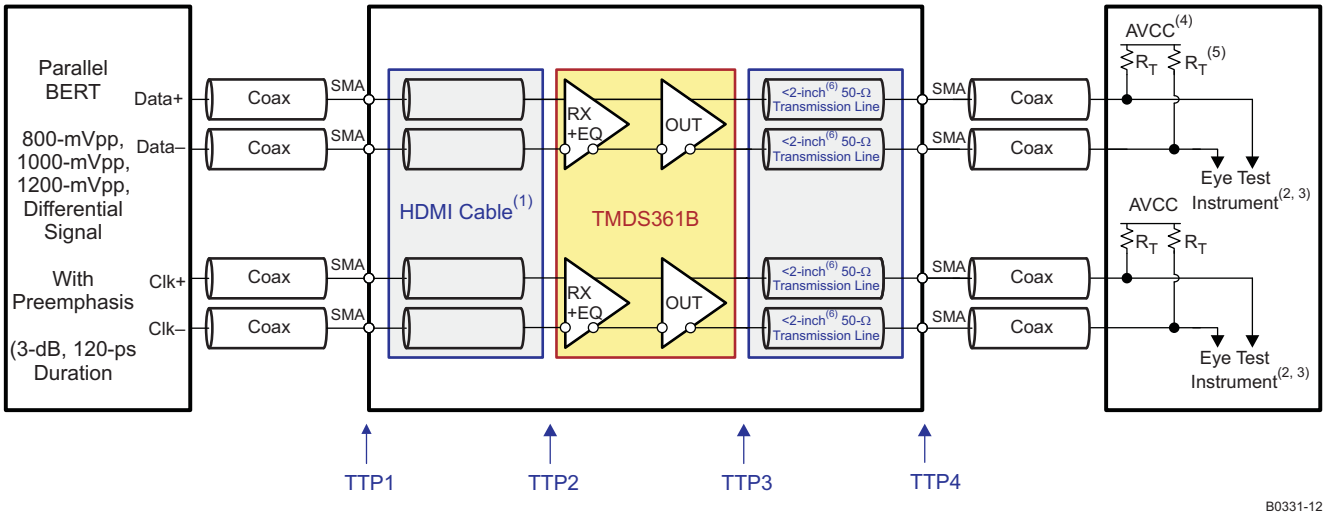


Figure 24. Input Pre-Emphasis Tolerance-Measurement Setup

TYPICAL CHARACTERISTICS (continued)

AVCC = 3.3 V, R_T = 50 Ω

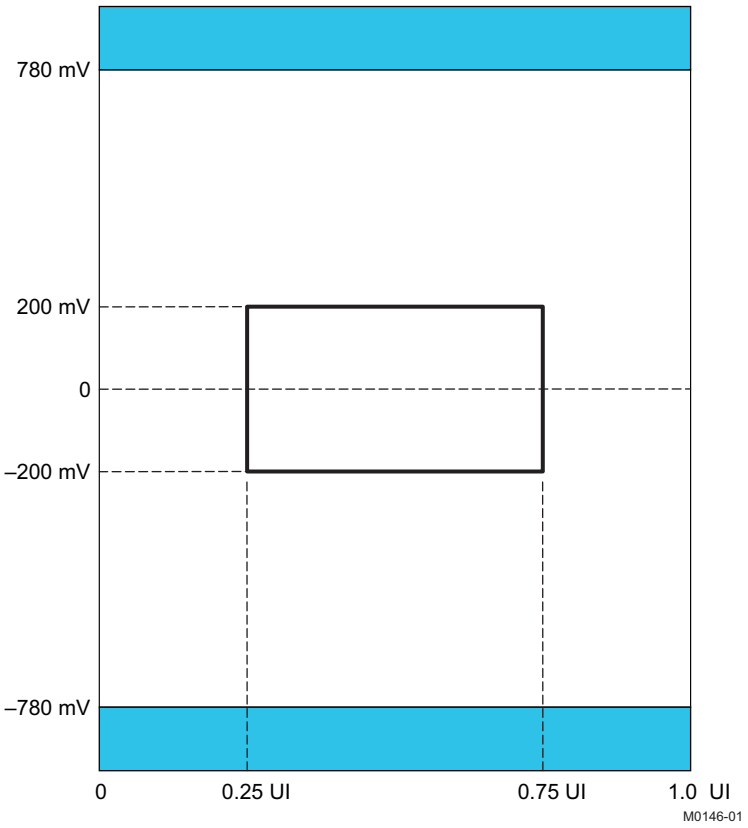


Figure 25. Output-Eye Mask at TTP4

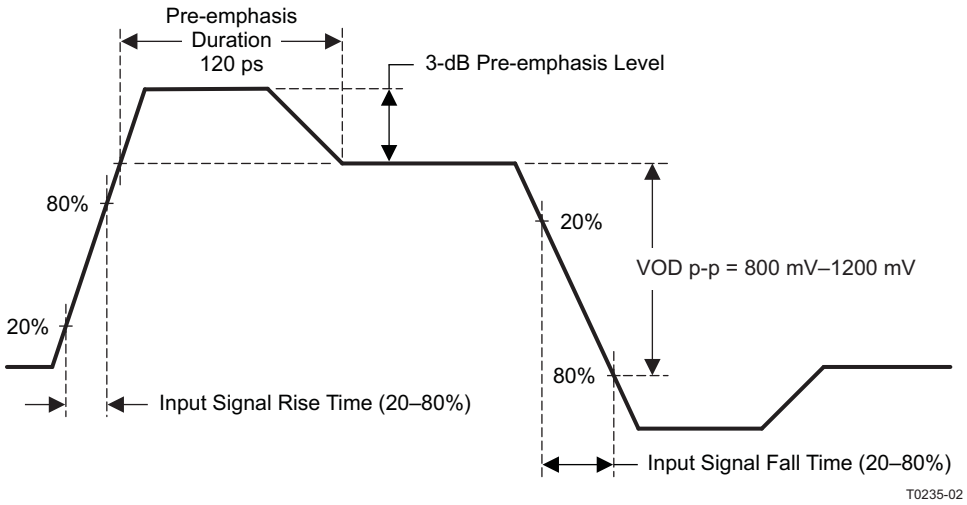
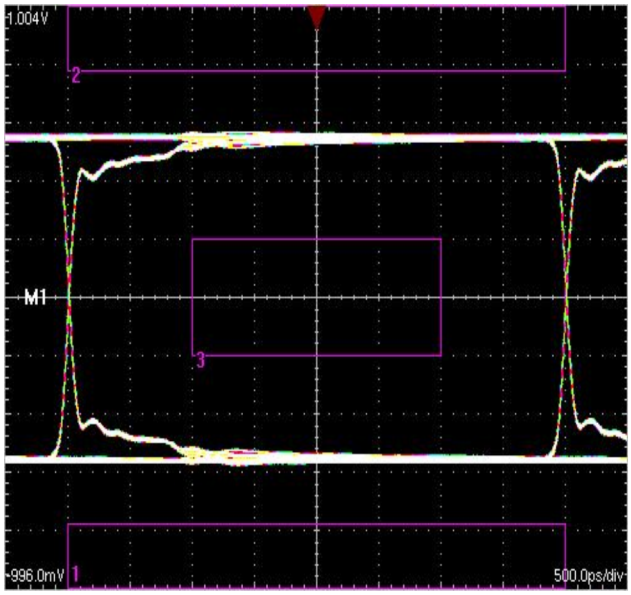


Figure 26. Acceptable Pre-Emphasis Into TMDS361B

Any input pre-emphasis higher than the input condition shown in Figure 26 can result in over-equalization and potential system failure. During over-equalization, the TMDS361B in the setup of Figure 24 fails the output eye mask as shown in Figure 25.

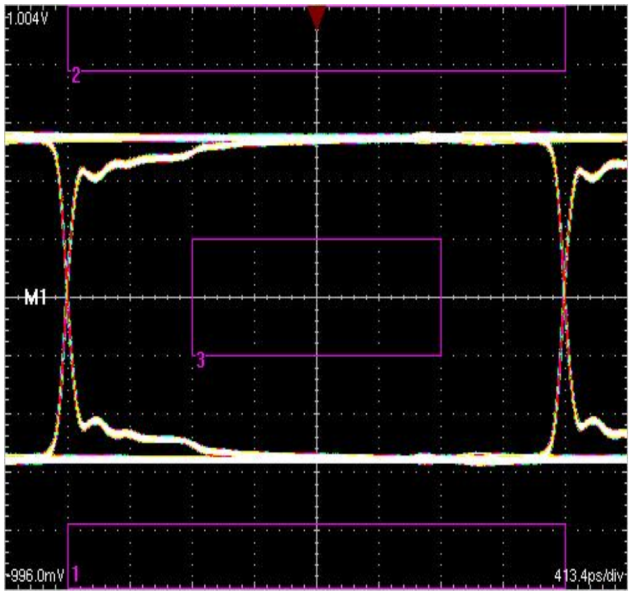
TYPICAL CHARACTERISTICS (continued)

AVCC = 3.3 V, R_T = 50 Ω



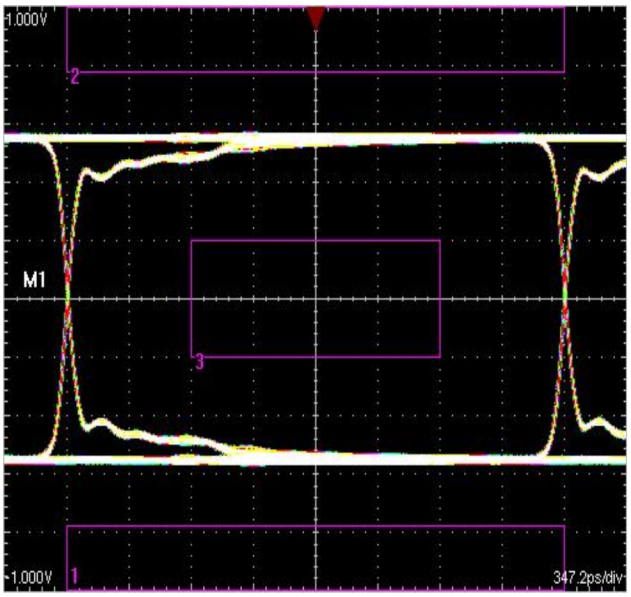
C001

Figure 27. TMDS Data Rate of 250 Mbps



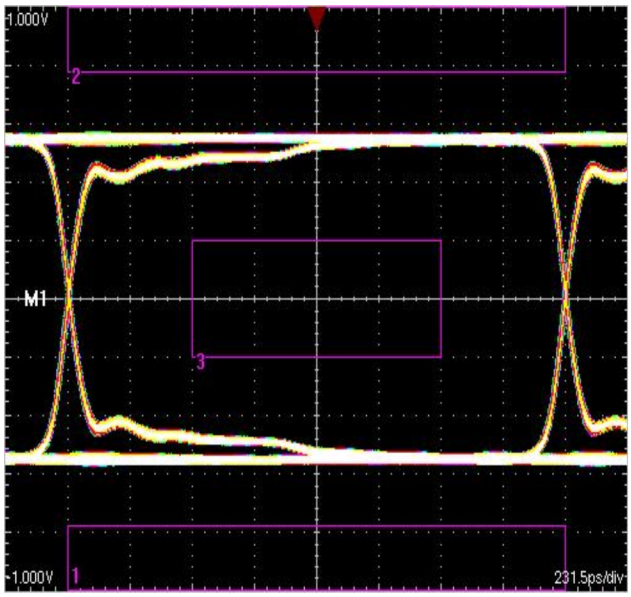
C002

Figure 28. TMDS Data Rate of 302.4 Mbps



C003

Figure 29. TMDS Data Rate of 360 Mbps

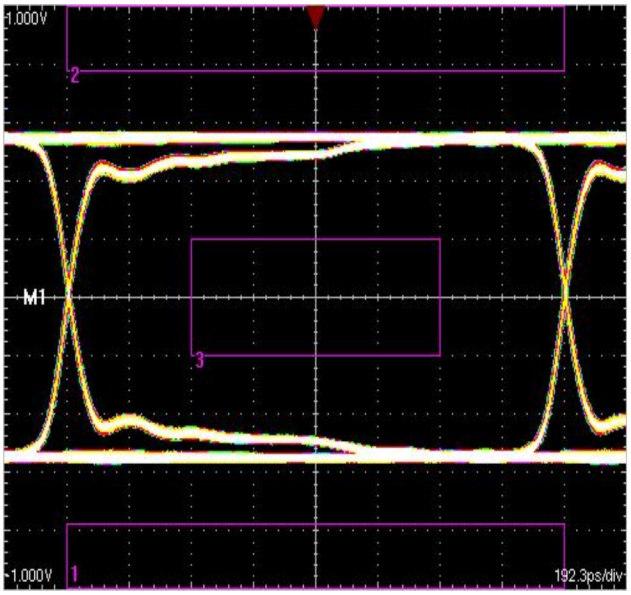


C004

Figure 30. TMDS Data Rate of 540 Mbps

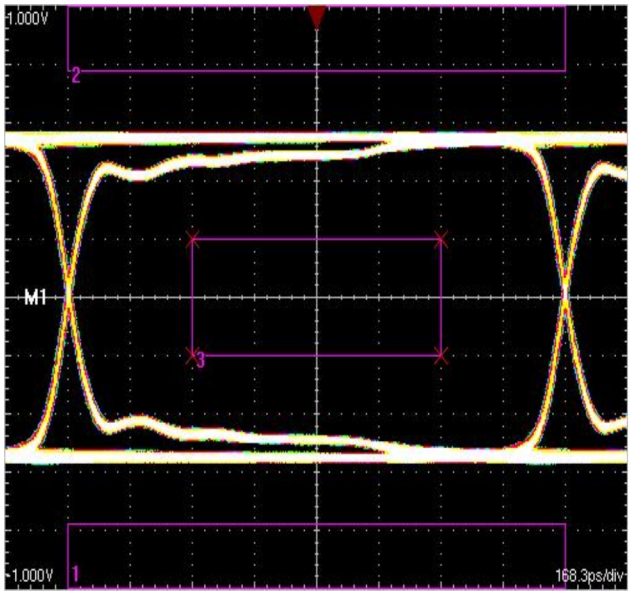
TYPICAL CHARACTERISTICS (continued)

AVCC = 3.3 V, R_T = 50 Ω



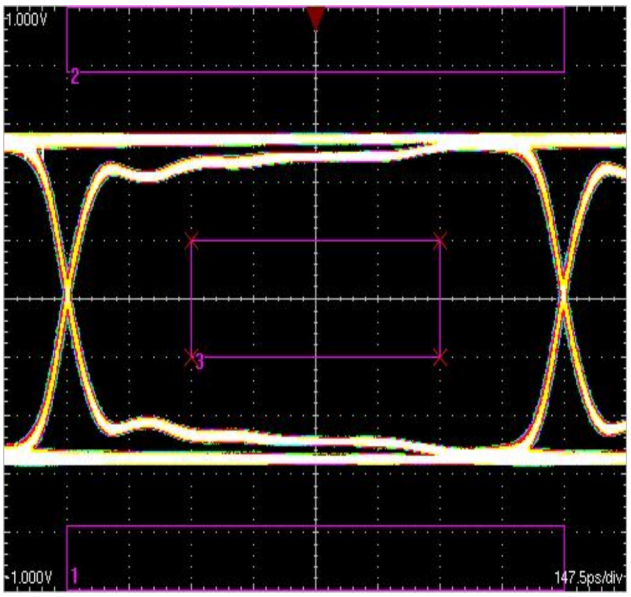
C005

Figure 31. TMDS Data Rate of 650 Mbps



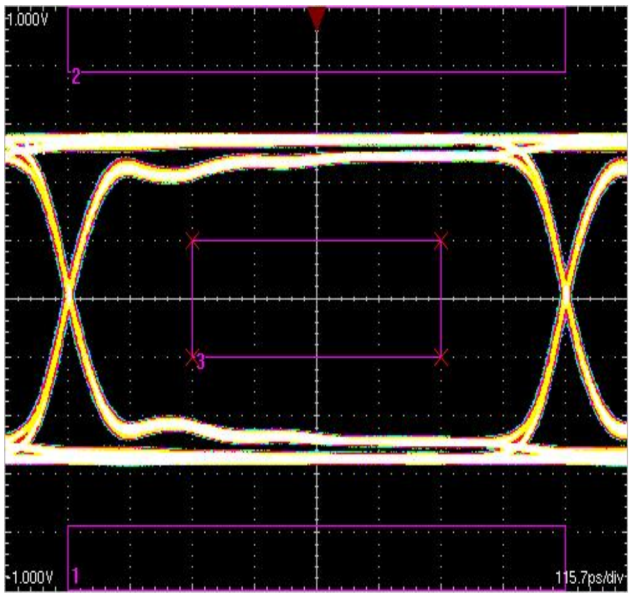
C006

Figure 32. TMDS Data Rate of 742.5 Mbps



C007

Figure 33. TMDS Data Rate of 847.5 Mbps

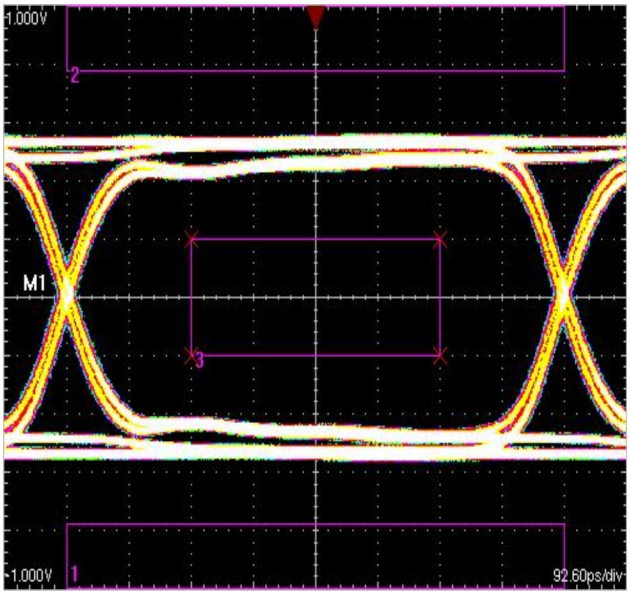


C008

Figure 34. TMDS Data Rate of 1080 Mbps

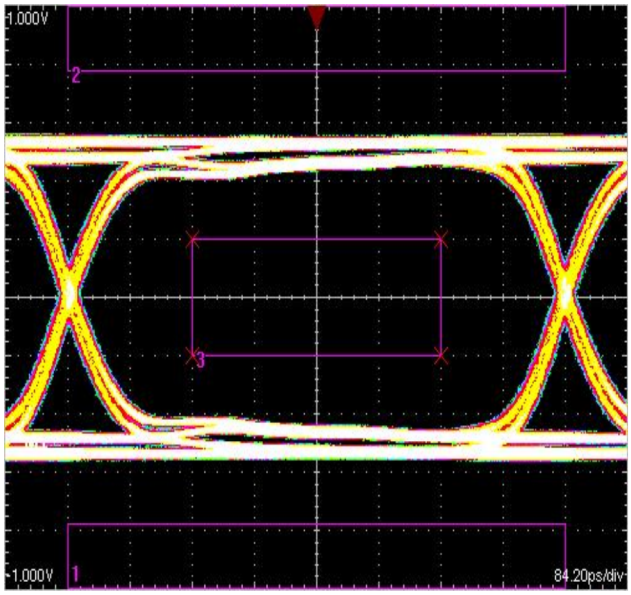
TYPICAL CHARACTERISTICS (continued)

AVCC = 3.3 V, R_T = 50 Ω



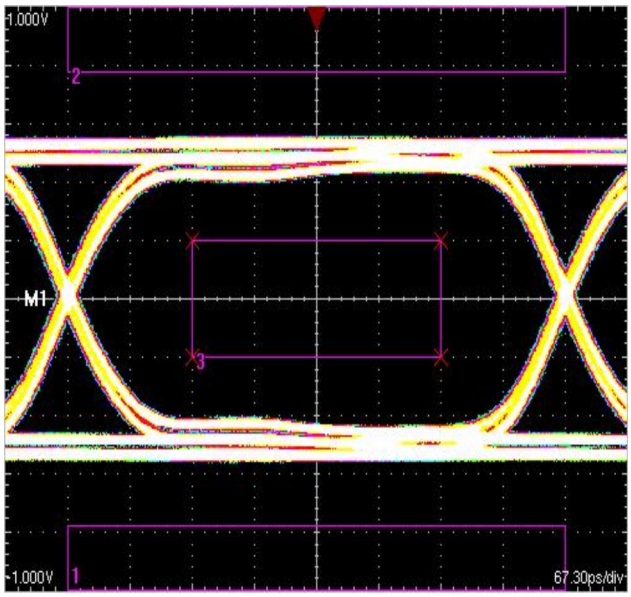
C009

Figure 35. TMDS Data Rate of 1350 Mbps



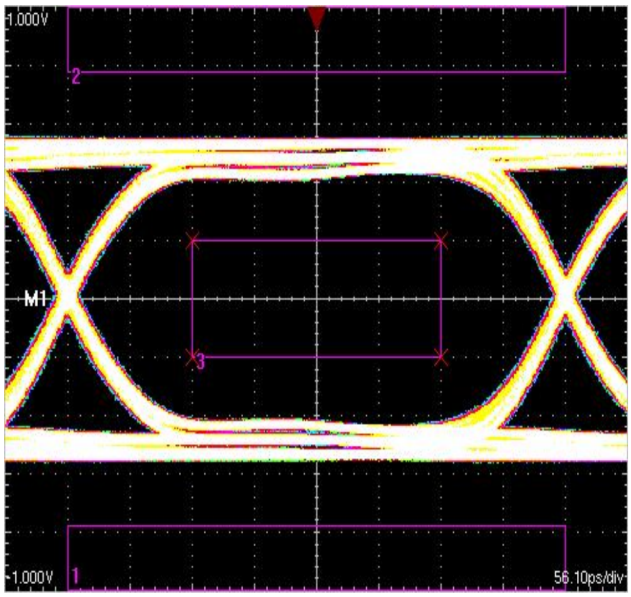
C010

Figure 36. TMDS Data Rate of 1485 Mbps



C011

Figure 37. TMDS Data Rate of 1856.25 Mbps



C012

Figure 38. TMDS Data Rate of 2227.5 Mbps

TYPICAL CHARACTERISTICS (continued)

AVCC = 3.3 V, R_T = 50 Ω

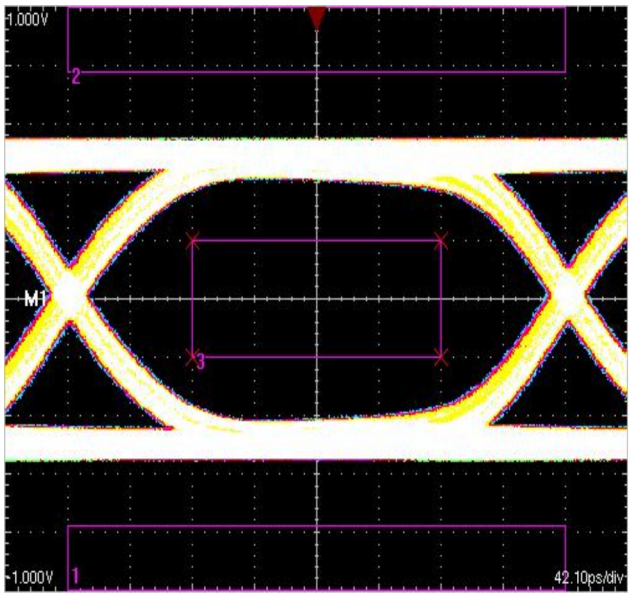


Figure 39. TMDS Data Rate of 2970 Mbps

APPLICATION INFORMATION

Table 3. TMDS361B vs TMDS351 Pinout

PIN NUMBER	I/O	TMDS351	TMDS361B
Pins 32 and 33	I	GPIO mode: S1 and S2 configured as source selector pins	GPIO mode: S1 and S2 configured as source selector pins (same as TMDS351) I^2C mode: S1 and S2 configured as SCL and SDA for local slave I^2C communication
Pin 34	I	EQ: TMDS input equalization control select EQ = High – 10-m 28 AWG HDMI cable EQ = Low – HDMI 1.3 compliant cable	I2C_SEL: GPIO / local I^2C control select I2C_SEL = High – Device is configured by GPIO logic. I2C_SEL= Low – Device is configured by I^2C logic.
Pin 49	—	VDD: HPD/DDC power supply	$\overline{LP}$: Low-power mode select bar $\overline{LP}$ = High – Normal operational mode $\overline{LP}$ = Low – Device goes into low-power state.

Based on the differences listed in Table 3, attention must be given to pin 34, which determines whether the device uses I^2C or GPIO control.

Supply Voltage

The TMDS361B is powered up with a single power source that is 3.3-V VCC for the TMDS circuitry for HPD, DDC, and most of the control logic.

TMDS Input Fail-Safe

The TMDS361B incorporates clock-detect circuitry. If there is no valid TMDS clock from the connected HDMI/DVI source, the TMDS361B does not switch on the terminations on the source-side data channels. Additionally, the TMDS outputs are placed in the high-impedance state. This prevents the TMDS361B from turning on its outputs if there is no valid incoming HDMI/DVI data.

TMDS Outputs

A 10% precision resistor, 4.02-kΩ, is recommended to control the output swing to the HDMI-supporting 800-mV to 1200-mV range $V_{OD(pp)}$ (1000 mV typical). The TMDS outputs are high-impedance under standby-mode operation, S1 = H and S2 = L.

DDC I^2C Function Description

The TMDS361B provides buffers on the DDC I^2C lines on all three input ports. This section explains the operation of the buffer. For representation, the source side of the TMDS361B is represented by RSCL/RSDA, and the sink side is represented by TSCL/TSDA. The buffers on the RSCL/RSDA and TSCL/TSDA pins are 5-V tolerant when the device is powered off and high-impedance under low supply voltage, 1.5 V or below. If the device is powered up, the driver T (see Figure 40) is turned on or off depending on the corresponding R-side voltage level.

When the R side is driven low, below 1.5 V, the corresponding T-side driver turns on and drives the T side down to a low-level output voltage, V_{OL}. The value of V_{OL} and V_{IL} on the T side or the sink side of the TMDS361B switch depends on the output-voltage select (OVS) control settings. OVS control can be changed by the slave I^2C; see Table 8. When the OVS1 setting is selected, V_{OL} is typically 0.7 V and V_{IL} is typically 0.4 V. When the OVS2 setting is selected, V_{OL} is typically 0.6 V and V_{IL} is typically 0.4 V. When the OVS3 setting (default) is selected, V_{OL} is typically 0.5 V and V_{IL} is typically 0.3 V. V_{OL} is always higher than the driver-R input threshold, V_{IL} on the T side or the sink side, preventing lockup of the repeater loop. The TMDS361B is targeted primarily as a switch in the HDTV market and is expected to be a companion chip to an HDMI receiver; thus, the OVS control has been provided on the sink side, so that the requirement of V_{IL} to be less than 0.4 V can be met. The V_{OL} value can be selected to improve or optimize noise margins between V_{OL} and V_{IL} of the repeater itself or V_{IL} of some external device connected on the T side.

When the R side is pulled up, above 1.5 V, the T-side driver turns off and the T-side pin is high-impedance.

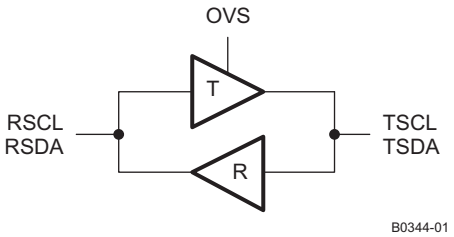


Figure 40. I^2C Drivers in the TMDS361B (R Side Is the HDMI Source Side, T Side Is the HDMI Sink Side)

When the T side is driven below 0.4 V by an external I^2C driver, both drivers R and T are turned on. Driver R drives the R side to near 0 V, and driver T is on, but is overridden by the external I^2C driver. If driver T is already on due to a low on the R side, driver R just turns on.

When the T side is released by the external I^2C driver, driver T is still on, so the T side is only able to rise to the V_{OL} of driver T. Driver R turns off, because V_{OL} is above its 0.4-V V_{IL} threshold, releasing the R side. If no external I^2C driver is keeping the R side low, the R side rises, and driver T turns off once the R side rises above 1.5 V; see Figure 41.

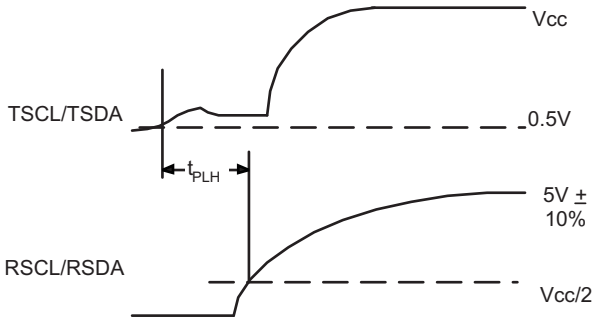


Figure 41. Waveform of Driver T Turning Off

It is important that any external I^2C driver on the T side is able to drive the bus below 0.4 V to achieve full operation. If the T side cannot be driven below 0.4 V, driver R may not recognize and transmit the low value to the R side.

DDC I^2C Behavior

The typical application of the TMDS361B is as a 3×1 switch in a TV connecting up to three HDMI input sources to an HDMI receiver. The I^2C repeater is 5-V tolerant, and no additional circuitry is required to translate between 3.3-V and 5-V bus voltages. In the following example, the system master is running on an R-side I^2C-bus while the slave is connected to a T-side bus. Both buses run at 100 kHz, supporting standard-mode I^2C operation. Master devices can be placed on either bus.

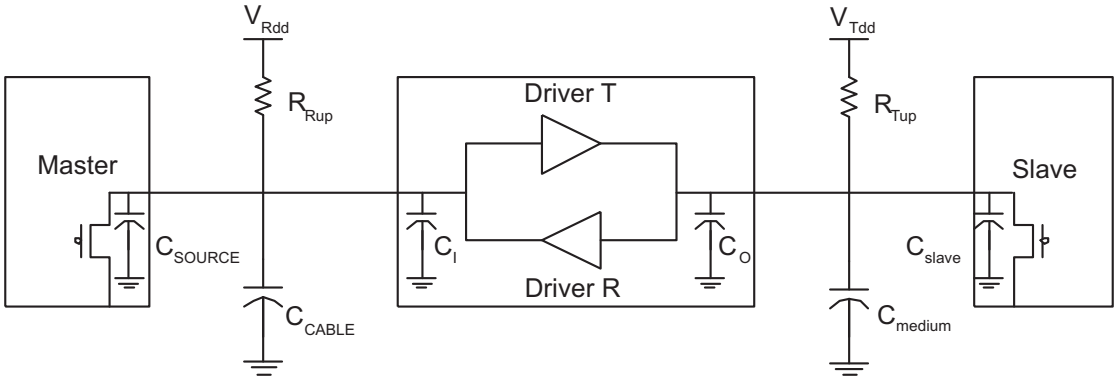


Figure 42. Typical Application

Figure 43 illustrates the waveforms seen on the R-side I²C-bus when the master writes to the slave through the I²C repeater circuit of the TMDS361B. This looks like a normal I²C transmission, and the turnon and turnoff of the acknowledge signals are slightly delayed.

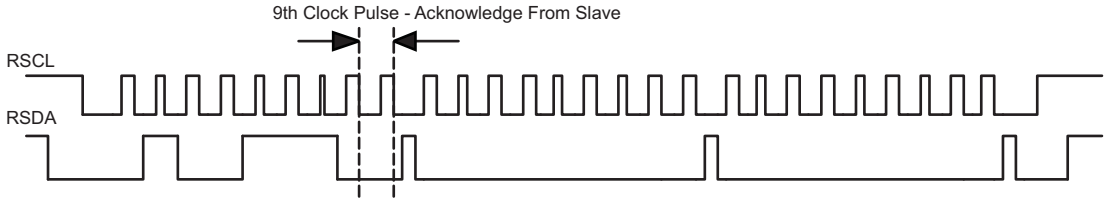


Figure 43. Bus-R Waveform

Figure 44 illustrates the waveforms seen on the T-side I²C-bus under the same operation as in Figure 43. On the T-side of the I²C repeater, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the driver T. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in this example. At the end of the acknowledge, the slave device releases and the bus level rises back to the V_{OL} set by the driver until the R-side rises above VCC/2, after which it continues to be high. It is important to note that any arbitration or clock-stretching events require that the low level on the T-side bus at the input of the TMDS361B I²C repeater is below 0.4 V to be recognized by the device and then transmitted to the R-side I²C bus.

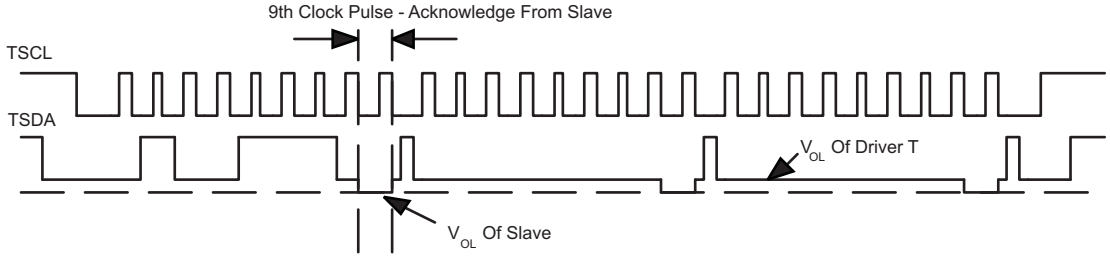


Figure 44. Bus-T Waveform

I²C Pullup Resistors

The pullup resistor value is determined by two requirements:

1. The maximum sink current of the I²C buffer:

   The maximum sink current is 3 mA or slightly higher for an I²C driver supporting standard-mode I²C operation.

   $$R_{up(min)} = V_{DD} / Isink \quad (1)$$

2. The maximum transition time on the bus:

   The maximum transition time, T, of an I²C bus is set by an RC time constant, where R is the pullup resistor value and C is the total load capacitance. The parameter, k, can be calculated from Equation 3 by solving for t, the times at which certain voltage thresholds are reached. Different input threshold combinations introduce different values of t. Table 4 summarizes the possible values of k under different threshold combinations.

   $$t = k \times RC \quad (2)$$

   $$V(t) = V_{DD}\left(1 - e^{-t/RC}\right) \quad (3)$$

Table 4. Value of k for Different Input Threshold Voltages

V_{th-}/V_{th+}	0.7 V_{DD}	0.65 V_{DD}	0.6 V_{DD}	0.55 V_{DD}	0.5 V_{DD}	0.45 V_{DD}	0.4 V_{DD}	0.35 V_{DD}	0.3 V_{DD}
0.1 V_{DD}	1.0986	0.9445	0.8109	0.6931	0.5878	0.4925	0.4055	0.3254	0.2513
0.15 V_{DD}	1.0415	0.8873	0.7538	0.6360	0.5306	0.4353	0.3483	0.2683	0.1942
0.2 V_{DD}	0.9808	0.8267	0.6931	0.5754	0.4700	0.3747	0.2877	0.2076	0.1335
0.25 V_{DD}	0.9163	0.7621	0.6286	0.5108	0.4055	0.3102	0.2231	0.1431	0.0690
0.3 V_{DD}	0.8473	0.6931	0.5596	0.4418	0.3365	0.2412	0.1542	0.0741	—

From Equation 1, $R_{up(min)}$ = 5.5 V/3 mA = 1.83 kΩ to operate the bus under a 5-V pullup voltage and provide less than 3 mA when the I^2C device is driving the bus to a low state. If a higher sink current, for example 4 mA, is allowed, $R_{up(min)}$ can be as low as 1.375 kΩ.

Given a 5-V I^2C device with input low- and high-threshold voltages at 0.3 V_{dd} and 0.7 V_{dd}, respectively, the value of k is 0.8473 from Table 4. Taking into account the 1.83-kΩ pullup resistor, the maximum total load capacitance is $C_{(total-5V)}$ = 645 pF. $C_{cable(max)}$ should be restricted to be less than 545 pF if C_{source} and C_i can be as high as 50 pF. Here the C_i is treated as C_{sink}, the load capacitance of a sink device.

Fixing the maximum transition time from Table 4, T = 1 µs, and using the k values from Table 4, the recommended maximum total resistance of the pullup resistors on an I^2C bus can be calculated for different system setups.

To support the maximum load capacitance specified in the HDMI spec, $C_{cable(max)}$ = 700 pF/C_{source} = 50 pF/C_i = 50 pF, $R_{(max)}$ can be calculated as shown in Table 5.

Table 5. Pullup Resistor for Different Threshold Voltages and 800-pF Load

V_{th-}/V_{th+}	0.7 V_{DD}	0.65 V_{DD}	0.6 V_{DD}	0.55 V_{DD}	0.5 V_{DD}	0.45 V_{DD}	0.4 V_{DD}	0.35 V_{DD}	0.3 V_{DD}	UNIT
0.1 V_{DD}	1.14	1.32	1.54	1.80	2.13	2.54	3.08	3.84	4.97	kΩ
0.15 V_{DD}	1.20	1.41	1.66	1.97	2.36	2.87	3.59	4.66	6.44	kΩ
0.2 V_{DD}	1.27	1.51	1.80	2.17	2.66	3.34	4.35	6.02	9.36	kΩ
0.25 V_{DD}	1.36	1.64	1.99	2.45	3.08	4.03	5.60	8.74	18.12	kΩ
0.3 V_{DD}	1.48	1.80	2.23	2.83	3.72	5.18	8.11	16.87	—	kΩ

Or, limiting the maximum load capacitance of each cable to 400 pF to accommodate with I^2C specification version 2.1, $C_{cable(max)}$ = 400 pF/C_{source} = 50 pF/C_i = 50 pF, the maximum values of $R_{(max)}$ are calculated as shown in Table 6.

Table 6. Pullup Resistor for Different Threshold Voltages and 500-pF Load

V_{th-}/V_{th+}	0.7 V_{DD}	0.65 V_{DD}	0.6 V_{DD}	0.55 V_{DD}	0.5 V_{DD}	0.45 V_{DD}	0.4 V_{DD}	0.35 V_{DD}	0.3 V_{DD}	UNIT
0.1 V_{DD}	1.82	2.12	2.47	2.89	3.40	4.06	4.93	6.15	7.96	kΩ
0.15 V_{DD}	1.92	2.25	2.65	3.14	3.77	4.59	5.74	7.46	10.30	kΩ
0.2 V_{DD}	2.04	2.42	2.89	3.48	4.26	5.34	6.95	9.63	14.98	kΩ
0.25 V_{DD}	2.18	2.62	3.18	3.92	4.93	6.45	8.96	13.98	28.99	kΩ
0.3 V_{DD}	2.36	2.89	3.57	4.53	5.94	8.29	12.97	26.99	—	kΩ

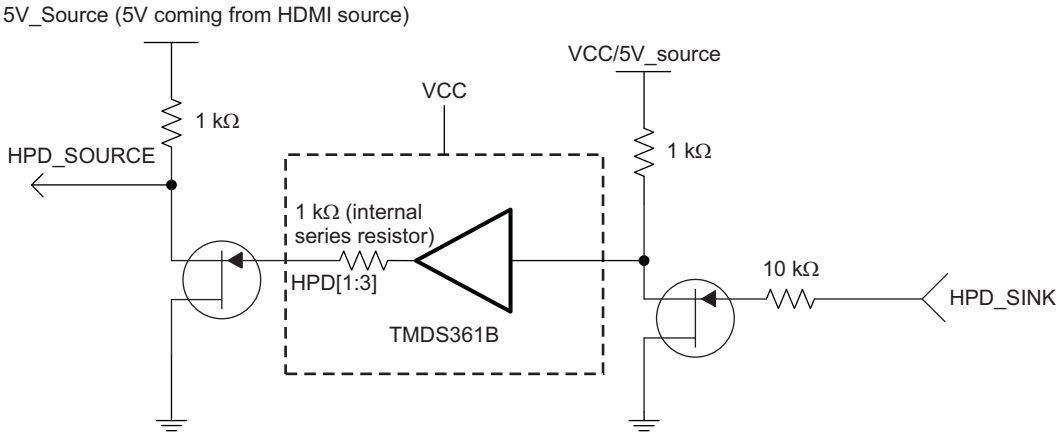
Obviously, to accommodate the 3-mA drive-current specification, a narrower threshold voltage range is required to support a maximum 800-pF load capacitance for a standard-mode I^2C bus.

When the input low- and high-level threshold voltages, V_{th-} and V_{th+}, are 0.7 V and 1.9 V, respectively, which is 0.15 V_{DD} and 0.4 V_{DD}, approximately, then with V_{DD} = 5 V from Table 5, the maximum pullup resistor is 3.59 kΩ. The allowable pullup resistor is in the range of 1.83 kΩ and 3.59 kΩ.

HPD Pins

The HPD circuits are powered by the 3.3-V VCC supply. This provides maximum V_{OH} = VCC and maximum V_{OL}= 0.4-V output signals to the SOURCE with a typical 1-kΩ output resistance. An external 1-kΩ resistor is not needed here. The HPD output of the selected source port follows the logic level of the HPD_SINK input. Unselected HPD outputs are kept low. When the device is in standby mode, all HPD outputs follow HPD_SINK.

If V_{OH} greater than VCC is desired, then an external circuit as shown in Figure 45 can be used. In this case, the max V_{OH} can be equal to the 5 V coming from the HDMI source.



VCC	HPD_SINK	HPD[1:3]	HPD_SOURCE
ON	L	H	L
ON	H	L	H
OFF	X	Z	H

S0387-08

Figure 45. External Circuit to Drive 5-V V_{OH} on HPD[1:3]

Layout Considerations

The high-speed differential TMDS inputs are the most critical paths for the TMDS361B. There are several considerations to minimize discontinuities on these transmission lines between the connectors and the device:

- Maintain 100-Ω differential transmission line impedance into and out of the TMDS361B.
- Keep an uninterrupted ground plane beneath the high-speed I/Os.
- Keep the ground-path vias to the device as close as possible to allow the shortest return current path.
- Keep the trace lengths of the TMDS signals between connector and device as short as possible.
- Keep intra-pair skew (trace length) between the positive and negative TMDS inputs to be matched to within 5 mils (0.005 inches or 0.127 mm).

Using the TMDS361B in Systems With Different CEC Link Requirements

The TMDS361B supports a DTV with up to three HDMI inputs when used in conjunction with a signal-port HDMI receiver. Figure 46 and Figure 47 show simplified application block diagrams for the TMDS361B in different DTVs with different consumer electronic control (CEC) requirements. The CEC is an optional feature of the HDMI interface for centralizing and simplifying user control instructions from multiple audio/video products in an interconnected system, even when all the audio/video products are from different manufacturers. This feature minimizes the number of remote controls in a system, as well as reducing the number of times buttons must be pressed.

A DTV Supporting a Passive CEC Link

In Figure 46, the DTV does not have the capability of handling CEC signals, but allows CEC signals to pass over the CEC bus. The source selection is done by the control command of the DTV. The user cannot force the command from any audio/video product on the CEC bus. The selected source reads the E-EDID data after receiving an asserted HPD signal. The microcontroller loads different CEC physical addresses while changing the source by means of the S1 and S2 pins.

E-EDID Reading Configurations in Standby Mode

When the DTV system is in standby mode, the sources do not read the E-EDID memory because the 1-kΩ pulldown resistor keeping the HPD_SINK input at logic-low forces all HPD pins to output logic-low to all sources. The source does not read the E-EDID data with a low on the HPD signal. However, if reading the E-EDID data in the system standby mode is preferred, then the TMDS361B can still support this need.

The recommended configuration sequences are:

1. Apply the same 3.3-V power to the VCC of the TMDS361B and the TMDS line termination at the HDMI receiver.
2. Because the TMDS361B has clock-detect circuitry and there is no valid input TMDS clock in the standby mode, the TMDS361B draws significanty less current.
3. Set S1 and S2 to select the source port which is allowed to read the E-EDID memory.

Note that if the source has a time-out limitation between the 5-V and the HPD signals, the foregoing configuration is not applicable. Uses individual EEPROMs assigned for each input port, see Figure 47. The solution uses E-EDID data to be readable during system power-off or standby-mode operations.

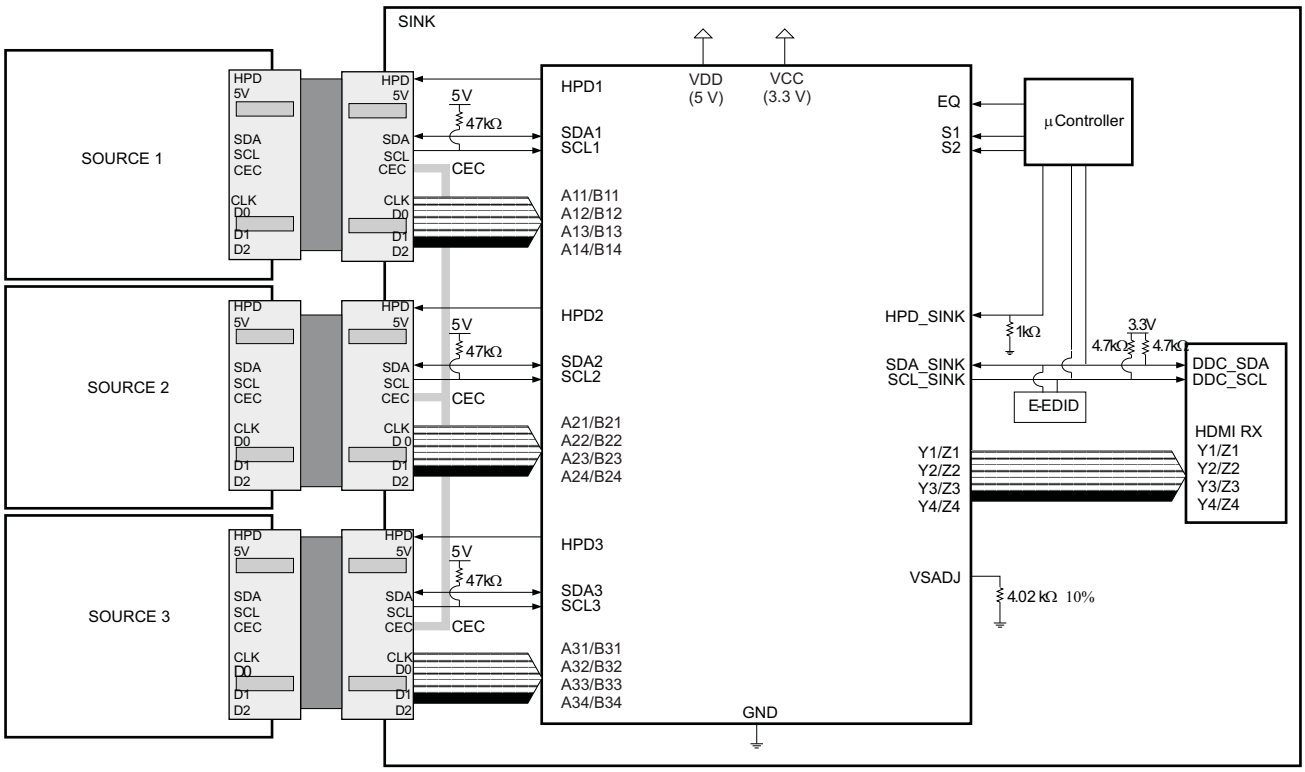


Figure 46. Three-Port HDMI-Enabled DTV With TMDS361B – CEC Commands Passing Through

A DTV Supporting an Active CEC Link

In Figure 47, the CEC PHY and CEC LOGIC functions are added. The DTV can initiate and/or react to CEC signals from its remote control or other audio/video products on the same CEC bus. All sources must have their own CEC physical address to support the full functionality of the CEC link.

A source reads its CEC physical address stored its E-EDID memory after receiving a logic-high from the HPD feedback. When HPD is high, the sink-assigned CEC physical address should be maintained. Otherwise, when HPD is low, the source sets the CEC physical address value to (F.F.F.F).

Case 1 – AC-Coupled Source (See Figure 47, Port 1)

When the source TMDS lines are ac-coupled or when the source cannot detect the TMDS termination provided in the connected sink, the indication of the source selection can only come from the HPD signal. The TMDS361B HPD1 pin should be applied directly as the HPD signal back to the source.

Case 2 – DC-Coupled Source (See Figure 47, Port 2)

When the source TMDS lines are dc-coupled, there are two methods to inform the source that it is the active source to the sink. One is checking the HPD signal from the sink, and the other is checking the termination condition in the sink.

In a full-CEC operation mode, the HPD signal is set high whether the port is selected or not. The source loads and maintains the CEC physical address when HPD is high. As soon as HPD goes low, the source loses the CEC physical address. To keep the CEC physical address to the source, the HPD signal loops back from the source-provided 5-V signal through a 1-kΩ pullup resistor in the sink. This method is acceptable in applications where the HDMI transmitter can detect the receiver termination by current sensing and the receiver has switchable termination on the TMDS inputs. The internal termination resistors are connected to the termination voltage when the port is selected, or they are disconnected when the port is not selected. The TMDS361B features switchable termination on the TMDS inputs.

Case 3 – External Logic Control for HPD (See Figure 47, Port 3)

When the HDMI transmitter does not have the capability of detecting the receiver termination, using the HPD signal as a reference for sensing port selections is the only possible method. External control logic for switching the connections of the HPD signals between the HPD pins of the TMDS361B and the 5-V signal from the source provides a good solution.

E-EDID Reading Configurations in Standby Mode

When the TMDS361B is in standby mode operation, S1 = H and S2 = L, all sources can read their E-EDID memories simultaneously with all HPD pins following HPD_SINK in logic-high. HPD_SINK input low prevents E-EDID reading in standby-mode operation. See Figure Figure 47.

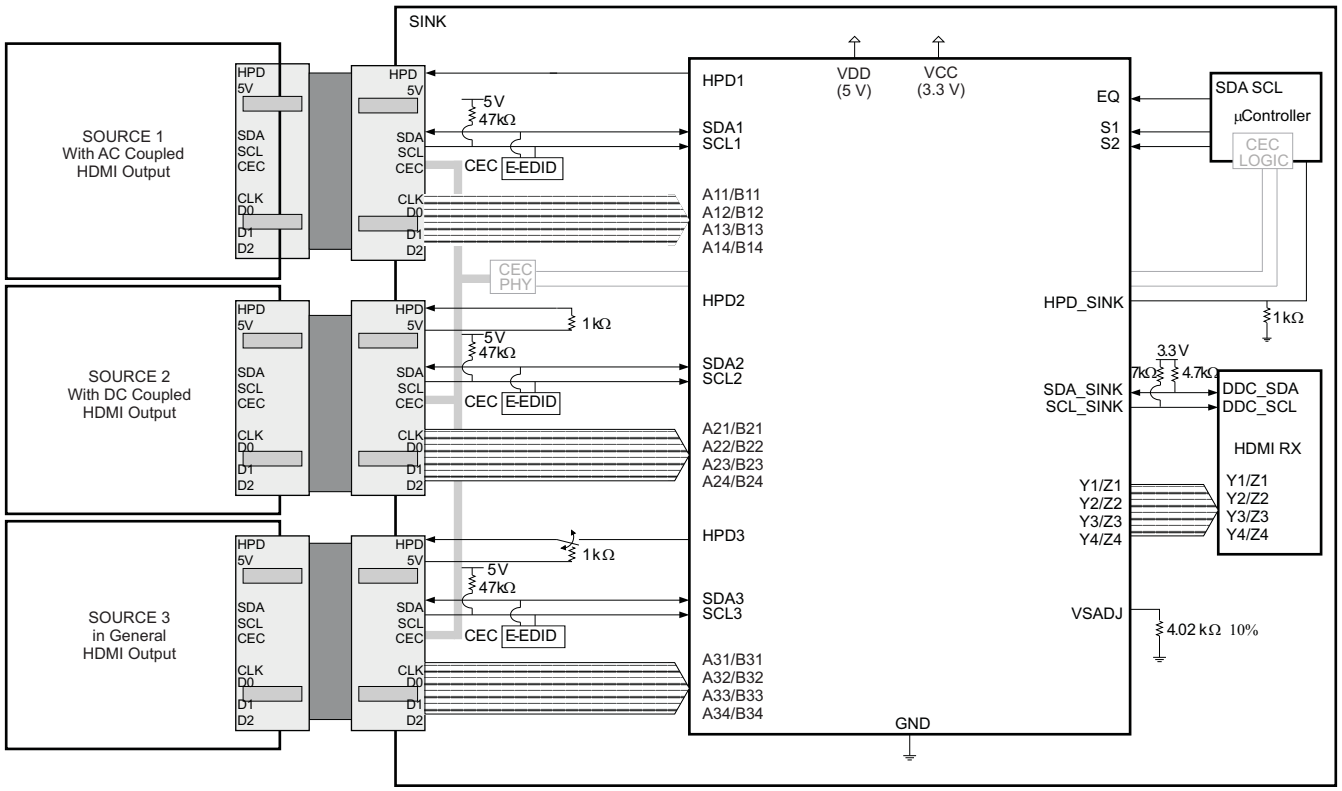


Figure 47. Three-Port HDMI-Enabled DTV With TMDS361B – CEC Commands Active

I²C INTERFACE NOTES

The I²C interface is used to access the internal registers of the TMDS361B. I²C is a two-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through open-drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device. The TMDS361B works as a slave and supports standard-mode transfer (100 kbps).

The basic I²C start and stop access cycles are shown in Figure 48.

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

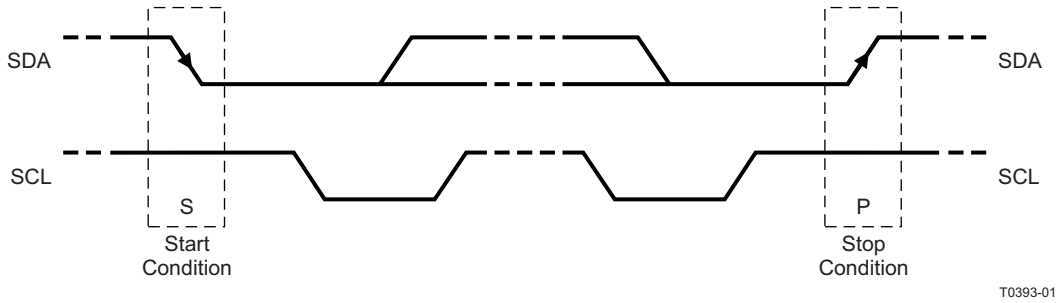


Figure 48. I²C Start and Stop Conditions

GENERAL I²C PROTOCOL

- The *master* initiates data transfer by generating a *start condition*. The *start condition* is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 48. All I²C-compatible devices should recognize a *start condition*.
- The master then generates the SCL pulses and transmits the 7-bit address and the *read/write direction bit* R/W on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid data* condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 49). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see Figure 50) by driving the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to either *transmit* data to the slave (R/W bit 0) or *receive* data from the slave (R/W bit 1). In either case, the *receiver* must acknowledge the data sent by the *transmitter*. So an acknowledge signal can be generated either by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (See Figure 52 through Figure 55).
- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see Figure 48). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a *stop condition*, all devices know that the bus is released, and they wait for a *start condition* followed by a matching address.

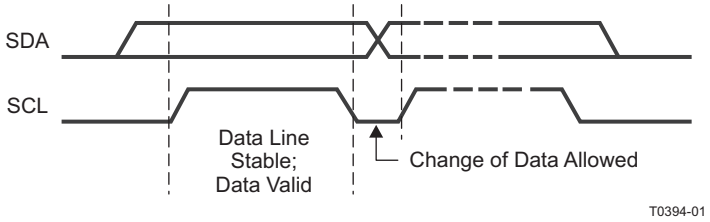


Figure 49. I²C Bit Transfer

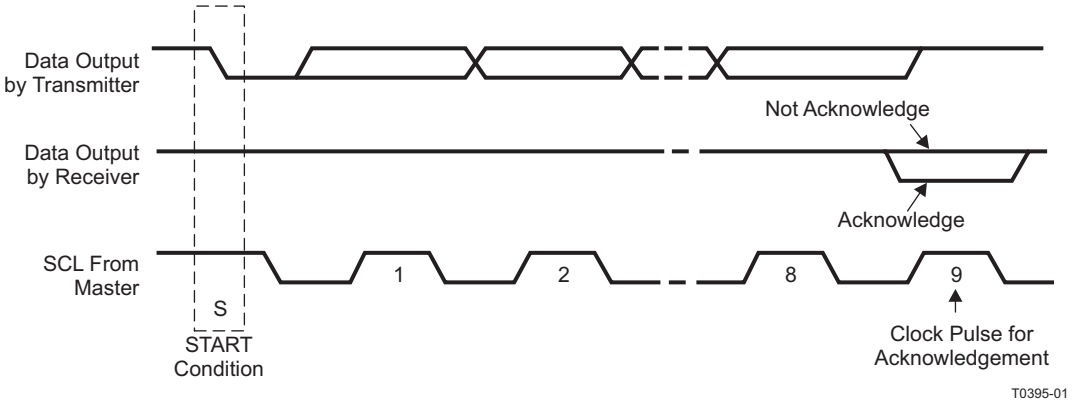


Figure 50. I²C Acknowledge

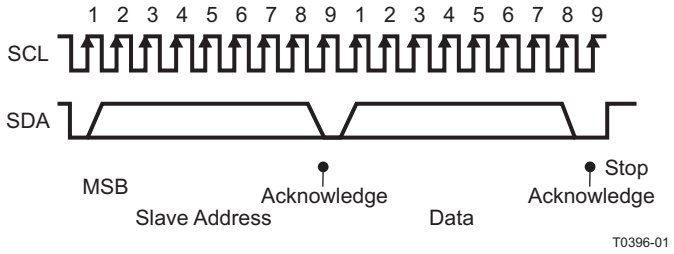


Figure 51. I²C Address, Data Cycle(s), and Stop

During a write cycle, the transmitting device must not drive the SDA signal line during the acknowledge cycle so that the receiving device may drive the SDA signal low. After each byte transfer following the address byte, the receiving device pulls the SDA line low for one SCL clock cycle. A stop condition is initiated by the transmitting device after the last byte is transferred. An example of a write cycle can be found in Figure 52 and Figure 53. Note that the TMDS361B allows multiple write transfers to occur. See the *Example – Writing to the TMDS361A* section for more information.

During a read cycle, the slave receiver acknowledges the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not-acknowledge ($\overline{A}$) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle as shown in Figure 54 and Figure 55. See the *Example – Reading from the TMDS361A* section for more information.

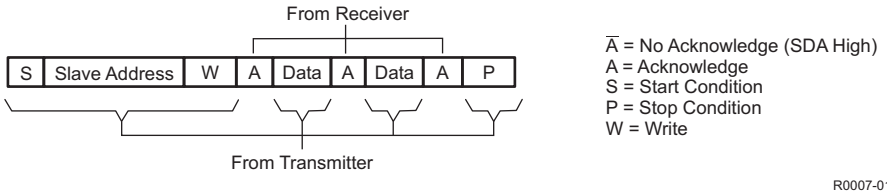


Figure 52. I²C Write Cycle

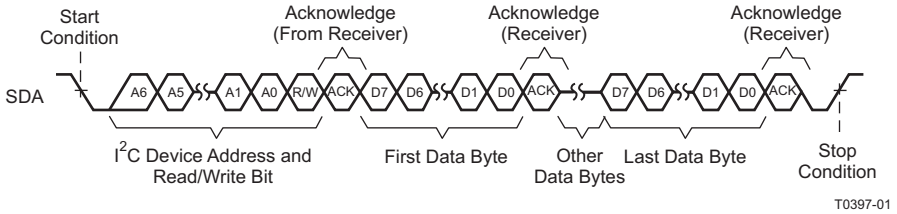


Figure 53. Multiple-Byte Write Transfer

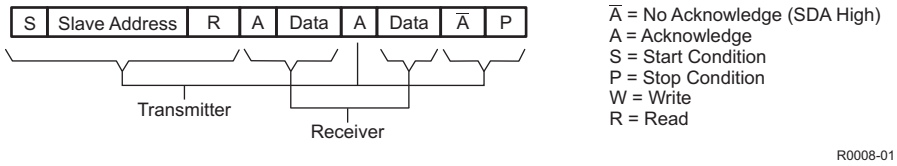


Figure 54. I²C Read Cycle

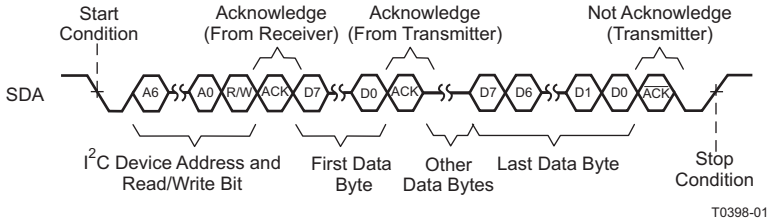


Figure 55. Multiple-Byte Read Transfer

Slave Address

Both SDA and SCL must be connected to a positive supply voltage via pullup resistors. These resistors should comply with the I²C specification that ranges from 2 kΩ to 19 kΩ. When the bus is free, both lines are high. The address byte is the first byte received following the START condition from the master device. The 7-bit address is factory preset to 0101 100. Table 7 lists the calls to which the TMDS361B responds.

Table 7. TMDS361B Slave Address

FIXED ADDRESS							READ/WRITE BIT
Bit 7 (MSB)	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (R/W)**
0	1	0	1	1	0	0	1/0

EXAMPLE – WRITING TO THE TMDS361B

The proper way to write to the TMDS361B is illustrated as follows:

An I²C master initiates a write operation to the TMDS361B by generating a start condition (S) followed by the TMDS361B I²C address (as shown following, in MSB-first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the TMDS361B, the master presents the subaddress (sink port) to be written, consisting of one byte of data, MSB-first. The TMDS361B acknowledges the byte after completion of the transfer. Finally, the master presents the data to be written to the register (sink port), and the TMDS361B acknowledges the byte. The master can continue presenting data to be written after the TMDS361B acknowledges the previous byte (steps 6, 7). After the last byte to be written has been acknowledged by the TMDS361B, the I²C master then terminates the write operation by generating a stop condition (P).

Step 1	**0**
I²C start (master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C general address (master)	0	1	0	1	1	0	0	0

Step 3	8
I^2C acknowledge (slave)	A

Step 4	7	6	5	4	3	2	1	0
I^2C write sink logic address (master)	0	0	0	0	Addr	Addr	Addr	Addr

Step 5	8
I^2C acknowledge (slave)	A

Step 6	7	6	5	4	3	2	1	0
I^2C write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

Data is the register address or register data to be written.

Step 7	8
I^2C acknowledge (slave)	A

Step 8	0
I^2C stop (master)	P

An example of the proper bit control for selecting port 2 is:

Step 4: 0000 0001

Step 6: 1001 0000

EXAMPLE – READING FROM THE TMDS361B

The read operation consists of two phases. The first phase is the address phase. In this phase, an I^2C master initiates a write operation to the TMDS361B by generating a start condition (S) followed by the TMDS361B I^2C address, in MSB-first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledges from the TMDS361B, the master presents the subaddress of the register to be read. After the cycle is acknowledged (A), the master may optionally terminate the cycle by generating a stop condition (P).

The second phase is the data phase. In this phase, an I^2C master initiates a read operation to the TMDS361B by generating a start condition followed by the TMDS361B I^2C address (as shown following for a read operation), in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the TMDS361B, the I^2C master receives one byte of data from the TMDS361B. The master can continue receiving data byes by issuing an acknowledge after each byte read (steps 10, 11). After the last data byte has been transferred from the TMDS361B to the master, the master generates a not-acknowledge followed by a stop.

TMDS361B Read Phase 1

Step 1	0
I^2C start (master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C general address (master)	0	1	0	1	1	0	0	0

Step 3	8
I^2C acknowledge (slave)	A

Step 4	7	6	5	4	3	2	1	0
I²C write sink logic address (master)	0	0	0	0	Addr	Addr	Addr	Addr

Where Addr is determined by the values shown in Table 7.

Step 5	8
I²C acknowledge (slave)	A

Step 6	0
I²C stop (master)	P

Step 6 is optional.

TMDS361B Read Phase 2

Step 7	0
I²C start (master)	S

Step 8	7	6	5	4	3	2	1	0
I²C general address (master)	0	1	0	1	1	0	0	1

Step 9	8
I²C acknowledge (slave)	A

Step 10	7	6	5	4	3	2	1	0
I²C read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

Where Data is determined by the logic values contained in the internal registers.

Step 11A	8
I²C acknowledge (master)	A

If Step 11A is executed, go to step 10. If Step 11B is executed, go to Step 12.

Step 11B	8
I²C not-acknowledge (master)	$\overline{A}$

Step 12	0
I²C stop (master)	P

Table 8. I²C Register 0x01 Lookup Table

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7:6	**Bit 7**	**Bit 6**		**Port Select I²C Mode**
	1	1	X	Port 1 is selected as the active port; HPD on non-selected ports is low. HPD1 can go low, high or high-Z.
	1	0		Port 2 is selected as the active port; HPD on non-selected ports is low. HPD2 can go low, high or high-Z.
	0	0		Port 3 is selected as the active port; HPD on non-selected ports is low. HPD3 can go low, high or high-Z.
	0	1		Standby mode: HPD[1:3] follow HPD_SINK.
5:4	**Bit 4**	**Bit 3**		**OVS Control**
	0	0		OVS2: DDC sink-side V_{OL} and V_{IL} offset range 2: $V_{IL2\ (max)}$: 0.4 V, $V_{OL2\ (max)}$: 0.6 V
	0	1	X	OVS3: DDC sink-side V_{OL} and V_{IL} offset range 3: $V_{IL3\ (max)}$: 0.3 V, $V_{OL3\ (max)}$: 0.5 V
	1	1		OVS1: DDC sink-side V_{OL} and V_{IL} offset range 1: $V_{IL1\ (max)}$: 0.4 V, $V_{OL1\ (max)}$: 0.7 V

Table 8. I²C Register 0x01 Lookup Table (continued)

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
3:2	**Bit 3**	**Bit 2**		**Output Edge Rate Control**
	1	1		Fastest TMDS output rise- and fall-time setting + 120 ps approximately (slowest rise- and fall-time setting)
	1	0		Fastest TMDS output rise- and fall-time setting + 100 ps approximately
	0	1		Fastest TMDS output rise- and fall-time setting + 50 ps approximately
	0	0	X	Fastest TMDS output rise- and fall-time setting
1:0	**Bit 1**	**Bit 0**		**Power Mode**
	1	0		Device enters low-power mode.
	1	1		Device enters low-power mode.
	0	1		Reserved
	0	0	X	Device is in normal-power mode.

Register 0x01 is read/write.

Table 9. I²C Register 0x02 Lookup Table

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7:6	**Bit 7**	**Bit 6**		**Port Select Status Indicator**
	1	1	X	Indicates port 1 is selected as the active port, all other ports are low.
	1	0		Indicates port 2 is selected as the active port, all other ports are low.
	0	0		Indicates port 3 is selected as the active port, all other ports are low.
	0	1		Indicates standby mode: HPD[1:3] follow HPD_SINK.
5:4	**Bit 4**	**Bit 3**		**OVS Control Status Indicator**
	0	0		Indicates DDC sink side V_{OL} and V_{IL} offset range 2: $V_{IL2\ (max)}$: 0.4 V, $V_{OL2\ (max)}$: 0.6 V
	0	1	X	Indicates DDC sink side V_{OL} and V_{IL} offset range 3: $V_{IL3\ (max)}$: 0.3 V, $V_{OL3\ (max)}$: 0.5 V
	1	1		Indicates DDC sink side V_{OL} and V_{IL} offset range 1: $V_{IL1\ (max)}$: 0.4 V, $V_{OL1\ (max)}$: 0.7 V
3:2	**Bit 3**	**Bit 2**		**Output Edge Rate Status Control**
	1	1		Indicates fastest TMDS output rise- and fall-time setting + 120 ps approximately (slowest rise and fall time setting)
	1	0		Indicates fastest TMDS output rise- and fall-time setting + 100 ps approximately
	0	1		Indicates fastest TMDS output rise- and fall-time setting + 50 ps approximately
	0	0	X	Indicates fastest TMDS output rise- and fall-time setting
1:0	**Bit 1**	**Bit 0**		**Power Mode Status Indicator**
	1	0		Indicates device enters low-power mode
	1	1		Indicates device enters low-power mode
	0	1		Reserved
	0	0	X	Indicates device is in normal-power mode

Register 0x02 is read-only.

Table 10. I²C Register 0x03 Lookup Table

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7	1	Clock detect disabled		Clock-detect circuit disabled. For HDMI compliance testing (TMDS termination-voltage test), the clock-detect feature should be disabled. In this mode, the terminations on the TMDS input data lines are always connected when the port is selected.
	0	Clock detect enabled	X	Clock-detect circuit enabled. It is recommended that TMDS361B is used in this default mode during normal operation where the clock detect circuit is enabled. The terminations on the TMDS input data lines are connected only when a valid TMDS clock is detected on the selected port.
6:5	X	RSVD		Reserved
4	0	RSVD	X	Note: Do not write a 1 to this bit.
3:0	0	RSVD	X	Reserved

Register 0x03 is read/write, For disabling clock detect, value of 80h or 1000 0000b can be written to register 0x03.

Table 11. I²C Register 0x04 Lookup Table

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7	1	Clock detected		A valid clock signal is detected on the selected port. If clock detect is disabled in register 0x03, then bit 7 of register 0x04 is always 1.
	0	No clock detect	X	The selected port does not have a valid clock signal.
6:5	X	RSVD		Reserved
4	0	RSVD	X	This bit should always read 0
3:0	0	RSVD	X	Reserved

Register 0x04 is read-only.

Table 12. I²C Register 0x05 Lookup Table

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7:0	—	RSVD	X	Reserved. Read-only, value is indeterministic.

Register 0x05 is TI internal use only.

Table 13. I²C Register 0x06 Lookup Table

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7:0	—	RSVD	X	Reserved. Read-only, value is indeterministic.

Register 0x06 is TI internal use only.

Table 14. I²C Register 0x07 Lookup Table

BIT	VALUE	STATE	DEFAULT	DESCRIPTION
7:0	—	RSVD	X	Reserved. Read-only, value is indeterministic.

Register 0x07 is TI internal use only.

REVISION HISTORY

Changes from Original (September 2009) to Revision A **Page**

- Added Junction Temperature to the THERMAL CHARACTERISTICS table 9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TMDS361BPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TMDS361BPAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

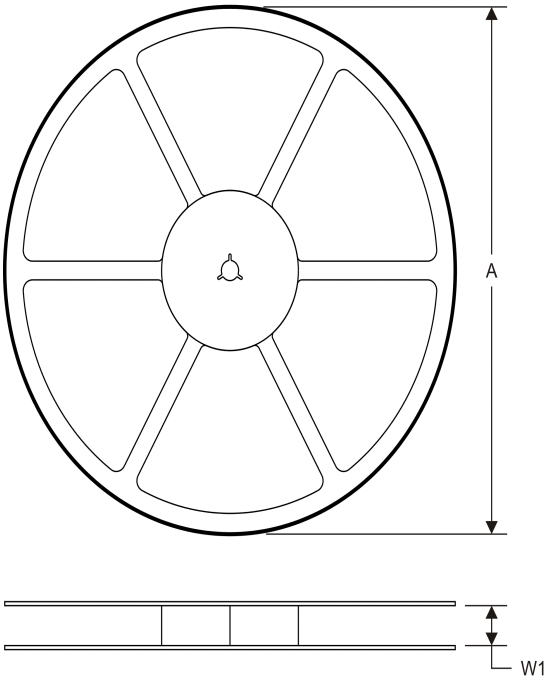
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

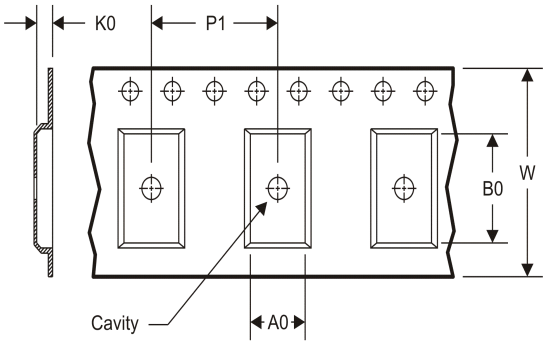
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



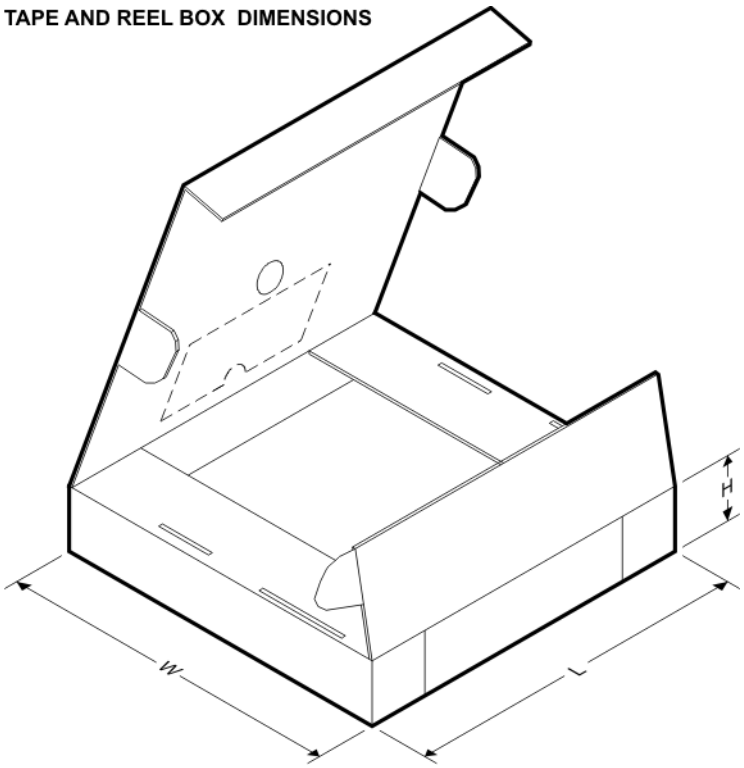
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMDS361BPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

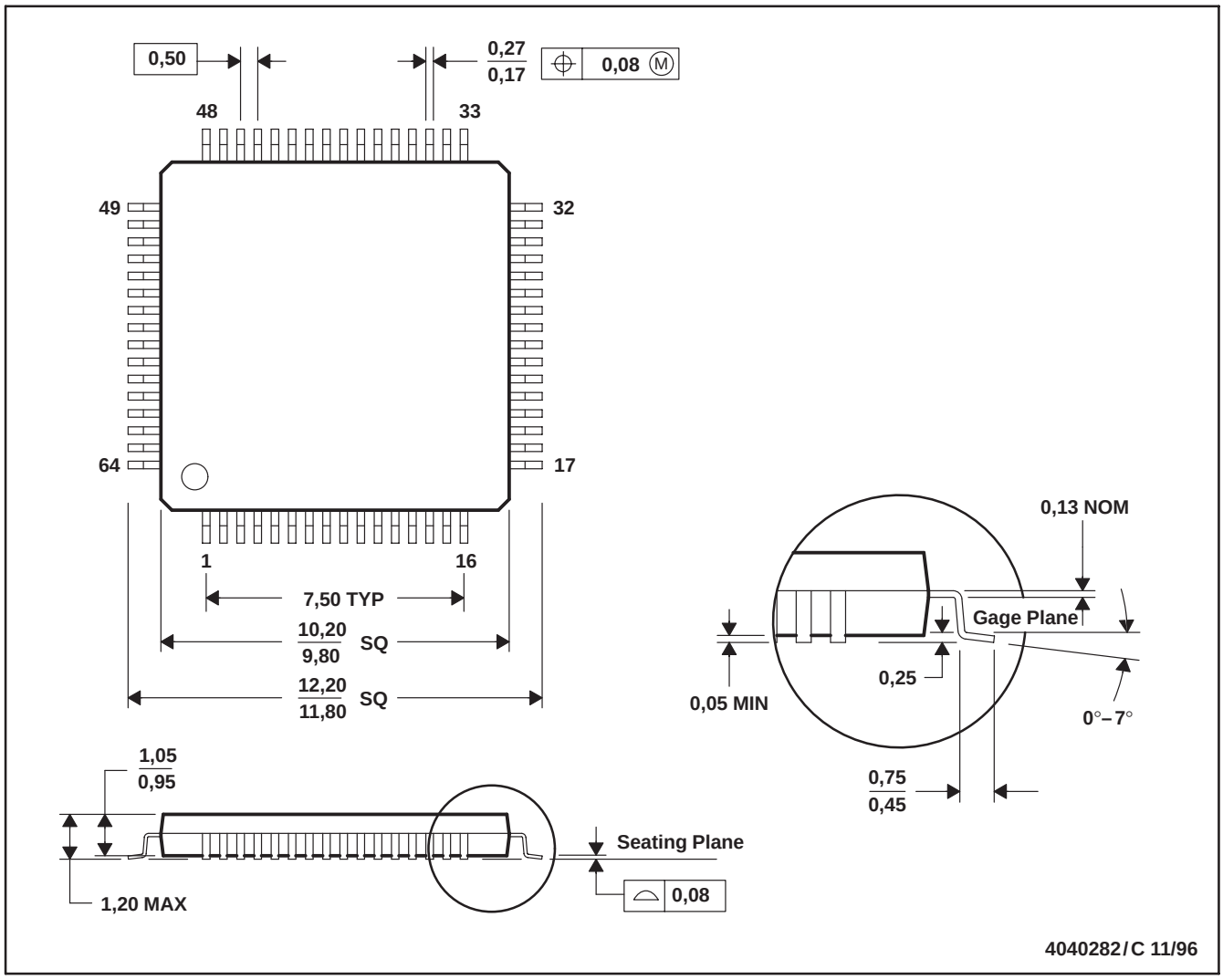
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

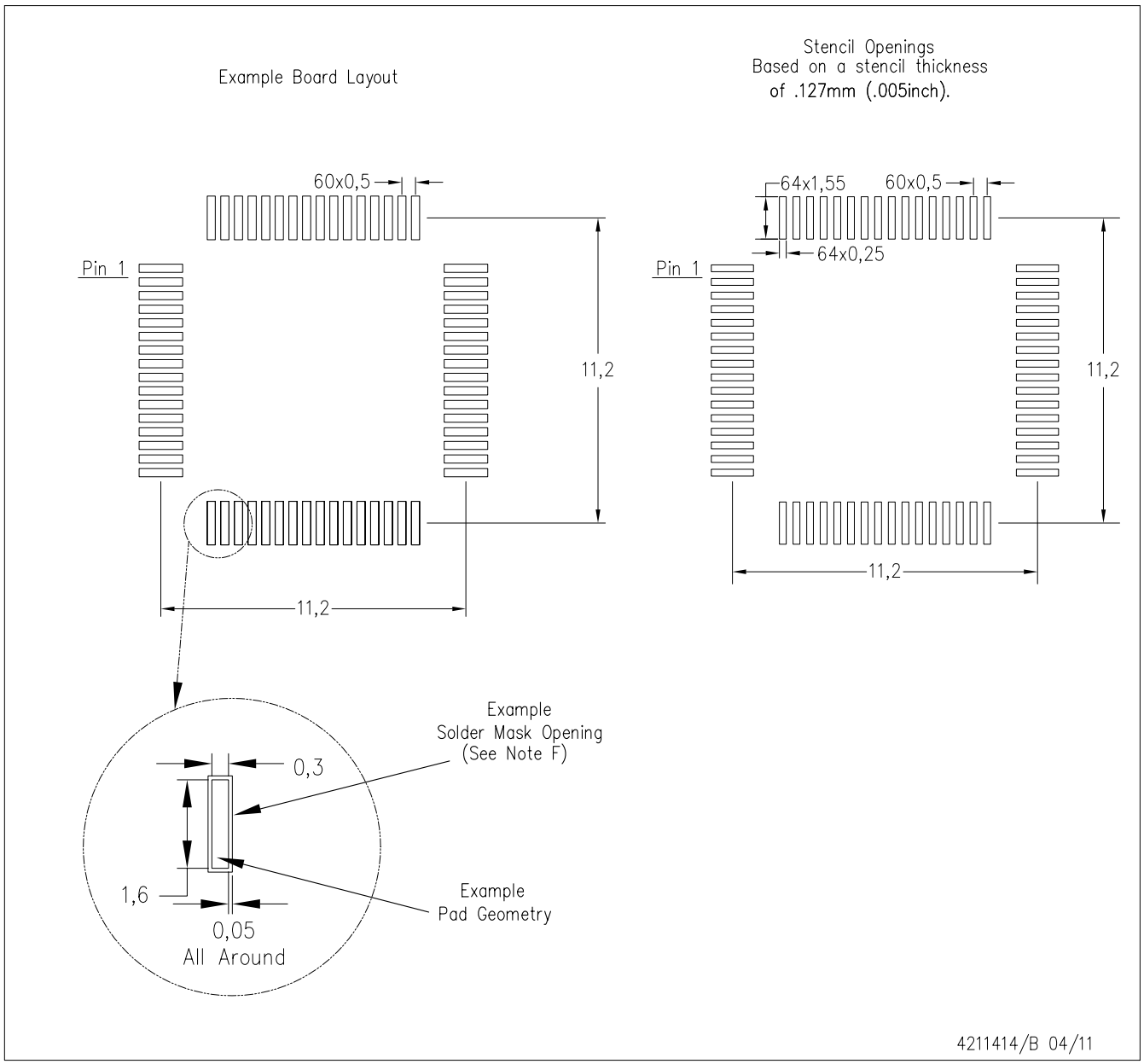
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMDS361BPAGR	TQFP	PAG	64	1500	367.0	367.0	45.0

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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