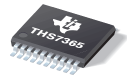


6-Channel Video Amplifier with 3-SD and 3-HD Sixth-Order Filters and 6-dB Gain

FEATURES

- **Three SDTV Video Amplifiers for CVBS, S-Video, Y'/P'$_B$/P'$_R$, 480i/576i, Y'U'V', or R'G'B'**
- **Three HDTV Video Amplifiers for Y'/P'$_B$/P'$_R$, 720p/1080i/1080p30, or G'B'R' (R'G'B')**
- **Bypassable Sixth-Order Low-Pass Filters:**
  - **SD Channels: –3 dB at 9.5-MHz**
  - **HD Channels: –3 dB at 36-MHz**
- **Versatile Input Biasing:**
  - **DC-Coupled with 300-mV Output Shift**
  - **AC-Coupled with Sync-Tip Clamp**
  - **AC-Coupling with Biasing**
- **Built-in 6-dB Gain (2 V/V)**
- **+2.7-V to +5-V Single-Supply Operation**
- **Rail-to-Rail Output:**
  - **Output Swings Within 100 mV from the Rails: Allows AC or DC Output Coupling**
  - **Supports Driving Two Video Lines/Channel**
- **Low Total Quiescent Current: 20.7 mA at 3.3 V**
- **Disabled Supply Current Function: 0.1 μA**
- **Low Differential Gain/Phase: 0.2%/0.3°**
- **RoHS-Compliant Package: TSSOP-20**

APPLICATIONS

- **Set Top Box Output Video Buffering**
- **PVR/DVDR/BluRay™ Output Buffering**
- **Low-Power Video Buffering**

DESCRIPTION

Fabricated using the revolutionary, complementary Silicon-Germanium (SiGe) BiCom3X process, the THS7365 is a low-power, single-supply, 2.7-V to 5-V, six-channel integrated video buffer. It incorporates three standard-definition (SDTV) and three high-definition (HDTV) filter channels. All filters feature bypassable sixth-order Butterworth filter characteristics that are useful as digital-to-analog converter (DAC) reconstruction filters or as analog-to-digital converter (ADC) anti-aliasing filters.

The THS7365 has flexible input coupling capabilities that can be configured for either ac- or dc-coupled inputs. The 300-mV output level shift allows for a full sync dynamic range at the output with 0-V input. The ac-coupled modes include a transparent sync-tip clamp for composite video (CVBS), Y', and R'G'B' signals with sync. AC-coupled biasing for C'/P'$_B$/P'$_R$ channels can easily be achieved by adding an external resistor to V_{S+}.

The THS7365 is an ideal choice for all video buffer applications. Its rail-to-rail output stage with 6-dB gain allows for both ac and dc line driving. The ability to drive two lines per channel, or 75-Ω loads, allows for maximum flexibility as a video line driver. The 20.7-mA total quiescent current at 3.3 V and 0.1 μA (disabled mode) makes it an excellent choice for power-sensitive video applications.

The THS7365 is available in a TSSOP-20 package that is lead-free and green (RoHS-compliant).

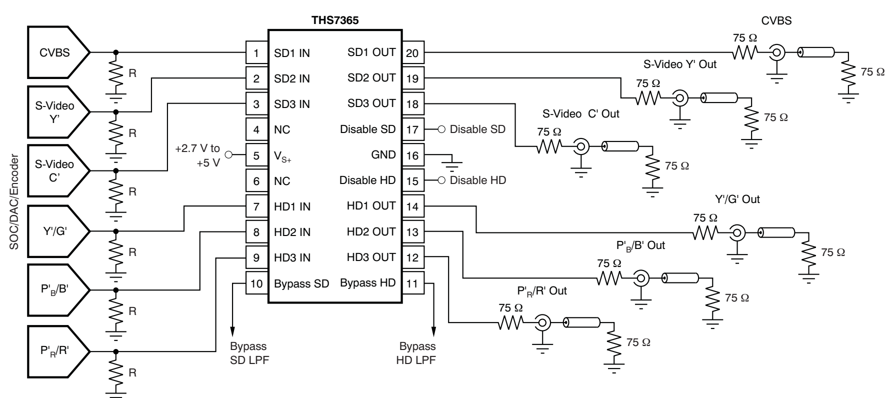


Figure 1. Single-Supply, DC-Input/DC-Output Coupled Video Line Driver

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)(2)

PRODUCT	PACKAGE-LEAD	TRANSPORT MEDIA, QUANTITY	ECO STATUS(2)
THS7365IPW	TSSOP-20	Rails, 70	Pb-Free, Green
THS7365IPWR		Tape and Reel, 2000	

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) These packages conform to Lead (Pb)-free and green manufacturing specifications. Additional details including specific material content can be accessed at www.ti.com/leadfree.
GREEN: TI defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight. N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree. Pb-FREE: TI defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		THS7365	UNIT
Supply voltage, V_{S+} to GND		5.5	V
Input voltage, V_I		–0.4 to V_{S+}	V
Output current, I_O		±90	mA
Continuous power dissipation		See the Dissipation Ratings Table	
Maximum junction temperature, any condition(2), T_J		+150	°C
Maximum junction temperature, continuous operation, long-term reliability(3), T_J		+125	°C
Storage temperature range, T_{STG}		–60 to +150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		+300	°C
ESD rating:	Human body model (HBM)	4000	V
	Charge device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	AT $T_A \leq$ +25°C POWER RATING	AT T_A = +85°C POWER RATING
TSSOP-20 (PW)	36	88(1)	1.13 W	0.45 W

(1) These data were taken with the JEDEC High-K test printed circuit board (PCB). For the JEDEC low-K test PCB, the θ_{JA} is 130°C/W.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{S+}	2.7		5	V
Ambient temperature, T_A	–40		+85	°C

ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V

At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7365 MIN	THS7365 TYP	THS7365 MAX	UNITS	TEST LEVEL (1)
AC PERFORMANCE (SD CHANNELS)						
Passband bandwidth	–1 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	7	8.2	10.2	MHz	B
Small- and large-signal bandwidth	–3 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	7.8	9.5	11.4	MHz	B
Bypass mode bandwidth	–3 dB; V_O = 0.2 V_{PP}	85	130		MHz	B
Slew rate	Bypass mode; V_O = 2 V_{PP}	75	100		V/µs	B
Attenuation	With respect to 500 kHz (2), f = 6.75 MHz	–0.9	0.2	1.1	dB	B
	With respect to 500 kHz (2), f = 27 MHz	42	54		dB	B
Group delay	f = 100 kHz		72		ns	C
Group delay variation	f = 5.1 MHz with respect to 100 kHz		10		ns	C
Channel-to-channel delay			0.3		ns	C
Differential gain	NTSC/PAL		0.2/0.35		%	C
Differential phase	NTSC/PAL		0.3/0.42		Degrees	C
Total harmonic distortion	f = 1 MHz, V_O = 1.4 V_{PP}		–70		dB	C
Signal-to-noise ratio	100 kHz to 6 MHz, non-weighted		70		dB	C
	100 kHz to 6 MHz, unified weighting		78		dB	C
Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
	All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B
Output impedance	f = 6.75 MHz, Filter mode		0.7		Ω	C
	f = 6.75 MHz, Bypass mode		0.6		Ω	C
	Disabled		20 || 3		kΩ || pF	C
Return loss	f = 6.75 MHz, Filter mode		46		dB	C
Crosstalk	f = 1 MHz, SD to SD channel and SD to HD channel		–78		dB	C
AC PERFORMANCE (HD CHANNELS)						
Passband bandwidth	–1 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	27.2	32	38.2	MHz	B
Small- and large-signal bandwidth	–3 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	30.3	36	43	MHz	B
Bypass mode bandwidth	–3 dB; V_O = 0.2 V_{PP}	170	250		MHz	B
Slew rate	Bypass mode; V_O = 2 V_{PP}	420	500		V/µs	B
Attenuation	With respect to 500 kHz (2), f = 27 MHz	–1	0	1	dB	B
	With respect to 500 kHz (2), f = 74 MHz	34	42		dB	B
Group delay	f = 100 kHz		22		ns	C
Group delay variation	f = 27 MHz with respect to 100 kHz		7.5		ns	C
Channel-to-channel delay			0.3		ns	C
Differential gain	NTSC/PAL		0.1/0.1		%	C
Differential phase	NTSC/PAL		0.2/0.25		Degrees	C
Total harmonic distortion	f = 10 MHz, V_O = 1.4 V_{PP}		–49		dB	C
Signal-to-noise ratio	100 kHz to 30 MHz, non-weighted		62		dB	C
	100 kHz to 30 MHz, unified weighting		72		dB	C
Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
	All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation only. **(C)** Typical value only for information.
(2) 3.3-V supply filter specifications are ensured by 100% testing at 5-V supply along with design and characterization.

ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V (continued)

At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7365 MIN	THS7365 TYP	THS7365 MAX	UNITS	TEST LEVEL (1)
AC PERFORMANCE (HD CHANNELS) (continued)						
Output impedance	f = 30 MHz, Filter mode		1.7		Ω	C
	f = 30 MHz, Bypass mode		2		Ω	C
	Disabled		1.8 || 3		kΩ || pF	C
Return loss	f = 30 MHz, Filter mode		39		dB	C
Crosstalk	f = 1 MHz, HD to SD channels		–74		dB	C
	f = 1 MHz, SD to HD channels		–78		dB	C
	f = 1 MHz, HD to HD channels		–70		dB	C
DC PERFORMANCE						
Biased output voltage	V_{IN} = 0 V, SD channels	200	300	400	mV	A
	V_{IN} = 0 V, HD channels	200	295	400	mV	A
Input voltage range	DC input, limited by output		–0.1/1.46		V	C
Sync-tip clamp charge current	V_{IN} = –0.1 V, SD channels	140	200		µA	A
	V_{IN} = –0.1 V, HD channels	280	400		µA	A
Input impedance			800 || 2		kΩ || pF	C
OUTPUT CHARACTERISTICS						
High output voltage swing	R_L = 150 Ω to +1.65 V		3.15		V	C
	R_L = 150 Ω to GND	2.85	3.1		V	A
	R_L = 75 Ω to +1.65 V		3.1		V	C
	R_L = 75 Ω to GND		3		V	C
Low output voltage swing	R_L = 150 Ω to +1.65 V (V_{IN} = –0.2 V)		0.04		V	C
	R_L = 150 Ω to GND (V_{IN} = –0.2 V)		0.03	0.1	V	A
	R_L = 75 Ω to +1.65 V (V_{IN} = –0.2 V)		0.1		V	C
	R_L = 75 Ω to GND (V_{IN} = –0.2 V)		0.05		V	C
Output current (sourcing)	R_L = 10 Ω to +1.65 V		80		mA	C
Output current (sinking)	R_L = 10 Ω to +1.65 V		70		mA	C
POWER SUPPLY						
Operating voltage		2.6	3.3	5.5	V	B
Total quiescent current, no load	V_{IN} = 0 V, all channels on	17	20.7	27	mA	A
	V_{IN} = 0 V, SD channels on, HD channels off	5.6	6.9	9	mA	A
	V_{IN} = 0 V, SD channels off, HD channels on	11.4	13.8	18	mA	A
	V_{IN} = 0 V, all channels off, $V_{DISABLE}$ = 3 V		0.1	10	µA	A
Power-supply rejection ratio (PSRR)	At dc		52		dB	C
LOGIC CHARACTERISTICS (3)						
V_{IH}	Disabled or Bypass mode		1.8	2	V	A
V_{IL}	Enabled or Filter mode	0.65	0.7		V	A
I_{IH}			0.2		µA	C
I_{IL}			0.2		µA	C
Disable time			100		ns	C
Enable time			140		ns	C
Bypass/filter switch time			5		ns	C

(3) The logic input pins should not be left floating. They must be connected to logic low (or GND) or logic high (or V_{S+}).

ELECTRICAL CHARACTERISTICS: V_{S+} = +5 V

At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7365 MIN	THS7365 TYP	THS7365 MAX	UNITS	TEST LEVEL (1)
AC PERFORMANCE (SD CHANNELS)						
Passband bandwidth	–1 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	7	8.2	10.2	MHz	B
Small- and large-signal bandwidth	–3 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	7.8	9.5	11.4	MHz	B
Bypass mode bandwidth	–3 dB; V_O = 0.2 V_{PP}	85	130		MHz	B
Slew rate	Bypass mode; V_O = 2 V_{PP}	75	100		V/µs	B
Attenuation	With respect to 500 kHz, f = 6.75 MHz	–0.9	0.2	1.1	dB	A
	With respect to 500 kHz, f = 27 MHz	42	54		dB	A
Group delay	f = 100 kHz		72		ns	C
Group delay variation	f = 5.1 MHz with respect to 100 kHz		10		ns	C
Channel-to-channel delay			0.3		ns	C
Differential gain	NTSC/PAL		0.2/0.35		%	C
Differential phase	NTSC/PAL		0.35/0.45		Degrees	C
Total harmonic distortion	f = 1 MHz, V_O = 1.4 V_{PP}		–72		dB	C
Signal-to-noise ratio	100 kHz to 6 MHz, non-weighted		70		dB	C
	100 kHz to 6 MHz, unified weighting		78		dB	C
Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
	All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B
Output impedance	f = 6.75 MHz, Filter mode		0.7		Ω	C
	f = 6.75 MHz, Bypass mode		0.6		Ω	C
	Disabled		20 || 3		kΩ || pF	C
Return loss	f = 6.75 MHz, Filter mode		46		dB	C
Crosstalk	f = 1 MHz, SD to SD channel and SD to HD channel		–78		dB	C
AC PERFORMANCE (HD CHANNELS)						
Passband bandwidth	–1 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	27.2	32	38.2	MHz	B
Small- and large-signal bandwidth	–3 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	30.3	36	43	MHz	B
Bypass mode bandwidth	–3 dB; V_O = 0.2 V_{PP}	170	250		MHz	B
Slew rate	Bypass mode; V_O = 2 V_{PP}	420	500		V/µs	B
Attenuation	With respect to 500 kHz, f = 27 MHz	–1	0	1	dB	A
	With respect to 500 kHz, f = 74 MHz	34	42		dB	A
Group delay	f = 100 kHz		22		ns	C
Group delay variation	f = 27MHz with respect to 100 kHz		7.5		ns	C
Channel-to-channel delay			0.3		ns	C
Differential gain	NTSC/PAL		0.1/0.1		%	C
Differential phase	NTSC/PAL		0.25/0.35		Degrees	C
Total harmonic distortion	f = 10 MHz, V_O = 1.4 V_{PP}		–52		dB	C
Signal-to-noise ratio	100 kHz to 30 MHz, non-weighted		62		dB	C
	100 kHz to 30 MHz, unified weighting		72		dB	C
Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
	All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B
Output impedance	f = 30 MHz, Filter mode		1.7		Ω	C
	f = 30 MHz, Bypass mode		2		Ω	C
	Disabled		1.8 || 3		kΩ || pF	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation only. **(C)** Typical value only for information.

ELECTRICAL CHARACTERISTICS: V_{S+} = +5 V (continued)

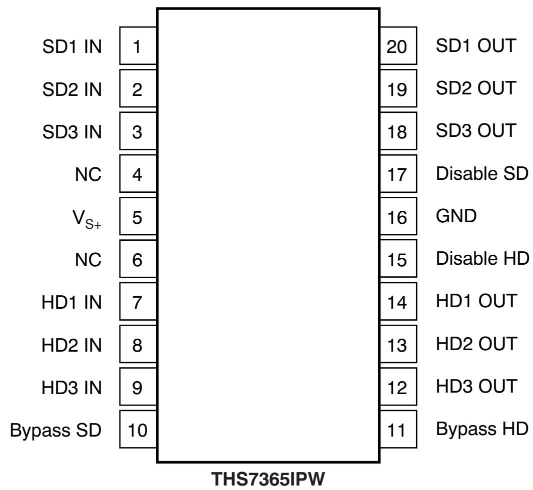
At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7365 MIN	THS7365 TYP	THS7365 MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE (HD CHANNELS) (continued)						
Return loss	f = 30 MHz, Filter mode		39		dB	C
Crosstalk	f = 1 MHz, HD to SD channels		–74		dB	C
	f = 1 MHz, SD to HD channels		–78		dB	C
	f = 1 MHz, HD to HD channels		–70		dB	C
DC PERFORMANCE						
Biased output voltage	V_{IN} = 0 V, SD channels	200	310	400	mV	A
	V_{IN} = 0 V, HD channels	200	305	400	mV	A
Input voltage range	DC input, limited by output		–0.1/2.3		V	C
Sync-tip clamp charge current	V_{IN} = –0.1 V, SD channels	140	200		µA	A
	V_{IN} = –0.1 V, HD channels	280	400		µA	A
Input impedance			800 || 2		kΩ || pF	C
OUTPUT CHARACTERISTICS						
High output voltage swing	R_L = 150 Ω to +2.5 V		4.85		V	C
	R_L = 150 Ω to GND	4.5	4.75		V	A
	R_L = 75 Ω to +2.5V		4.7		V	C
	R_L = 75 Ω to GND		4.5		V	C
Low output voltage swing	R_L = 150 Ω to +2.5 V (V_{IN} = –0.2 V)		0.05		V	C
	R_L = 150 Ω to GND (V_{IN} = –0.2 V)		0.03	0.1	V	A
	R_L = 75 Ω to +2.5 V (V_{IN} = –0.2 V)		0.1		V	C
	R_L = 75 Ω to GND (V_{IN} = –0.2 V)		0.05		V	C
Output current (sourcing)	R_L = 10 Ω to +2.5 V		90		mA	C
Output current (sinking)	R_L = 10 Ω to +2.5 V		85		mA	C
POWER SUPPLY						
Operating voltage		2.6	5	5.5	V	B
Total quiescent current, no load	V_{IN} = 0 V, all channels on	18	21.6	28.5	mA	A
	V_{IN} = 0 V, SD channels on, HD channels off	6	7.2	9.5	mA	A
	V_{IN} = 0 V, SD channels off, HD channels on	12	14.4	19	mA	A
	V_{IN} = 0 V, all channels off, $V_{DISABLE}$ = 3 V		1	10	µA	A
Power-supply rejection ratio (PSRR)	At dc		52		dB	C
LOGIC CHARACTERISTICS(2)						
V_{IH}	Disabled or Bypass engaged		2.1	2.2	V	A
V_{IL}	Enabled or Bypass disengaged	0.8	0.8		V	A
I_{IH}			0.2		µA	C
I_{IL}			0.2		µA	C
Disable time			80		ns	C
Enable time			100		ns	C
Bypass/filter switch time			5		ns	C

(2) The logic input pins should not be left floating. They must be connected to logic low (or GND) or logic high (or V_{S+}).

PIN CONFIGURATION

**PW PACKAGE
TSSOP-20
(TOP VIEW)**

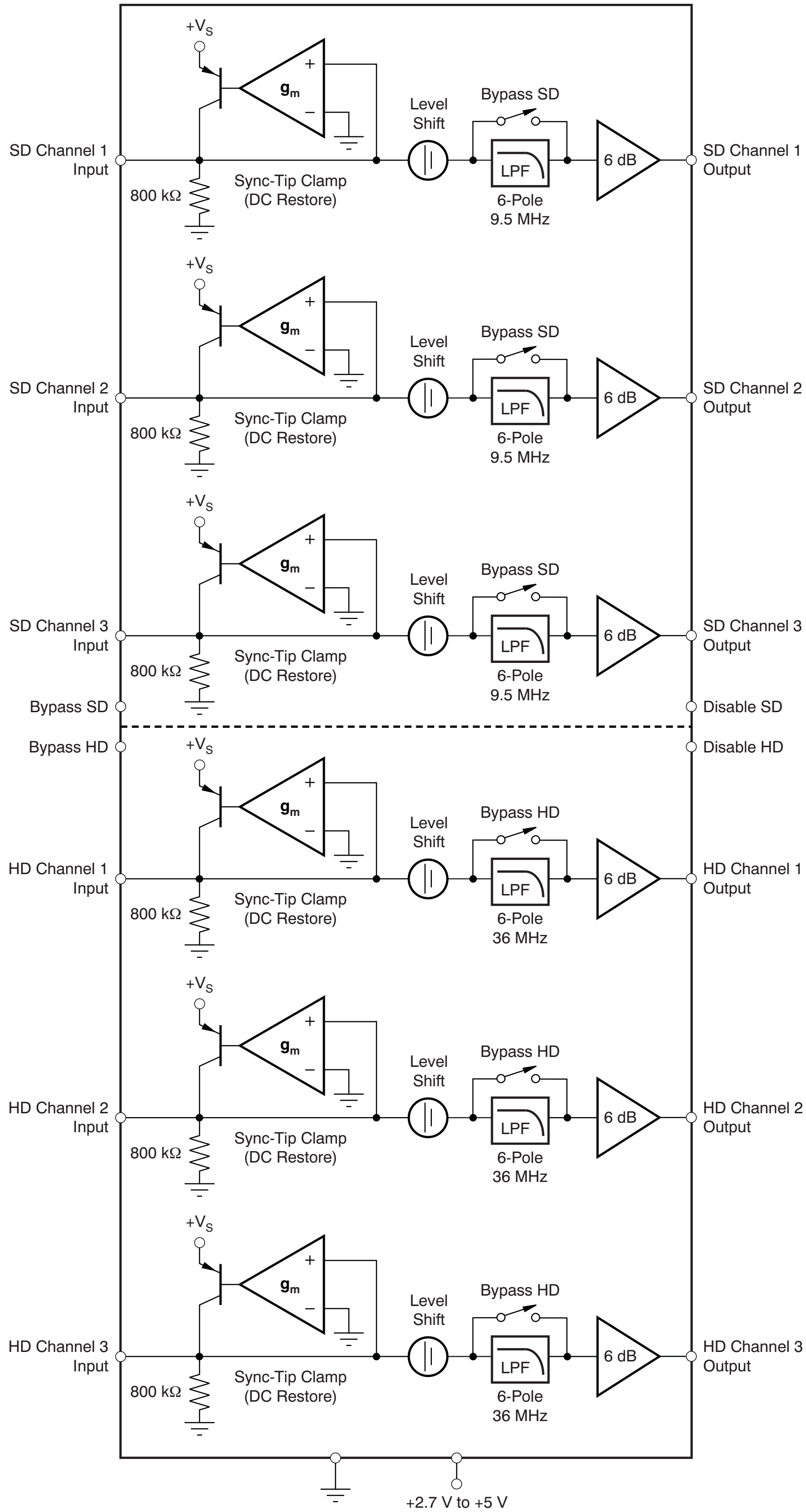


NOTE: NC = No connection.

TERMINAL FUNCTIONS

TERMINAL			
NAME	NO.	I/O	DESCRIPTION
SD1 IN	1	I	Standard-definition video input, channel 1; LPF = 9.5 MHz
SD2 IN	2	I	Standard-definition video input, channel 2; LPF = 9.5 MHz
SD3 IN	3	I	Standard-definition video input, channel 3; LPF = 9.5 MHz
NC	4, 6	—	No internal connection. It is recommended to connect NC to GND.
V_{S+}	5	I	Positive power-supply pin; connect to +2.7 V up to +5 V
HD1 IN	7	I	High-definition video input, channel 1; LPF = 36 MHz
HD2 IN	8	I	High-definition video input, channel 2; LPF = 36 MHz
HD3 IN	9	I	High-definition video input, channel 3; LPF = 36 MHz
Bypass SD	10	I	Bypass all SD channel filters. Logic high bypasses the internal filters and logic low engages the internal filters. Do not leave floating.
Bypass HD	11	I	Bypass all HD channel filters. Logic high bypasses the internal filters and logic low engages the internal filters. Do not leave floating.
HD3 OUT	12	O	High-definition video output, channel 3; LPF = 36 MHz
HD2 OUT	13	O	High-definition video output, channel 2; LPF = 36 MHz
HD1 OUT	14	O	High-definition video output, channel 1; LPF = 36 MHz
Disable HD	15	I	Disable high definition channels. Logic high disables the HD channels and logic low enables the HD. Do not leave floating.
GND	16	I	Ground pin for all internal circuitry
Disable SD	17	I	Disable standard definition channels. Logic high disables the SD channels and logic low enables the SD channels. Do not leave floating.
SD3 OUT	18	O	Standard-definition video output, channel 3; LPF = 9.5 MHz
SD2 OUT	19	O	Standard-definition video output, channel 2; LPF = 9.5 MHz
SD1 OUT	20	O	Standard-definition video output, channel 1; LPF = 9.5 MHz

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Table of Graphs: +3.3 V and +5 V

TITLE	FIGURE
Maximum Output Voltage vs Temperature	Figure 2
Minimum Output Voltage vs Temperature	Figure 3
SD Channel Output Impedance vs Frequency	Figure 4
SD Channel S22 Output Reflection Ratio vs Frequency	Figure 5
HD Channel Output Impedance vs Frequency	Figure 6
HD Channel S22 Output Reflection Ratio vs Frequency	Figure 7
SD Channel Disabled Output Impedance vs Frequency	Figure 8
HD Channel Disabled Output Impedance vs Frequency	Figure 9
Input Resistance vs Temperature	Figure 10

Table of Graphs: 3.3 V, Standard-Definition (SD) Channels

TITLE	FIGURE
SD Channel Small-Signal Gain vs Frequency	Figure 11, Figure 12, Figure 15, Figure 16, Figure 17, Figure 18
SD Channel Large-Signal Gain vs Frequency	Figure 13, Figure 14
SD Channel Phase vs Frequency	Figure 19
SD Channel Group Delay vs Frequency	Figure 20, Figure 21
SD Channel PSRR vs Frequency	Figure 22
SD Channel Differential Gain	Figure 23, Figure 25
SD Channel Differential Phase	Figure 24, Figure 26
SD Channel Second-Order Harmonic Distortion vs Frequency	Figure 27, Figure 29
SD Channel Third-Order Harmonic Distortion vs Frequency	Figure 28, Figure 30
SD Channel Small-Signal Pulse Response vs Time	Figure 31, Figure 33
SD Channel Large-Signal Pulse Response vs Time	Figure 32, Figure 34
Crosstalk vs Frequency	Figure 35, Figure 36
SD Channel Slew Rate vs Output Voltage	Figure 37
Total Quiescent Current vs Temperature	Figure 38
Output Offset Voltage vs Temperature	Figure 39

Table of Graphs: 3.3 V, High-Definition (HD) Channels

TITLE	FIGURE
HD Channel Small-Signal Gain vs Frequency	Figure 40, Figure 41, Figure 44, Figure 45, Figure 46, Figure 47
HD Channel Large-Signal Gain vs Frequency	Figure 42, Figure 43
HD Channel Phase vs Frequency	Figure 48
HD Channel Group Delay vs Frequency	Figure 49, Figure 50
HD Channel PSRR vs Frequency	Figure 51
HD Channel Second-Order Harmonic Distortion vs Frequency	Figure 52, Figure 54
HD Channel Third-Order Harmonic Distortion vs Frequency	Figure 53, Figure 55
HD Channel Small-Signal Pulse Response vs Time	Figure 56, Figure 58
HD Channel Large-Signal Pulse Response vs Time	Figure 57, Figure 59
HD Channel Slew Rate vs Output Voltage	Figure 60

Table of Graphs: 5 V, Standard-Definition (SD) Channels

TITLE	FIGURE
SD Channel Small-Signal Gain vs Frequency	Figure 61, Figure 62, Figure 65, Figure 66, Figure 67, Figure 68
SD Channel Large-Signal Gain vs Frequency	Figure 63, Figure 64
SD Channel Phase vs Frequency	Figure 69
SD Channel Group Delay vs Frequency	Figure 70, Figure 71
SD Channel PSRR vs Frequency	Figure 72
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TYPICAL CHARACTERISTICS: +3.3 V and +5 V

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

MAXIMUM OUTPUT VOLTAGE vs TEMPERATURE

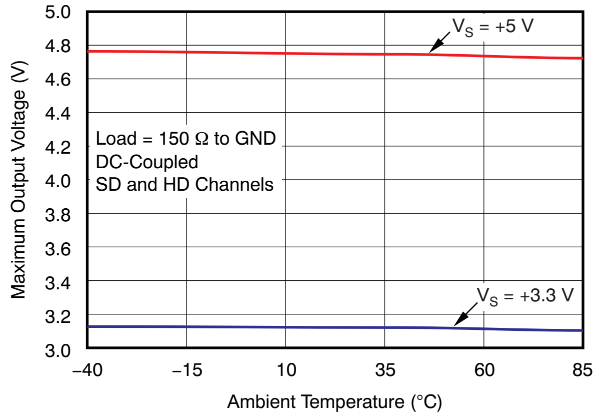


Figure 2.

MINIMUM OUTPUT VOLTAGE vs TEMPERATURE

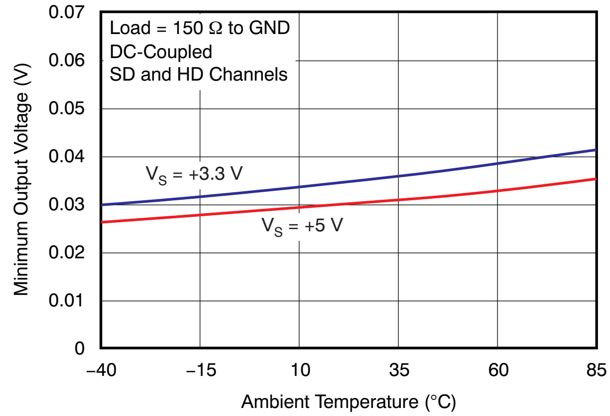


Figure 3.

SD CHANNEL OUTPUT IMPEDANCE vs FREQUENCY

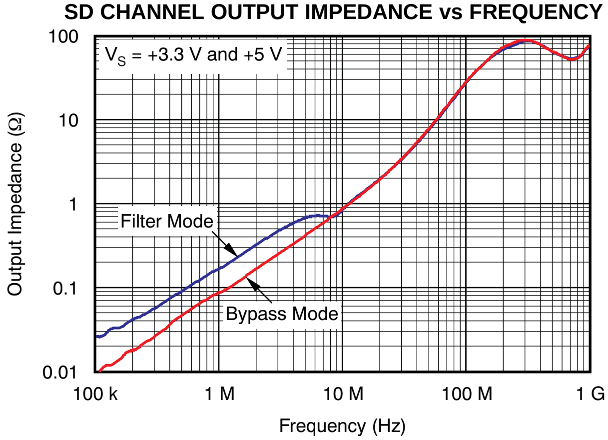


Figure 4.

SD CHANNEL S22 OUTPUT REFLECTION RATIO vs FREQUENCY

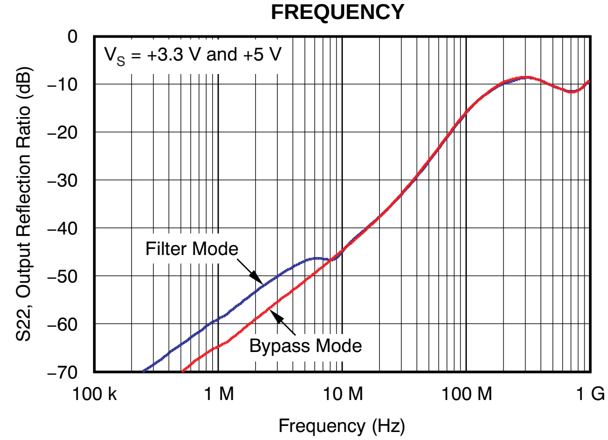


Figure 5.

HD CHANNEL OUTPUT IMPEDANCE vs FREQUENCY

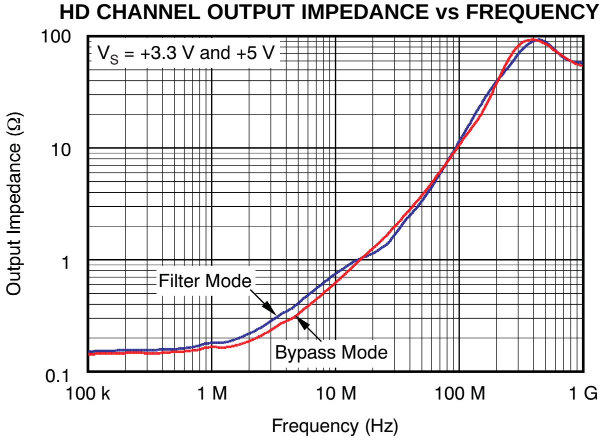


Figure 6.

HD CHANNEL S22 OUTPUT REFLECTION RATIO vs FREQUENCY

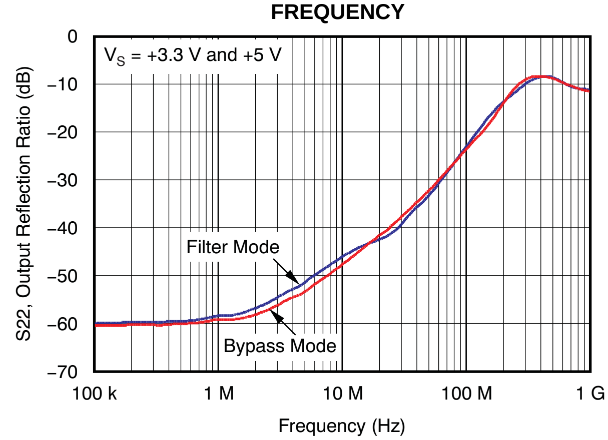


Figure 7.

TYPICAL CHARACTERISTICS: +3.3 V and +5 V (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNEL DISABLED OUTPUT IMPEDANCE vs FREQUENCY

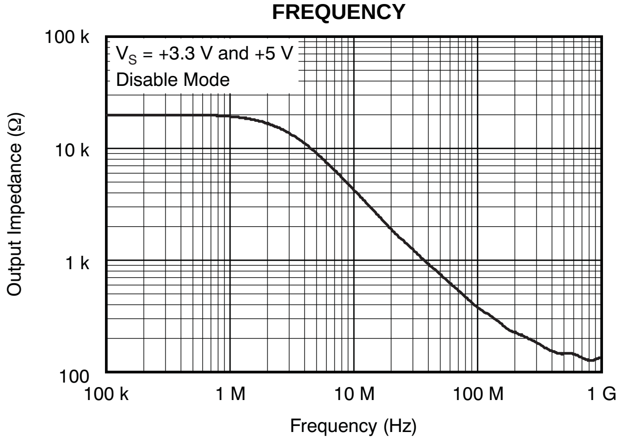


Figure 8.

HD CHANNEL DISABLED OUTPUT IMPEDANCE vs FREQUENCY

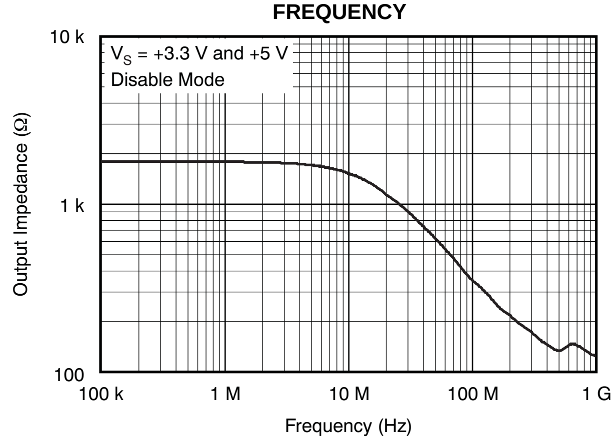


Figure 9.

INPUT RESISTANCE vs TEMPERATURE

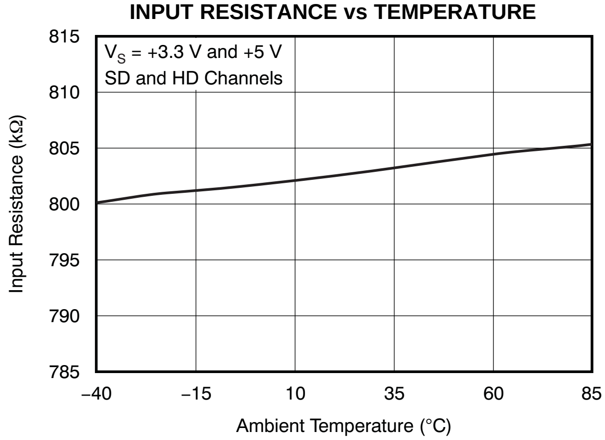


Figure 10.

TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (SD) Channels

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

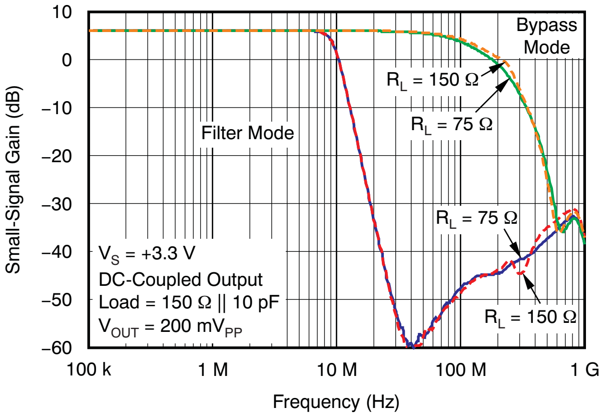


Figure 11.

SD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

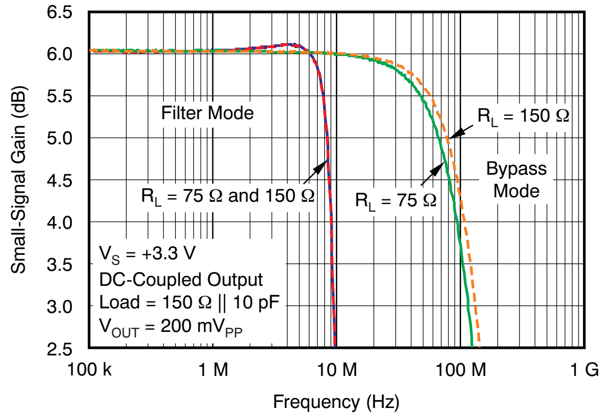


Figure 12.

SD CHANNEL LARGE-SIGNAL GAIN vs FREQUENCY

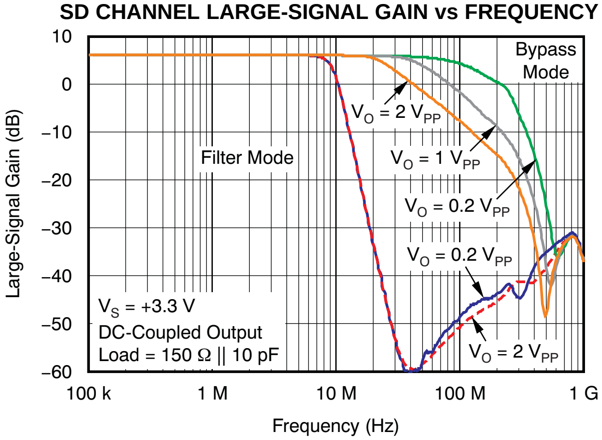


Figure 13.

SD CHANNEL LARGE-SIGNAL GAIN vs FREQUENCY

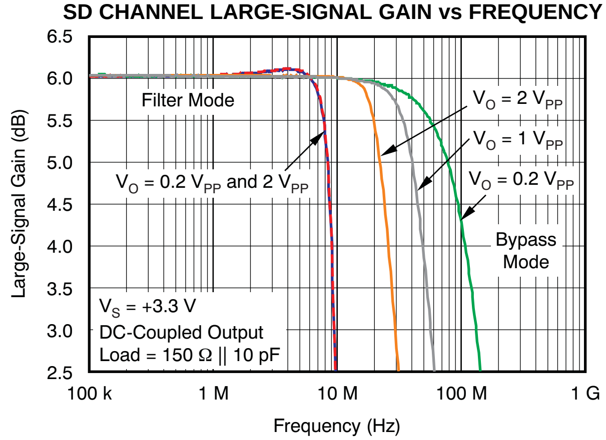


Figure 14.

SD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

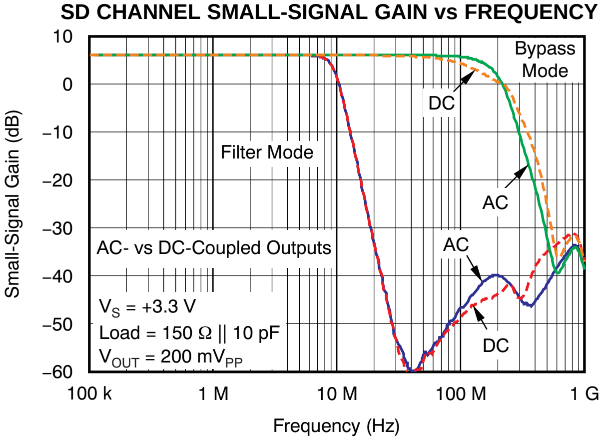


Figure 15.

SD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

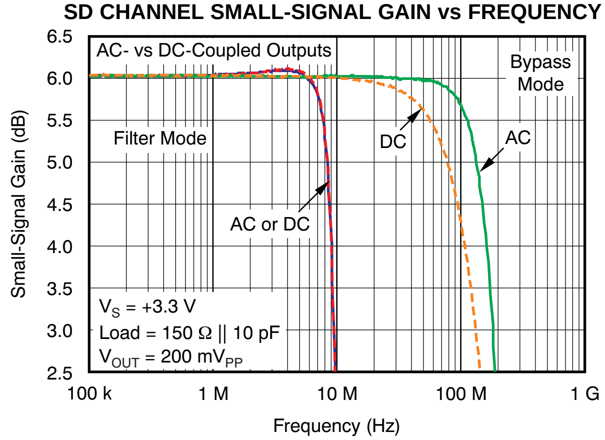


Figure 16.

TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

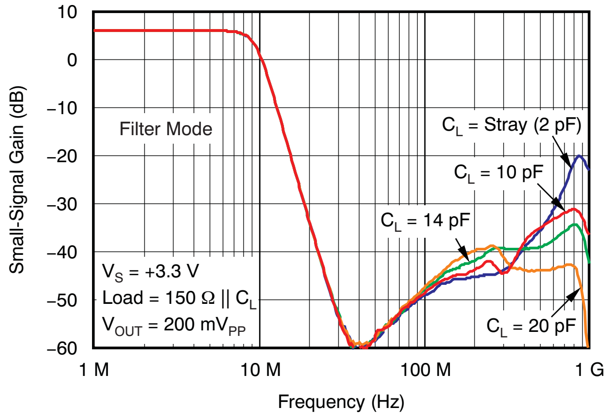


Figure 17.

SD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

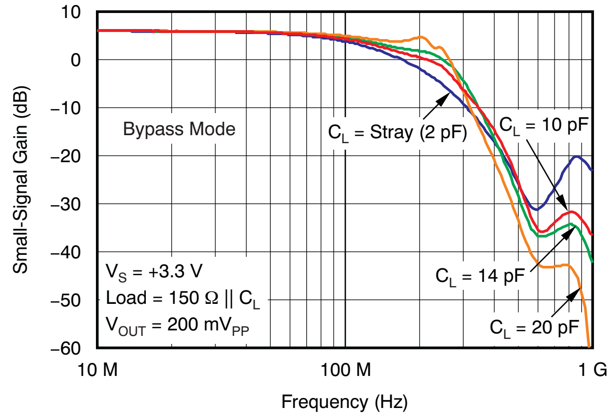


Figure 18.

SD CHANNEL PHASE vs FREQUENCY

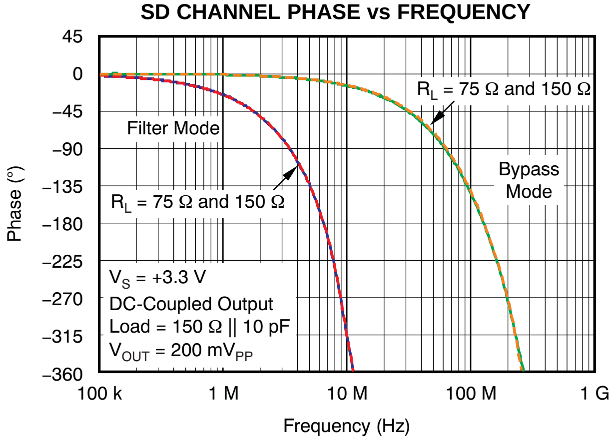


Figure 19.

SD CHANNEL GROUP DELAY vs FREQUENCY

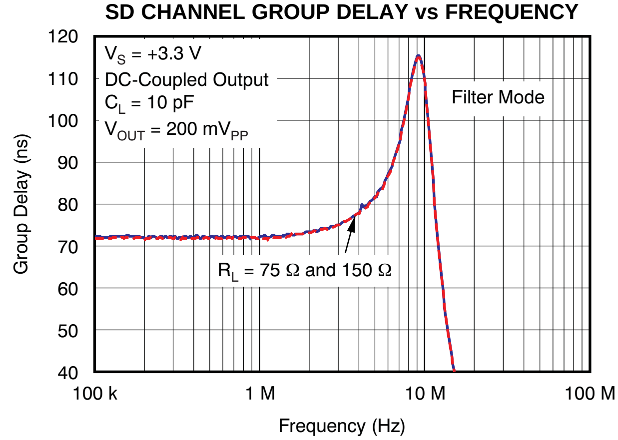


Figure 20.

SD CHANNEL GROUP DELAY vs FREQUENCY

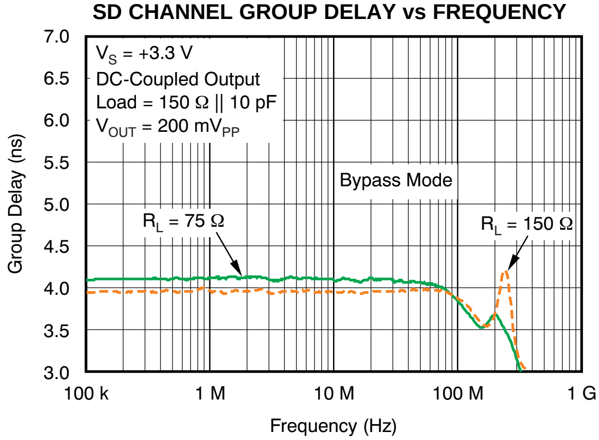


Figure 21.

SD CHANNEL PSRR vs FREQUENCY

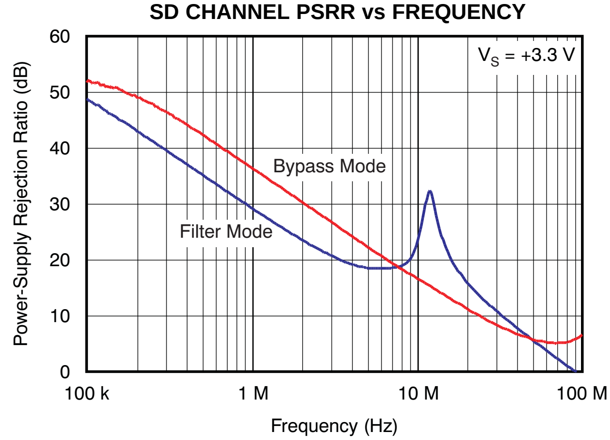


Figure 22.

TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

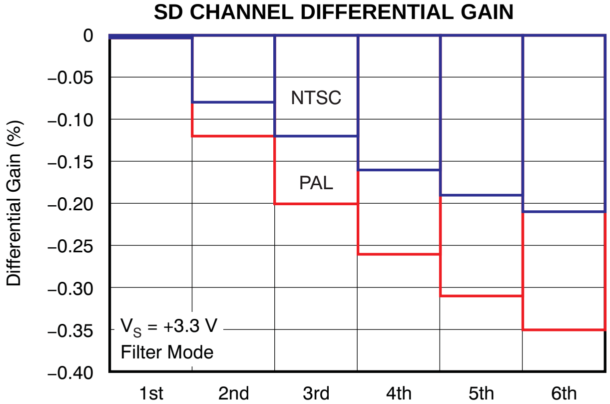


Figure 23.

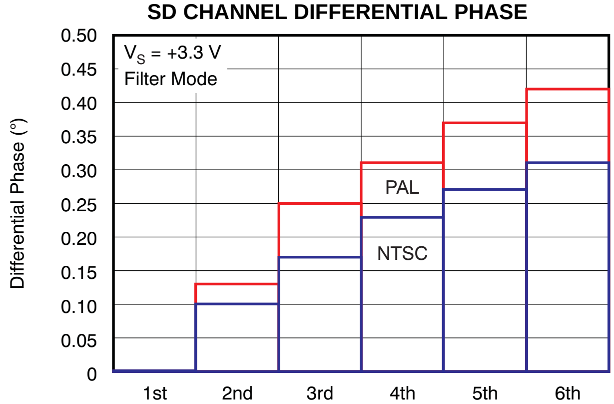


Figure 24.

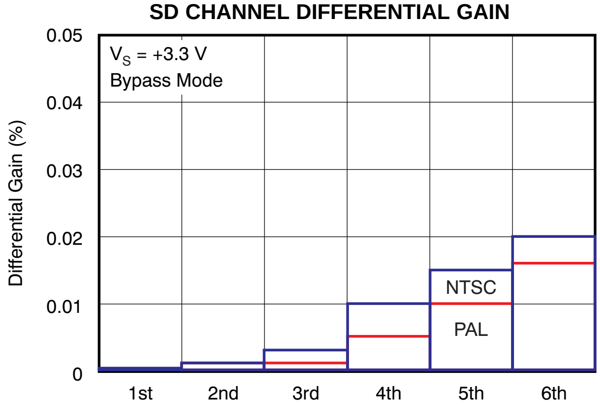


Figure 25.

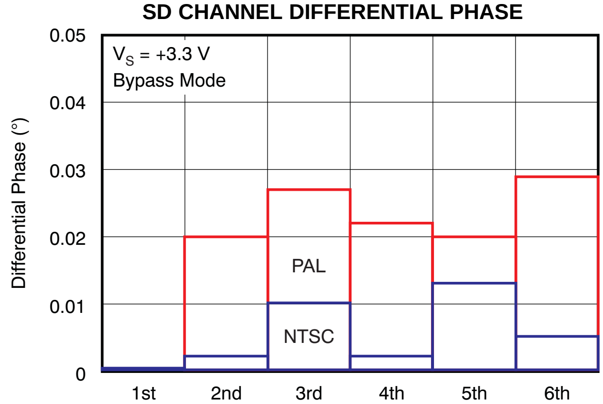


Figure 26.

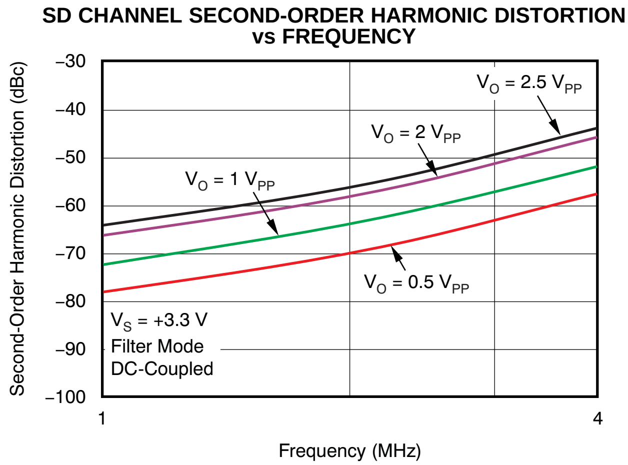


Figure 27.

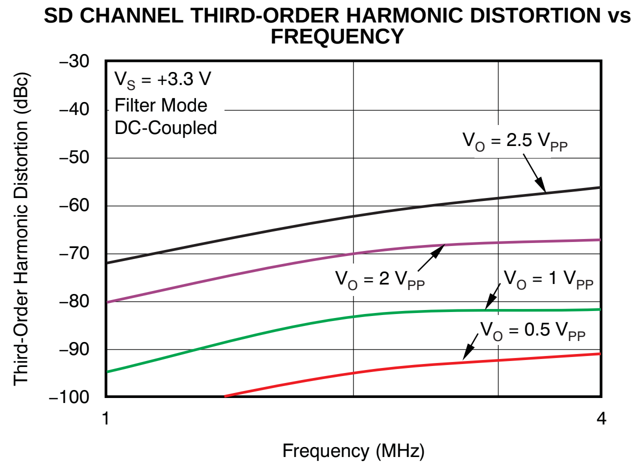


Figure 28.

TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

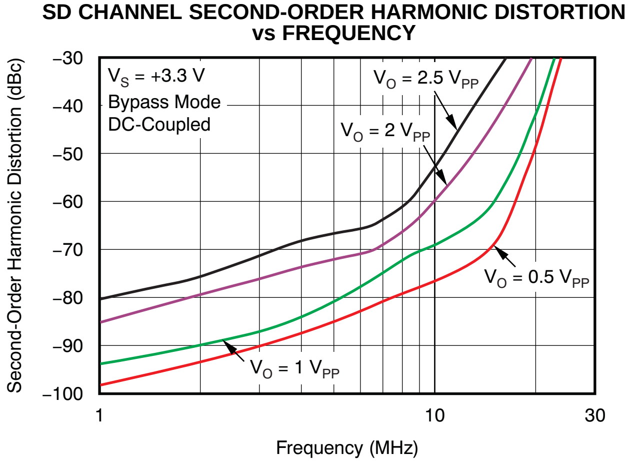


Figure 29.

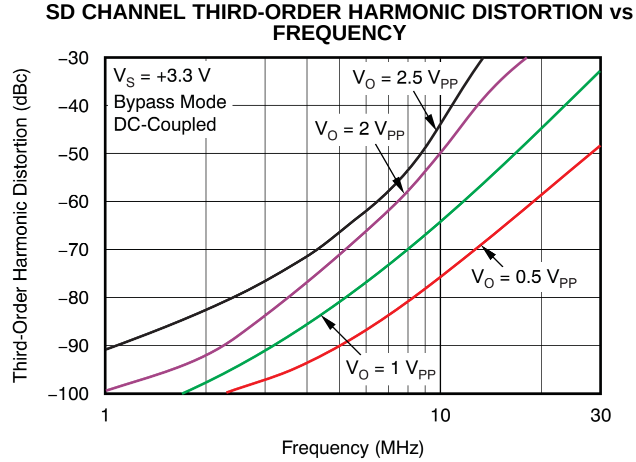


Figure 30.

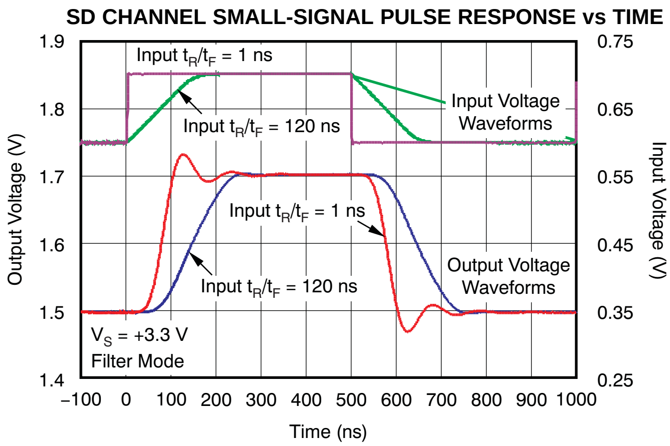


Figure 31.

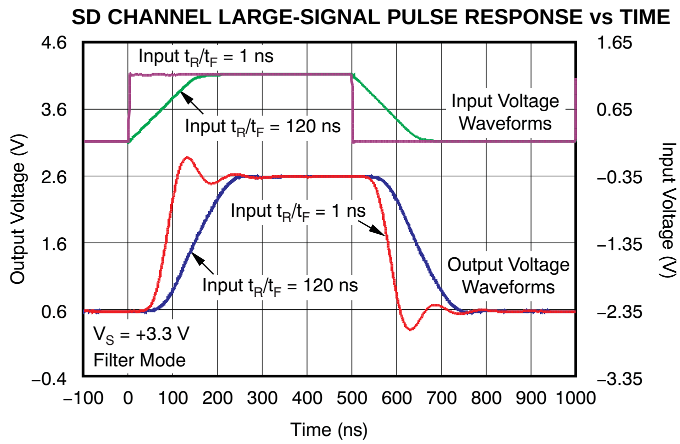


Figure 32.

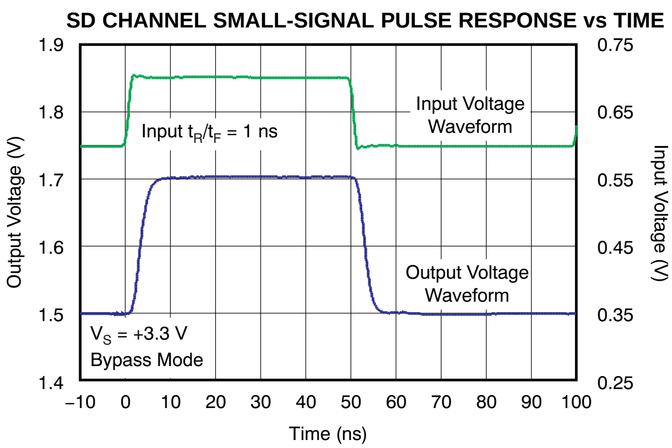


Figure 33.

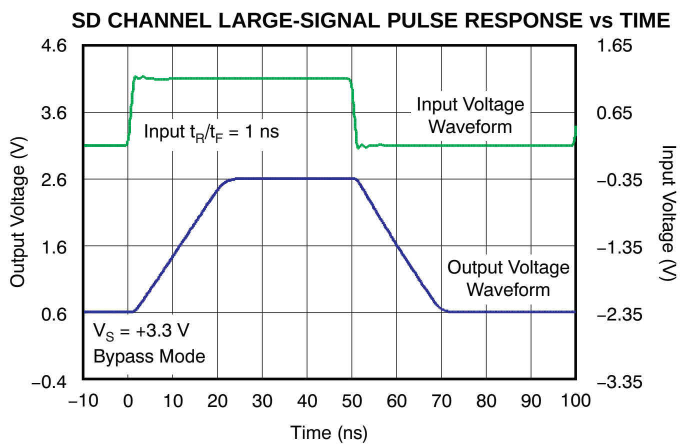


Figure 34.

TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

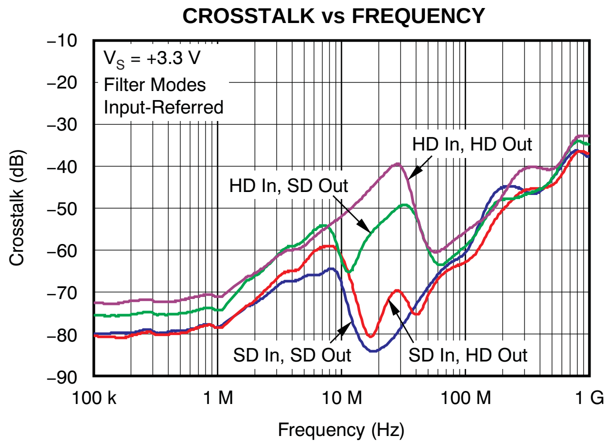


Figure 35.

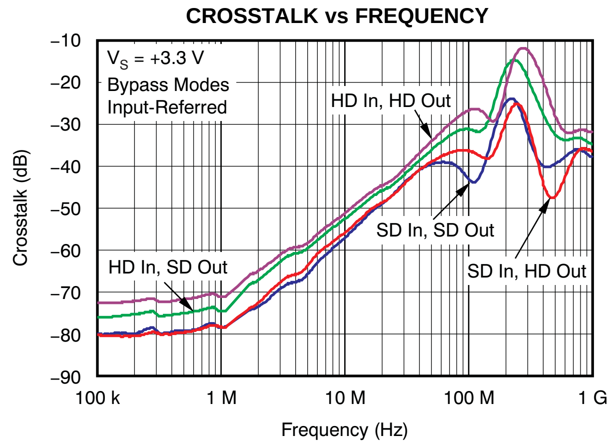


Figure 36.

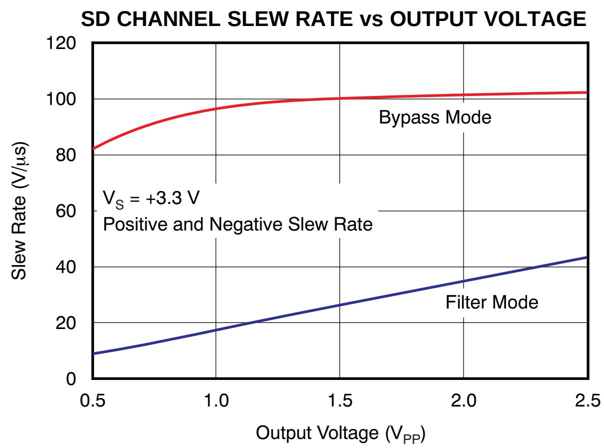


Figure 37.

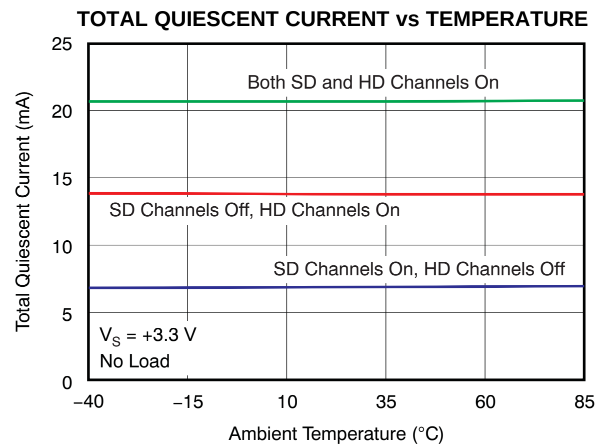


Figure 38.

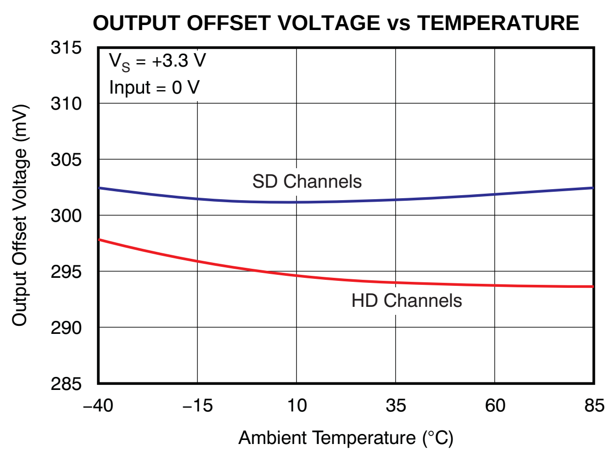


Figure 39.

TYPICAL CHARACTERISTICS: 3.3 V, High-Definition (HD) Channels

With load = 150 Ω || 8 pF, dc-coupled input and output, unless otherwise noted.

HD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

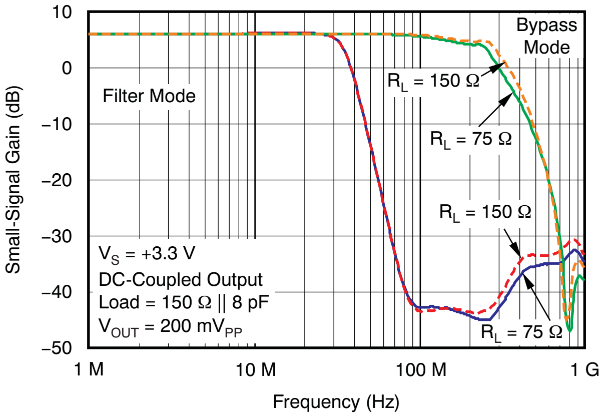


Figure 40.

HD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

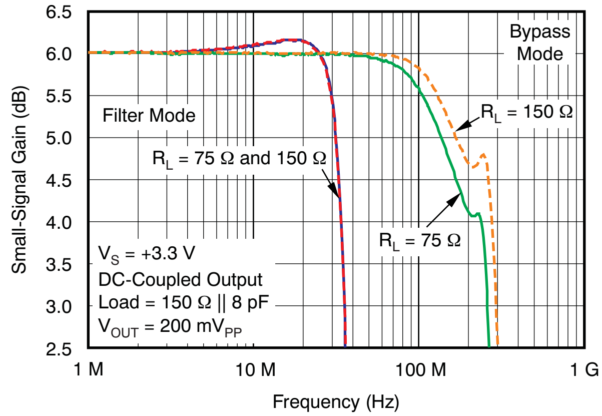


Figure 41.

HD CHANNEL LARGE-SIGNAL GAIN vs FREQUENCY

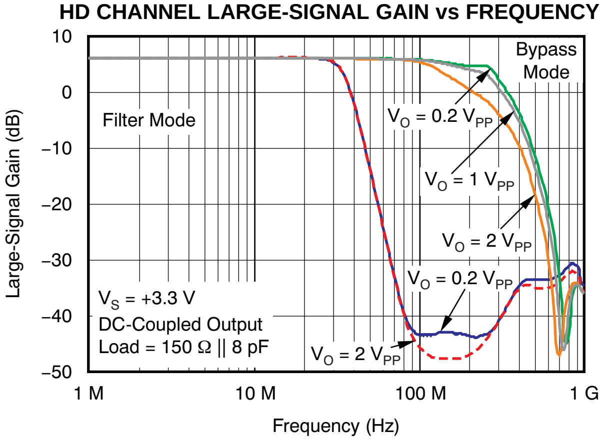


Figure 42.

HD CHANNEL LARGE-SIGNAL GAIN vs FREQUENCY

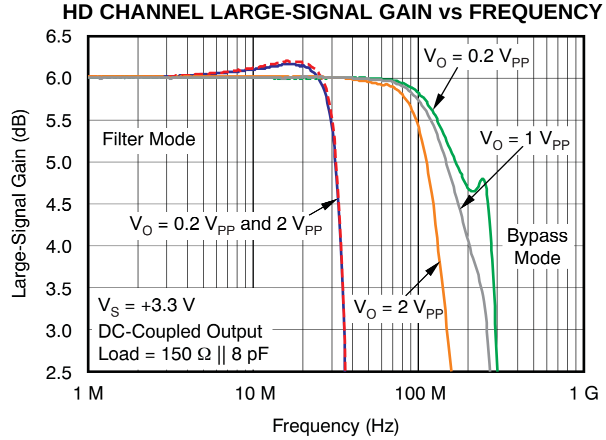


Figure 43.

HD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

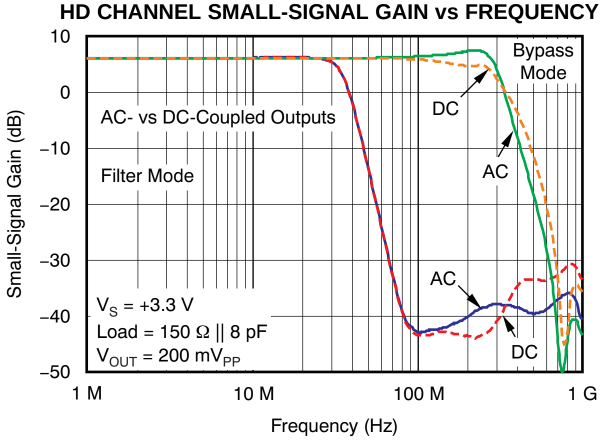


Figure 44.

HD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

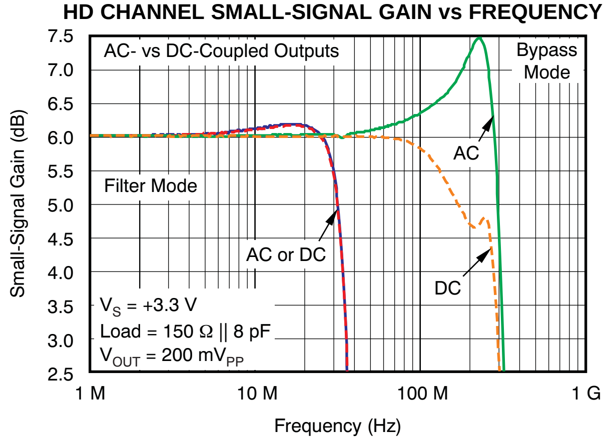


Figure 45.

TYPICAL CHARACTERISTICS: 3.3 V, High-Definition (HD) Channels (continued)

With load = 150 Ω || 8 pF, dc-coupled input and output, unless otherwise noted.

HD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

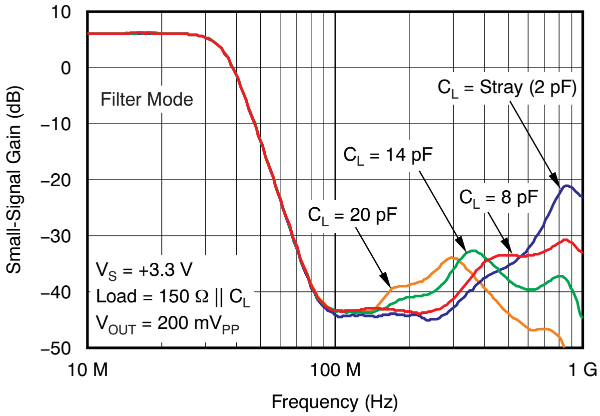


Figure 46.

HD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

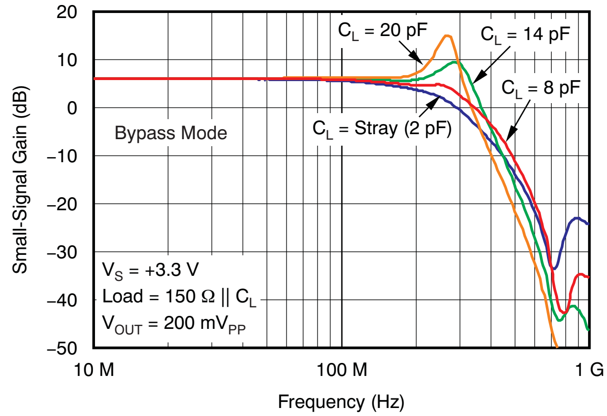


Figure 47.

HD CHANNEL PHASE vs FREQUENCY

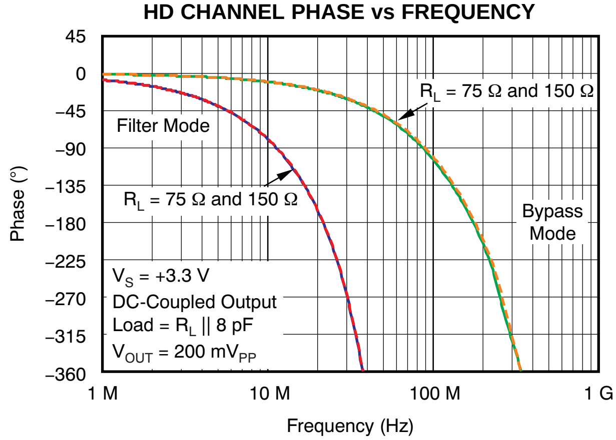


Figure 48.

HD CHANNEL GROUP DELAY vs FREQUENCY

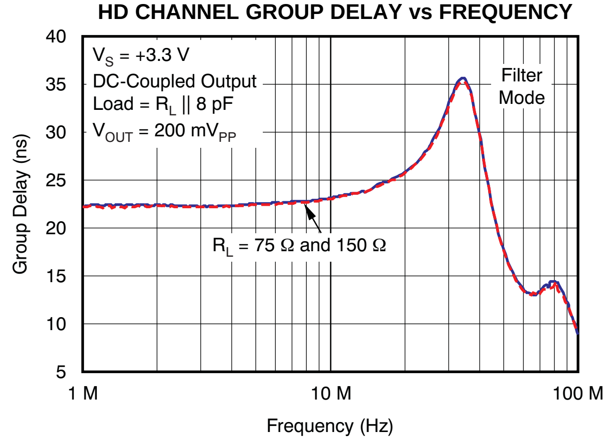


Figure 49.

HD CHANNEL GROUP DELAY vs FREQUENCY

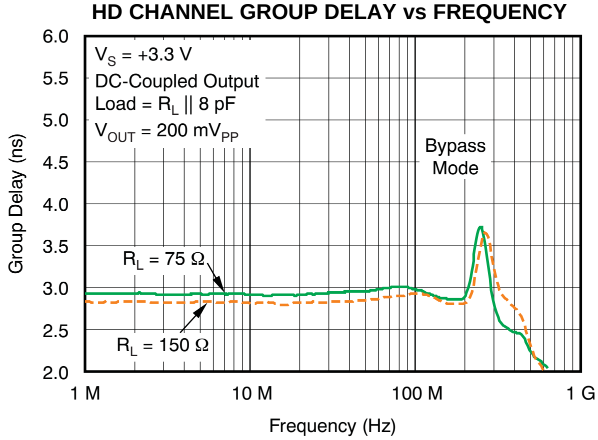


Figure 50.

HD CHANNEL PSRR vs FREQUENCY

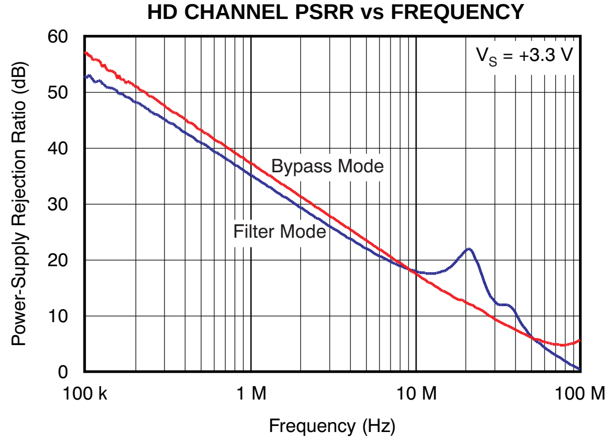


Figure 51.

TYPICAL CHARACTERISTICS: 3.3 V, High-Definition (HD) Channels (continued)

With load = 150 Ω || 8 pF, dc-coupled input and output, unless otherwise noted.

HD CHANNEL SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

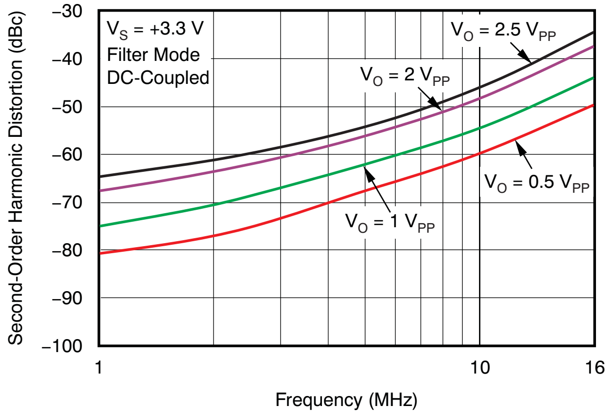


Figure 52.

HD CHANNEL THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

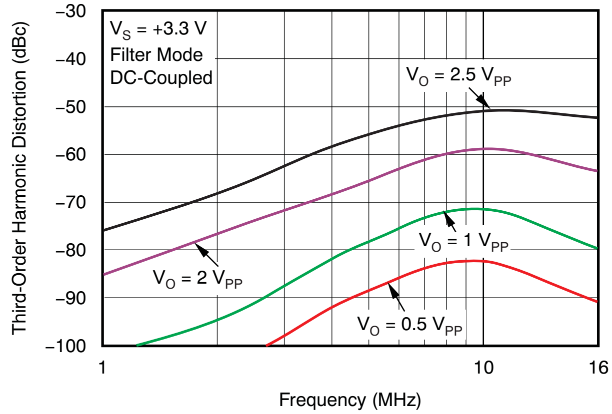


Figure 53.

HD CHANNEL SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

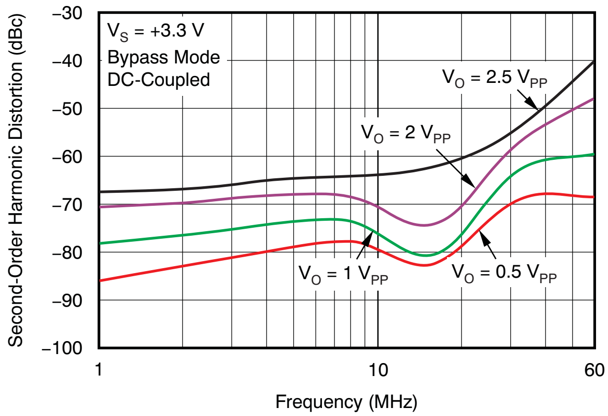


Figure 54.

HD CHANNEL THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

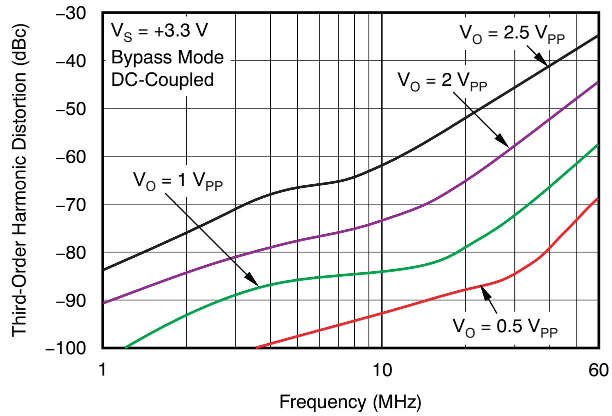


Figure 55.

HD CHANNEL SMALL-SIGNAL PULSE RESPONSE vs TIME

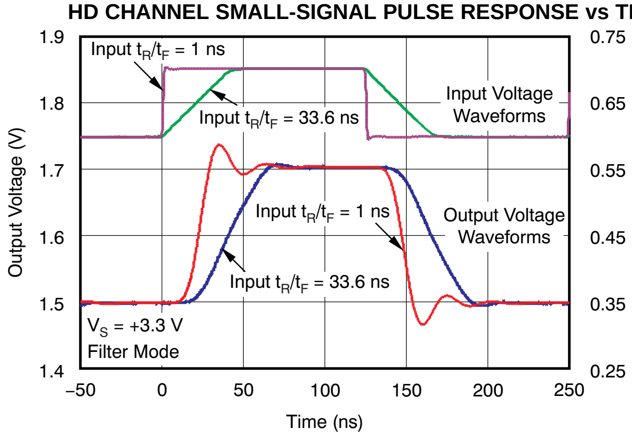


Figure 56.

HD CHANNEL LARGE-SIGNAL PULSE RESPONSE vs TIME

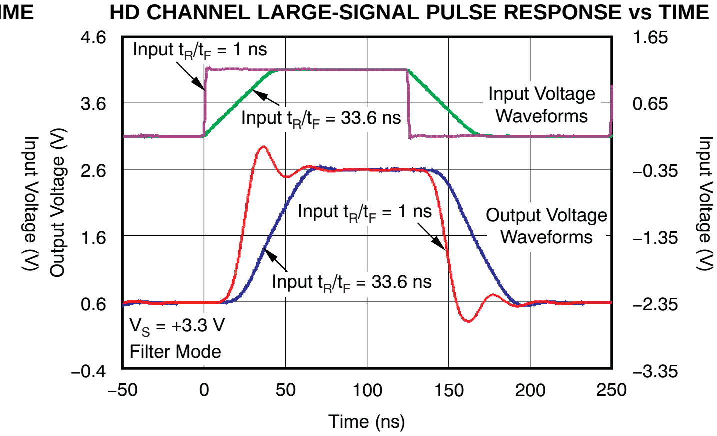


Figure 57.

TYPICAL CHARACTERISTICS: 3.3 V, High-Definition (HD) Channels (continued)

With load = 150 Ω || 8 pF, dc-coupled input and output, unless otherwise noted.

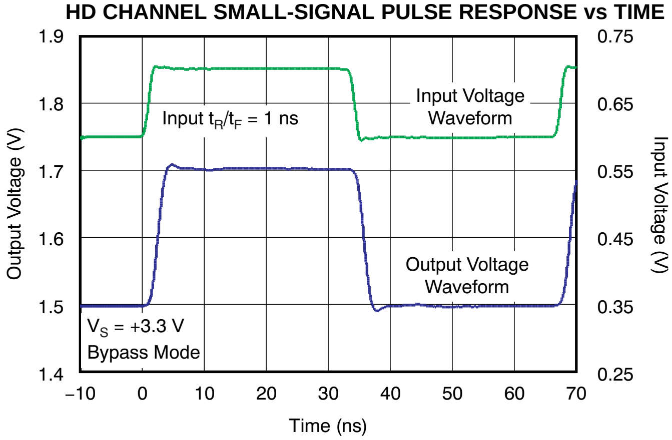


Figure 58.

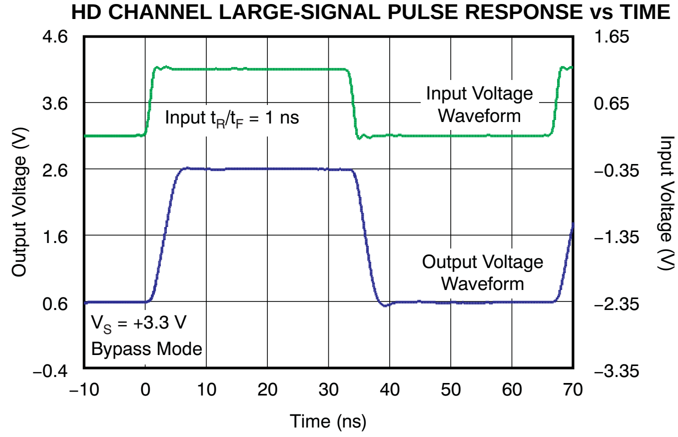


Figure 59.

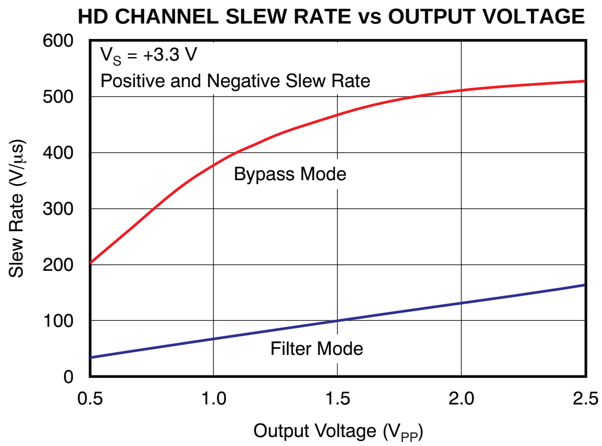


Figure 60.

TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (SD) Channels

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

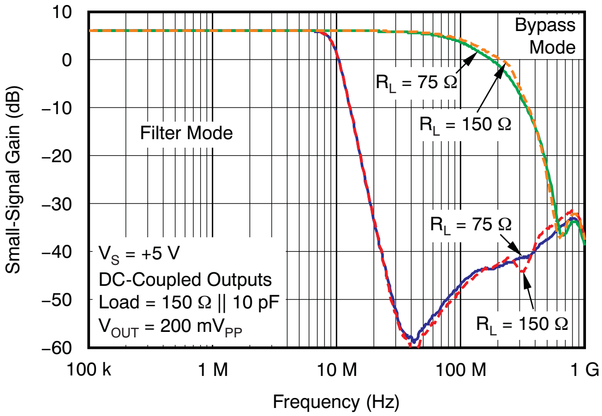


Figure 61.

SD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

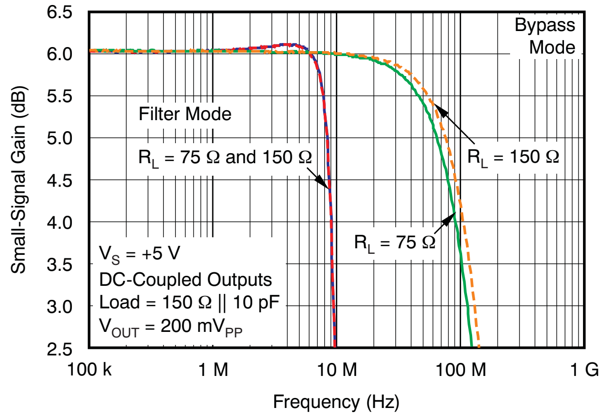


Figure 62.

SD CHANNEL LARGE-SIGNAL GAIN vs FREQUENCY

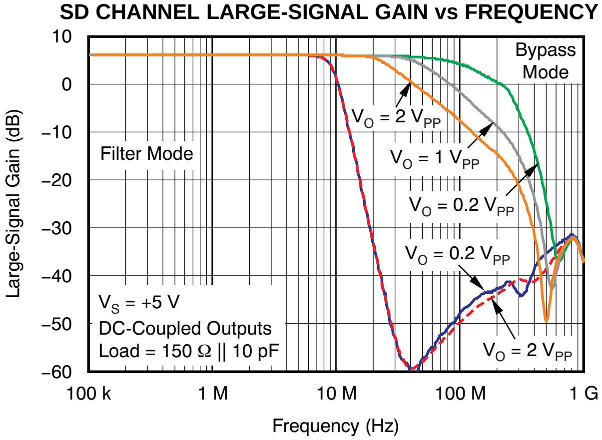


Figure 63.

SD CHANNEL LARGE-SIGNAL GAIN vs FREQUENCY

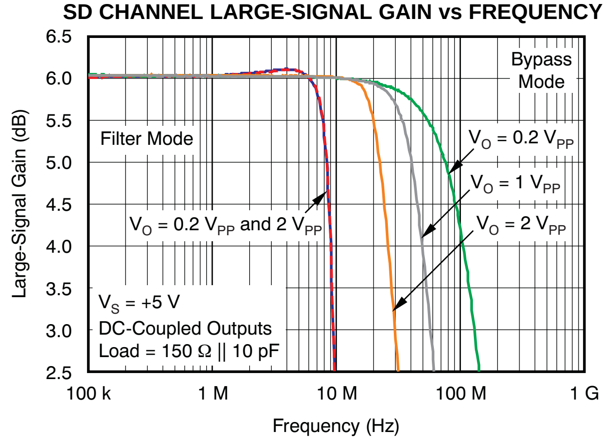


Figure 64.

SD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

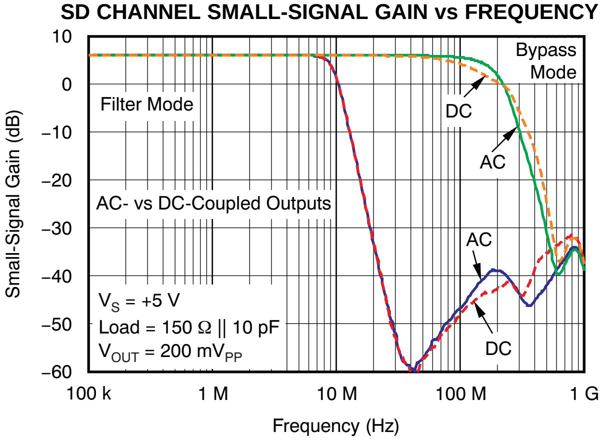


Figure 65.

SD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

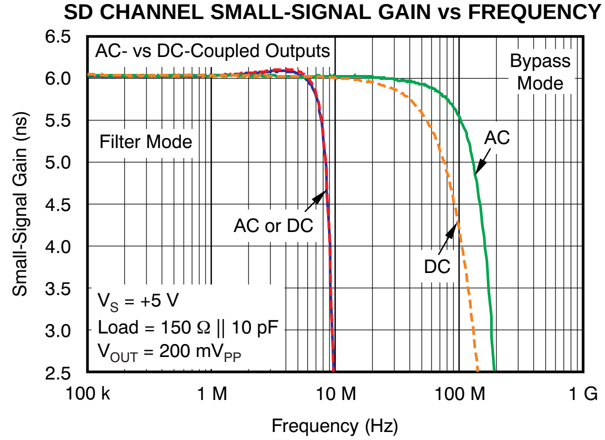


Figure 66.

TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

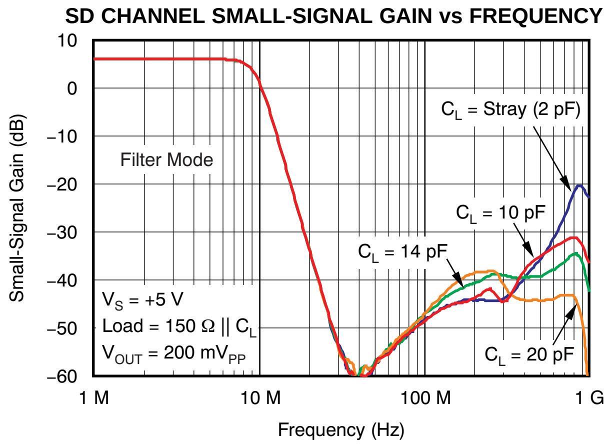


Figure 67.

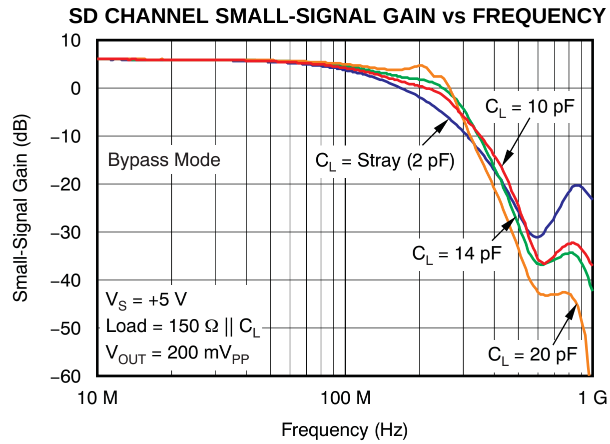


Figure 68.

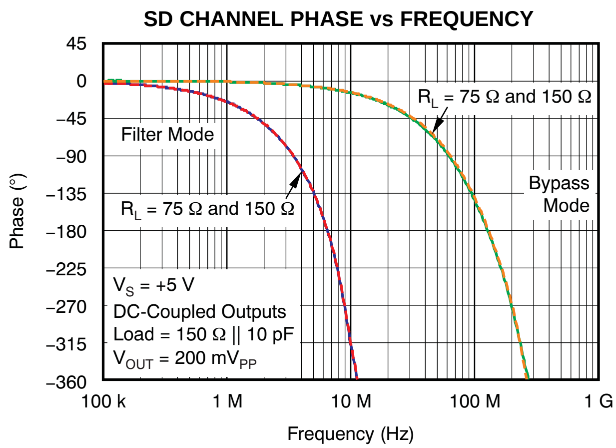


Figure 69.

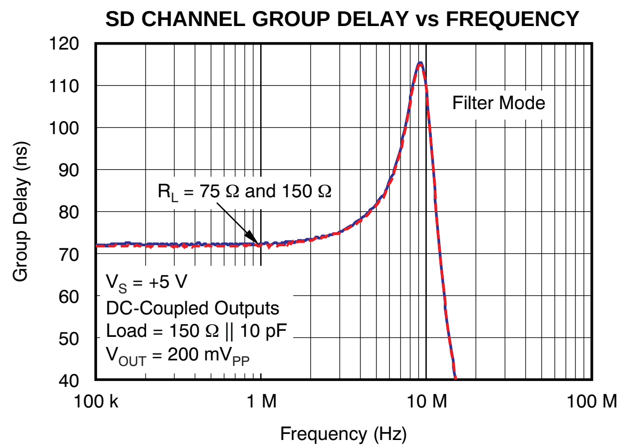


Figure 70.

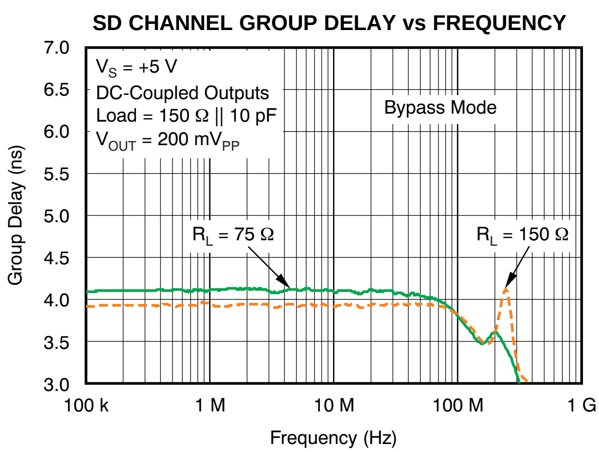


Figure 71.

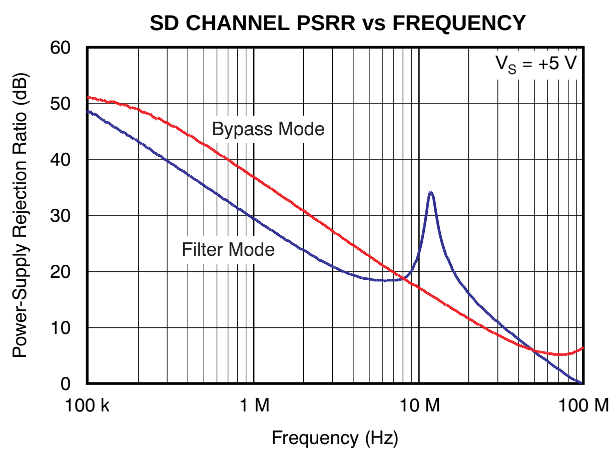


Figure 72.

TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

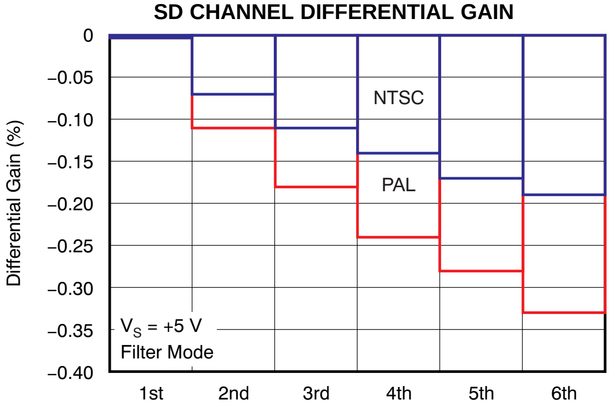


Figure 73.

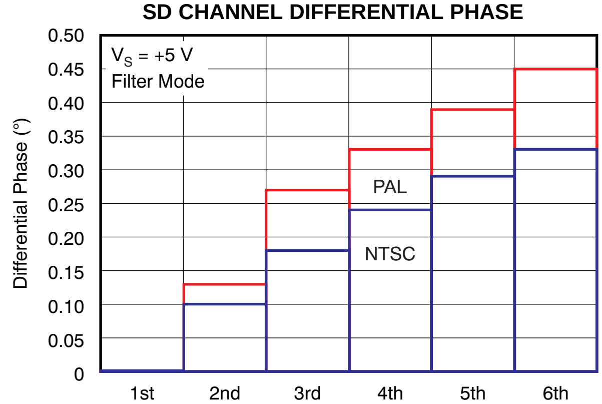


Figure 74.

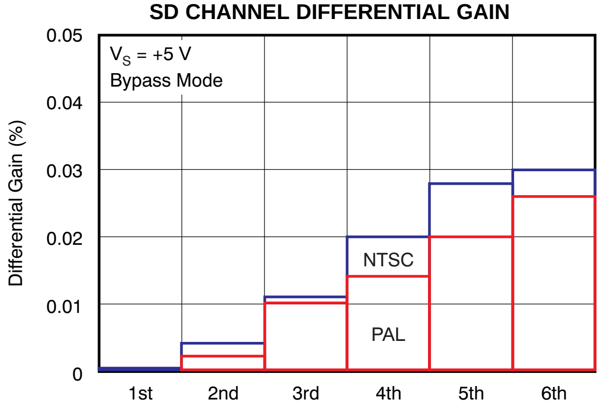


Figure 75.

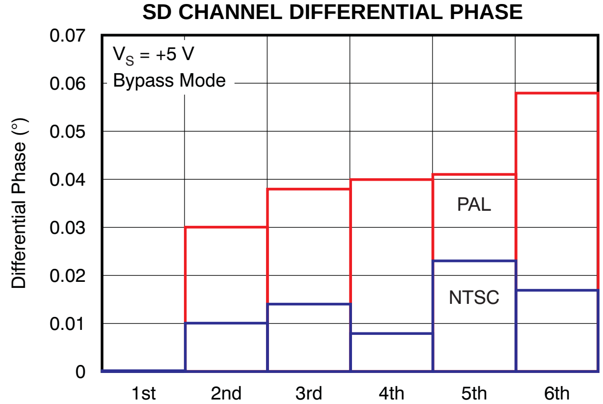


Figure 76.

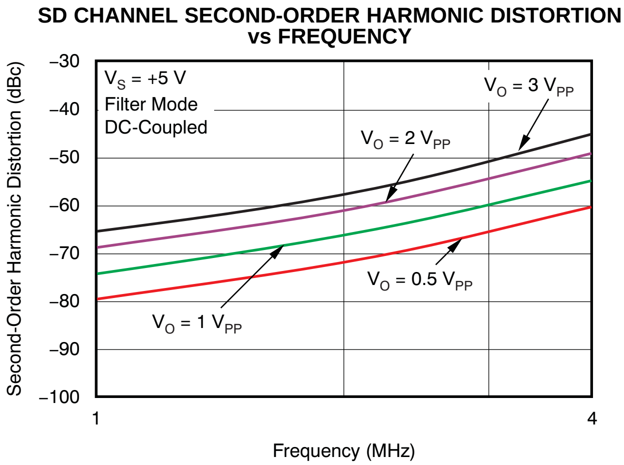


Figure 77.

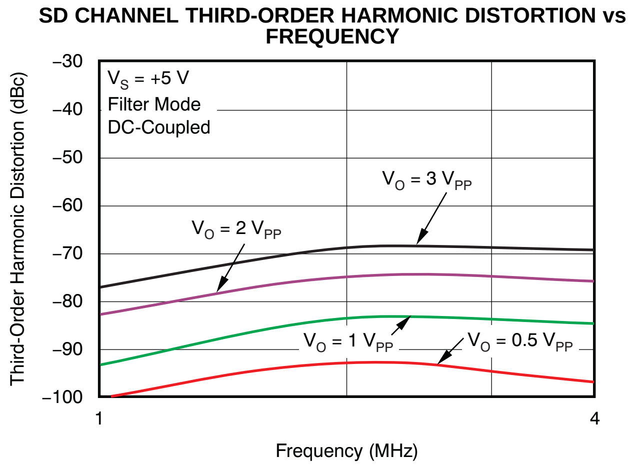


Figure 78.

TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNEL SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

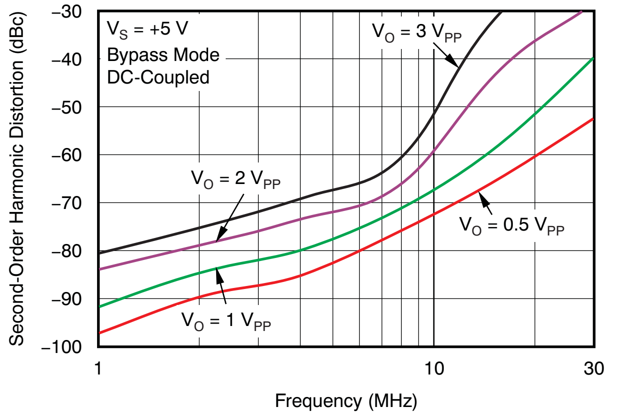


Figure 79.

SD CHANNEL THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

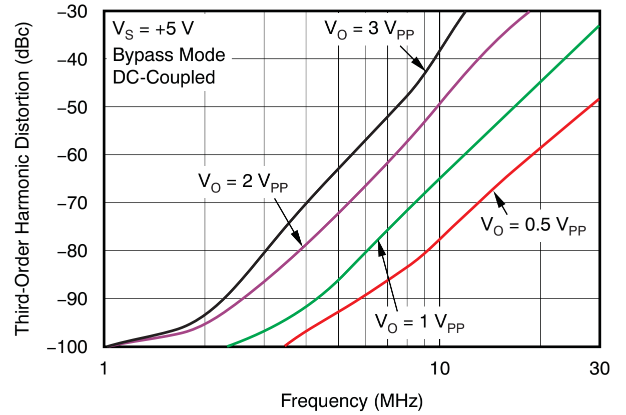


Figure 80.

SD CHANNEL SMALL-SIGNAL PULSE RESPONSE vs TIME

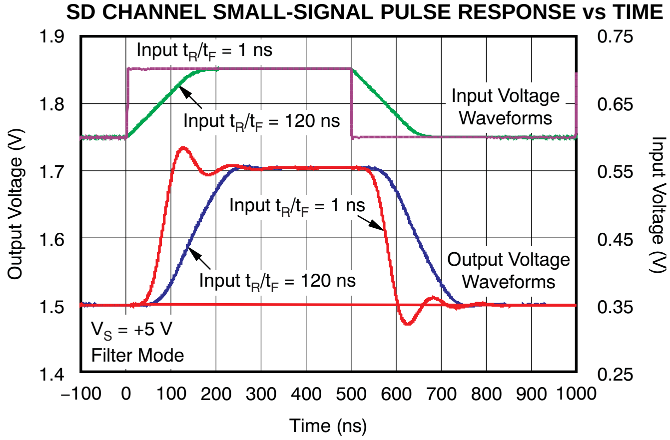


Figure 81.

SD CHANNEL LARGE-SIGNAL PULSE RESPONSE vs TIME

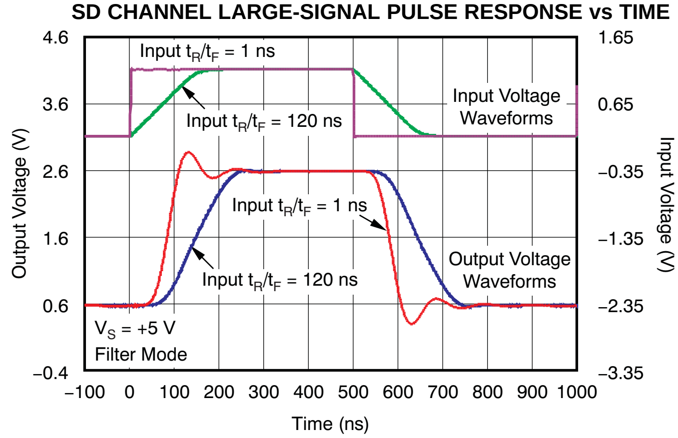


Figure 82.

SD CHANNEL SMALL-SIGNAL PULSE RESPONSE vs TIME

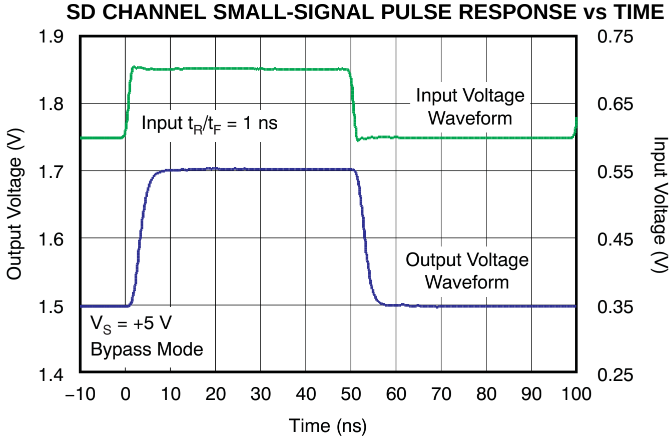


Figure 83.

SD CHANNEL LARGE-SIGNAL PULSE RESPONSE vs TIME

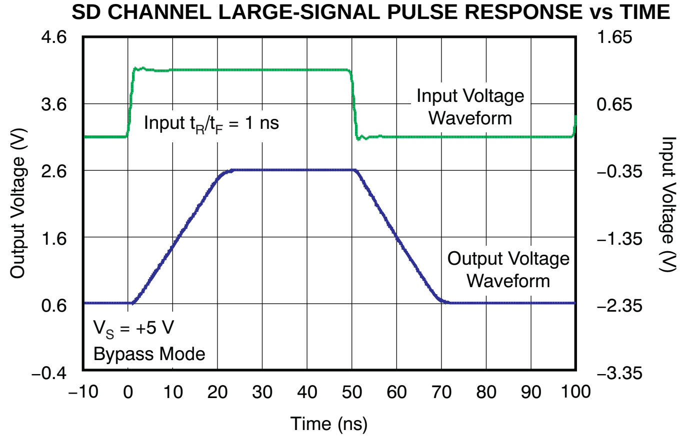


Figure 84.

TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

CROSSTALK vs FREQUENCY

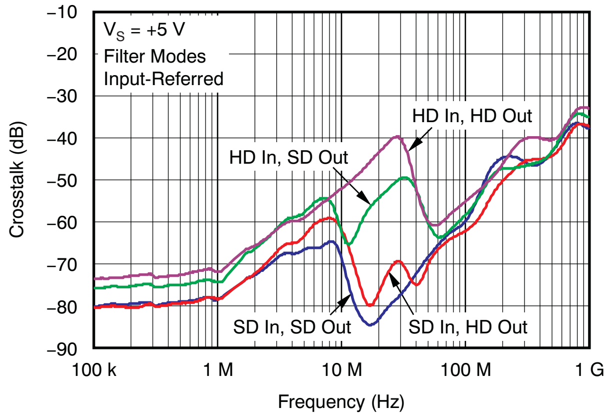


Figure 85.

CROSSTALK vs FREQUENCY

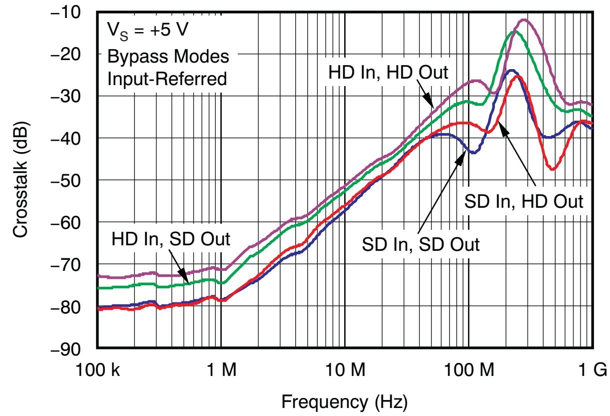


Figure 86.

SD CHANNEL SLEW RATE vs OUTPUT VOLTAGE

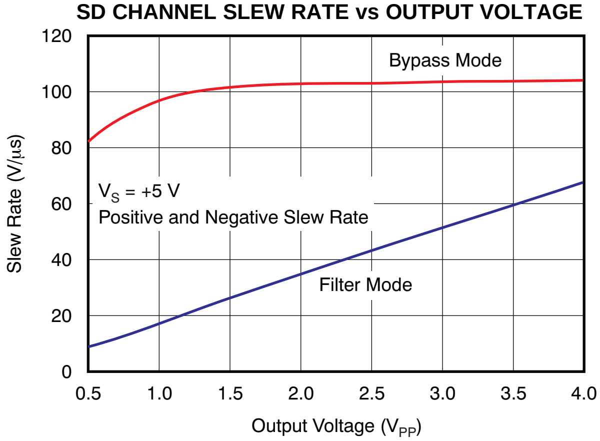


Figure 87.

TOTAL QUIESCENT CURRENT vs TEMPERATURE

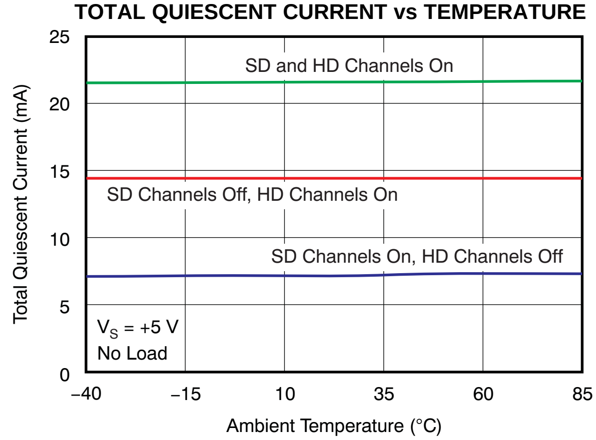


Figure 88.

SD CHANNEL ATTENUATION AT 6.75 MHz vs TEMPERATURE

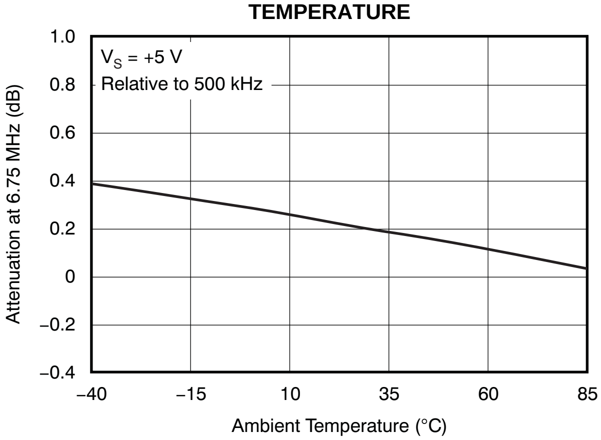


Figure 89.

SD CHANNEL ATTENUATION AT 27 MHz vs TEMPERATURE

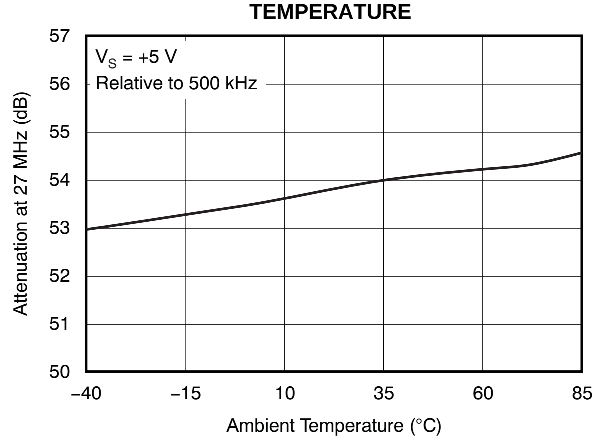


Figure 90.

TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

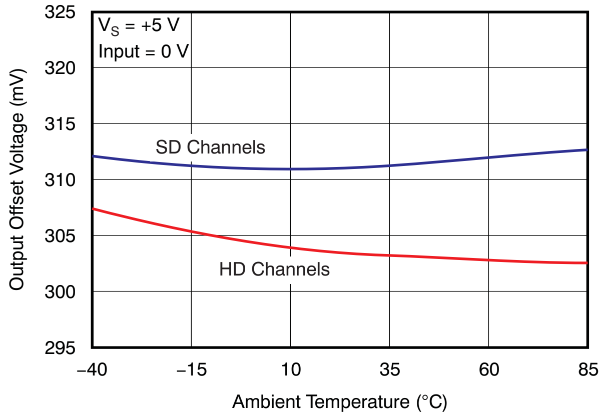


Figure 91.

TYPICAL CHARACTERISTICS: 5 V, High-Definition (HD) Channels

With load = 150 Ω || 8 pF, dc-coupled input and output, unless otherwise noted.

HD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

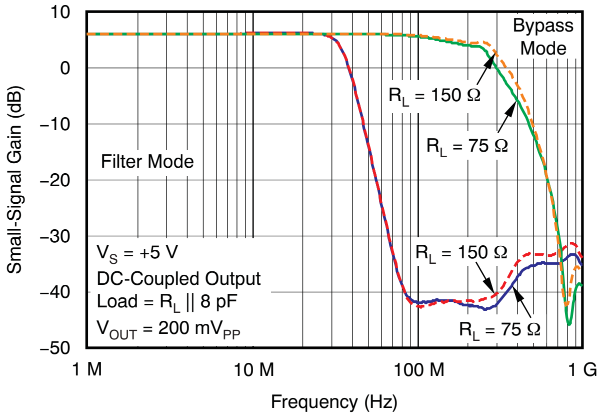


Figure 92.

HD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

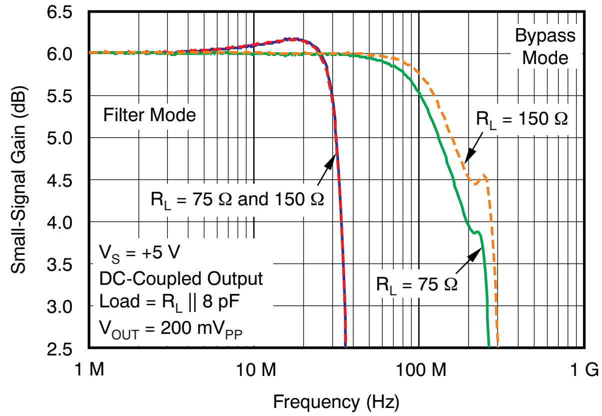


Figure 93.

HD CHANNEL LARGE-SIGNAL GAIN vs FREQUENCY

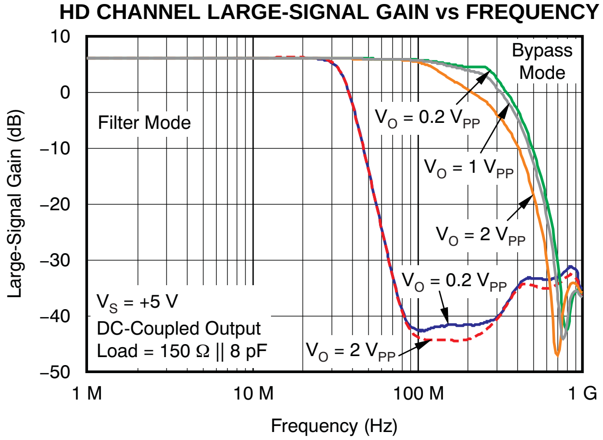


Figure 94.

HD CHANNEL LARGE-SIGNAL GAIN vs FREQUENCY

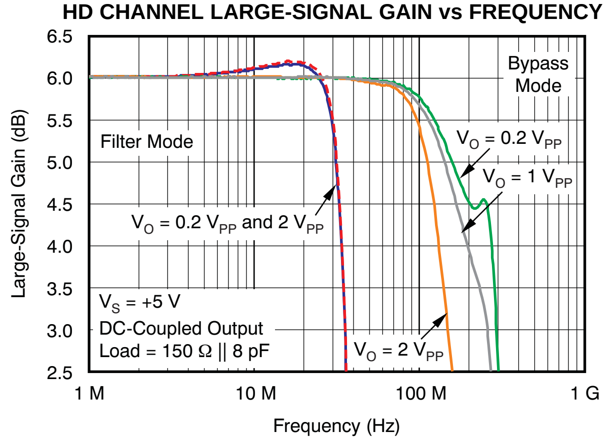


Figure 95.

HD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

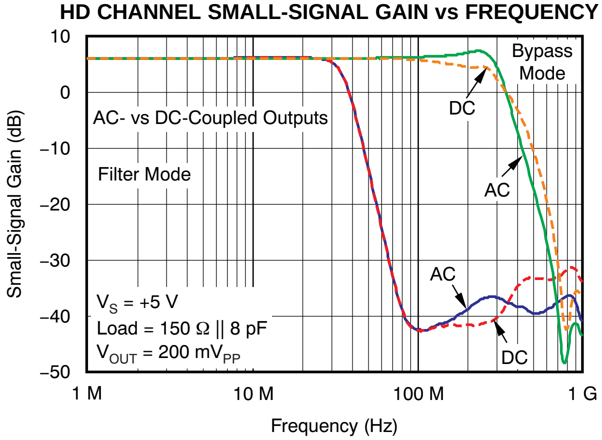


Figure 96.

HD CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

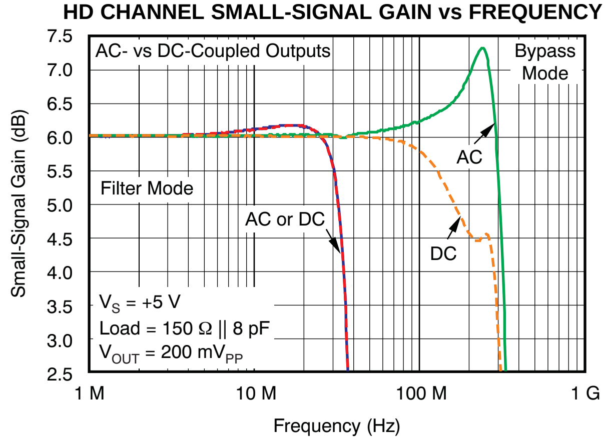


Figure 97.

TYPICAL CHARACTERISTICS: 5 V, High-Definition (HD) Channels (continued)

With load = 150 Ω || 8 pF, dc-coupled input and output, unless otherwise noted.

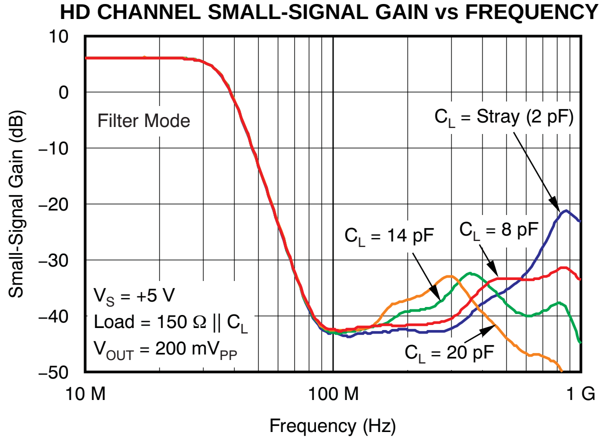


Figure 98.

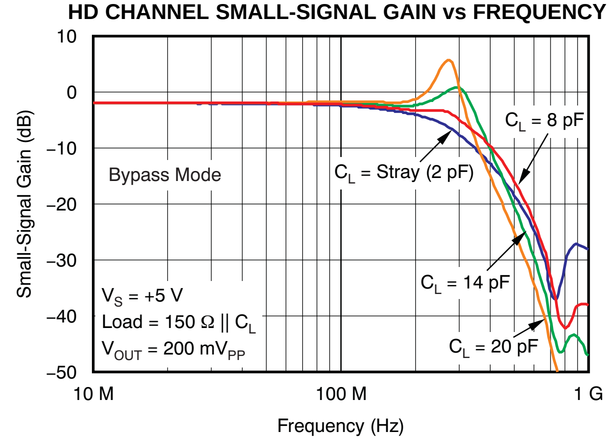


Figure 99.

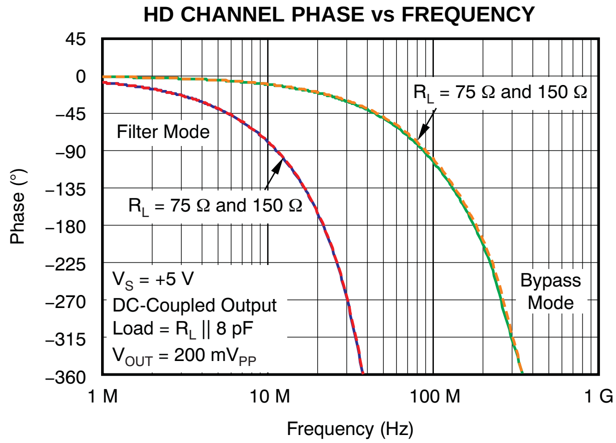


Figure 100.

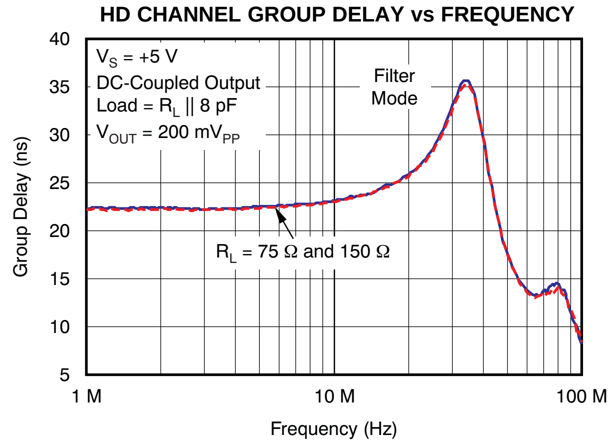


Figure 101.

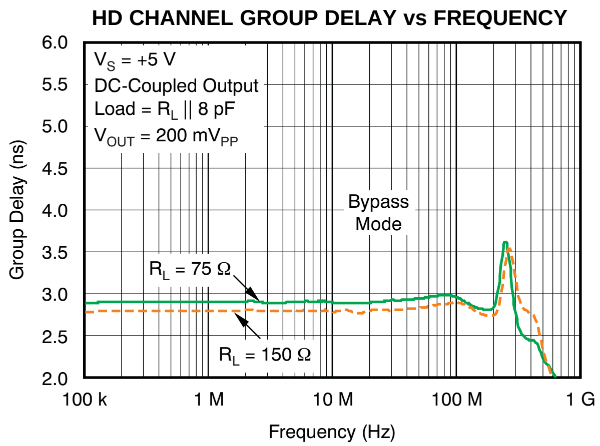


Figure 102.

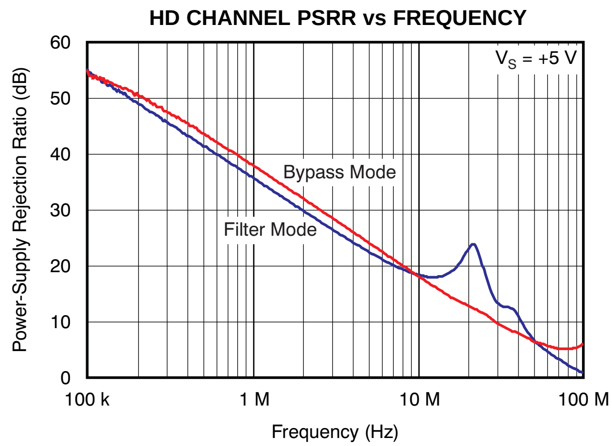


Figure 103.

TYPICAL CHARACTERISTICS: 5 V, High-Definition (HD) Channels (continued)

With load = 150 Ω || 8 pF, dc-coupled input and output, unless otherwise noted.

HD CHANNEL SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

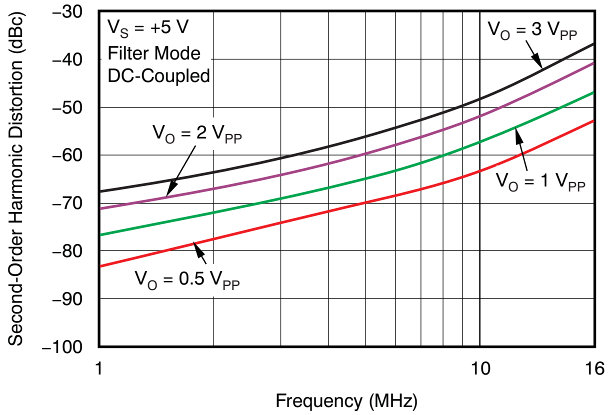


Figure 104.

HD CHANNEL THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

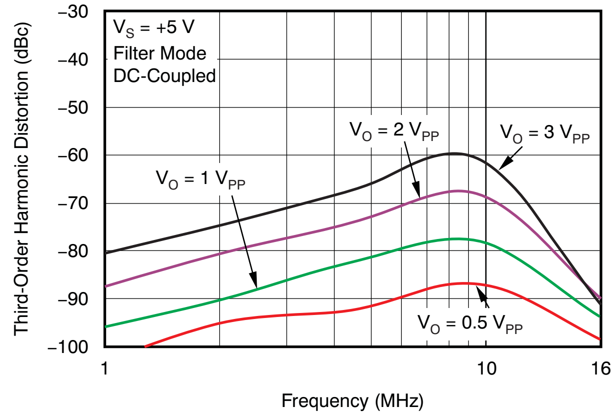


Figure 105.

HD CHANNEL SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

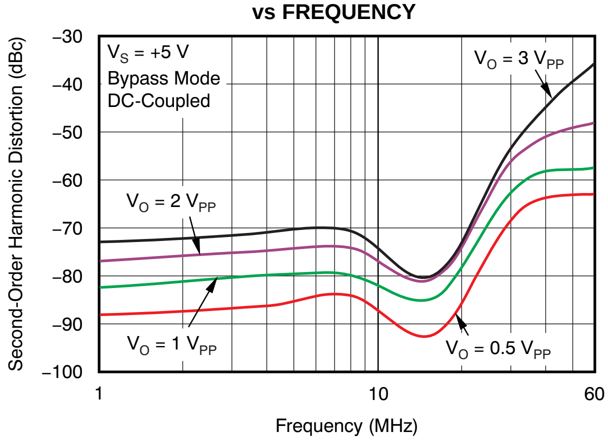


Figure 106.

HD CHANNEL THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

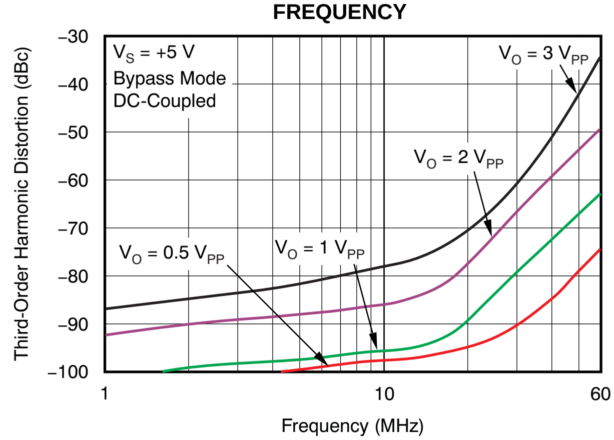


Figure 107.

HD CHANNEL SMALL-SIGNAL PULSE RESPONSE vs TIME

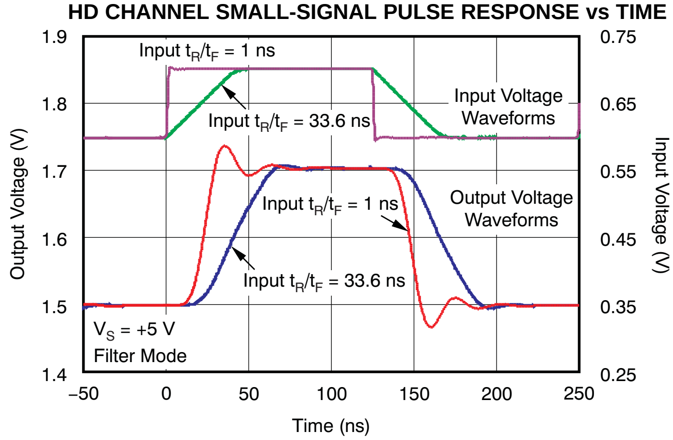


Figure 108.

HD CHANNEL LARGE-SIGNAL PULSE RESPONSE vs TIME

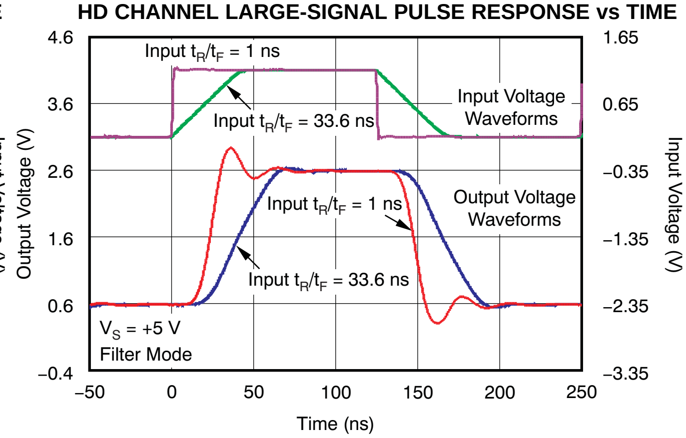


Figure 109.

TYPICAL CHARACTERISTICS: 5 V, High-Definition (HD) Channels (continued)

With load = 150 Ω || 8 pF, dc-coupled input and output, unless otherwise noted.

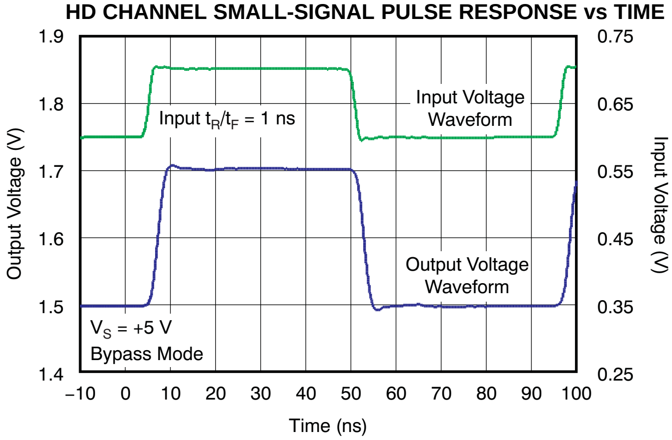


Figure 110.

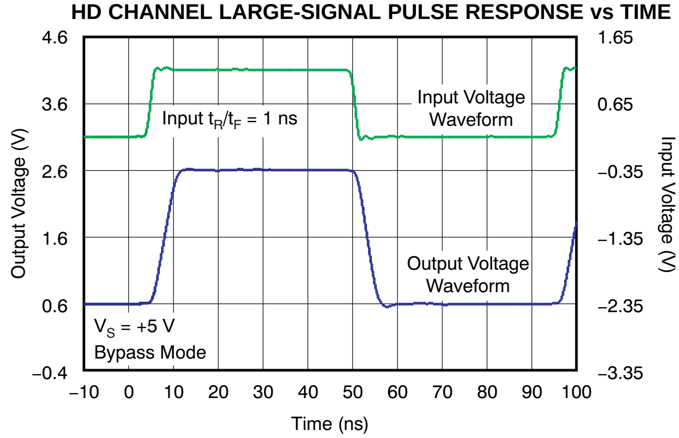


Figure 111.

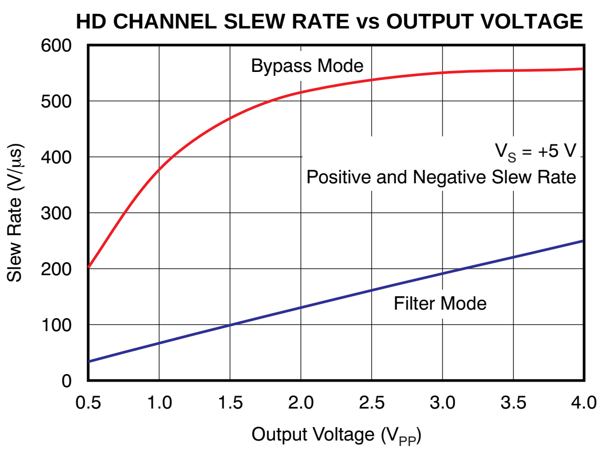


Figure 112.

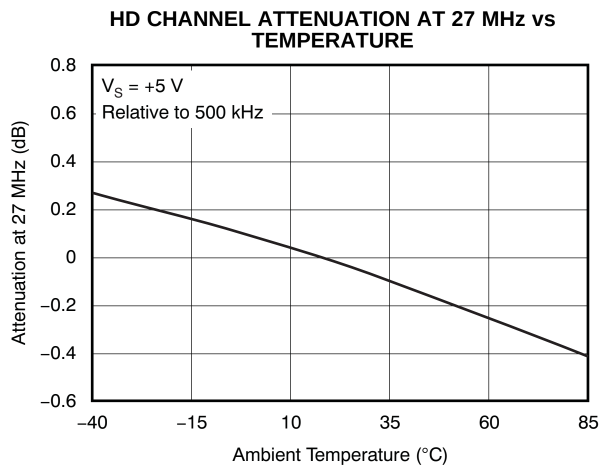


Figure 113.

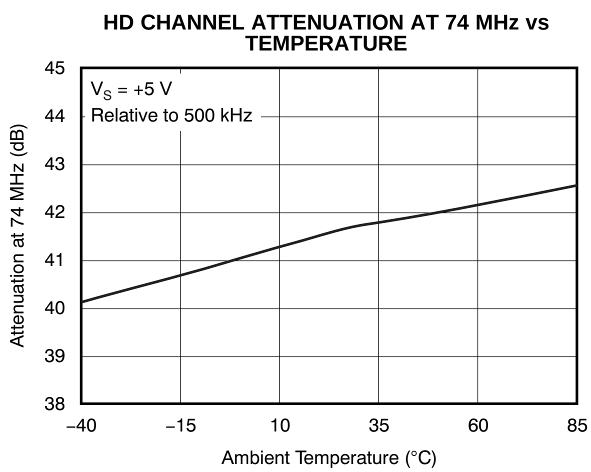


Figure 114.

APPLICATION INFORMATION

The THS7365 is targeted for six-channel video output applications that require three standard-definition (SD) video output buffers and three high-definition (HD) output buffers. Although it can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the THS7365. Built on the revolutionary, complementary Silicon Germanium (SiGe) BiCom3X process, the THS7365 incorporates many features not typically found in integrated video parts while consuming very low power. The THS7365 includes the following features:

- Single-supply 2.7-V to 5-V operation with low total quiescent current of 20.7 mA at 3.3 V and 21.6 mA at 5 V
- Disable mode allows for shutting down individual SD/HD blocks of amplifiers to save system power in power-sensitive applications
- Input configuration accepting dc + level shift, ac sync-tip clamp, or ac-bias
  - AC-biasing is allowed with the use of external pull-up resistors to the positive power supply
- Sixth-order, low-pass filter for DAC reconstruction or ADC image rejection:
  - 9.5 MHz for NTSC, PAL, SECAM, composite video (CVBS), S-Video Y'/C', 480i/576i, Y'/P'$_B$/P'$_R$, and G'B'R' (R'G'B') signals
  - 36 MHz for 720p, 1080i, or up to 1080p30 Y'/P'$_B$/P'$_R$ or G'B'R' signals; also allows up to XGA (1024 × 768 at 60 Hz) R'G'B' video
- Individually-controlled Bypass mode bypasses the low-pass filters for each SD/HD block of amplifiers
  - SD bypass mode features 130-MHz and 100-V/µs performance
  - HD bypass mode features 250-MHz and 500-V/µs performance
- Individually-controlled Disable mode shuts down all amplifiers in each SD/HD block to reduce quiescent current to less than 1 µA
- Internally-fixed gain of 2-V/V (+6-dB) buffer that can drive two video lines with dc-coupling or traditional ac-coupling
- Flow-through configuration using a TSSOP-20 package that complies with the latest lead-free (RoHS-compatible) and green manufacturing requirements

OPERATING VOLTAGE

The THS7365 is designed to operate from 2.7 V to 5 V over a –40°C to +85°C temperature range. The impact on performance over the entire temperature range is negligible as a result of the implementation of thin film resistors and high-quality, low-temperature coefficient capacitors. The design of the THS7365 allows operation down to 2.6 V, but it is recommended to use at least a 3-V supply to ensure that no issues arise with headroom or clipping with 100% color-saturated CVBS signals. If only 75% color saturated CVBS is supported, then the output voltage requirements are reduced to 2 V_{PP} on the output, allowing a 2.7-V supply to be utilized without issues.

A 0.1-µF to 0.01-µF capacitor should be placed as close as possible to the power-supply pins. Failure to do so may result in the THS7365 outputs ringing or oscillating. Additionally, a large capacitor (such as 22 µF to 100 µF) should be placed on the power-supply line to minimize interference with 50-/60-Hz line frequencies.

INPUT VOLTAGE

The THS7365 input range allows for an input signal range from –0.2 V to approximately (V_{S+} – 1.5 V). However, because of the internal fixed gain of 2 V/V (+6 dB) and the internal input level shift of 150 mV (typical), the output is generally the limiting factor for the allowable linear input range. For example, with a 5-V supply, the linear input range is from –0.2 V to 3.5 V. However, because of the gain and level shift, the linear output range limits the allowable linear input range to approximately –0.1 V to 2.3 V.

INPUT OVERVOLTAGE PROTECTION

The THS7365 is built using a very high-speed, complementary, bipolar, and CMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 115.

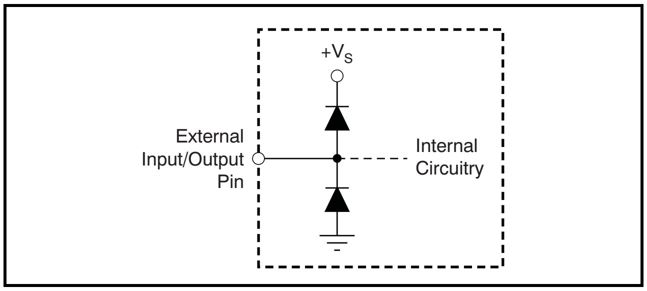


Figure 115. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above and below the supplies as well. The protection diodes can typically support 30 mA of continuous current when overdriven.

TYPICAL CONFIGURATION AND VIDEO TERMINOLOGY

A typical application circuit using the THS7365 as a video buffer is shown in Figure 116. It shows a DAC or encoder driving the input channels of the THS7365. One channel is a CVBS connection while two other channels are for the S-Video Y'/C' signals of an SD video system. These signals can be NTSC, PAL, or SECAM signals. The other three channels are the component video Y'/P'$_B$/P'$_R$ (sometimes labeled Y'U'V' or incorrectly labeled Y'/C'$_B$/C'$_R$) signals. These signals are typically 720p, 1080i, or up to 1080p30 signals. If the video DAC / SOC samples at greater than 74.25 MHz, then 480i/576i or 480p/576p signals are also supported while effectively minimizing DAC images. Because the filters can be bypassed, other formats such as 1080p60 (also known as Full-HD or True-HD) and R'G'B' video up to UWXGA can also be supported with the THS7365.

Note that the *Y'* term is used for the luma channels throughout this document rather than the more common luminance (*Y*) term. This usage accounts for the definition of luminance as stipulated by the International Commission on Illumination (CIE). Video departs from true luminance because a nonlinear term, *gamma*, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Thus, luminance (Y) is not maintained, providing a difference in terminology.

This rationale is also used for the chroma (*C'*) term. Chroma is derived from the nonlinear R'G'B' terms and, thus, it is nonlinear. Chominance (*C*) is derived from linear RGB, giving the difference between chroma (C') and chrominance (C). The color difference signals (P'$_B$/P'$_R$/U'/V') are also referenced in this manner to denote the nonlinear (gamma corrected) signals.

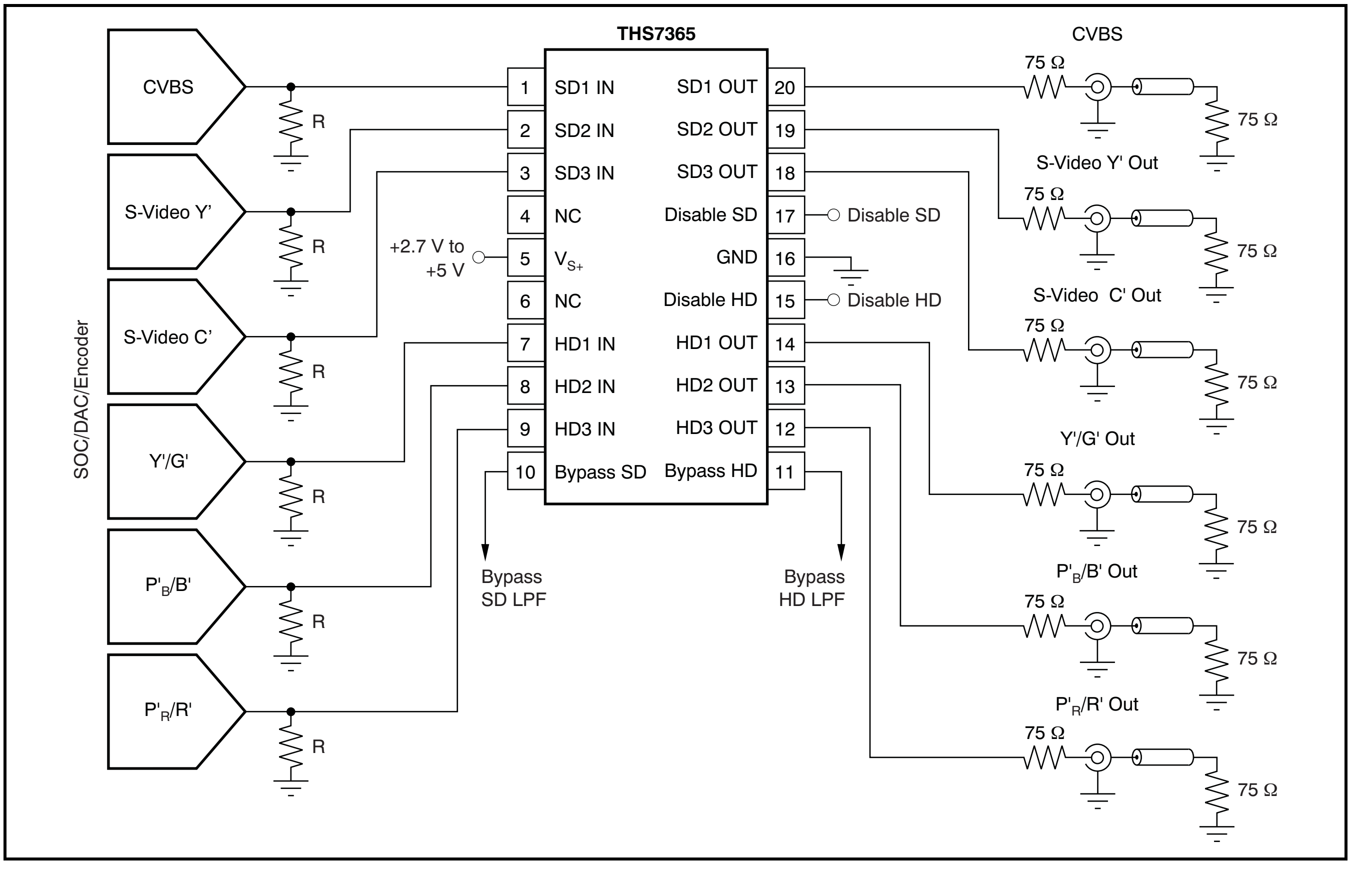


Figure 116. Typical Six-Channel System Inputs from DC-Coupled Encoder/DAC with DC-Coupled Line Driving

R'G'B' (commonly mislabeled *RGB*) is also called G'B'R' (again commonly mislabeled as *GBR*) in professional video systems. The Society of Motion Picture and Television Engineers (SMPTE) component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This practice is consistent with the Y'/P'$_B$/P'$_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be placed first in the system. Because the blue color difference channel (P'$_B$) is next and the red color difference channel (P'$_R$) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel, respectfully. Thus, hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems, sync is embedded on all three channels, but this configuration may not always be the case in all systems.

INPUT MODE OF OPERATION: DC

The inputs to the THS7365 allow for both ac- and dc-coupled inputs. Many DACs or video encoders can be dc-connected to the THS7365. One of the drawbacks to dc-coupling is when 0 V is applied to the input. Although the input of the THS7365 allows for a 0-V input signal without issue, the output swing of a traditional amplifier cannot yield a 0-V signal resulting in possible clipping. This limitation is true for any single-supply amplifier because of the characteristics of the output transistors. Neither CMOS nor bipolar transistors can achieve 0 V while sinking current. This transistor characteristic is also the same reason why the highest output voltage is always less than the power-supply voltage when sourcing current.

This output clipping can reduce the sync amplitudes (both horizontal and vertical sync) on the video signal. A problem occurs if the video signal receiver uses an automatic gain control (AGC) loop to account for losses in the transmission line. Some video AGC circuits derive gain from the horizontal sync amplitude. If clipping occurs on the sync amplitude, then the AGC circuit can increase the gain too much—resulting in too much luma and/or chroma amplitude gain correction. This correction may result in a picture with an overly bright display with too much color saturation.

Other AGC circuits use the chroma burst amplitude for amplitude control; reduction in the sync signals does not alter the proper gain setting. However, it is good engineering design practice to ensure that saturation/clipping does not take place. Transistors always take a finite amount of time to come out of saturation. This saturation could possibly result in timing delays or other aberrations on the signals.

To eliminate saturation or clipping problems, the THS7365 has a 150-mV input level shift feature. This feature takes the input voltage and adds an internal +150-mV shift to the signal. Because the THS7365 also has a gain of 6 dB (2 V/V), the resulting output with a 0-V applied input signal is approximately 300 mV. The THS7365 rail-to-rail output stage can create this output level while connected to a typical video load. This configuration ensures that no saturation or clipping of the sync signals occur. This shift is constant, regardless of the input signal. For example, if a 1-V input is applied, the output is 2.3 V.

Because the internal gain is fixed at +6 dB, the gain dictates what the allowable linear input voltage range can be without clipping concerns. For example, if the power supply is set to 3 V, the maximum output is approximately 2.9 V while driving a significant amount of current. Thus, to avoid clipping, the allowable input is ([2.9 V/2] – 0.15 V) = 1.3 V. This range is valid for up to the maximum recommended 5-V power supply that allows approximately a ([4.9 V/2] – 0.15 V) = 2.3 V input range while avoiding clipping on the output.

The input impedance of the THS7365 in this mode of operation is dictated by the internal, 800-kΩ pull-down resistor, as shown in Figure 117. Note that the internal voltage shift does not appear at the input pin; it only shows at the output pin.

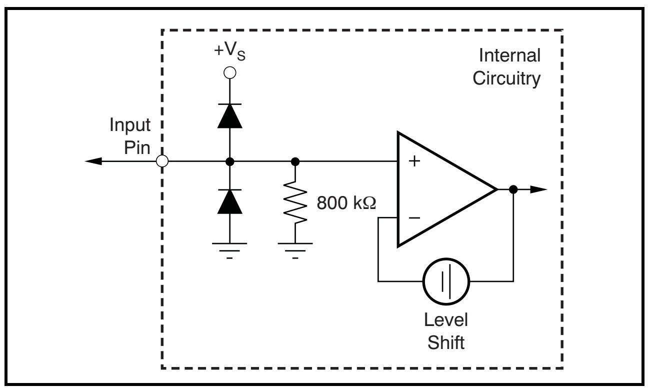


Figure 117. Equivalent DC Input Mode Circuit

INPUT MODE OF OPERATION: AC SYNC TIP CLAMP

Some video DACs or encoders are not referenced to ground but rather to the positive power supply. The resulting video signals are generally at too great a voltage for a dc-coupled video buffer to function properly. To account for this scenario, the THS7365 incorporates a sync-tip clamp circuit. This function requires a capacitor (nominally 0.1 µF) to be in series with the input. Although the term *sync-tip-clamp* is used throughout this document, it should be noted that the THS7365 would probably be better termed as a *dc restoration circuit* based on how this function is performed. This circuit is an active clamp circuit and not a passive diode clamp function.

The input to the THS7365 has an internal control loop that sets the lowest input applied voltage to clamp at ground (0 V). By setting the reference at 0 V, the THS7365 allows a dc-coupled input to also function. Therefore, the sync-tip-clamp (STC) is considered transparent because it does not operate unless the input signal goes below ground. The signal then goes through the same 150-mV level shifter, resulting in an output voltage low level of 300 mV. If the input signal tries to go below 0 V, the THS7365 internal control loop sources up to 6 mA of current to increase the input voltage level on the THS7365 input side of the coupling capacitor. As soon as the voltage goes above the 0-V level, the loop stops sourcing current and becomes very high impedance.

One of the concerns about the sync-tip-clamp level is how the clamp reacts to a sync edge that has overshoot—common in VCR signals, noise, DAC overshoot, or reflections found in poor printed circuit board (PCB) layouts. Ideally, the STC should not react to the overshoot voltage of the input signal. Otherwise, this response could result in clipping on the rest of the video signal because it may raise the bias voltage too much.

To help minimize this input signal overshoot problem, the control loop in the THS7365 has an internal low-pass filter, as shown in Figure 118. This filter reduces the response time of the STC circuit. This delay is a function of how far the voltage is below ground, but in general it is approximately a 400-ns delay for the 9.5-MHz filters and approximately a 150-ns delay for the 36-MHz filters. The effect of this filter is to slow down the response of the control loop so as not to clamp on the input overshoot voltage but rather the flat portion of the sync signal.

As a result of this delay, sync may have an apparent voltage shift. The amount of shift depends on the amount of droop in the signal as dictated by the input capacitor and the STC current flow. Because sync is used primarily for timing purposes with syncing occurring on the edge of the sync signal, this shift is transparent in most systems.

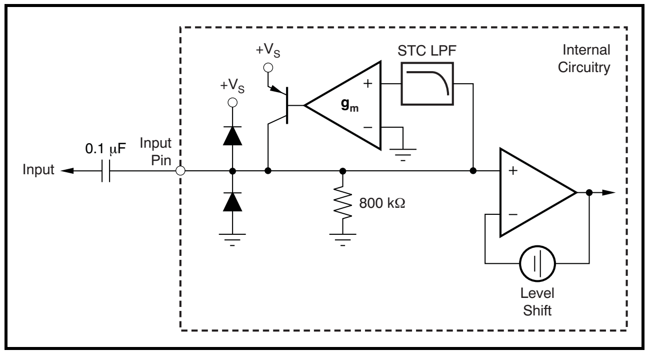


Figure 118. Equivalent AC Sync-Tip-Clamp Input Circuit

While this feature may not fully eliminate overshoot issues on the input signal, in cases of extreme overshoot and/or ringing, the STC system should help minimize improper clamping levels. As an additional method to help minimize this issue, an external capacitor (for example, 10 pF to 47 pF) to ground in parallel with the external termination resistors can help filter overshoot problems.

It should be noted that this STC system is dynamic and does not rely upon timing in any way. It only depends on the voltage that appears at the input pin at any given point in time. The STC filtering helps minimize level shift problems associated with switching noises or very short spikes on the signal line. This architecture helps ensure a very robust STC system.

When the ac STC operation is used, there must also be some finite amount of discharge bias current. As previously described, if the input signal goes below the 0-V clamp level, the internal loop of the THS7365 sources current to increase the voltage appearing at the input pin. As the difference between the signal level and the 0-V reference level increases, the amount of source current increases proportionally—supplying up to 6 mA of current. Thus, the time to re-establish the proper STC voltage can be very fast. If the difference is very small, then the source current is also very small to account for minor voltage droop.

However, what happens if the input signal goes above the 0-V input level? The problem is the video signal is always above this level and must not be altered in any way. Thus, if the sync level of the input signal is above this 0-V level, then the internal discharge (sink) current reduces the ac-coupled bias signal to the proper 0-V level.

This discharge current must not be large enough to alter the video signal appreciably or picture quality issues may arise. This effect is often seen by looking at the tilt (droop) of a constant luma signal being applied and the resulting output level. The associated change in luma level from the beginning and end of the video line is the amount of line tilt (droop).

If the discharge current is very small, the amount of tilt is very low, which is a generally a good thing. However, the amount of time for the system to capture the sync signal could be too long. This effect is also termed *hum rejection*. Hum arises from the ac line voltage frequency of 50 Hz or 60 Hz. The value of the discharge current and the ac-coupling capacitor combine to dictate the hum rejection and the amount of line tilt.

To allow for both dc- and ac-coupling in the same part, the THS7365 incorporates an 800-kΩ resistor to ground. Although a true constant current sink is preferred over a resistor, there can be issues when the voltage is near ground. This configuration can cause the current sink transistor to saturate and cause potential problems with the signal. The 800-kΩ resistor is large enough to not impact a dc-coupled DAC termination. For discharging an ac-coupled source, Ohm's Law is used. If the video signal is 1 V, then there is 1 V/800 kΩ = 1.25-µA of discharge current. If more hum rejection is desired or there is a loss of sync occurring, then simply decrease the 0.1-µF input coupling capacitor. A decrease from 0.1 µF to 0.047 µF increases the hum rejection by a factor of 2.1. Alternatively, an external pull-down resistor to ground may be added that decreases the overall resistance and ultimately increases the discharge current.

To ensure proper stability of the ac STC control loop, the source impedance must be less than 1-kΩ with the input capacitor in place. Otherwise, there is a possibility of the control loop ringing, which may appear on the output of the THS7365. Because most DACs or encoders use resistors to establish the voltage, which are typically less than 300-Ω, meeting the less than 1-kΩ requirement is easily done. However, if the source impedance looking from the THS7365 input perspective is very high, then simply adding a 1-kΩ resistor to GND ensures proper operation of the THS7365.

INPUT MODE OF OPERATION: AC BIAS

Sync-tip clamps work very well for signals that have horizontal and/or vertical syncs associated with them; however, some video signals do not have a sync embedded within the signal. If ac-coupling of these signals is desired, then a dc bias is required to properly set the dc operating point within the THS7365. This function is easily accomplished with the THS7365 by simply adding an external pull-up resistor to the positive power supply, as shown in Figure 119.

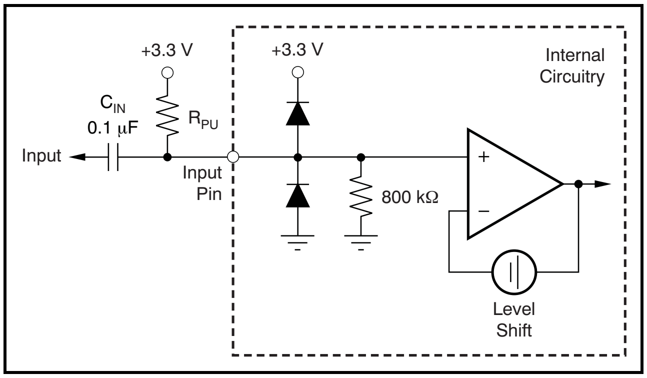


Figure 119. AC-Bias Input Mode Circuit Configuration

The dc voltage appearing at the input pin is equal to Equation 1:

$$V_{DC} = V_S \left(\frac{800\ k\Omega}{800\ k\Omega + R_{PU}} \right) \quad (1)$$

The THS7365 allowable input range is approximately 0 V to (V_{S+} – 1.5 V), allowing for a very wide input voltage range. As such, the input dc bias point is very flexible, with the output dc bias point being the primary factor. For example, if the output dc bias point is desired to be 1.6 V on a 3.3-V supply, then the input dc bias point should be (1.6 V – 300 mV)/2 = 0.65 V. Thus, the pull-up resistor calculates to approximately 3.3 MΩ, resulting in 0.644 V. If the output dc-bias point is desired to be 1.6 V with a 5-V power supply, then the pull-up resistor calculates to approximately 5.36 MΩ.

Keep in mind that the internal 800-kΩ resistor has approximately a ±20% variance. As such, the calculations should take this variance into account. For the 0.644-V example above, using an ideal 3.3-MΩ resistor, the input dc bias voltage is approximately 0.644 V ± 0.1 V.

The value of the output bias voltage is very flexible and is left to each individual design. It is important to ensure that the signal does not clip or saturate the video signal. Thus, it is recommended to ensure the output bias voltage is between 0.9 V and (V_{S+} – 1 V). For 100% color saturated CVBS or signals with

Macrovision®, the CVBS signal can reach up to 1.23 V_{PP} at the input, or 2.46 V_{PP} at the output of the THS7365. In contrast, other signals are typically 1 V_{PP} or 0.7 V_{PP} at the input which translate to an output voltage of 2 V_{PP} or 1.4 V_{PP}. The output bias voltage must account for a worst-case situation, depending on the signals involved.

One other issue that must be taken into account is the dc-bias point is a function of the power supply. As such, there is an impact on system PSRR. To help reduce this impact, the input capacitor combines with the pull-up resistance to function as a low-pass filter. Additionally, the time to charge the capacitor to the final dc bias point is a function of the pull-up resistor and the input capacitor size. Lastly, the input capacitor forms a high-pass filter with the parallel impedance of the pull-up resistor and the 800-kΩ resistor. In general, it is good to have this high-pass filter at approximately 3 Hz to minimize any potential droop on a P'_B, P'_R, or non-sync B' or R' signal. A 0.1-µF input capacitor with a 3.3-MΩ pull-up resistor equates to approximately a 2.5-Hz high-pass corner frequency.

This mode of operation is recommended for use with chroma (C'), P'_B, P'_R, U', V', and non-sync R'G'B' signals. This method can also be used with sync signals if desired. The benefit of using the STC function over the ac-bias configuration on embedded sync signals is that the STC maintains a constant *back-porch* voltage as opposed to a back-porch voltage that fluctuates depending on the video content. Because the high-pass corner frequency is a very low 2.5 Hz, the impact on the video signal is negligible relative to the STC configuration.

One question may arise over the P'_B and P'_R channels. For 480i, 576i, 480p, and 576p signals, a sync may or may not be present. If no sync exists within the signal, then it is obvious that ac-bias is the preferred method of ac-coupling the signal.

For 720p, 1080i, and 1080p signals, or for the the 480i, 576i, 480p, and 576p signals with sync present on the P'_B and P'_R channels, the lowest voltage of the sync is –300 mV below the midpoint reference voltage of 0 V. The P'_B and P'_R signals allow a signal to be as low as –350 mV below the midpoint reference voltage of 0 V. This allowance corresponds to 100% yellow for P'_B signal or 100% cyan for P'_R signal . Because the P'_B and P'_R signal voltage can be lower than the sync voltage, there exists a potential for clipping of the signal for a short period of time if the signals drop below the sync voltage.

The THS7365 does include a 150-mV input level shift, or 300 mV at the output, that should mitigate any clipping issues. For example, if a STC is used, then the bottom of the sync is 300 mV at the output. If the signal does go the lowest level, or 50 mV lower than the sync at the input, then the instantaneous output is (–50 mV + 150 mV) × 2 = 200 mV at the output.

Another potential risk is that if this signal (100% yellow for P'_B or 100% cyan for P'_R) exists for several pixels, then the STC circuit engages to raise the voltage back to 0 V at the input. This function can cause a 50-mV level shift at the input midway through the active video signal. This effect is undesirable and can cause errors in the decoding of the signal.

It is therefore recommended to use ac bias mode for component P'_B and P'_R signals when ac-coupling is desired.

OUTPUT MODE OF OPERATION: DC-COUPLED

The THS7365 incorporates a rail-to-rail output stage that can be used to drive the line directly without the need for large ac-coupling capacitors. This design offers the best line tilt and field tilt (droop) performance because no ac-coupling occurs. Keep in mind that if the input is ac-coupled, then the resulting tilt as a result of the input ac-coupling continues to be seen on the output, regardless of the output coupling. The 80-mA output current drive capability of the THS7365 is designed to drive two video lines simultaneously—essentially, a 75-Ω load—while keeping the output dynamic range as wide as possible. Figure 120 shows the THS7365 driving two video lines while keeping the output dc-coupled.

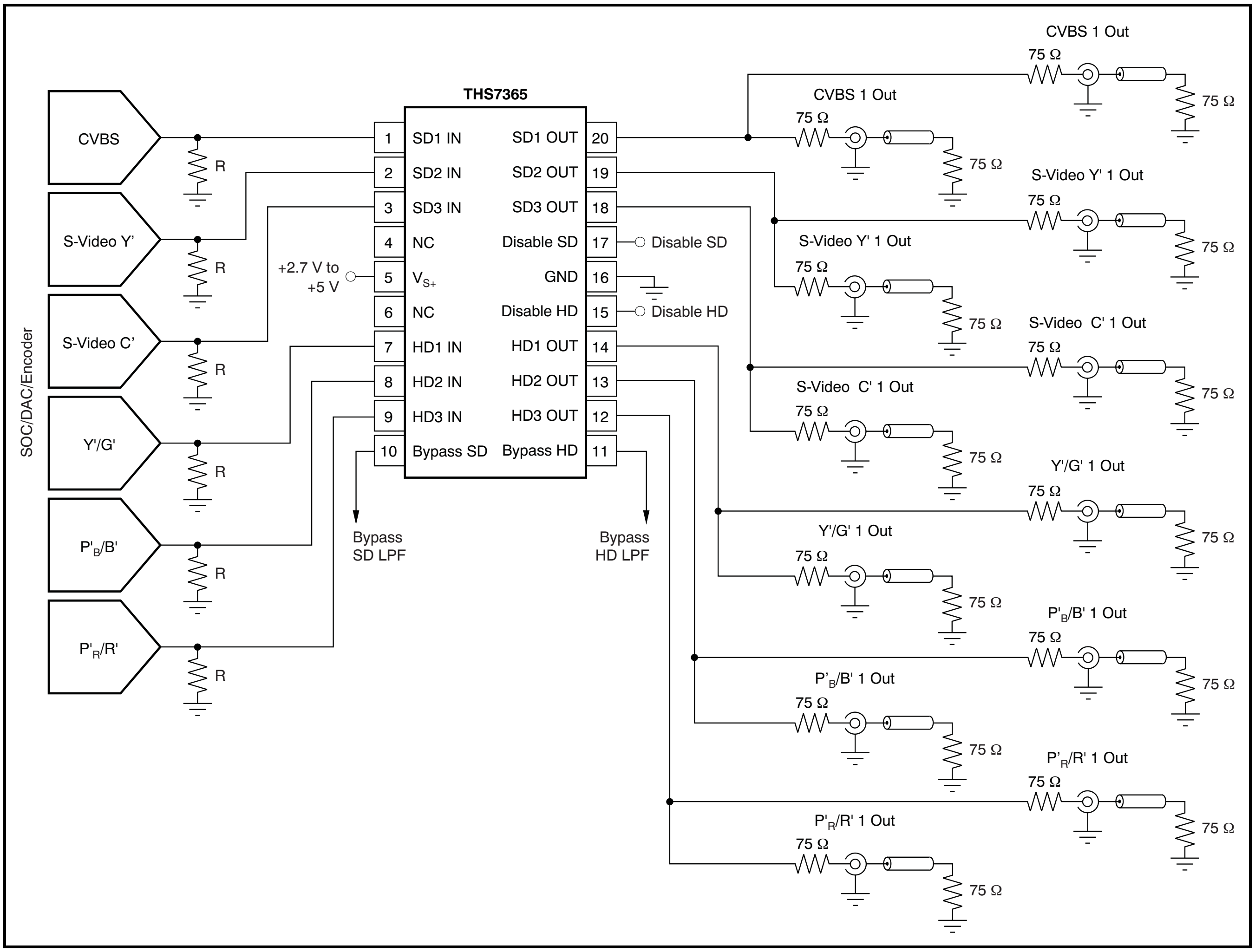


Figure 120. Typical Six-Channel System with DC-Coupled Line Driving and Two Outputs Per Channel

One concern of dc-coupling, however, arises if the line is terminated to ground. If the ac-bias input configuration is used, the output of the THS7365 has a dc bias on the output, such as 1.6 V. With two lines terminated to ground, this configuration allows a dc current path to flow, such as 1.6 V/75-Ω = 21.3 mA. The result of this configuration is a slightly decreased high output voltage swing and an increase in power dissipation of the THS7365. While the THS7365 was designed to operate with a junction temperature of up to +125°C, care must be taken to ensure that the junction temperature does not exceed this level or else long-term reliability could suffer. Using a 5-V supply, this configuration can result in an additional dc power dissipation of (5 V – 1.6 V) × 21.3 mA = 72.5 mW per channel. With a 3.3-V supply, this dissipation reduces to 36.2 mW per channel. The overall low quiescent current of the THS7365 design minimizes potential thermal issues even when using the TSSOP package at high ambient temperatures, but power and thermal analysis should always be examined in any system to ensure that no issues arise. Be sure to utilize RMS power and not instantaneous power when evaluating the thermal performance.

Note that the THS7365 can drive the line with dc-coupling regardless of the input mode of operation. The only requirement is to make sure the video line has proper termination in series with the output (typically 75 Ω). This requirement helps isolate capacitive loading effects from the THS7365 output. Failure to isolate capacitive loads may result in instabilities with the output buffer, potentially causing ringing or oscillations to appear. The stray capacitance appearing directly at the THS7365 output pins should be kept below 220 pF for the 9.5-MHz filter channels and below 15 pF for the 36-MHz filter channels. One way to help ensure this condition is satisfied is to make sure the 75-Ω source resistor is placed next to each THS7365 output pin. If a large ac-coupling capacitor is used, the capacitor should be placed after this resistor.

There are many reasons dc-coupling is desirable, including reduced costs, PCB area, and no line tilt. A common question is whether or not there are any drawbacks to using dc-coupling. There are some potential issues that must be examined, such as the dc current bias as discussed above. Another potential risk is whether this configuration meets industry standards. EIA-770 stipulates that the back-porch shall be 0 V ± 1 V as measured at the receiver. With a double-terminated load system, this requirement implies a 0 V ± 2 V level at the video amplifier output. The THS7365 can easily meet this requirement without issue. However, in Japan, the EIAJ CP-1203 specification stipulates a 0 V ± 0.1 V level with no signal. This requirement can be met with the THS7365 in shutdown mode, but while active it cannot meet this specification without output ac-coupling. AC-coupling the output essentially ensures that the video signal works with any system and any specification. For many modern systems, however, dc-coupling can satisfy most needs.

OUTPUT MODE OF OPERATION: AC-COUPLED

A very common method of coupling the video signal to the line is with a large capacitor. This capacitor is typically between 220 μF and 1000 μF, although 470 μF is very typical. The value of this capacitor must be large enough to minimize the line tilt (droop) and/or field tilt associated with ac-coupling as described previously in this document. AC-coupling is performed for several reasons, but the most common is to ensure full interoperability with the receiving video system. This approach ensures that regardless of the reference dc voltage used on the transmitting side, the receiving side re-establishes the dc reference voltage to its own requirements.

In the same way as the dc output mode of operation discussed previously, each line should have a 75-Ω source termination resistor in series with the ac-coupling capacitor. This 75-Ω resistor should be placed next to the THS7365 output to minimize capacitive loading effects. If two lines are to be driven, it is best to have each line use its own capacitor and resistor rather than sharing these components. This configuration helps ensure line-to-line dc isolation and eliminates the potential problems as described previously. Using a single, 1000-μF capacitor for two lines is permissible, but there is a chance for interference between the two receivers.

Lastly, because of the edge rates and frequencies of operation, it is recommended (but not required) to place a 0.1-μF to 0.01-μF capacitor in parallel with the large 220-μF to 1000-μF capacitor. These large value capacitors are most commonly aluminum electrolytic. It is well-known that these capacitors have significantly large equivalent series resistance (ESR), and the impedance at high frequencies is rather large as a result of the associated inductances involved with the leads and construction. The small 0.1-μF to 0.01-μF capacitors help pass these high-frequency signals (greater than 1 MHz) with much lower impedance than the large capacitors.

Although it is common to use the same capacitor values for all the video lines, the frequency bandwidth of the chroma signal in a S-Video system is not required to go as low (or as high of a frequency) as the luma channels. Thus, the capacitor values of the chroma line(s) can be smaller, such as 0.1 μF.

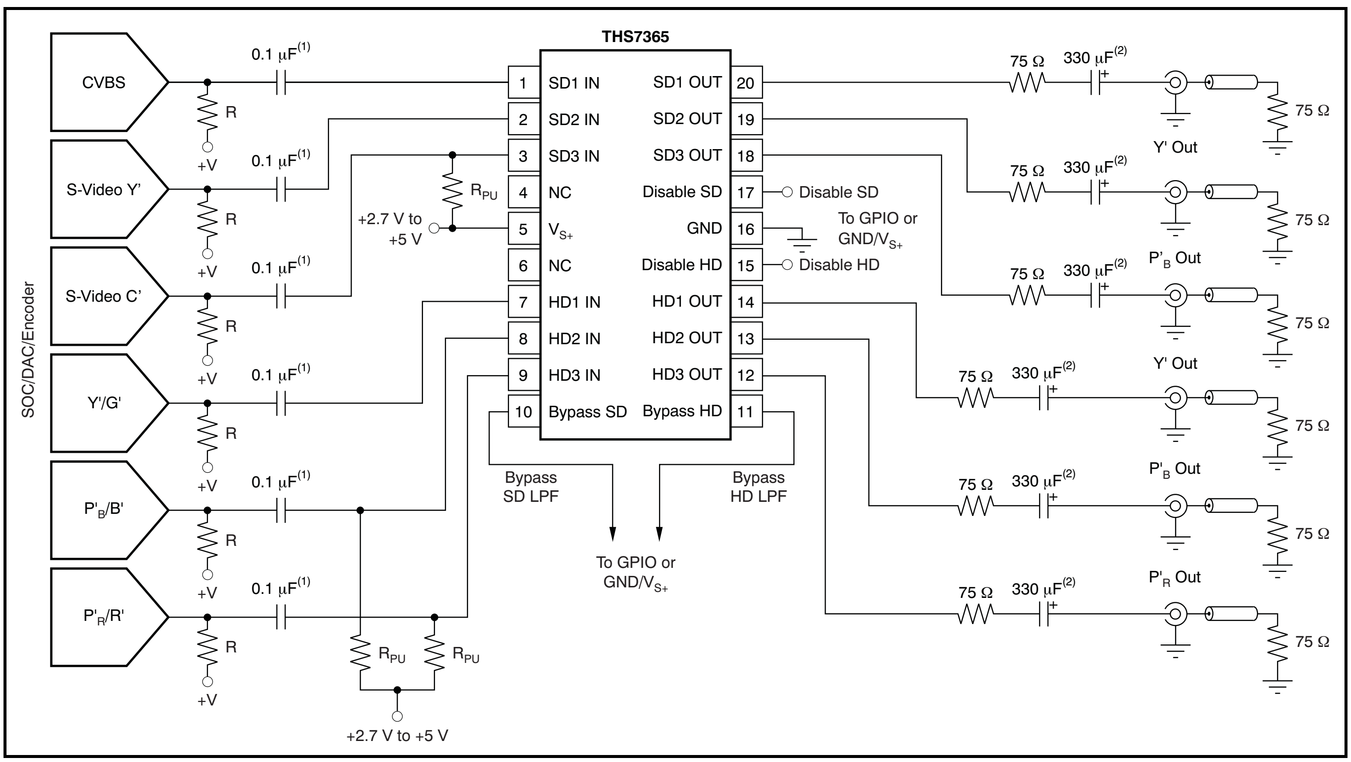
Figure 121 shows a typical configuration where the input is ac-coupled and the output is also ac-coupled. AC-coupled inputs are generally required when current-sink DACs are used or the input is connected to an unknown source, such as when the THS7365 is used as an input device.

LOW-PASS FILTER

Each channel of the THS7365 incorporates a sixth-order, low-pass filter. These video reconstruction filters minimize DAC images from being passed onto the video receiver. Depending on the receiver design, failure to eliminate these DAC images can cause picture quality problems because of aliasing of the ADC in the receiver. Another benefit of the filter is to smooth out aberrations in the signal that some DACs can have if the internal filtering is not very good. This benefit helps with picture quality and ensures that the signal meets video bandwidth requirements.

Each filter has an associated Butterworth characteristic. The benefit of the Butterworth response is that the frequency response is flat with a relatively steep initial attenuation at the corner frequency. The problem with this characteristic is that the group delay rises near the corner frequency. Group delay is defined as the change in phase (radians/second) divided by a change in frequency. An increase in group delay corresponds to a time domain pulse response that has overshoot and some possible ringing associated with the overshoot.

The use of other type of filters, such as elliptic or chebyshev, are not recommended for video applications because of the very large group delay variations near the corner frequency resulting in significant overshoot and ringing. While these filters may help meet the video standard specifications with respect to amplitude attenuation, the group delay is well beyond the standard specifications. Considering this delay with the fact that video can go from a white pixel to a black pixel over and over again, it is easy to see that ringing can occur. Ringing typically causes a display to have ghosting or fuzziness appear on the edges of a sharp transition. On the other hand, a Bessel filter has ideal group delay response, but the rate of attenuation is typically too low for acceptable image rejection. Thus, the Butterworth filter is a respectable compromise for both attenuation and group delay.



(1) AC-coupled input is shown in this example. DC-coupling is also allowed as long as the DAC output voltage is within the allowable linear input and output voltage range of the THS7365. To apply dc-coupling, remove the 0.1-µF input capacitors and the R_{PU} pull-up resistors along with connecting the DAC termination resistors (R) to ground.

(2) This example shows an ac-coupled output. DC-coupling is also allowed by simply removing these capacitors.

Figure 121. Typical AC Input System Driving AC-Coupled Video Lines

The THS7365 SD filters have a nominal corner (–3 dB) frequency at 9.5MHz and a –1-dB passband typically at 8.2MHz. This 9.5-MHz filter is ideal for SD NTSC, PAL, and SECAM composite video (CVBS) signals. It is also useful for S-Video signals (Y'C'), 480i/576i Y'/P'$_B$/P'$_R$, Y'U'V', broadcast G'B'R' signals, and computer R'G'B' video signals. The 9.5-MHz, –3-dB corner frequency was designed to achieve 54 dB of attenuation at 27 MHz—a common sampling frequency between the DAC/ADC second and third Nyquist zones found in many video systems. This consideration is important because any signal that appears around this frequency can also appear in the baseband as a result of aliasing effects of an ADC found in a receiver.

The THS7365 HD filters have a nominal corner (–3 dB) frequency at 36MHz and a –1-dB passband typically at 32MHz. This 36-MHz filter is ideal for HD 720p, 1080i, up to 1080p30 Y'/P'$_B$/P'$_R$, broadcast G'B'R' signals, and computer R'G'B' video signals up to XGA. The 36-MHz, –3-dB corner frequency was designed to achieve 42 dB of attenuation at 74.25 MHz—a common sampling frequency between the DAC/ADC second and third Nyquist zones found in many video systems.

Keep in mind that images do not stop at the DAC sampling frequency, f_S (for example, 27 MHz for traditional SD DACs); they continue around the sampling frequencies of 2x f_S, 3x f_S, 4x f_S, and so on (that is, 54-MHz, 81-MHz, 108-MHz, etc.). Because of these multiple images, an ADC can fold down into the baseband signal, meaning that the low-pass filter must also eliminate these higher-order images. The THS7365 filters are Butterworth filters and, as such, do not *bounce* at higher frequencies, thus maintaining good attenuation performance.

The filter frequencies were chosen to account for process variations in the THS7365. To ensure the required video frequencies are effectively passed, the filter corner frequency must be high enough to allow component variations. The other consideration is that the attenuation must be large enough to ensure the anti-aliasing/reconstruction filtering is sufficient to meet the system demands. Thus, the selection of the filter frequencies was not arbitrarily selected and is a good compromise that should meet the demands of most systems.

One of the features of the THS7365 is that these filters can be bypassed. Bypassing the SD filters results in an amplifier with 130-MHz bandwidth and 100-V/µs slew rate. This configuration can be helpful when diagnosing potential system issues or when simply wishing to pass higher frequency signals through the system.

Bypassing the HD filters results in a amplifier supporting 250-MHz bandwidth and 500-V/µs slew rate. This configuration supports 1080p60 signals and also computer R'G'B' signals up to UWXGA resolution.

BENEFITS OVER PASSIVE FILTERING

Two key benefits of using an integrated filter system, such as the THS7365, over a passive system are PCB area and filter variations. The small TSSOP-20 package for six video channels is much smaller over a passive RLC network, especially a six-pole passive network. Additionally, consider that inductors have at best ±10% tolerances (normally, ±15% to ±20% is common) and capacitors typically have ±10% tolerances. Using a Monte Carlo analysis shows that the filter corner frequency (–3 dB), flatness (–1 dB), Q factor (or peaking), and channel-to-channel delay have wide variations. These variances can lead to potential performance and quality issues in mass-production environments. The THS7365 solves most of these problems with the corner frequency being essentially the only variable.

Another concern about passive filters is the use of inductors. Inductors are magnetic components, and are therefore susceptible to electromagnetic coupling/interference (EMC/EMI). Some common coupling can occur because of other video channels nearby using inductors for filtering, or it can come from nearby switched-mode power supplies. Some other forms of coupling could be from outside sources with strong EMI radiation and can cause failure in EMC testing such as required for CE compliance.

One concern about an active filter in an integrated circuit is the variation of the filter characteristics when the ambient temperature and the subsequent die temperature changes. To minimize temperature effects, the THS7365 uses low-temperature coefficient resistors and high-quality, low-temperature coefficient capacitors found in the BiCom3X process. These filters have been specified by design to account for process variations and temperature variations to maintain proper filter characteristics. This approach maintains a low channel-to-channel time delay that is required for proper video signal performance.

Another benefit of the THS7365 over a passive RLC filter is the input and output impedance. The input impedance presented to the DAC varies significantly, from 35 Ω to over 1.5 kΩ with a passive network, and may cause voltage variations over frequency. The THS7365 input impedance is 800 kΩ, and only the 2-pF input capacitance plus the PCB trace capacitance impact the input impedance. As such, the voltage variation appearing at the DAC output is better controlled with a fixed termination resistor and the high input impedance buffer of the THS7365.

On the output side of the filter, a passive filter again has a large impedance variation over frequency. The EIA770 specifications require the return loss to be at least 25 dB over the video frequency range of usage. For a video system, this requirement implies the source impedance (which includes the source, series resistor, and the filter) must be better than 75 Ω, +9/–8 Ω. The THS7365 is an operational amplifier that approximates an ideal voltage source, which is desirable because the output impedance is very low and can source and sink current. To properly match the transmission line characteristic impedance of a video line, a 75-Ω series resistor is placed on the output. To minimize reflections and to maintain a good return loss meeting EIA specifications, this output impedance must maintain a 75-Ω impedance. A wide impedance variation of a passive filter cannot ensure this level of performance. On the other hand, the THS7365 has approximately 0.7 Ω of output impedance, or a return loss of 46 dB, at 6.75 MHz for the SD filters and approximately 1.7 Ω of output impedance, or a return loss of 39 dB, at 30 MHz for the HD filters. Thus, the system is matched significantly better with a THS7365 compared to a passive filter.

One final benefit of the THS7365 over a passive filter is power dissipation. A DAC driving a video line must be able to drive a 37.5-Ω load: the receiver 75-Ω resistor and the 75-Ω impedance matching resistor next to the DAC to maintain the source impedance requirement. This requirement forces the DAC to drive at least 1.25 V_P (100% saturation CVBS)/37.5 Ω = 33.3 mA. A DAC is a current-steering element, and this amount of current flows internally to the DAC even if the output is 0 V. Thus, power dissipation in the DAC may be very high, especially when six channels are being driven. Using the THS7365 with a high input impedance and the capability to drive up to two video lines per channel can reduce DAC power dissipation significantly. This outcome is possible because the resistance that the DAC drives can be substantially increased. It is common to set this resistance in a DAC by a current-setting resistor on the DAC itself. Thus, the resistance can be 300 Ω or more, substantially reducing the current drive demands from the DAC and saving significant amounts of power. For example, a 3.3-V, six-channel DAC dissipates 660 mW alone for the steering current capability (six channels × 33.3 mA × 3.3 V) if it must drive a 37.5-Ω load. With a 300-Ω load, the DAC power dissipation as a result of current steering current would only be 82 mW (six channels × 4.16 mA × 3.3 V).

EVALUATION MODULE

To evaluate the THS7365, an evaluation module (EVM) is available. The EVM allows for testing the THS7365 in many different configurations. Inputs and outputs include BNC connectors commonly found in video systems, along with 75-Ω input termination resistors, 75-Ω series source termination resistors, and 75-Ω characteristic impedance traces. Several unpopulated component pads are found on the EVM to allow for different input and output configurations as dictated by the user. This EVM is designed to be used with a single supply from 2.6 V up to 5 V.

The EVM default input configuration sets all channels for dc input coupling. The input signal must be within 0 V to approximately 1.4 V for proper operation. Failure to be within this range saturates and/or clips the output signal. If the input range is beyond this, or if the signal voltage is unknown, or coming from a current sink DAC, then ac input configuration is desired. This option is easily accomplished with the EVM by simply replacing Z_1 through Z_6 0-Ω resistors with 0.1-μF capacitors.

For ac-coupled input and sync-tip clamp (STC) functionality commonly used for CVBS, s-video Y', component Y' signals, and R'G'B' signals with embedded sync, no other changes are needed. However, if a bias voltage is needed after the input capacitor which is commonly needed for s-video C', component $P_{'B}$ and P'_R, and non-sync embedded R'G'B' signals, then a pull-up resistor should be added to the signal on the EVM. This configuration is easily achieved by simply adding a resistor to any of the following resistor pads; RX7 to RX12. A common value to use is 3.3 MΩ. Note that even signals with embedded sync can also use bias mode if desired.

The EVM default output configuration sets all channels for ac output coupling. The 470-μF and 0.1-μF capacitors work well for most ac-coupled systems. However, if dc-coupled output is desired, then replacing the 0.1-μF capacitors (C20, C22, C24, C26, C28, and/or C30) with 0-Ω resistors works well. Removing the 470-μF capacitors is optional, but removing them from the EVM eliminates a few picofarads of stray capacitance on each signal path which may be desirable.

The THS7365 incorporates an easy method to configure the bypass modes and the disable modes. The use of JP4 controls the SD channels disable feature; JP6 controls the HD Channels disable feature; JP3 controls the SD channels filter/bypass mode; and JP5 controls the HD channels filter/bypass mode. While there is a space on the EVM for JP1 and JP2, these are not used for the THS7365.

Connection of JP4 and JP6 to GND applies 0 V to the disable pins and the THS7365 operates normally. Moving JP4 to $+V_S$ causes the THS7365 SD channels to be in disable mode, while moving JP6 to $+V_S$ causes the THS7365 HD channels to be in disable mode .

Connection of JP3 to GND places the THS7365 SD channels in filter mode while moving JP3 to $+V_S$ places the THS7365 HD channels in bypass mode. Connection of JP5 to GND places the THS7365 HD channels in filter mode while moving JP5 to $+V_S$ places the THS7365 HD channels in bypass mode.

Figure 122 shows the EVM schematic. Figure 123 and Figure 124 illustrate the two layers of the EVM PCB, incorporating standard high-speed layout practices. Table 1 lists the bill of materials as the board comes supplied from Texas Instruments.

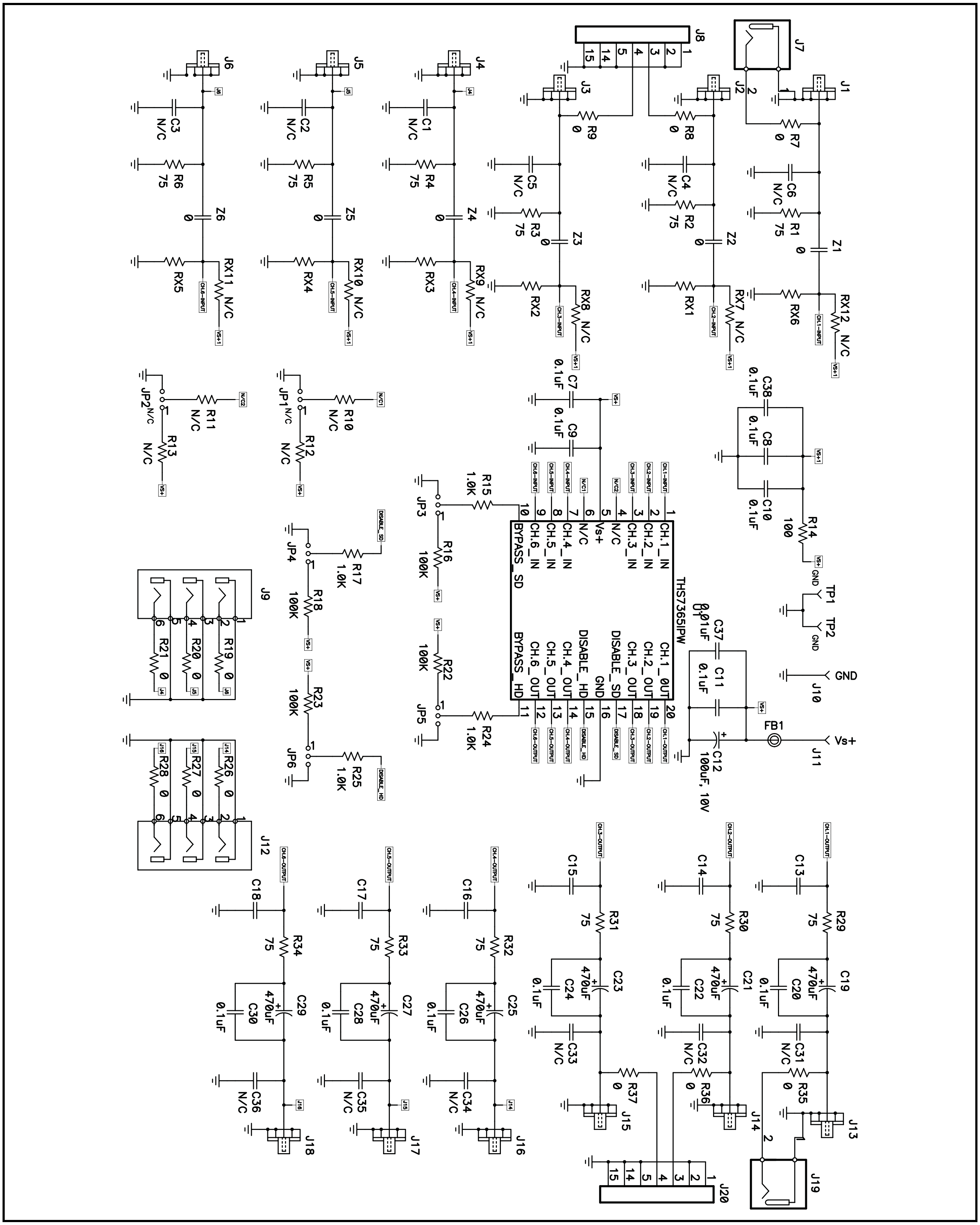


Figure 122. THS7365 EVM Schematic

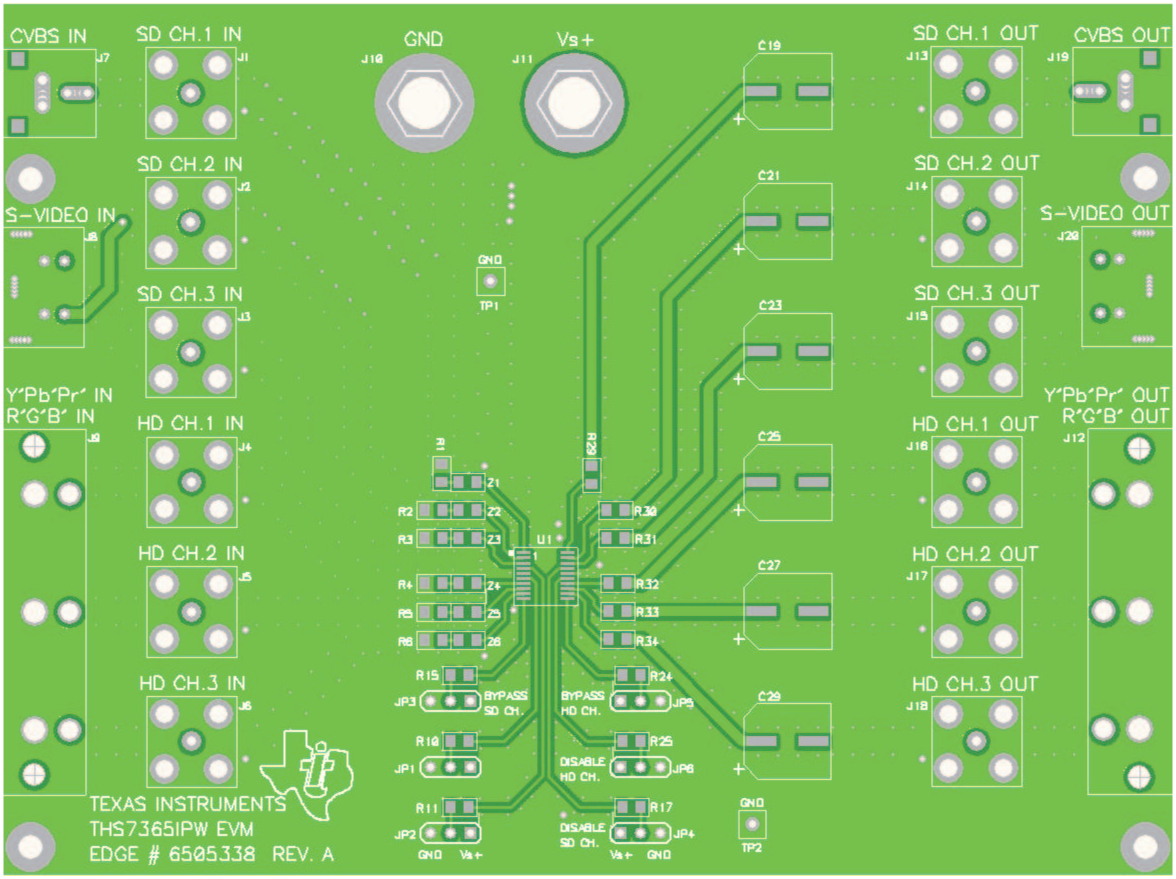


Figure 123. THS7365 EVM PCB Top Layer

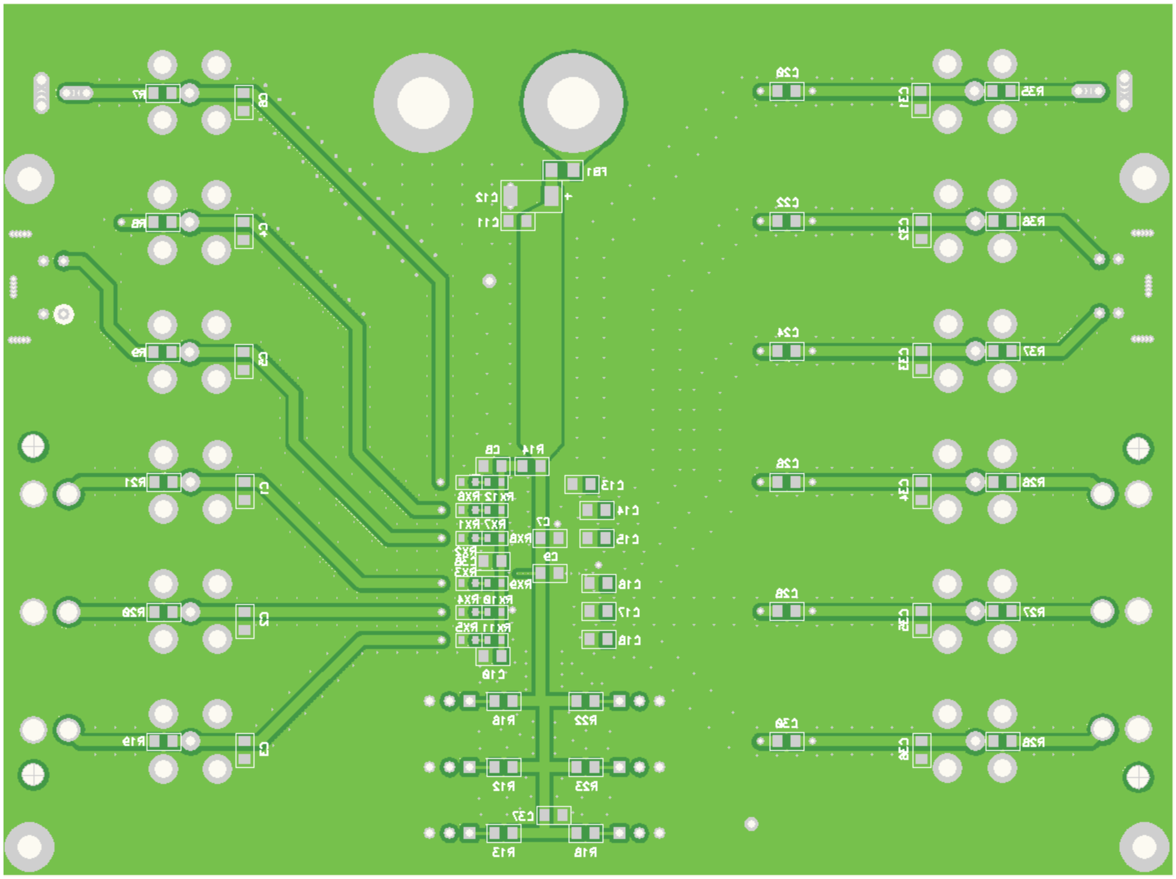


Figure 124. THS7365 EVM PCB Bottom Layer

THS7365EVM Bill of Materials

Table 1. THS7365 EVM

ITEM	REF DES	QTY	DESCRIPTION	SMD SIZE	MANUFACTURER PART NUMBER	DISTRIBUTOR PART NUMBER
1	FB1	1	Bead, Ferrite, 2.5 A, 330 Ω	0805	(TDK) MPZ2012S331A	(Digi-Key) 445-1569-1-ND
2	C12	1	Capacitor, 100 µF, Tantalum, 10 V, 10%, Low-ESR	C	(AVX) TPSC107K010R0100	(Digi-Key) 478-1765-1-ND
3	C1-C6, C13-C18, C31-C36	18	Open	0805		
4	C37	1	Capacitor, 0.01 µF, Ceramic, 100 V, X7R	0805	(AVX) 08051C103KAT2A	(Digi-Key) 478-1358-1-ND
5	C7-C11, C20, C22, C24, C26, C28, C30, C38	12	Capacitor, 0.1 µF, Ceramic, 50 V, X7R	0805	(AVX) 08055C104KAT2A	(Digi-Key) 478-1395-1-ND
6	C19, C21, C23, C25, C27, C29	6	Capacitor, Aluminum, 470 µF, 10 V, 20%	F	(Cornell) AFK477M10F24B-F	(Newark) 66K0965
7	RX1-RX12	12	Open	0603		
8	R10-R13	4	Open	0805		
9	Z1-Z4	18	Resistor, 0 Ω	0805	(ROHM) MCR10EZHJ000	(Digi-Key) RHM0.0ACT-ND
10	R1-R6, R29-R34	12	Resistor, 75 Ω, 1/8 W, 1%	0805	(ROHM) MCR10EZHF75.0	(Digi-Key) RHM75.0CCT-ND
11	R14	1	Resistor, 100 Ω, 1/8 W, 1%	0805	(ROHM) MCR10EZHF1000	(Digi-Key) RHM100CCT-ND
12	R15, R17, R24, R25	4	Resistor, 1 kΩ, 1/8 W, 1%	0805	(ROHM) MCR10EZHF1001	(Digi-Key) RHM1.00KCCT-ND
13	R16, R18, R22, R23	4	Resistor, 100 kΩ, 1/8 W, 1%	0805	(ROHM) MCR10EZHF1003	(Digi-Key) RHM100KCCT-ND
14	J10, J11	2	Jack, Banana Receptance, 0.25" dia. hole		(SPC) 813	(Newark) 39N867
15	J1-J6, J13-J18	12	Connector, BNC, Jack, 75 Ω		(Amphenol) 31-5329-72RFX	(Newark) 93F7554
16	J8, J20	2	Connector, Mini Circular DIN		(CUI) MD-40SM	(Digi-Key) CP-2240-ND
17	J7, J19	2	Connector, RCA Jack, Yellow		(CUI) RCJ-044	(Digi-Key) CP-1421-ND
18	J9, J12	2	Connector, RCA, Jack, R/A		(CUI) RCJ-32265	(Digi-Key) CP-1446-ND
19	TP1, TP2	2	Test Point, Black		(Keystone) 5001	(Digi-Key) 5001K-ND
20	JP1, JP2	2	Open	3 possible		
21	JP3-JP6	4	Header, 0.1" CTRS, 0.025" sq. pins	3 possible	(Sullins) PBC36SAAN	(Digi-Key) S1011E-36-ND
22	JP3-JP6	4	Shunts		(Sullins) SSC02SYAN	(Digi-Key) S9002-ND
23	U1	1	IC, THS7365	PW	(TI) THS7365IPW	
24		4	Standoff, 4-40 HEX, 0.625" length		(Keystone) 1808	(Digi-Key) 1808K-ND
25		4	Screw, Phillips, 4-40, 0.250"		(BF) PMS 440 0031 PH	(Digi-Key) H343-ND
26		1	Printed Circuit Board		(TI) Edge# 6505338 Rev. A	

EVALUATION BOARD/KIT IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User’s Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.6 V to 5.5 V single-supply and the output voltage range of 0 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
THS7365IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7365	Samples
THS7365IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7365	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

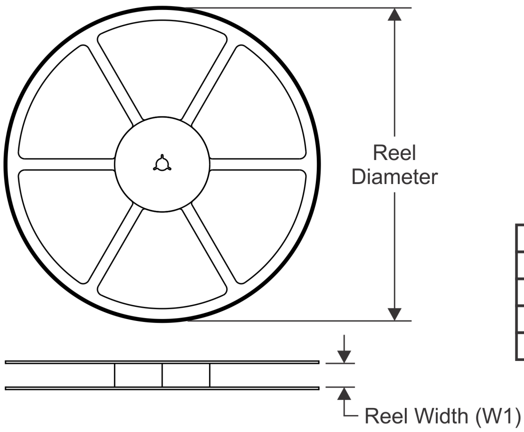
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

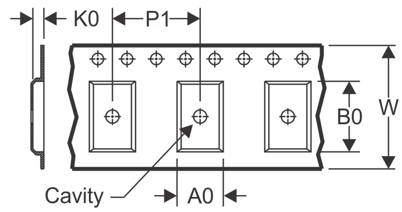
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

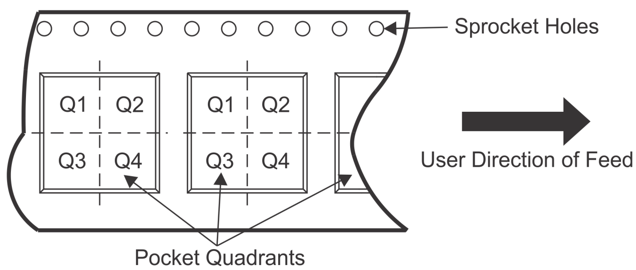


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

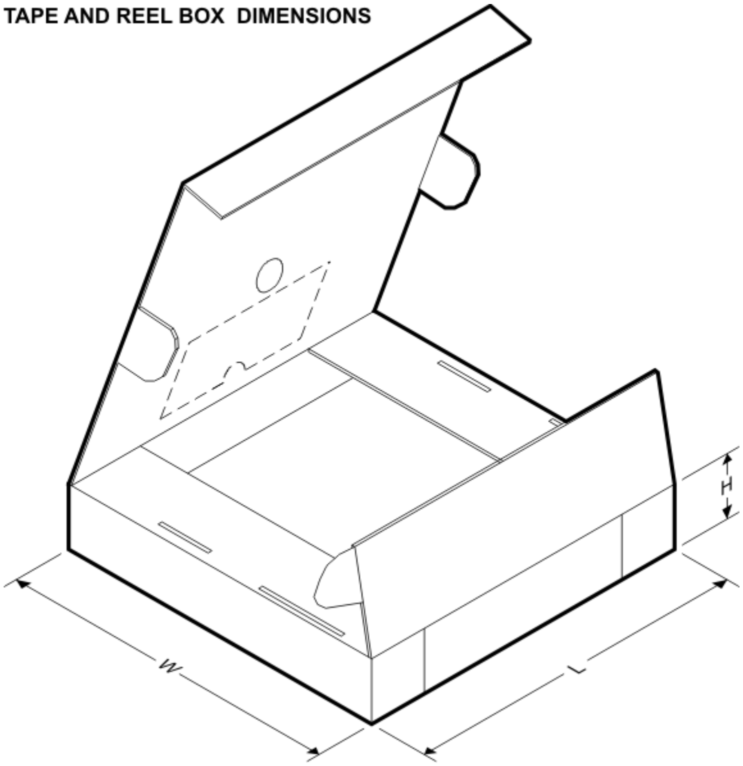
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7365IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

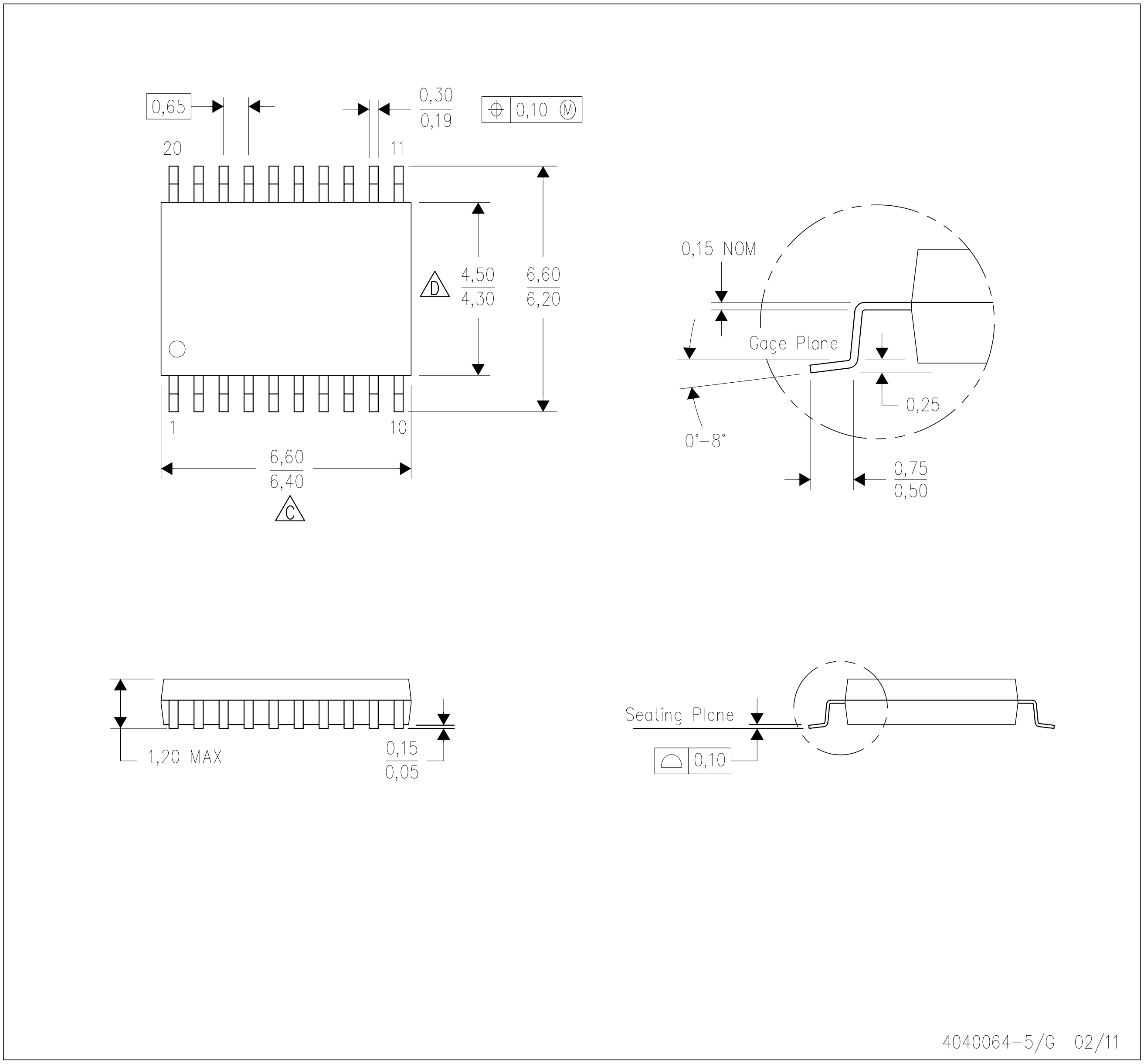
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

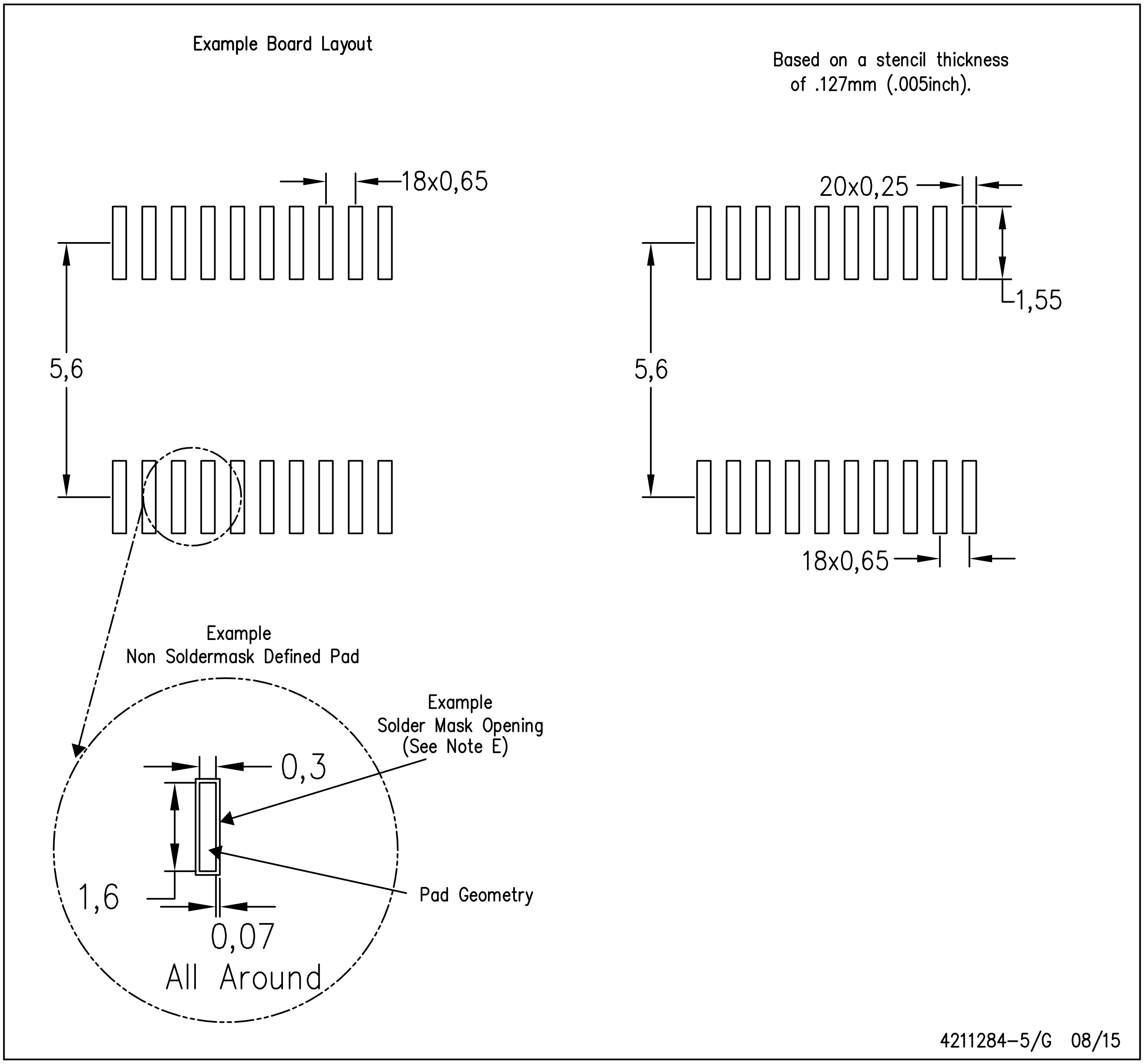
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7365IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.