2.7 V TO 5.5 V 12-BIT PARALLEL DIGITAL-TO-ANALOG CONVERTER WITH POWER DOWN

FEATURES

- **Single Supply 2.7-V to 5.5-V Operation**
- **± 0.4 LSB Differential Nonlinearity (DNL), ±1.5 LSB Integral Nonlinearity (INL)**
- **12-Bit Parallel Interface**
- **Compatible With TMS320 DSP**
- **Internal Power On Reset**
- **Settling Time 1 µs Typ**
- **Low Power Consumption:**
  - **8 mW for 5-V Supply**
  - **4.3 mW for 3-V Supply**
- **Reference Input Buffers**
- **Voltage Output**
- **Monotonic Over Temperature**
- **Asynchronous Update**

APPLICATIONS

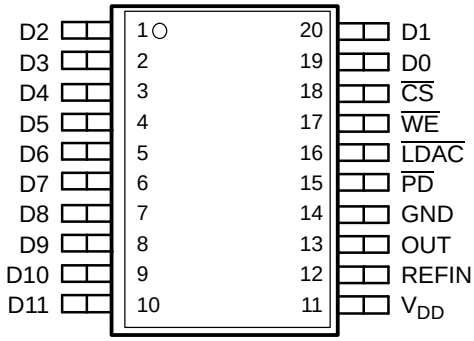
- **Battery Powered Test Instruments**
- **Digital Offset and Gain Adjustment**
- **Battery Operated/Remote Industrial Controls**
- **Machine and Motion Control Devices**
- **Cordless and Wireless Telephones**
- **Speech Synthesis**
- **Communication Modulators**
- **Arbitrary Waveform Generation**

DESCRIPTION

The TLV5619 is a 12-bit voltage output DAC with a microprocessor and TMS320 compatible parallel interface. The 12 data bits are double buffered so that the output can be updated asynchronously using the $\overline{\text{LDAC}}$ pin. During normal operation, the device dissipates 8 mW at a 5-V supply and 4.3 mW at a 3-V supply. The power consumption can be lowered to 50 nW by setting the DAC to power-down mode.

The output voltage is buffered by a ×2 gain rail-to-rail amplifier, which features a Class A output stage to improve stability and reduce settling time.

DW OR PW PACKAGE
(TOP VIEW)

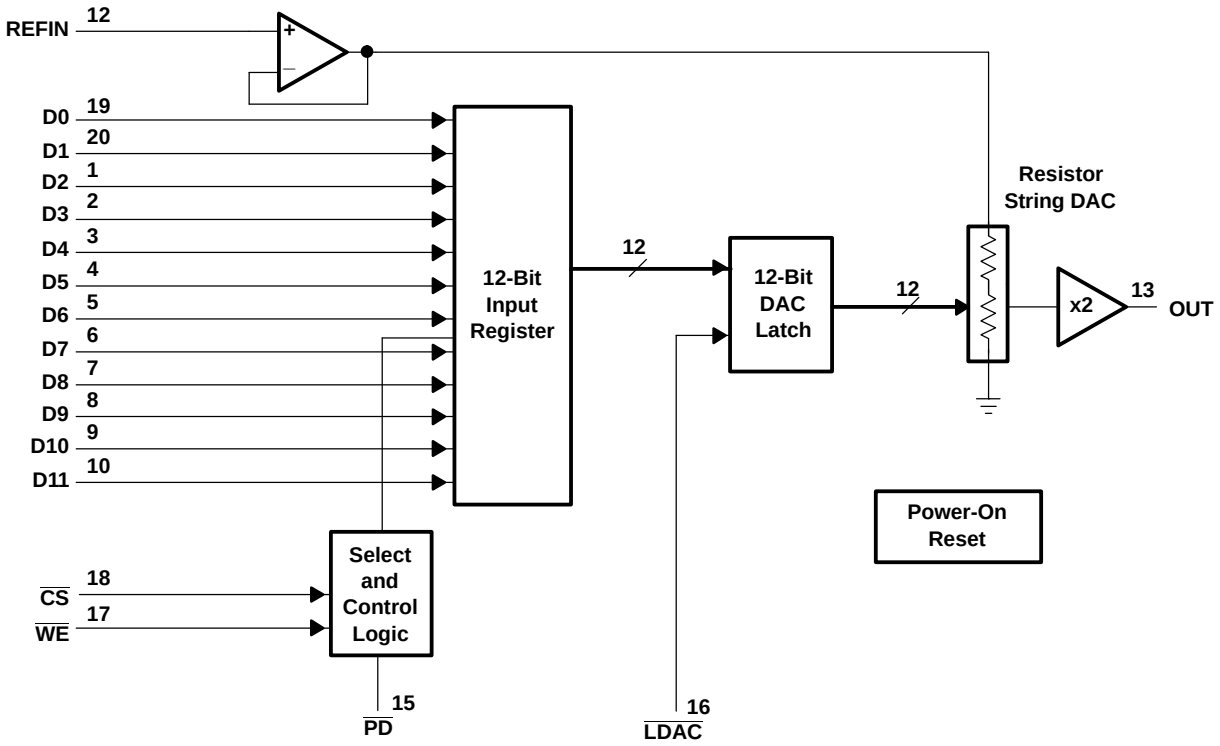


AVAILABLE OPTIONS

PACKAGE		
T_A	SMALL OUTLINE (DW)	TSSOP (PW)
0°C to 70°C	TLV5619CDW	TLV5619CPW
40°C to 85°C	TLV5619IDW	TLV5619IPW
40°C to 125°C	TLV5619QDW	—

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{CS}$	18	I	Chip select
D0 (LSB)-D11 (MSB)	19, 20, 1-10	I	Parallel data input
GND	14		Ground
$\overline{LDAC}$	16	I	Load DAC
OUT	13	O	Analog output
$\overline{PD}$	15	I	When low, disables all buffer amplifier voltages to reduce supply current
REFIN	12	I	Voltage reference input
V_{DD}	11		Positive power supply
$\overline{WE}$	17	I	Write enable

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Supply voltage (V_{DD} to GND)		7 V
Analog input voltage range		- 0.3 V to V_{DD} + 0.3 V
Reference input voltage		V_{DD} + 0.3 V
Digital input voltage range to GND		- 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A	TLV5619C	0°C to 70°C
	TLV5619I	-40°C to 85°C
	TLV5619Q	-40°C to 125°C
Storage temperature range, T_{stg}		-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under„ absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under„ recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (5-V Supply)			4.5	5	5.5	V
Supply voltage, V_{DD} (3-V Supply)			2.7	3	3.3	V
High-level digital input voltage, V_{IH}	DV_{DD} = 2.7 V		2			V
	DV_{DD} = 5.5 V		2.4			
Low-level digital input voltage, V_{IL}	DV_{DD} = 2.7 V				0.6	V
	DV_{DD} = 5.5 V	TLV5619C and TLV5619I			1	
		TLV5619Q			0.8	
Reference voltage, V_{ref} to REFIN terminal (5-V Supply)			0	2.048	V_{DD}-1.5	V
Reference voltage, V_{ref} to REFIN terminal (3-V Supply)			0	1.024	V_{DD}-1.5	V
Load resistance, R_L			2	10		kΩ
Load capacitance, C_L					100	pF
Operating free-air temperature, T_A	TLV5619C		0		70	°C
	TLV5619I		40		85	
	TLV5619Q		40		125	

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, sdupply voltages, and reference voltages (unless otherwise noted)

STATIC DAC SPECIFICATIONS							
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Resolution		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V		12			bits
	Integral nonlinearity (INL)		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V,	See (1)		±1.5	±4	LSB
	Differential nonlinearity (DNL)		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V,	See (2)		±0.4	±1	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V,	See (3)		±3	±20	mV
	Zero-scale-error temperature coefficient		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V,	See (4)		3		ppm/°C
E_G	Gain error		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V,	See (5)		±0.25	±0.5	% of FS voltage
	Gain error temperature coefficient		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V,	See (6)		1		ppm/°C
PSRR	Power-supply rejection ratio	Zero scale	See (7) and (8)			65		dB
		Gain				65		

(1) The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
(2) The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
(3) Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
(4) Zero-scale-error temperature coefficient is given by: E_{ZS} TC = $[E_{ZS} (T_{max}) - E_{ZS} (T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
(5) Gain error is the deviation from the ideal output ($2 \times V_{ref}$ - 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-error.
(6) Gain temperature coefficient is given by: E_G TC = $[E_G(T_{max}) - E_G (T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
(7) Zero-scale-error rejection ratio (EZS-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
(8) Gain-error rejection ratio (EG-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.

OUTPUT SPECIFICATIONS							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Voltage output range	R_L = 10 kΩ		0		V_{DD}-0.4	V
	Output load regulation accuracy	$V_{O(OUT)}$= 4.096 V, 2.048 V	R_L = 2 kΩ		0.1	0.29	% of FS voltage
$I_{OSC(source)}$	Output short circuit source current	$V_{O(OUT)}$ = 0 V, Full scale code	5-V Supply		100		mA
			3-V Supply		25		
$I_{O(source)}$	Output source current	R_L = 100Ω	5-V Supply		10		mA
			3-V Supply		10		

REFERENCE INPUT (REFIN)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ref}	Reference input voltage	See (1)	0		V_{DD}-1.5	V
R_i	Reference input resistance			10		MΩ
C_i	Reference input capacitance			5		pF
	Reference feed through	REFIN = 1 V_{pp} at 1 kHz + 1.024 V dc (see (2))		60		dB
	Reference input bandwidth	REFIN = 0.2 V_{pp} + 1.024 V dc at -3 dB		1.4		MHz
DIGITAL INPUTS (D0-D11, $\overline{CS}$, $\overline{WE}$, $\overline{LDAC}$, $\overline{PD}$)						
I_{IH}	High-level digital input current	$V_I = V_{DD}$			1	µA
I_{IL}	Low-level digital input current	V_I = 0 V			1	µA
C_i	Input capacitance			8		pF

(1) Reference input voltages greater than $V_{DD}/2$ will cause output saturation for large DAC codes.
(2) Reference feedthrough is measured at the DAC output with an input code = 0x000 and a $V_{ref(REFIN)}$ input = 1.024 V dc + 1 V_{pp} at 1 kHz.

POWER SUPPLY						
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Power supply current	No load, All inputs 0 V or V_{DD}	5-V Supply		1.6	3	mA
			3-V Supply		1.44	2.7	
	Power down supply current				0.01	10	µA

ANALOG OUTPUT DYNAMIC PERFORMANCE							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate	C_L = 100 pF, R_L = 10 kΩ; $V_{ref(REFIN)}$ = 2.048 V, $V_{ref(REFIN)}$ =1.024 V, V_O from 10% to 90% / V_O from 90% to 10%	5-V Supply	8	12		V/µs
			3-V Supply	6	9		V/µs
t_s	Output settling time (full scale)	To ±0.5 LSB, R_L = 10 kΩ, C_L = 100 pF, See (1)			1	3	µs
	Glitch energy	DIN = all 0s to all 1s			5		nV-s
S/N	Signal to noise	f_s = 480 kSPS, BW = 20 kHz, C_L = 100 pF, f_{OUT} = 1 kHz, R_L = 10 kΩ , T_A = 25°C, See (2)	5-V Supply	65	78		dB
S/(N+D)	Signal to noise + distortion	f_s = 480 kSPS, BW = 20 kHz, C_L = 100 pF, f_{OUT} = 1 kHz, R_L = 10 kΩ, T_A = 25°C, See (2)	5-V Supply	58	67		
			3-V Supply	58	69		
	Total harmonic distortion	f_s = 480 kSPS, BW = 20 kHz, C_L = 100 pF, f_{OUT} = 1 kHz, R_L = 10 kΩ, T_A = 25°C, See (2)			68	60	
	Spurious free dynamic range	f_s = 480 kSPS, BW = 20 kHz, C_L = 100 pF, f_{OUT} = 1 kHz, R_L = 10 kΩ, T_A = 25°C, See (2)		60	72		

(1) Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 32 to 4063 or 4063 to 32. Limits are ensured by design and characterization, but are not production tested.
(2) 1 kHz sinewave generated by DAC, reference voltage = 1.024 V at 3 V and 2.048 V at 5 V.

TIMING REQUIREMENTS

DIGITAL INPUTS					
		MIN	NOM	MAX	UNIT
$t_{su(CS-WE)}$	Setup time, $\overline{CS}$ low before positive $\overline{WE}$ edge	13			ns
$t_{su(D)}$	Setup time, data ready before positive $\overline{WE}$ edge	9			ns
$t_{h(D)}$	Hold time, data held after positive $\overline{WE}$ edge	0			ns
$t_{su(WE-LD)}$	Setup time, positive $\overline{WE}$ edge before $\overline{LDAC}$ low	0			ns
$t_{wh(WE)}$	Pulse width, $\overline{WE}$ high	25			ns
$t_{w(LD)}$	Pulse width, $\overline{LDAC}$ low	25			ns

PARAMETER MEASUREMENT INFORMATION

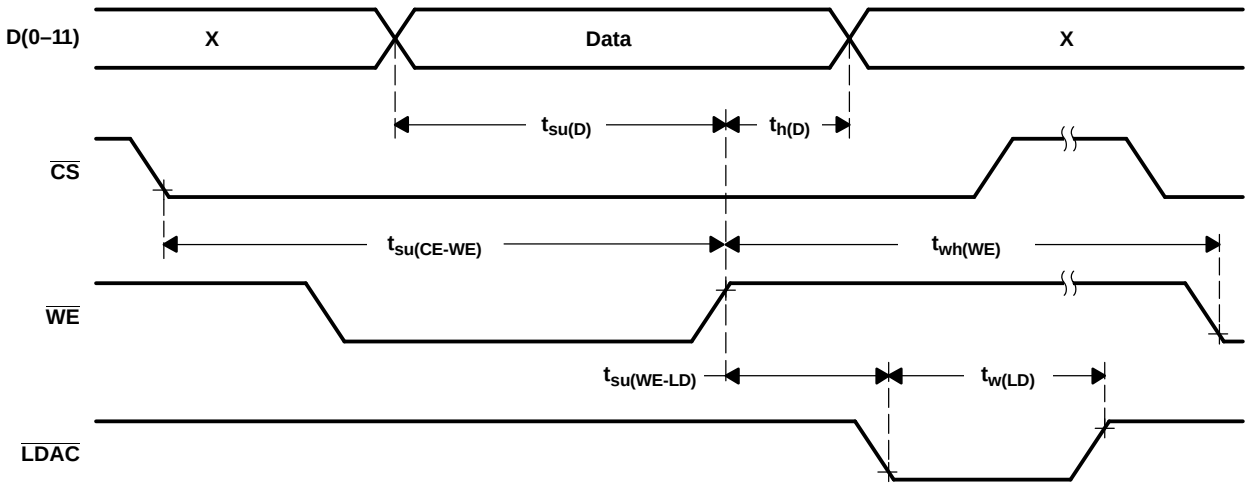


Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT VOLTAGE vs LOAD

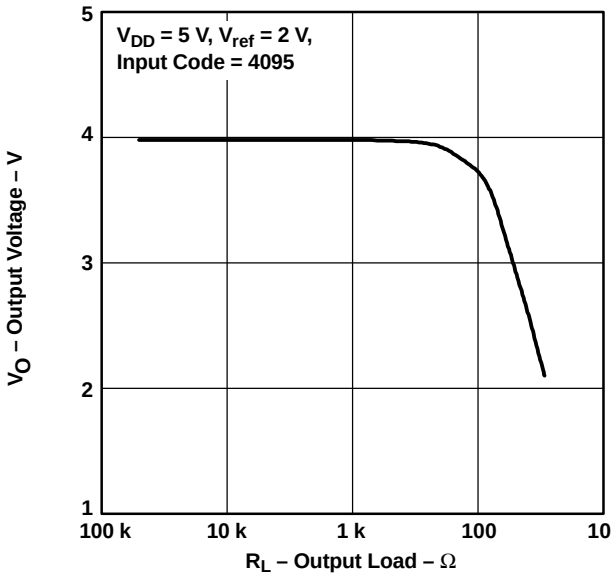


Figure 2.

MAXIMUM OUTPUT VOLTAGE vs LOAD

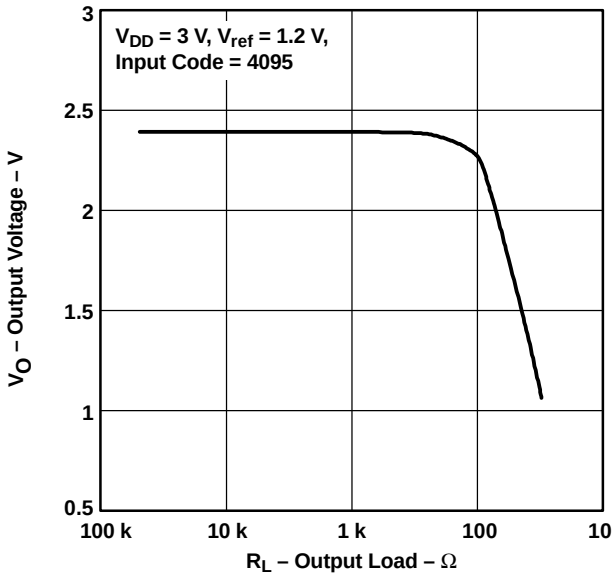


Figure 3.

TOTAL HARMONIC DISTORTION vs LOAD

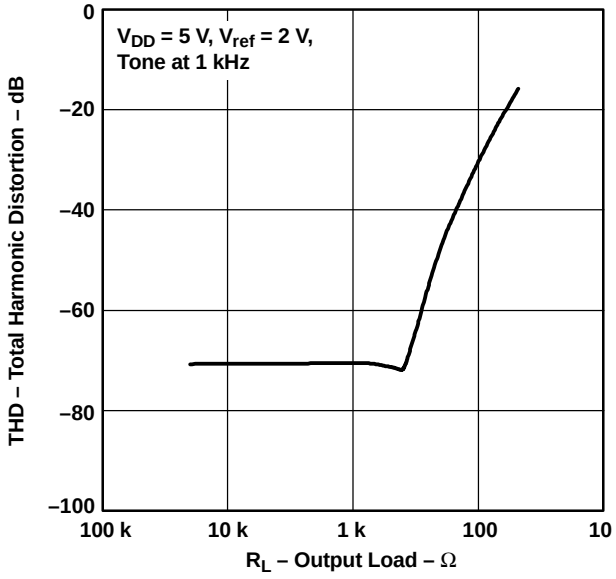


Figure 4.

TOTAL HARMONIC DISTORTION vs FREQUENCY

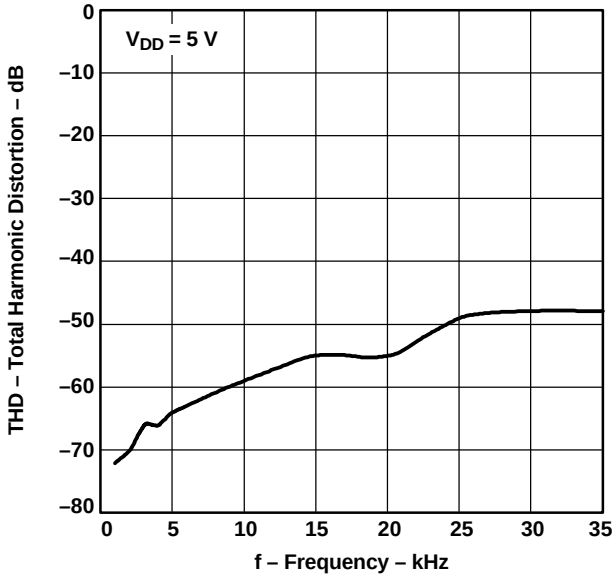


Figure 5.

TYPICAL CHARACTERISTICS (continued)

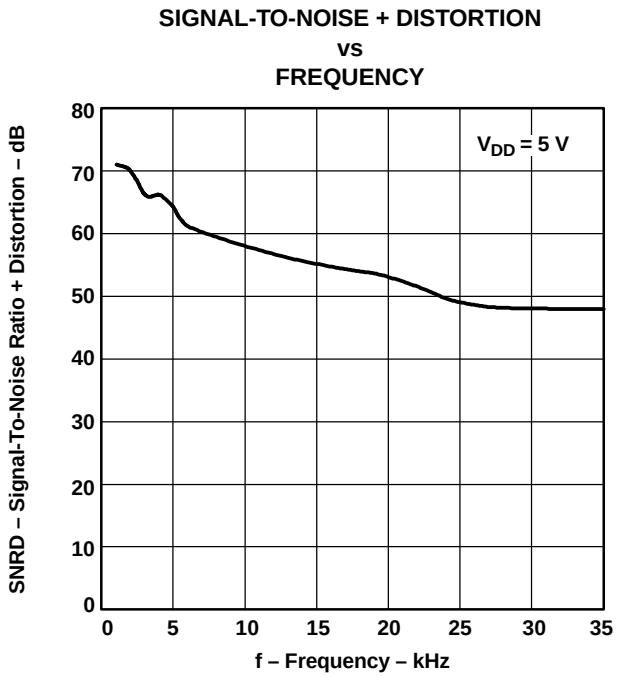


Figure 6.

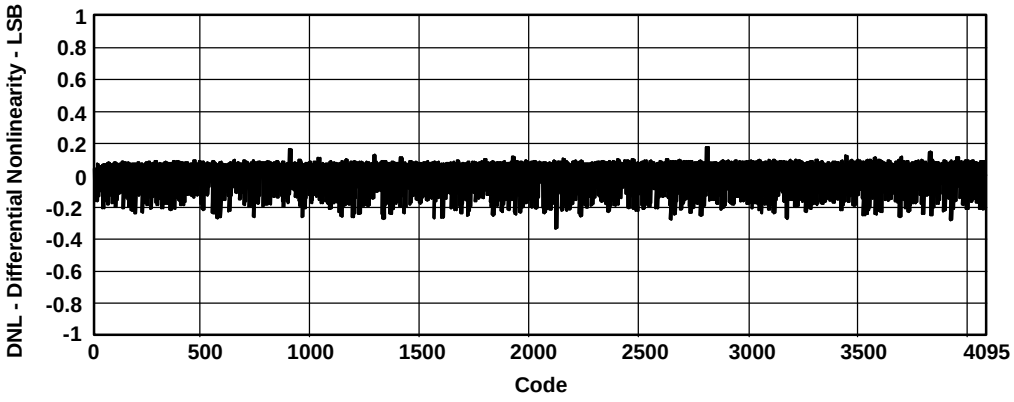


Figure 7. Differential Nonlinearity

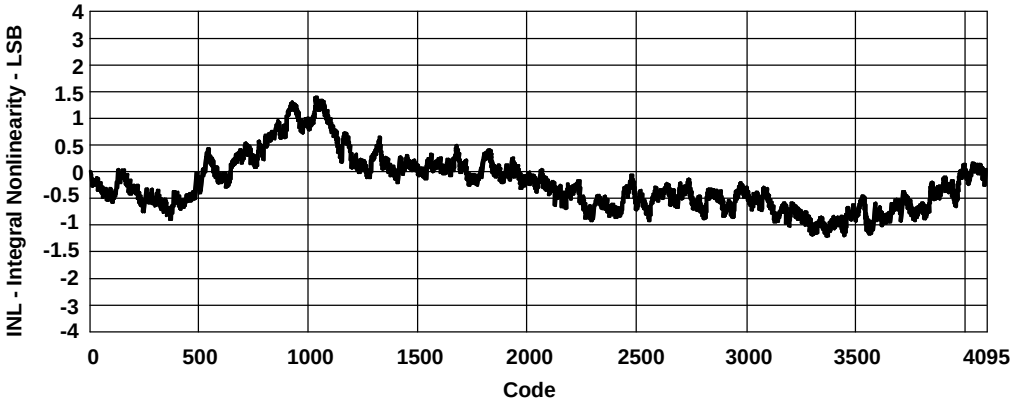


Figure 8. Integral Nonlinearity

TYPICAL CHARACTERISTICS (continued)

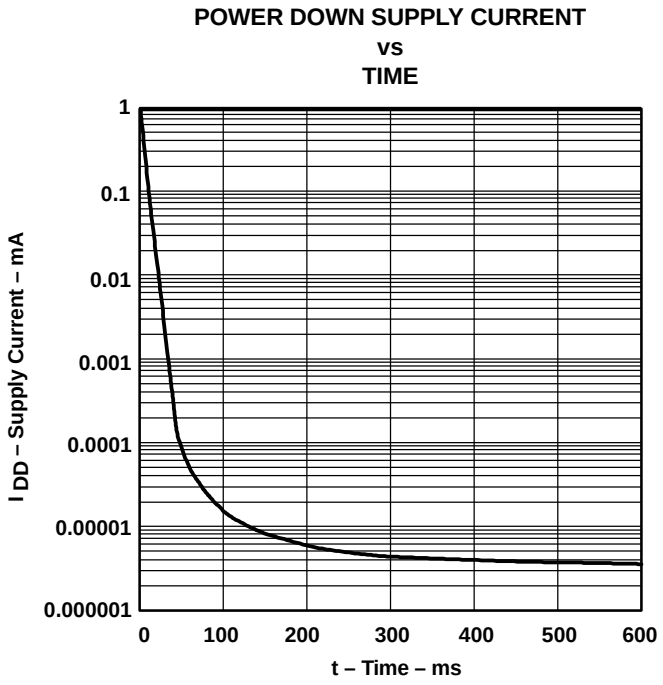


Figure 9.

APPLICATION INFORMATION

DEFINITIONS OF SPECIFICATIONS AND TERMINOLOGY

Integral Nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

Differential Nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

Zero-Scale Error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

Gain Error (E_G)

Gain error is the error in slope of the DAC transfer function.

Signal-to-Noise Ratio + Distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Spurious Free Dynamic Range (SFDR)

SFDR is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental signal and is expressed in decibels.

APPLICATION INFORMATION (continued)

LINEARITY, OFFSET, AND GAIN ERROR SUING SINGLE END SUPPLIES

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 10.

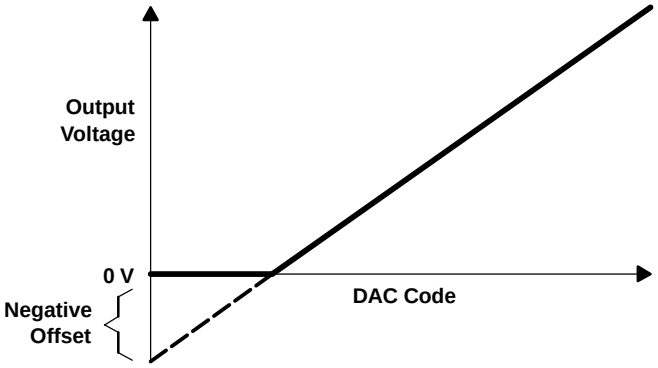


Figure 10. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full scale code and the lowest code that produces a positive output voltage.

GENERAL FUNCTION

The TLV5619 is a 12-bit, single supply DAC, based on a resistor string architecture. It consists of a parallel interface, a power down control logic, a resistor string, and a rail-to-rail output buffer. The output voltage (full scale determined by reference) is given by:

$$2\ \mathrm{REF}\ \frac{\mathrm{CODE}}{0\mathrm{x}1000}\ [\mathrm{V}]$$

Where REF is the reference voltage and CODE is the digital input value, range 0x000 to 0xFFF. A power on reset initially puts the internal latches to a defined state (all bits zero).

APPLICATION INFORMATION (continued)

PARALLEL INTERFACE

The device latches data on the positive edge of $\overline{WE}$. It must be enabled with $\overline{CS}$ low. $\overline{LDAC}$ low updates the DAC with the value in the holding latch. $\overline{LDAC}$ is an asynchronous input and can be held low, if a separate update is not necessary. However, to control the DAC using the load feature, $\overline{LDAC}$ can be driven low after the positive $\overline{WE}$ edge.

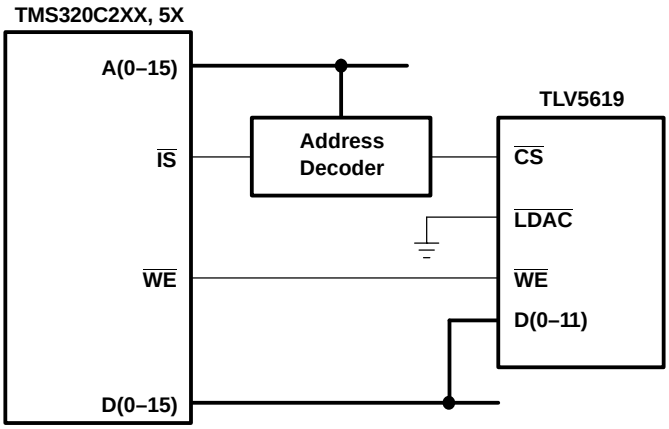


Figure 11. Proposed Interface Between TLV5619 and TMS320C2XX, 5X DSPs

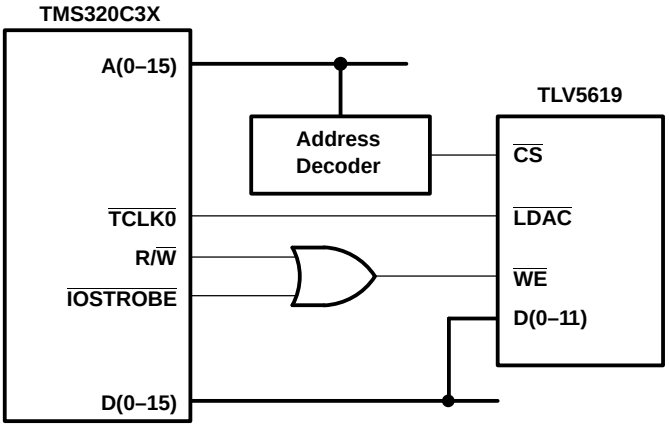


Figure 12. Proposed Interface Between TLV5619 and TMS320C3X DSPs

APPLICATION INFORMATION (continued)

TLV5619 INTERFACED TO TMS320C203 DSP

Hardware Interface

Figure 13 shows an example of the connection between the TLV5619 and the TMS320C203 DSP. The only other device that is needed in addition to the DSP and the DAC is the 74AC138 address decoding circuit . Using this configuration, the DAC address is 0x0084 within the I/O memory space of the TMS320C203.

$\overline{\text{LDAC}}$ is held low so that the output voltage is updated with the rising $\overline{\text{WE}}$ edge. The power down mode is deactivated permanently by pulling $\overline{\text{PD}}$ to V_{DD}.

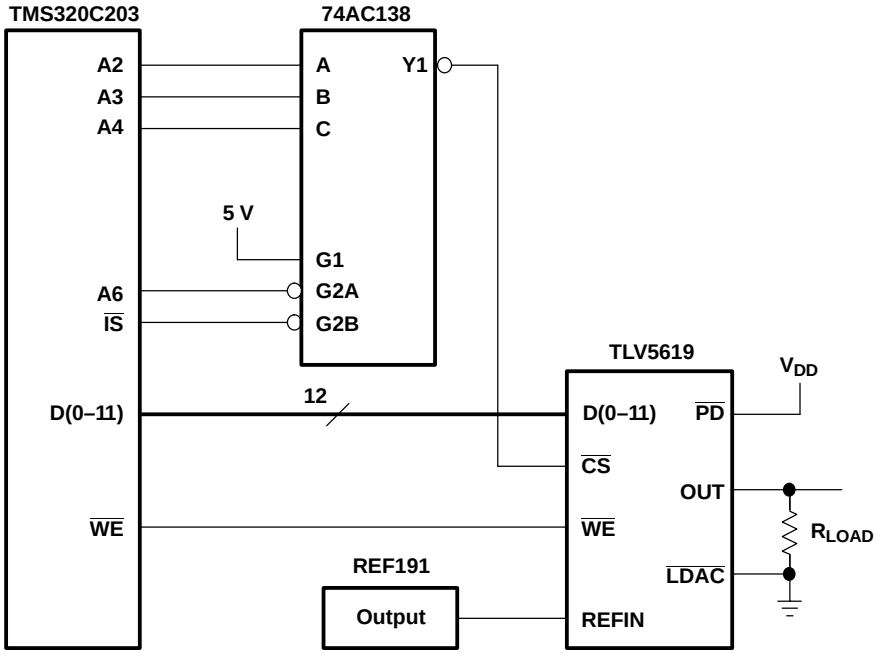


Figure 13. TLV5619 to TMS320C203 DSP Interface Connection

Software

No setup procedure is needed to access the TLV5619. The output voltage can be set using one command:

```
out data_addr,  DAC_addr
```

Where data_addr points to the address location (in this example 0x0060) holding the new output voltage data and DAC_addr is the I/O space address of the TLV5619 (in this example 0x0084).

The following code shows, how to use the timer of the TMS320C203 as a time base to generate a voltage ramp with the TLV5619. A timer interrupt is generated every 205 µs. The corresponding interrupt service routine increments the output code (stored at 0x0060) for the DAC and writes the new code to the TLV5619. Only the 12 LSBs of the data in 0x0060 are used by the DAC, so that the resulting period of the saw waveform is:

- t = 4096 × 205 E-6 s = 0.84 s

APPLICATION INFORMATION (continued)

SOFTWARE LISTING

```
; File: ramp.asm
; Description: This program generates a ramp.


;------------- I/O and memory mapped regs -----------
               .include "regs.asm"
TLV5619        .equ   0084h
;------------- vectors -------------------------------
               .ps    0h
               b      start
               b      INT1
               b      INT23
               b      TIM_ISR


*********************************************************************
* Main Program
*********************************************************************


               .ps    1000h
               .entry
start:
               ldp    #0    ; set data page to 0
; disable interrupts
               setc   INTM  ; disable maskable interrupts
               splk   #0ffffh,  IFR
               splk   #0004h,   IMR


; set up the timer
               splk   #0000h,   60h
               splk   #0042h,   61h
               out    61h. PRD
               out    60h, TIM
               splk   #0c2fh,   62h
               out    62h, TCR


; enable interrupts
               clrc   INTM ; enable maskable interrupts


; loop forever!
next           idle        ; wait for interrupt
               b    next
; all else fails stop here
done           b    done ; hang there


*********************************************************************
* Interrupt Service Routines
*********************************************************************


INT1:      ret          ; do nothing and return


INT23:     ret          ; do nothing and return


TIM_ISR:
       ; useful code
          add       #1h ; increment accumulator
          sacl      60h
```

APPLICATION INFORMATION (continued)

```
            out       60h, TLV5619  ; write to DAC
            clrc      intm; re-enable interrupts
            ret           ; return from interrupt
            .end
```

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV5619CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5619C	Samples
TLV5619CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5619C	Samples
TLV5619CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5619C	Samples
TLV5619CPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5619	Samples
TLV5619CPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5619	Samples
TLV5619CPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5619	Samples
TLV5619IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5619I	Samples
TLV5619IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5619I	Samples
TLV5619IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5619I	Samples
TLV5619IDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5619I	Samples
TLV5619IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5619	Samples
TLV5619IPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5619	Samples
TLV5619IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5619	Samples
TLV5619IPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5619	Samples
TLV5619QDW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 125		
TLV5619QDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLV5619Q	Samples
TLV5619QDWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV5619 :

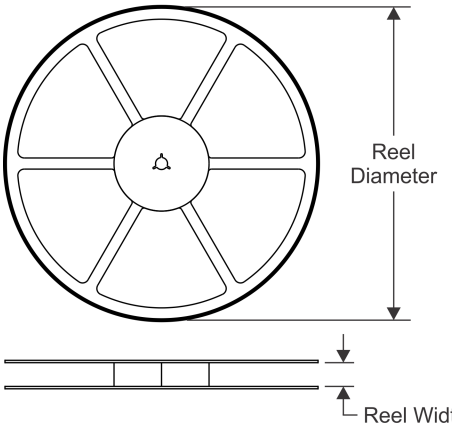
- Enhanced Product: TLV5619-EP

NOTE: Qualified Version Definitions:

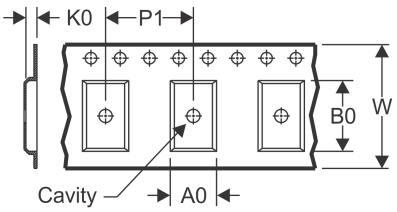
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

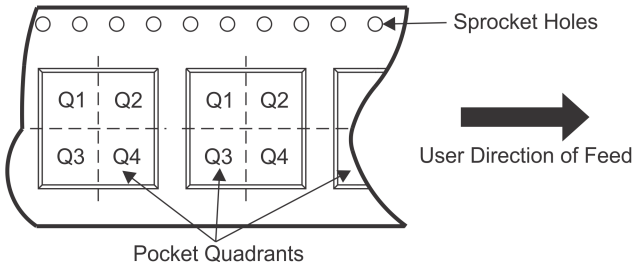


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

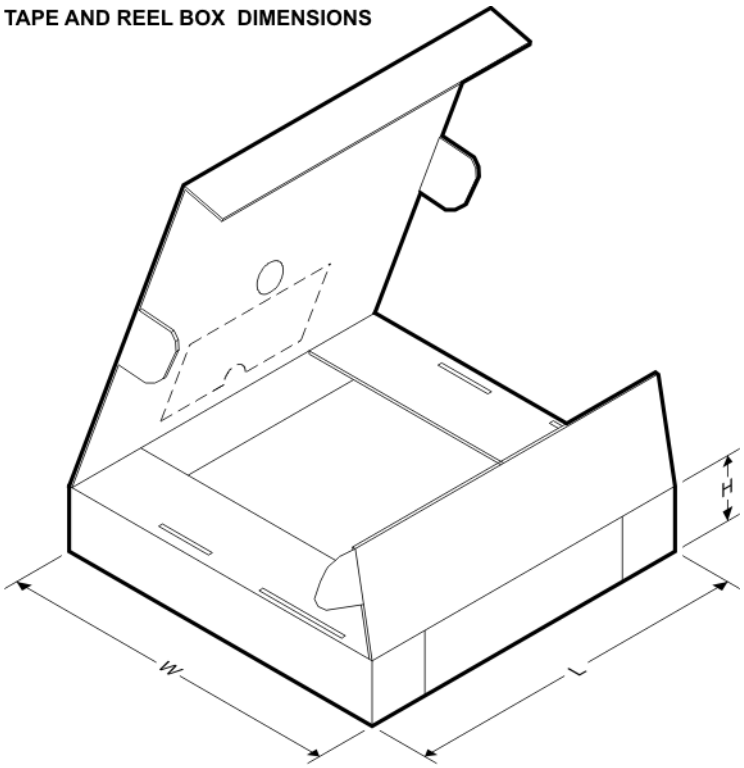
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

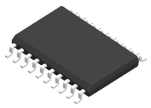
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5619CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV5619CPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLV5619IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV5619IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5619CDWR	SOIC	DW	20	2000	367.0	367.0	45.0
TLV5619CPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TLV5619IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
TLV5619IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

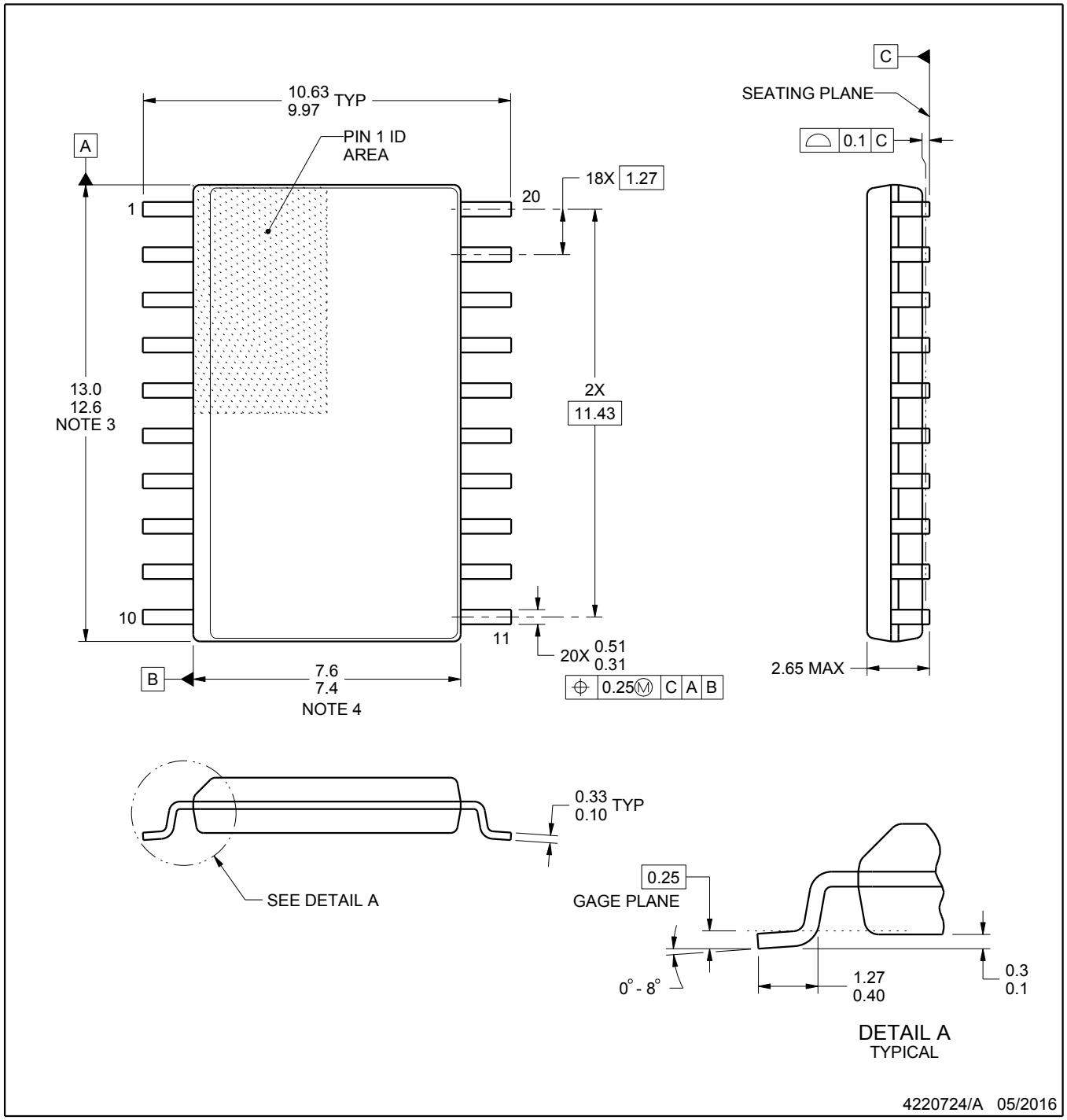


PACKAGE OUTLINE

DW0020A

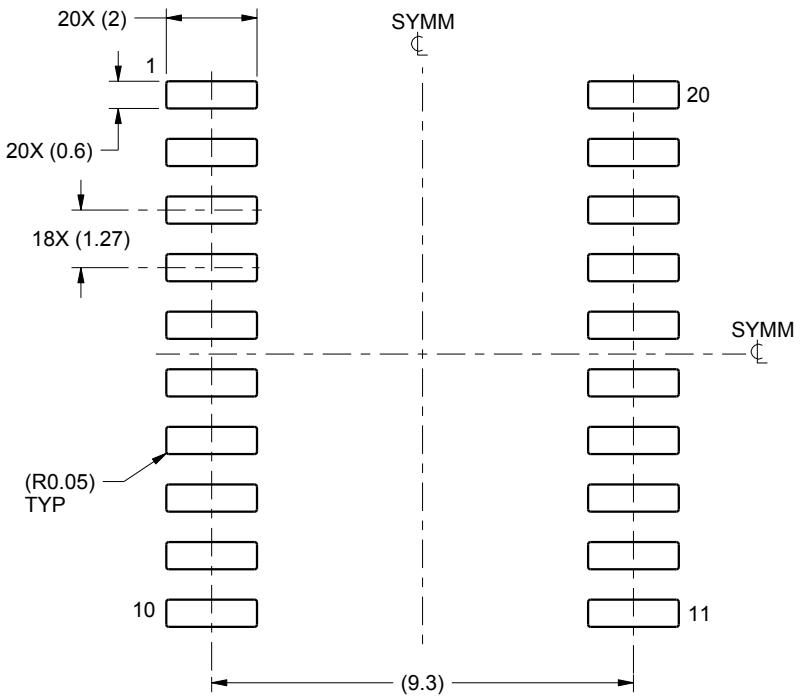
SOIC - 2.65 mm max height

SOIC

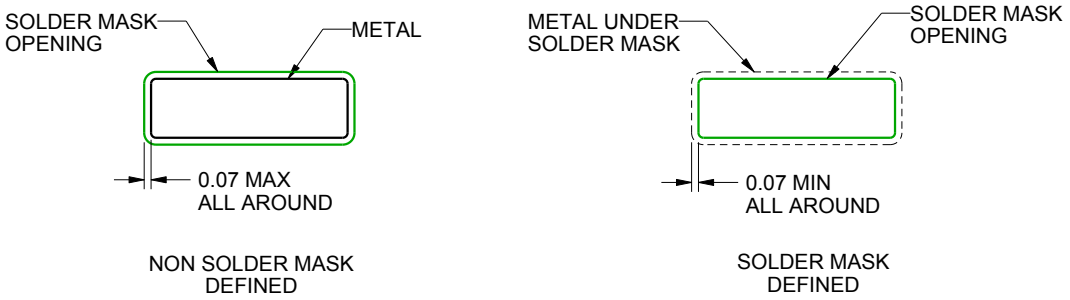


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

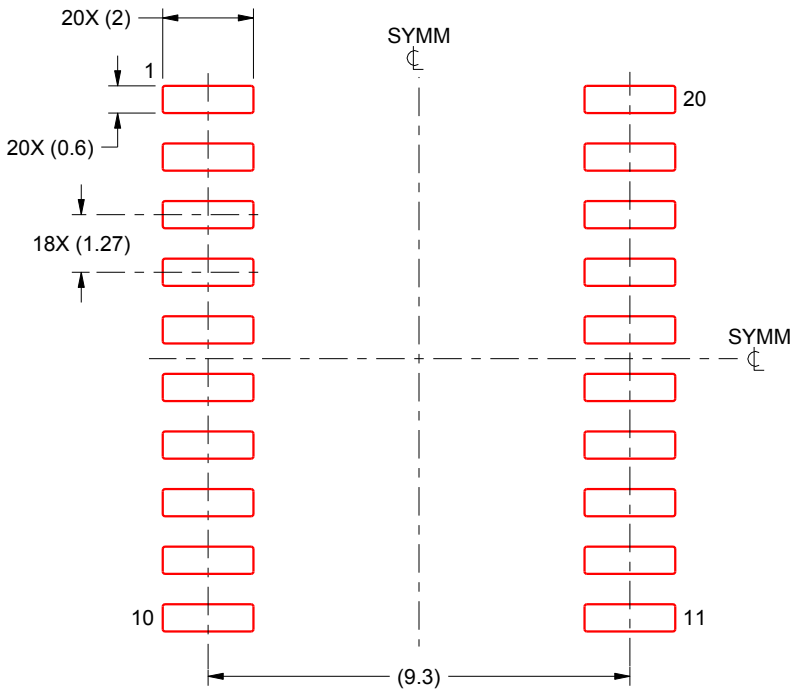


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



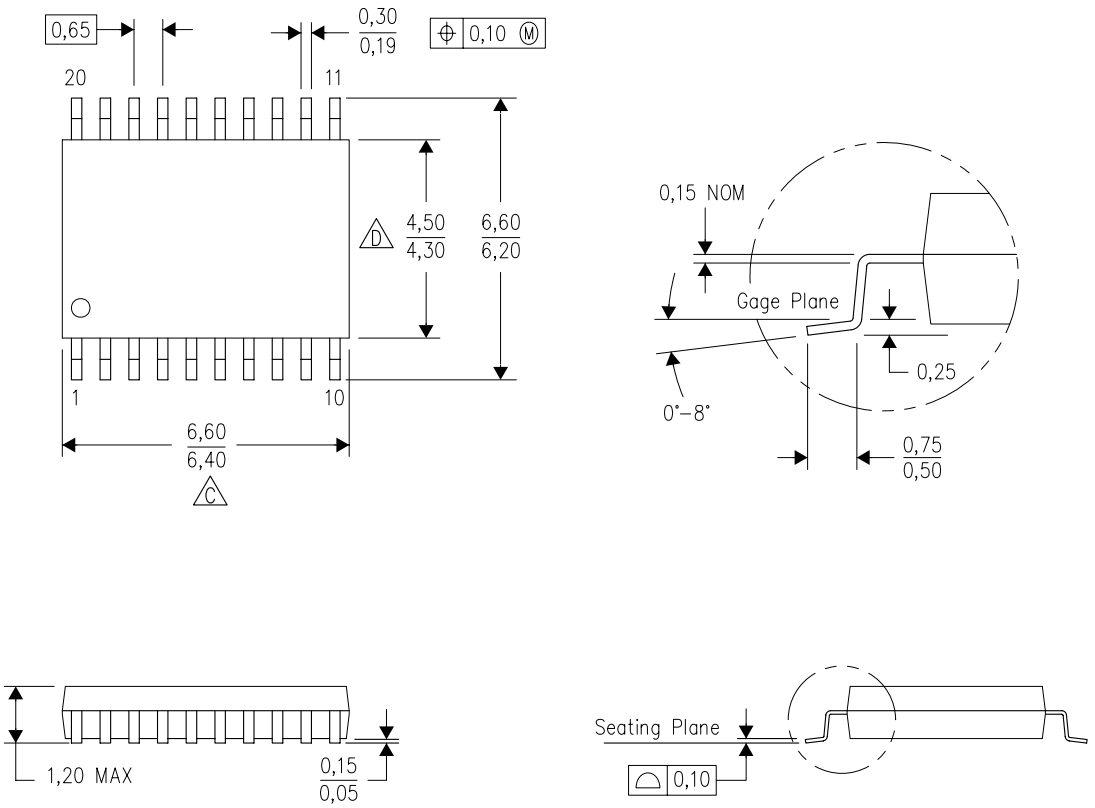
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

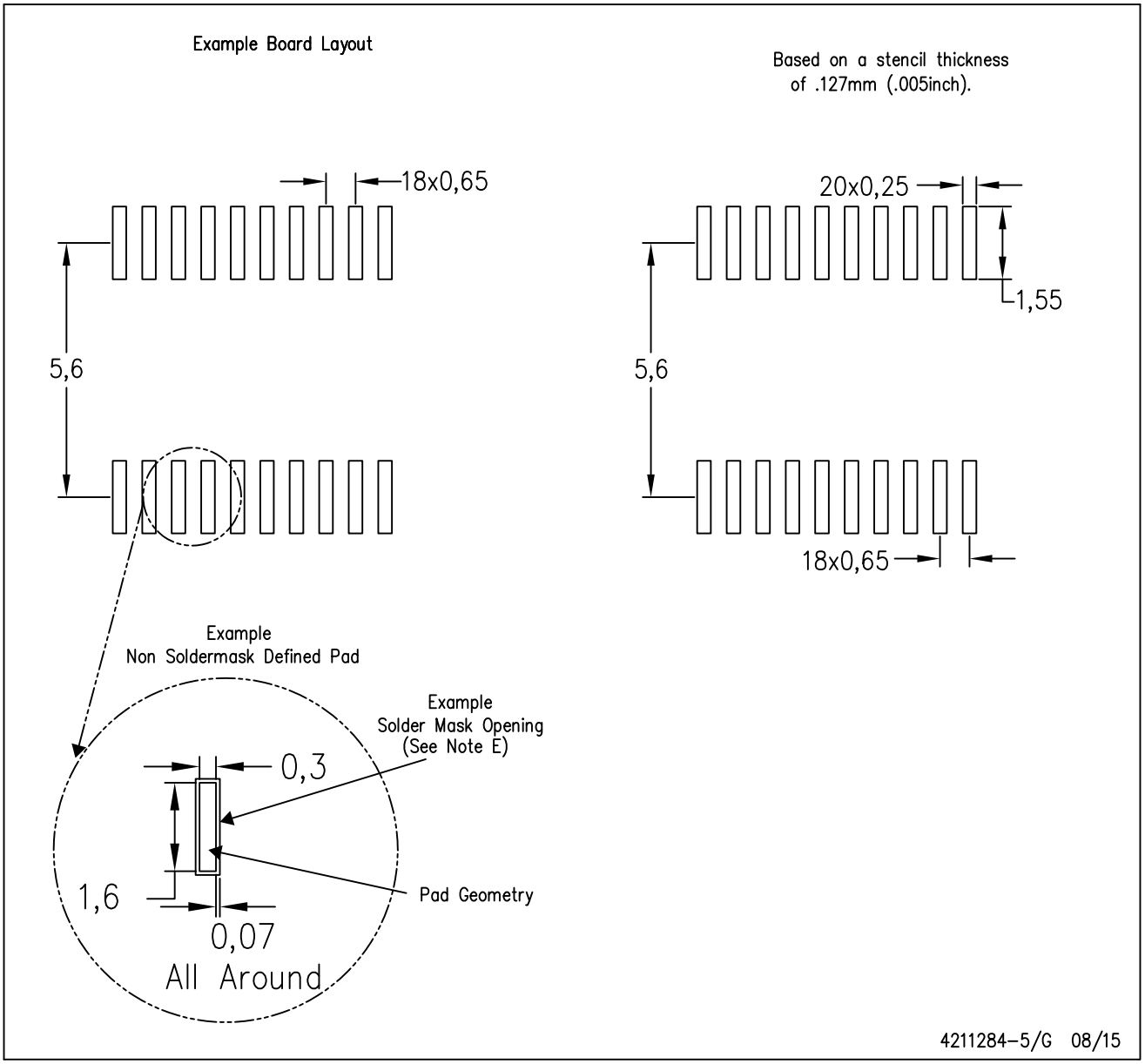
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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