#### TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE µPOWER OPERATIONAL AMPLIFIERS

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- Excellent Output Drive Capability  $V_O = \pm 2.5 \text{ V Min at R}_L = 100 \Omega$ ,  $V_{CC\pm} = \pm 5 \text{ V}$   $V_O = \pm 12.5 \text{ V Min at R}_L = 600 \Omega$ ,  $V_{CC+} = \pm 15 \text{ V}$ 
  - Low Supply Current . . . 280 μA Typ
- Decompensated for High Slew Rate and Gain-Bandwidth Product A<sub>VD</sub> = 0.5 Min

Slew Rate = 10 V/µs Typ
Gain-Bandwidth Product = 6.5 MHz Typ

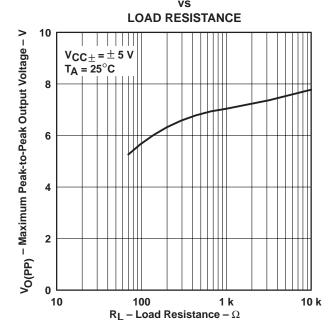
#### description

The TLE2161, TLE2161A, and TLE2161B are JFET-input, low-power, precision operational amplifiers manufactured using the Texas Instruments Excalibur process. Decompensated for stability with a minimum closed-loop gain of 5, these devices combine outstanding output drive capability with low power consumption, excellent dc precision, and high gain-bandwidth product.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a device that remains precise even with changes in temperature and over years of use.

- Wide Operating Supply Voltage Range
   V<sub>CC ±</sub> = ± 3.5 V to ± 18 V
- High Open-Loop Gain . . . 280 V/mV Typ
- Low Offset Voltage . . . 500 μV Max
- Low Offset Voltage Drift With Time 0.04 μV/Month Typ
- Low Input Bias Current . . . 5 pA Typ

# MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE



#### **AVAILABLE OPTIONS**

			PACK	AGE	
TA	V <sub>IO</sub> max AT 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV 1.5 mV 3 mV	— TLE2161ACD TLE2161CD	1 1	1 1	TLE2161BCP TLE2161ACP TLE2161CP
-40°C to 85°C	500 μV 1.5 mV 3 mV	— TLE2161AID TLE2161ID	1 1	1 1	TLE2161BIP TLE2161AIP TLE2161IP
−55°C to 125°C	500 μV 1.5 mV 3 mV	— TLE2161AMD TLE2161MD	— TLE2161AMFK TLE2161MFK	TLE2161BMJG TLE2161AMJG TLE2161MJG	TLE2161BMP TLE2161AMP TLE2161MP

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2161ACDR).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



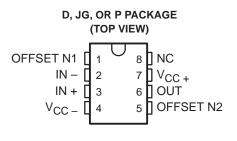
#### TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE µPOWER OPERATIONAL AMPLIFIERS

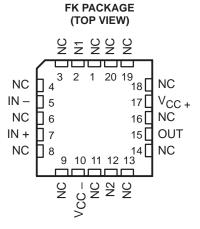
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#### description (continued)

A variety of available options includes small-outline packages and chip-carrier versions for high-density system applications.

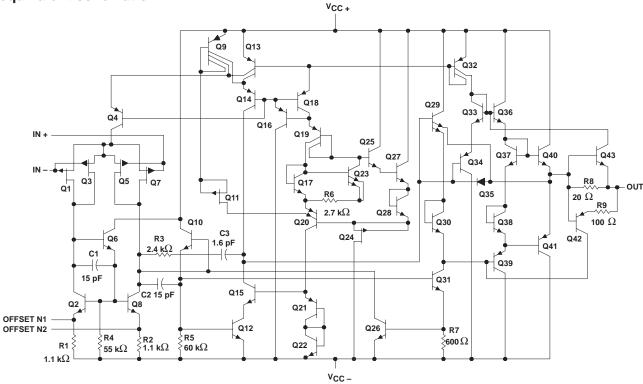
The C-suffix devices are characterized for operation from  $0^{\circ}$ C to  $70^{\circ}$ C. The I-suffix devices are characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C. The M-suffix devices are characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C.





NC - No internal connection

#### equivalent schematic



All component values are nominal.



### TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE μPOWER OPERATIONAL AMPLIFIERS

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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC +</sub> (see Note 1)	19 V
Supply voltage, V <sub>CC</sub>	
Differential input voltage, V <sub>ID</sub> (see Note 2)	
Input voltage range, V <sub>I</sub> (any input)	V <sub>CC ±</sub>
Input current, I <sub>I</sub> (each input)	±1 mA
Output current, I <sub>O</sub>	
Total current into V <sub>CC +</sub>	
Total current out of V <sub>CC</sub>	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T <sub>A</sub> : C suffix	0°C to 70°C
I suffix	– 40°C to 85°C
M suffix	– 55°C to 125°C
Storage temperature range, T <sub>Stg</sub>	– 65°C to 150°C
Case temperature for 60 seconds: FK package	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P	package 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60seconds: JG pac	kage 300°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC}$  +, and  $V_{CC}$  -.

- 2. Differential voltages are at IN+ with respect to IN-.
- 3. The output may be shorted to either supply. Temperature and /or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

#### **DISSIPATION RATING TABLE**

PACKAGE	$T_{\mbox{\scriptsize A}} \leq 25^{\circ}\mbox{\scriptsize C}$ POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

#### recommended operating conditions

		C SUF	FIX	I SUF	FIX	M SUF	FIX	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Supply voltage, V <sub>CC±</sub>		±3.5	±18	±3.5	±18	+3.5	±18	V
Common-mode input voltage, V <sub>IC</sub>	$V_{CC \pm} = \pm 5 V$	-1.6	4	-1.6	4	-1.6	4	V
Common-mode input voltage, vIC	$V_{CC \pm} = \pm 15 \text{ V}$	-11	13	-11	13	-11	13	V V
Operating free-air temperature, T <sub>A</sub>		0	70	-40	85	-55	125	°C



### TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE µPOWER OPERATIONAL AMPLIFIERS

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## electrical characteristics at specified free-air temperature, $V_{CC\,\pm}$ = $\pm\,5$ V (unless otherwise noted)

	PARAMETER		TEST CON	IDITIONS	T <sub>A</sub> †	TLE2161 TL	C, TLE2 <sup>-</sup> E2161BC		UNIT
						MIN	TYP	MAX	
		TI FOACAC			25°C		0.8	3.1	
		TLE2161C			Full range			4	
\ \	lanut effect valtage	TI FOACAAC	1		25°C		0.6	2.6	>/
VIO	Input offset voltage	TLE2161AC			Full range			3.5	mV
		TI FOAGADO	1		25°C		0.5	1.9	
		TLE2161BC	V: 0	$R_S = 50 \Omega$	Full range			2.4	
ανιο	Temperature coefficient of in	put offset voltage	$V_{IC} = 0$ ,	KS = 50.22	Full range		6		μV/°C
	Input offset voltage long-tern	n drift (see Note 4)			25°C		0.04		μV/mo
li o	Input offeet ourrent		1		25°C		1		pА
10	Input offset current				Full range			0.8	nA
lun.	Input bigg ourrant		]		25°C		3		pА
İΙΒ	Input bias current				Full range			2	nA
\/	Common mode input veltage	a range			25°C	-1.6 to 4	-2 to 6		V
VICR	Common-mode input voltage	e range			Full range	-1.6 to 4			V
			D 40 ho		25°C	3.5	3.7		
.,	Mar Sarrian and Street and a street	ant and the same and a same	$R_L = 10 \text{ k}\Omega$		Full range	3.3			.,
V <sub>OM+</sub> I	Maximum positive peak outp	out voitage swing	D 400.0		25°C	2.5	3.1		V
			$R_L = 100 \Omega$ Full range 2	-					
			D 4010		25°C	-3.7	-3.9		
<b>.</b>	Maritania		$R_L = 10 \text{ k}\Omega$		Full range	-3.3			
VOM –	Maximum negative peak out	put voltage swing	D 400.0		25°C	-2.5	-2.7		V
1			$R_L = 100 \Omega$		Full range	-2			
			V 100V	D 401-0	25°C	15	80		
			$V_0 = \pm 2.8 \text{ V},$	$R_L = 10 \text{ k}\Omega$	Full range	2			
A	l anno airead differential colta		V- 0+-0V	D: 400.0	25°C	0.75	45		\//\/
AVD	Large-signal differential volta	age amplification	$V_0 = 0 \text{ to } 2 \text{ V},$	K[ = 100 \( \O \)	Full range	0.5			V/mV
			V- 0+- 0V	D: 400.0	25°C	0.5	3		
			$V_0 = 0 \text{ to } -2 \text{ V},$	K[ = 100 \( \O \)	Full range	0.25			
rį	Input resistance				25°C		1012		Ω
c <sub>i</sub>	Input capacitance				25°C		4		pF
z <sub>o</sub>	Open-loop output impedance	Э	I <sub>O</sub> = 0		25°C		280		Ω
CMRR	Common-mode rejection rati	in	V <sub>IC</sub> =V <sub>ICR</sub> min,	Ro = 50 O	25°C	65	82		dB
CIVINN	Common-mode rejection rati		VIC-VICRIIIII,	1/2 - 20 22	Full range	65			ub
ko) (D	Supply-voltage rejection ratio	2 (4)/22 : /4)/22)	$V_{CC\pm} = \pm 5 \text{ V to}$	o ±15 V,	25°C	75	93		dB
ksvr	Ouppry-voltage rejection ratio		$R_S = 50 \Omega$		Full range	75			ub
loc	Supply current				25°C		280	325	^
ICC	очрріу сипені		$V_0 = 0$ ,	No load	Full range			350	μΑ
∆ICC	Supply-current change over temperature range	operating		.10 1044	Full range		29		μА

<sup>†</sup> Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150$ °C extrapolated to  $T_A = 25$ °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



# TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE µPOWER OPERATIONAL AMPLIFIERS SLOS049D - NOVEMBER 1989 - REVISED MAY 1996

# operating characteristics at specified free-air temperature, V $_{\text{CC}}\,{}_{\pm}\text{=}\,{}_{\pm}5$ V (unless otherwise noted)

	PARAMETER	TE:	ST CONDITION	IS	T <sub>A</sub> †	TLE216 <sup>2</sup> TL	1C, TLE2 .E2161B0		UNIT
						MIN	TYP	MAX	
					25°C	7	10		
SR	Slew rate (see Figure 1)	$A_{VD} = 5$ ,	$R_L = 10 \text{ k}\Omega$ ,	C <sub>L</sub> = 100 pF	Full range	5			V/μs
Vn	Equivalent input noise voltage	$R_S = 20 \Omega$ ,	f = 10 Hz		25°C		59	100	nV/√ <del>Hz</del>
٧n	(see Figure 2)	$R_S = 20 \Omega$ ,	f = 1 kHz		25 0		43	60	IIV/√⊓Z
V <sub>n(PP)</sub>	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10	Hz		25°C		1.1		μV
In	Equivalent input noise current	f = 1 kHz			25°C		1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)} = 2 V$ , $R_L = 10 \text{ k}\Omega$	$A_{VD} = 5$ ,	f = 10 kHz,	25°C		0.025%		
	Gain-bandwidth product	f = 100 kHz,	$R_L = 10 \text{ k}\Omega$	C <sub>L</sub> = 100 pF	25°C		5.8		MHz
	(see Figure 3)	f = 100 kHz,	$R_L = 100 \text{ k}\Omega$ ,	C <sub>L</sub> = 100 pF	25 C		4.3		IVII IZ
	Settling time	ε = 0.1%			25°C		5		μs
t <sub>S</sub>	Settling time	ε = 0.01%			25 0		10		μ5
ВОМ	Maximum output-swing bandwidth	A <sub>VD</sub> = 5,	R <sub>L</sub> = 10 kΩ		25°C		420		kHz
φ.	Phase margin (see Figure 3)	$A_{VD} = 5$ ,	$R_L = 10 \text{ k}\Omega$	C <sub>L</sub> = 100 pF	25°C		70°		
Φm	rnase margin (see rigure 3)	A <sub>VD</sub> = 5,	$R_L = 100 \Omega$ ,	C <sub>L</sub> = 100 pF	20 0		84°		

<sup>†</sup> Full range is 0°C to 70°C.

# TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE μPOWER OPERATIONAL AMPLIFIERS SLOS049D – NOVEMBER 1989 – REVISED MAY 1996

# electrical characteristics at specified free-air temperature, V $_{\text{CC}\,\pm}$ = $\pm$ 15 V (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	T <sub>A</sub> †		C, TLE21 E2161BC		UNIT
						MIN	TYP	MAX 3 3.9 1.5 2.5 0.5	
		TI F0464C			25°C		0.6	3	
		TLE2161C			Full range			3.9	
\/10	Input offset voltage	TLE2161AC	1		25°C		0.5	1.5	mV
VIO	input onset voltage	TLLZIOIAC			Full range			2.5	1110
		TLE2161BC	1		25°C		0.3	0.5	
		TELEZIOIBO			Full range			1	
αVIO	Temperature coefficient of		$V_{IC} = 0$ ,	$R_S = 50 \Omega$	Full range		6		μV/°C
	Input offset voltage long-to (see Note 4)	erm drift			25°C		0.04		μV/mo
li o	Input offset ourrent		1		25°C		2		pА
lio	Input offset current				Full range			1	nA
lin	Input bias current		1		25°C		4		pА
lΒ	input bias current				Full range			3	nA
V. 0.0	Common-mode input volta	ogo rango			25°C	-11 to 13	-12 to 16		V
VICR	Common-mode input voite	age range			Full range	-11 to 13			٧
			P 10 k0		25°C	13.2	13.7		
V <sub>OM +</sub>	Maximum positivo poak o	utnut voltago swing	$R_L = 10 \text{ k}\Omega$		Full range	13			V
VOM +	Maximum positive peak output voltage	utput voltage swilig	R <sub>L</sub> = 600 Ω		25°C	12.5	13.2		V
			IXL = 000 32		Full range	12			
			$R_{I} = 10 \text{ k}\Omega$		25°C	-13.2	-13.7		
Vom –	Maximum negative peak of	output voltage swing			Full range	-13			V
· Olvi –	a	Julput Tollago olig	R <sub>L</sub> = 600 Ω		25°C	-12.5	-13		•
					Full range	-12			
			$V_0 = \pm 10 \text{ V},$	$R_L = 10 \text{ k}\Omega$	25°C	30	230		
			,		Full range	20			
AVD	Large-signal differential vo	oltage amplification	$V_0 = 0 \text{ to } 8 \text{ V},$	$R_L = 600 \Omega$	25°C	25	100		V/mV
VD					Full range	10			
			$V_0 = 0 \text{ to } -8 \text{ V},$	$R_L = 600 \Omega$	25°C	3	25		
	1				Full range	1	1012		
ri	Input resistance				25°C		1012		Ω
ci	Input capacitance				25°C	<u> </u>	4		pF
z <sub>0</sub>	Open-loop output impedar	nce	IO = 0		25°C		280		Ω
CMRR	Common-mode rejection r	atio	V <sub>IC</sub> = V <sub>ICR</sub> min,	$R_S = 50 \Omega$	25°C	72	90		dB
	•				Full range	70			
ksvr	Supply-voltage rejection ra	atio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	$V_{CC\pm} = \pm 5 \text{ V to } :$ RS = 50 $\Omega$	±15 V,	25°C	75 75	93		dB
			V2 = 20.77		Full range	75	200	250	
Icc	Supply current				25°C		290		μΑ
ΔICC	Supply-current change ov	er operating	VO = 0,	No load	Full range Full range		34	3/5	μΑ
	temperature range								

<sup>†</sup> Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^{\circ}C$  extrapolated to  $T_A = 25^{\circ}$ C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



# TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE μPOWER OPERATIONAL AMPLIFIERS SLOS049D – NOVEMBER 1989 – REVISED MAY 1996

# operating characteristics at specified free-air temperature, $V_{CC\pm}$ = $\pm 15$ V (unless otherwise noted)

	PARAMETER	TE	ST CONDITIO	NS	T <sub>A</sub> †		1C, TLE2 .E2161B0		UNIT
					^	MIN	TYP	MAX	
SR	Slow rate (and Figure 1)	A. (5 – 5	Pr = 10 kO	C <sub>L</sub> = 100 pF	25°C	7	10		V/μs
SK	Slew rate (see Figure 1)	$A_{VD} = 5$ ,	KL = 10  Ks2,	CL = 100 pr	Full range	5			ν/μδ
.,	Equivalent input noise voltage	$R_S = 20 \Omega$ ,	f = 10 Hz		25°C		70	100	->4/15
V <sub>n</sub>	(see Figure 2)	$R_S = 20 \Omega$ ,	f = 1 kHz		25.0		40	60	nV/√Hz
V <sub>n(PP)</sub>	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10	) Hz		25°C		1.1		μV
In	Equivalent input noise current	f = 1 kHz			25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)} = 2 V$ , $R_L = 10 \text{ k}\Omega$	A <sub>VD</sub> = 5,	f = 10 kHz,	25°C		0.025%		
	Gain-bandwidth product	f = 100 kHz,	$R_L = 10 \text{ k}\Omega$	C <sub>L</sub> = 100 pF	25°C		6.4		MHz
	(see Figure 3)	f = 100 kHz,	$R_L = 600 \Omega$ ,	C <sub>L</sub> = 100 pF	25.0		5.6		IVITZ
	Cottling time	ε = 0.1%			25°C		5		
t <sub>S</sub>	Settling time	ε = 0.01%			25°C		10		μs
ВОМ	Maximum output-swing bandwidth	A <sub>VD</sub> = 5,	R <sub>L</sub> = 10 kΩ		25°C		116		kHz
4	Dhaga marain (aga Figura 2)	$A_{VD} = 5$ ,	$R_L = 10 \text{ k}\Omega$	C <sub>L</sub> = 100 pF	2500		72°		
Φm	Phase margin (see Figure 3)	$A_{VD} = 5$ ,	$R_1 = 600 \Omega$	$C_{I} = 100 pF$	25°C		78°		

<sup>†</sup> Full range is 0°C to 70°C.

# TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE μPOWER OPERATIONAL AMPLIFIERS SLOS049D – NOVEMBER 1989 – REVISED MAY 1996

# electrical characteristics at specified free-air temperature, V<sub>CC $\pm$ </sub> = $\pm$ 5 V (unless otherwise noted)

	PARAMETER		TEST CON	IDITIONS	T <sub>A</sub> †				UNIT
					TA†         Milk           25°C         Full range           25°C         Total           4         4           25°C         3.5           Full range         3.1           25°C         2.5           Full range         2.2           25°C         -3.7           Full range         -2.5           Full range         0.5           25°C         15           Full range         0.5           25°C         0.5           Full range         0.25           25°C         0.5           Full range         0.25           25°C         65           Full range         65           25°C         75           Full range         65           25°C         75           Full range         65           25°C         75           Full range         65	MIN	TYP	MAX	
		TI E21611			25°C		MIN TYP MAX  0.8 3.1  4.4  0.6 2.6  3.9  0.5 1.9  2.7  6		
		TLE2161I			Full range			4.4	
VIO	Input offset voltage	TLE2161AI			25°C		0.6	2.6	mV
VIO	input onset voltage	TEEZTOTAI	_					3.9	111 V
		TLE2161BI					0.5		
			١,, ,	B 50.0				2.7	
αΛΙΟ	Temperature coefficient of inpu		$V_{IC} = 0$ ,	$R_S = 50 \Omega$	Full range		6		μV/°C
	Input offset voltage long-term ( (see Note 4)	drift			25°C		0.04		μV/mc
lio	Input offset current						1		pА
.10	mput oncot outront		_					2	nA
lв	Input bias current						3		pA
					Full range			4	nA
					25°€	ı			
					25 0				
VICR	Common-mode input voltage r	ange				-1.6			V
					Full range				
					0500				
V <sub>OM</sub> +	Maximum positive peak output voltage		$R_L = 10 \text{ k}\Omega$			_	3.7		
							2.1		٧
		$R_L = 100 \Omega$				3.1		1	
			+				-39		
			$R_L = 10 \text{ k}\Omega$				0.0		
VOM –	Maximum negative peak output	t voltage swing				-2.5	-2.7		V
			$R_L = 100 \Omega$				-		
			14 10014			15	80		
			$V_0 = \pm 2.8 \text{ V},$	$R_L = 10 \text{ k}\Omega$	Full range	2			
۸	Lorge signal differential volteg	amplification	$V_{O} = 0 \text{ to } 2 \text{ V},$	D 100 O	25°C	0.75	45		V/mV
AVD	Large-signal differential voltage	e amplification	VO = 0 to 2 V,	K[ = 100 t2	Full range	0.5			V/IIIV
			$V_0 = 0 \text{ to } -2 \text{ V},$	Ri = 100 O	25°C	0.5	3		
			VO=010 2 V,	11 - 100 32		0.25			
r <sub>i</sub>	Input resistance						1012		Ω
ci	Input capacitance								pF
z <sub>o</sub>	Open-loop output impedance		IO = 0						Ω
CMRR	Common-mode rejection ratio		V <sub>IC</sub> =V <sub>ICR</sub> min,	$R_S = 50 \Omega$		_	82		dB
			10 1011						
ksvr	Supply-voltage rejection ratio (	ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	n)			75 05	93		dB
			$R_{\rm S} = 50 \Omega$ Full ra		65	200	205		
lcc	Supply current					<del>                                     </del>	280	325 350	μΑ
ΔlCC	Supply-current change over op temperature range	erating	$V_0 = 0$ ,	No load	Full range		29	350	μА

<sup>†</sup> Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^{\circ}C$  extrapolated to TA= 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



# TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE µPOWER OPERATIONAL AMPLIFIERS SLOS049D - NOVEMBER 1989 - REVISED MAY 1996

# operating characteristics at specified free-air temperature, V $_{\text{CC}}\,{}_{\pm}$ = $\pm$ 5 V (unless otherwise noted)

	PARAMETER	TE	ST CONDITIO	NS	T <sub>A</sub> †		•		UNIT
						43 60  1.1  1  0.025%  5.8  4.3  5  10  420  70°	MIN TYP		
SR	Slew rate (see Figure 1)	AVD = 5,	$R_I = 10 \text{ k}\Omega$	C <sub>I</sub> = 100 pF	25°C	7	10		V/µs
J N	Siew rate (see rigule 1)	AVD = 3,	N_ = 10 K22,	CL = 100 pr	Full range	5			ν/μ5
V	Equivalent input noise	$R_S = 20 \Omega$ ,	f = 10 Hz		25°C		59	100	nV/√ <del>Hz</del>
V <sub>n</sub>	voltage (see Figure 2)	$R_S = 20 \Omega$ ,	f = 1 kHz		25 C		43	60	IIV/∀⊓Z
V <sub>n(PP)</sub>	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10	Hz		25°C		1.1		μV
In	Equivalent input noise current	f = 1 kHz			25°C		1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)} = 2 \text{ V},$ $R_L = 10 \text{ k}\Omega$	$A_{VD} = 5$ ,	f = 10 kHz,	25°C		0.025%		
	Gain-bandwidth product	f = 100 kHz,	$R_L = 10 \text{ k}\Omega$	C <sub>L</sub> = 100 pF	25°C		5.8		MHz
	(see Figure 3)	f = 100 kHz,	$R_L = 100 \Omega$	C <sub>L</sub> = 100 pF	25 C		4.3		IVITZ
	Settling time	ε = 0.1%			25°C		5		
t <sub>S</sub>	Settiling time	ε = 0.01%			25 C		10		μs
ВОМ	Maximum output-swing bandwidth	A <sub>VD</sub> = 5,	R <sub>L</sub> = 10 kΩ		25°C		420		kHz
4	Phone margin (and Figure 2)	$A_{VD} = 5$ ,	$R_L = 10 \text{ k}\Omega$	C <sub>L</sub> = 100 pF	25°C		70°		
φ <sub>m</sub>	Phase margin (see Figure 3)	A <sub>VD</sub> = 5,	R <sub>L</sub> = 100 Ω,	C <sub>L</sub> = 100 pF	25.0		84°		

<sup>†</sup> Full range is – 40°C to 85°C.

## TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE µPOWER OPERATIONAL AMPLIFIERS

SLOS049D - NOVEMBER 1989 - REVISED MAY 1996

# electrical characteristics at specified free-air temperature, V $_{\text{CC}\,\pm}$ = $\pm$ 15 V (unless otherwise noted)

	PARAMETER	1	TEST CON	IDITIONS	T <sub>A</sub> †				UNIT
					``	MIN	0.6 3 4.3 0.5 1.5 2.9 0.3 0.5 1.3 6 0.04 2 3 4 5 -11 -12 to to to 13 16 -11 to 13 13.2 13.7 13 12.5 13.2 12 13.2 -13.7 -13		
		TI F04641			25°C		0.6	3	
		TLE2161I			Full range			4.3	
\/.a	Input offeet voltage	TLE2161AI	1		25°C		0.5	1.5	mV
VIO	Input offset voltage	TLEZIOTAI			Full range			2.9	IIIV
		TLE2161BI			25°C		0.3	0.5	
			V <sub>IC</sub> = 0,	$R_S = 50 \Omega$	Full range			1.3	
αΛΙΟ	Temperature coefficient of		1 10 = 0,	113 - 00 22	Full range		6		μV/°C
	Input offset voltage long-te	rm drift (see Note 4)	_		25°C		0.04		μV/mo
lio	Input offset current				25°C		2		pА
10	input onoct outront		_		Full range			3	nA
IIB	Input bias current				25°C		4		pА
חוי סוי	input blub current				Full range			5	nA
					0500				.,
					25°C				V
VICR	Common-mode input volta	ge range			<u> </u>		10		
					Full range	1			V
						13			
			R <sub>L</sub> = 10 kΩ		25°C	13.2	13.7	$\equiv$	
V <sub>OM</sub> +	Maximum positive peak ou	struit voltago euring	K[ = 10 K22		Full range	13			V
VOM +	iviaximum positive peak ou	Airium positive peak output voltage swing			25°C	12.5	13.2		V
			$R_L = 600 \Omega$		Full range	12			
			R <sub>L</sub> = 10 kΩ		25°C	-13.2	-13.7		
Vom –	Maximum negative peak o	utnut voltage swing	T(_ = 10 K22		Full range				V
VOIVI —	Maximum negative peak o	atput voltage swing	R <sub>L</sub> = 600 Ω		25°C	-12.5	-13		v
			TAL = 000 11		Full range				
			$V_0 = \pm 10 \text{ V},$	R <sub>L</sub> = 10 kΩ	25°C		230		
			v0 = ±10 v,		Full range				
A <sub>VD</sub>	Large-signal differential vo	Itage amplification	$V_0 = 0 \text{ to } 8 \text{ V},$	$R_1 = 600 \Omega$	25°C		100		V/mV
- VD	gg		10 1111		Full range	_			.,,,,
			$V_0 = 0 \text{ to} - 8 \text{ V},$	$R_1 = 600 \Omega$	25°C		25		
			10 010 01,		Full range	1	40		
rį	Input resistance				25°C				Ω
ci	Input capacitance				25°C				pF
z <sub>o</sub>	Open-loop output impedan	ice	IO = 0		25°C				Ω
CMRR	Common-mode rejection ra	atio	V <sub>IC</sub> =V <sub>ICR</sub> min,	Re = 50 O	25°C		90		dB
J					Full range				<u> </u>
ksvr	Supply-voltage rejection ra	atio $(\Delta V_{CC+}/\Delta V_{IC})$	$V_{CC\pm} = \pm 5 \text{ V to}$	±15 V,	25°C		93		dB
··ovk			$R_S = 50 \Omega$		Full range	65			
Icc	Supply current				25°C		290		μΑ
.00			$V_0 = 0$ ,	No load	Full range			375	por t
ΔICC	Supply-current change over temperature range	er operating			Full range		34		μΑ

<sup>†</sup> Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^{\circ}C$  extrapolated to  $T_A = 25^{\circ}C$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



# TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE μPOWER OPERATIONAL AMPLIFIERS SLOS049D – NOVEMBER 1989 – REVISED MAY 1996

# operating characteristics at specified free-air temperature, V $_{CC~\pm}$ = $\pm$ 15 V (unless otherwise noted)

	PARAMETER	TE	ST CONDITION	NS	T <sub>A</sub> †		•		UNIT
					Full range 5  25°C 70  40  25°C 1.1  25°C 1.1  25°C 0.025%  0.025%  0.0F 25°C 5.6  25°C 10  25°C 116  0.0F 25°C 116	MAX			
SR	Slew rate (see Figure 1)	A. 45 – E	Pr = 10 kO	C <sub>I</sub> = 100 pF	25°C	7	10		V/μs
SIX	Siew rate (see Figure 1)	$A_{VD} = 5$ ,	KL = 10 KS2,	CL = 100 pr	Full range	5			ν/μ5
V	Equivalent input noise voltage	$R_S = 20 \Omega$ ,	f = 10 Hz		25°€		70	100	-> //s/II=
Vn	(see Figure 2)	$R_S = 20 \Omega$ ,	f = 1 kHz		25 C		40	60	nV/√Hz
V <sub>n(PP)</sub>	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10	Hz		25°C		1.1		μV
In	Equivalent input noise current	f = 1 kHz			25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)} = 2 V$ , $R_L = 10 \text{ k}\Omega$	A <sub>VD</sub> = 5,	f = 10 kHz,	25°C		0.025%		
	Gain-bandwidth product	f = 100 kHz,	$R_L = 10 \text{ k}\Omega$ ,	C <sub>L</sub> = 100 pF	2500		6.4		MHz
	(see Figure 3)	f = 100 kHz,	$R_L = 600 \Omega$ ,	C <sub>L</sub> = 100 pF	25 C		5.6		IVITZ
	Settling time	ε = 0.1%			2500		5		
t <sub>S</sub>	Settling time	ε = 0.01%			25 C		10		μs
ВОМ	Maximum output-swing bandwidth	A <sub>VD</sub> = 5,	R <sub>L</sub> = 10 kΩ		25°C		116		kHz
φ.	Phase margin (see Figure 3)	$A_{VD} = 5$ ,	$R_L = 10 \text{ k}\Omega$	C <sub>L</sub> = 100 pF	25°€		72°		
Φm	Filase margin (see Figure 3)	$A_{VD} = 5$ ,	$R_L = 600 \Omega$	C <sub>L</sub> = 100 pF	250		78°		

<sup>†</sup> Full range is – 40°C to 85°C.

## TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE µPOWER OPERATIONAL AMPLIFIERS

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# electrical characteristics at specified free-air temperature, V $_{\text{CC}}$ $_{\pm}$ = $\pm$ 5 V (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	T <sub>A</sub> †	TL	E2161N E2161A E2161B	М	UNIT
						MIN	TYP	MAX	
		TLE2161M			25°C		0.8	3.1	
		TLEZIONI			Full range			6	
V <sub>IO</sub>	Input offset voltage	TLE2161AM			25°C		0.6	2.6	mV
V10	input onset voltage	TELEZIOTAW			Full range			4.6	1117
		TLE2161BM			25°C		0.5	1.9	
		TEEZTOTEM			Full range			3.1	
αVIO	Temperature coefficient of i voltage	nput offset	V <sub>IC</sub> = 0,	$R_S = 50 \Omega$	Full range		6		μV/°C
	Input offset voltage long-ter (see Note 4)	m drift			25°C		0.04		μV/mo
1	Innut offert gurrent				25°C		1		рΑ
ΙΟ	Input offset current				Full range			15	nA
1	Innut bigg gurrant		7		25°C		3		pА
IΒ	Input bias current				Full range			30	nA
V:	Common mode input valte				25°C	-1.6 to 4	-2 to 6		V
VICR	Common-mode input volta	ge range			Full range	-1.6 to 4			V
	All poeks are		D. 40 kg		25°C	3.5	3.7		V
		All packages	$R_L = 10 \text{ k}\Omega$		Full range	3			V
\/014	Maximum positive peak	FK and JG	R <sub>L</sub> = 600 Ω		25°C	2.5	3.6		
VOM +	output voltage swing	packages	K_ = 000 22		Full range	2			V
		D and P	R <sub>L</sub> = 100 Ω		25°C	2.5	3.1		V
		packages	11/2 = 100 22		Full range	2			
		All packages	R <sub>L</sub> = 10 kΩ		25°C	-3.7	-3.9		
		All packages	17[ = 10 1/22		Full range	-3			
V <sub>OM</sub> –	Maximum negative peak	FK and JG	$R_L = 600 \Omega$		25°C	-2.5	-3.5		V
* OIVI =	output voltage swing	packages			Full range	-2			
		D and P	R <sub>L</sub> = 100 Ω		25°C	-2.5	-2.7		
		packages	112 - 100 22		Full range	-2			
		All packages	$V_0 = \pm 2.8 \text{ V},$	R <sub>L</sub> = 10 kΩ	25°C	15	80		
		7 III paokageo	v <sub>0</sub> = ±2.0 v,		Full range	2			
			$V_0 = 0 \text{ to } 2.5 \text{ V},$	Rt = 600 O	25°C	1	65		
		FK and JG	v <sub>0</sub> = 0 to 2.0 v,	11 - 000 22	Full range	0.5			
AVD	Large-signal differential	packages	$V_0 = 0 \text{ to } -2.5 \text{ V},$	Ri = 600 O	25°C	1	16		V/mV
ט עי	voltage amplification		10 5.5 2.5 4,	500 12	Full range	0.5			
			$V_0 = 0 \text{ to } 2 \text{ V}$	R <sub>1</sub> = 100 O	25°C	0.75	45		
		D and P	$V_0 = 0 \text{ to } 2 \text{ V}, \qquad F$	$V$ , $R_L = 100 \Omega$	Full range	0.5			
	packages		$V_0 = 0 \text{ to } -2 \text{ V},  R_L = 100 \Omega$		25°C	0.5	3		
			1 v0 = 0 to 2 v,	L = 100 a2	Full range	0.25			

 $<sup>^{\</sup>dagger}$  Full range is - 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150$ °C extrapolated to  $T_A = 25$ °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



# electrical characteristics at specified free-air temperature, V $_{\text{CC}\,\pm}$ = $\pm$ 5 V (unless otherwise noted continued)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TI TL TL	UNIT		
				MIN	TYP	MAX	
rį	Input resistance		25°C		1012		Ω
ci	Input capacitance		25°C		4		pF
z <sub>O</sub>	Open-loop output impedance	IO = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50 \Omega$	25°C	65	82		dB
CIVIKK	Common-mode rejection ratio	AIC = AICKIIIIII' VZ = 20.75	Full range	60			uВ
kova	Supply-voltage rejection ratio (ΔV <sub>CC+</sub> /ΔV <sub>IO</sub> )	$V_{CC\pm} = \pm 5 \text{ V to } \pm 15 \text{ V},$	25°C	75	93		dB
ksvr	Supply-voltage rejection ratio (\(\Delta\delta\CC\frac{1}{2}\Delta\delta\O)	$R_S = 50 \Omega$	Full range	65			иь
la a	Cupply ourrent		25°C		280	325	
Icc	Supply current	$V_{O} = 0$ , No load	Full range			350	μΑ
ΔICC	Supply-current change over operating temperature range	, ite iouu	Full range		39		μΑ

<sup>†</sup> Full range is – 55°C to 125°C.

# operating characteristics, V<sub>CC $\pm$ </sub> = $\pm$ 5 V, T<sub>A</sub> = 25°C

	PARAMETER	т	EST CONDITIO	NS	TLE2161M TLE2161AM TLE2161BM			UNIT
					MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	$A_{VD} = 5$ ,	$R_L = 10 \text{ k}\Omega$ ,	C <sub>L</sub> = 100 pF		10		V/μs
\ /	Equivalent input poins voltage (see Figure 2)	$R_S = 20 \Omega$ ,			59			
V <sub>n</sub>	Equivalent input noise voltage (see Figure 2)	$R_S = 20 \Omega$ ,	f = 1 kHz		43		nV/√Hz	
V <sub>n(PP)</sub>	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to	10 Hz			1.1		μV
In	Equivalent input noise current	f = 1 kHz				1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 5$ , $R_L = 10 \text{ k}\Omega$	$V_{O(PP)} = 2 V$	f = 10 kHz,		0.025%		
	Cain bandwidth product (and Figure 3)	f = 100 kHz,	$R_L = 10 \text{ k}\Omega$	C <sub>L</sub> = 100 pF		5.8		MHz
	Gain-bandwidth product (see Figure 3)	f = 100 kHz,	$R_L = 600 \text{ k}\Omega$	C <sub>L</sub> = 100 pF		4.3		IVITZ
	Cottling time	ε = 0.1%				5		
t <sub>S</sub>	Settling time	ε = 0.01%				10		μs
ВОМ	Maximum output-swing bandwidth	$A_{VD} = 5$ ,	R <sub>L</sub> = 10 kΩ			420		kHz
4	Phono morgin (con Figure 2)	$A_{VD} = 5$ ,	$R_L = 10 \text{ k}\Omega$ ,	C <sub>L</sub> = 100 pF		70°		
Φm	Phase margin (see Figure 3)	A <sub>VD</sub> = 5,	$R_L = 600 \Omega$ ,	C <sub>L</sub> = 100 pF		84°		

## TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE µPOWER OPERATIONAL AMPLIFIERS

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# electrical characteristics at specified free-air temperature, V $_{CC~\pm}$ = $\pm 15$ V (unless otherwise noted)

	PARAMETE	R	TEST CON	DITIONS	T <sub>A</sub> †	TL	LE2161N E2161A E2161B	м	UNIT
						MIN	TYP	MAX	
		TI FOAGANA			25°C		0.6	3	
		TLE2161M			Full range			6	
\/	Innut offeet veltere	TI F0464 AM			25°C		0.5	1.5	\/
VIO	Input offset voltage	TLE2161AM			Full range			3.6	mV
		TLE2161BM	1		25°C		0.3	0.5	
		TLLZ TO TOW		_	Full range			1.7	
αΝΙΟ	Temperature coefficient	<u> </u>	$V_{IC} = 0$ ,	$R_S = 50 \Omega$	Full range		6		μV/°C
	Input offset voltage long (see Note 4)	-term drift			25°C		0.04		μV/mo
li o	Input offeet current		1		25°C		2		рΑ
lio	Input offset current				Full range			20	nA
lin.	Input bias current		1		25°C		4		pА
IB	input bias current				Full range			40	nA
\/.05	Common mode input ve	altogo rongo			25°C	-11 to 13	-12 to 16		<b>V</b>
VICR	Common-mode input vo	mage range			Full range	-11 to 13			V
			R <sub>L</sub> = 10 kΩ		25°C	13.2	13.7		
V <sub>OM</sub> +	Maximum positive peak	K[ = 10 K22	Full range	12.5			V		
	Maximum positive peak	output voltage swilig	R <sub>L</sub> = 600 Ω	25°C	12.5	13.2		V	
			11_ = 000 11		Full range	12			
			R <sub>L</sub> = 10 kΩ		25°C	-13.2	-13.7		
V <sub>OM</sub> –	Maximum negative peal	k output voltage swing	RL = 10 KΩ		Full range	-12.5			V
VOINI –	Maximum negative pear	k output voltage swing	R <sub>L</sub> = 600 Ω		25°C	-12.5	-13		v
			11 - 000 22		Full range	-12			
			$V_0 = \pm 10 \text{ V},$	$R_L = 10 \text{ k}\Omega$	25°C	30	230		
			-0 = 10 1,		Full range	20			
A <sub>VD</sub>	Large-signal differential	voltage amplification	$V_0 = 0 \text{ to } 8 \text{ V},$	$R_L = 600 \Omega$	25°C	25	100		V/mV
1.40	gg		10 0 10 0 1,		Full range	7	-		.,
			$V_0 = 0 \text{ to } -8 \text{ V},$	$R_1 = 600 \Omega$	25°C	3	25		
			,		Full range	1	10		_
rį	Input resistance				25°C		1012		Ω
ci	Input capacitance				25°C		4		pF
z <sub>0</sub>	Open-loop output imped	dance	IO = 0		25°C	<u> </u>	280		Ω
CMRR	Common-mode rejectio	n ratio	V <sub>IC</sub> = V <sub>ICR</sub> min,	$R_S = 50 \Omega$	25°C	72	90		dB
	•				Full range	65			
ksvr	Supply-voltage rejection	ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	$V_{CC\pm} = \pm 5 \text{ V to}$ $R_S = 50 \Omega$	±15 V,	25°C	75 05	93		dB
			1.8 - 30 22		Full range	65		050	
Icc	Supply current				25°C	├──	290	350	μΑ
ΔlCC	Supply-current change temperature range	over operating	$V_{O} = 0,$	No load	Full range Full range		46	375	μΑ
t Full ran	go is 55°C to 125°C			-			-		

<sup>†</sup> Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150$ °C extrapolated to  $T_A = 25$ °C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



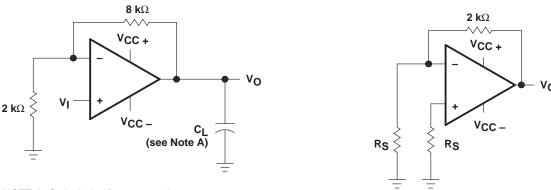
# TLE2161, TLE2161A, TLE2161B EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE μPOWER OPERATIONAL AMPLIFIERS SLOS049D – NOVEMBER 1989 – REVISED MAY 1996

# operating characteristics at specified free-air temperature, V $_{CC~\pm}$ = $\pm 15$ V (unless otherwise noted)

	PARAMETER	TE	ST CONDITION	NS	T <sub>A</sub> †	TL TL	VI	UNIT	
						MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	A <sub>VD</sub> = 5,	$R_1 = 10 \text{ k}\Omega$	C <sub>I</sub> = 100 pF	25°C	7	10		V/μs
SK	Siew rate (see rigure 1)	AVD = 3,	K_ = 10 KS2,	CL = 100 pr	Full range	5			ν/μδ
v <sub>n</sub>	Equivalent input noise voltage	$R_S = 20 \Omega$ ,	f = 10 Hz		25°C		70		nV/√ <del>Hz</del>
v n	(see Figure 2)	$R_S = 20 \Omega$ ,	f = 1 kHz		25 0		40		IIV/ VIIZ
V <sub>N(PP)</sub>	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10	) Hz		25°C	1.1			μV
In	Equivalent input noise current	f = 1 Hz			25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)} = 2 V$ , $R_L = 10 \text{ k}\Omega$	$A_{VD} = 5$ ,	f = 10 kHz,	25°C		0.025%		
	Gain-bandwidth product	f = 100 kHz,	$R_L = 10 \text{ k}\Omega$ ,	C <sub>L</sub> = 100 pF	25°C		6.4		MHz
	(see Figure 3)	f = 100 kHz,	$R_L = 600 \Omega$ ,	C <sub>L</sub> = 100 pF	25 C		5.6		IVITIZ
	Cottling time	ε = 0.1%			25°C		5		
t <sub>S</sub>	Settling time	ε = 0.01%			25 C		10		μs
ВОМ	Maximum output-swing bandwidth	A <sub>VD</sub> = 5,	R <sub>L</sub> = 10 kΩ		25°C		116		kHz
_	Dhose margin (see Figure 2)	$A_{VD} = 5$ ,	$R_L = 10 \text{ k}\Omega$	C <sub>L</sub> = 100 pF	2500				
Φm	Phase margin (see Figure 3)	A <sub>VD</sub> = 5,	$R_L = 600 \Omega$ ,	C <sub>L</sub> = 100 pF	25°C		78°		

<sup>†</sup>Full range is – 55°C to 125°C.

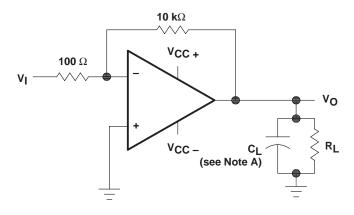
#### PARAMETER MEASUREMENT INFORMATION



NOTE A: C<sub>L</sub> includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

Figure 2. Noise-Voltage Test Circuit



NOTE A: C<sub>I</sub> includes fixture capacitance.

Figure 3. Gain-Bandwidth Product and Phase-Margin Test Circuit

#### typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

#### Input bias and offset current

At the picoampere bias-current level typical of the TLE2161, TLE2161A, and TLE2161B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket, and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.



#### **TYPICAL CHARACTERISTICS**

#### **Table of Graphs**

			FIGURE
VIO	Input offset voltage	Distribution	4
I <sub>IB</sub>	Input bias current	vs Common-mode input voltage vs Free-air temperature	5 6
I <sub>IO</sub>	Input offset current	vs Free-air temperature	6
VICR	Common-mode input voltage range limits	vs Free-air temperature	7
VOM	Maximum positive peak output voltage	vs Output current	8
Vом	Maximum negative peak output voltage	vs Output current	9
Vом	Maximum peak output voltage	vs Supply voltage	10, 11, 12
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	13, 14, 15
AVD	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	16 17
los	Short-circuit output current	vs Elapsed time	18
	Large-signal voltage amplification	vs Free-air temperature	19
z <sub>O</sub>	Output impedance	vs Frequency	20
CMRR	Common-mode rejection ratio	vs Frequency	21
ICC	Supply current	vs Supply voltage vs Free-air temperature	22 23
	Pulse response	Small signal Large signal	24, 25 26, 27
	Noise voltage (referred to input)	0.1 to 10 Hz	28
Vn	Equivalent input noise voltage	vs Frequency	29
THD	Total harmonic distortion	vs Frequency	30, 31
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	32 33
φm	Phase margin	vs Supply voltage vs Free-air temperature	34 35
	Phase shift	vs Frequency	16

#### TYPICAL CHARACTERISTICS<sup>†</sup>

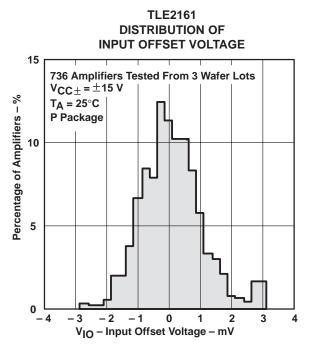
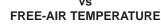
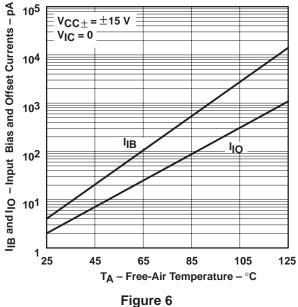


Figure 4

# **INPUT BIAS CURRENT** AND INPUT OFFSET CURRENT





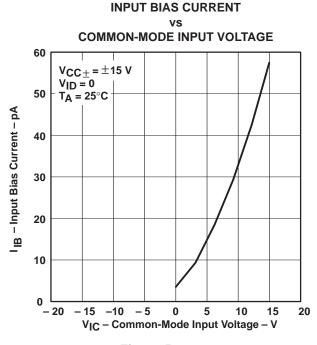


Figure 5

#### **COMMON-MODE INPUT VOLTAGE RANGE LIMITS**

#### FREE-AIR TEMPERATURE

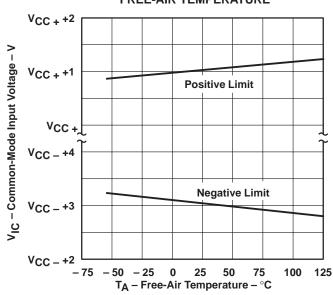


Figure 7

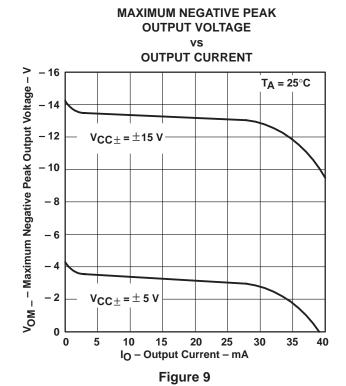
<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



#### TYPICAL CHARACTERISTICS

### **MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE OUTPUT CURRENT** 16 VOM+ - Maximum Positive Peak Output Voltage - V T<sub>A</sub> = 25°C 14 12 $V_{CC} + = \pm 15 V$ 10 8 6 $V_{CC\pm} = \pm 5 V$ 2 0 L - 20 - 30 - 40 - 50 IO - Output Current - mA

Figure 8



MAXIMUM PEAK OUTPUT VOLTAGE

vs

SUPPLY VOLTAGE

MAXIMUM PEAK OUTPUT VOLTAGE

vs

SUPPLY VOLTAGE

SUPPLY VOLTAGE

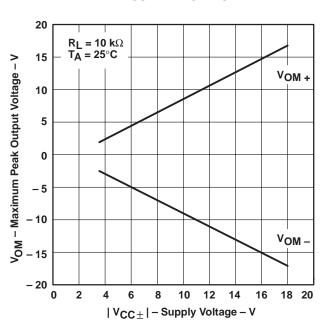


Figure 10

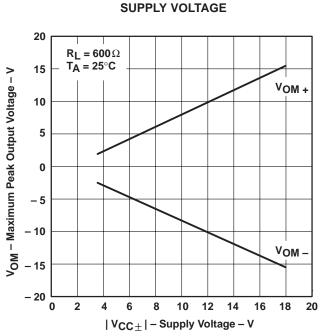


Figure 11

TEXAS INSTRUMENTS

#### TYPICAL CHARACTERISTICS

# **MAXIMUM PEAK OUTPUT VOLTAGE SUPPLY VOLTAGE**

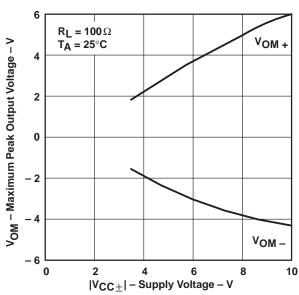


Figure 12

## **MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE** ٧s **FREQUENCY** VO(PP) - Maximum Peak-to-Peak Output Voltage - V 10 $V_{CC\pm} = \pm 5 V$ $R_L = 10 \text{ k}\Omega$ $T_A = 25^{\circ}C$ 8 6 4 2 10 k 100 k 10 M 1 M f - Frequency - Hz

Figure 13

#### **MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE**

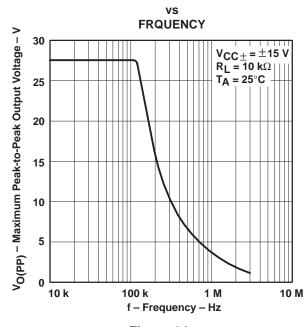


Figure 14

#### **MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE**

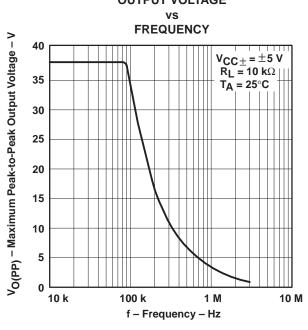
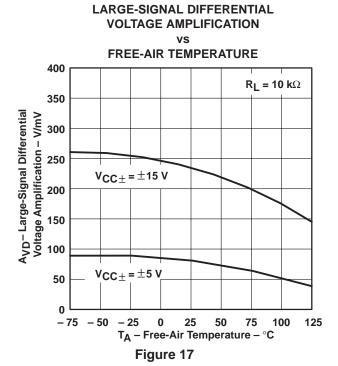


Figure 15

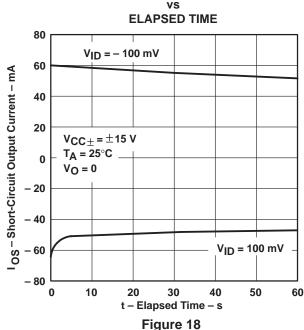
#### TYPICAL CHARACTERISTICS<sup>†</sup>

#### **AMPLIFICATION AND PHASE SHIFT FRQUENCY** 60° 120 80° 100 **Phase Shift** A<sub>VD</sub>- Large-Signal Differential Voltage Amplification - dB 80 100° AVD Phase Shift 60 120° 40 140° 20 160° $V_{CC\pm} = \pm 15 V$ $R_L = 10 \text{ k}\Omega$ 0 180° $C_{L} = 100 pF$ T<sub>A</sub> = 25°C - 20 200° 0.1 100 1k 10k 100k 1M 10M f - Frequency - Hz Figure 16

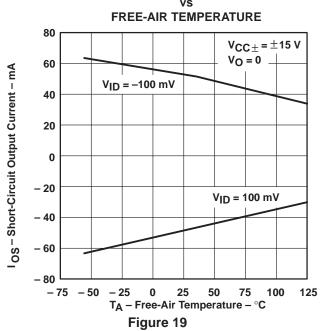
LARGE-SIGNAL DIFFERENTIAL VOLTAGE



# SHORT-CIRCUIT OUTPUT CURRENT vs



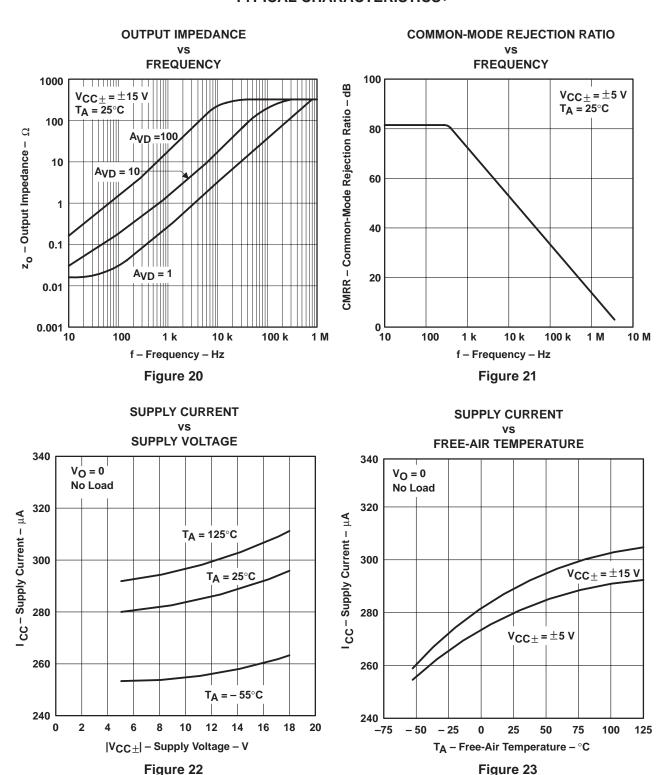
# LARGE-SIGNAL VOLTAGE AMPLIFICATION



<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



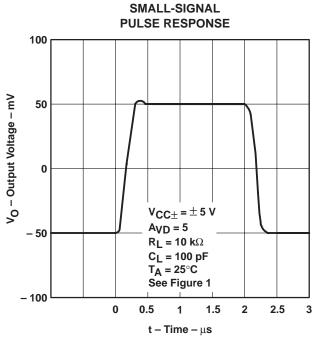
#### TYPICAL CHARACTERISTICS<sup>†</sup>



<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



#### **TYPICAL CHARACTERISTICS**



t – Time – μs
Figure 24

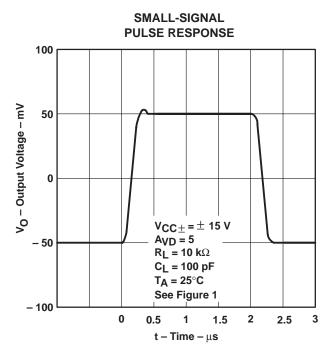
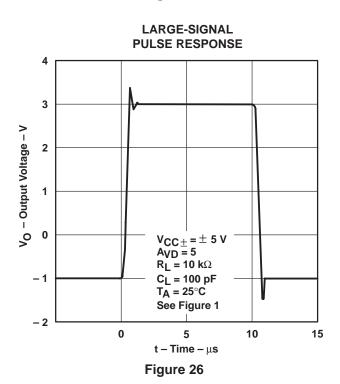
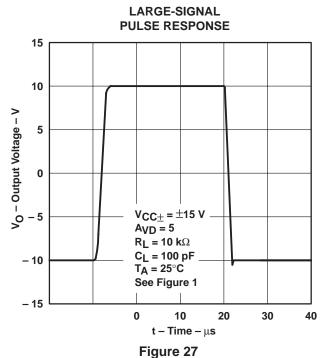
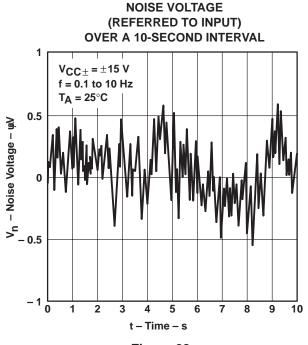


Figure 25





#### TYPICAL CHARACTERISTICS





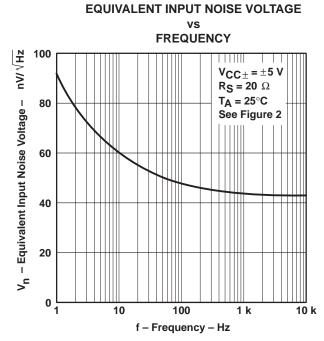
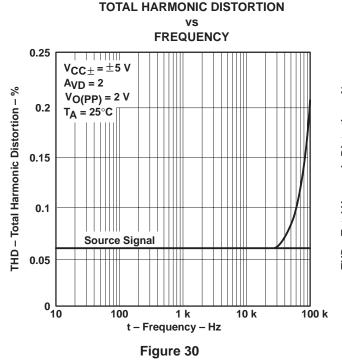


Figure 29

**TOTAL HARMONIC DISTORTION** 



vs **FREQUENCY** 0.6 V<sub>CC±</sub> = ± 5 V A<sub>VD</sub> = 10 **IHD – Total Harmonic Distortion – %** 0.5  $V_{O(PP)} = 2 V$ TA = 25°C 0.4 0.3

Source Signal

0<sub>10</sub> 100 1 k 10 k 100 k f - Frequency - Hz

Figure 31

0.2

0.1

#### TYPICAL CHARACTERISTICS

7

#### **GAIN-BANDWIDTH PRODUCT SUPPLY VOLTAGE** 7 f = 100 kHz $R_L = 10 \text{ k}\Omega$ Gain-Bandwidth Product - MHz C<sub>L</sub> = 100 pF 6.6 T<sub>A</sub> = 25°C See Figure 3 6.2 5.8 5.4 5 0 8 12 16 20 $|V_{CC\pm}|$ – Supply Voltage – V

Figure 32

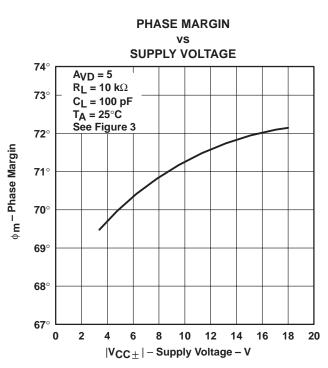


Figure 34

# **GAIN-BANDWIDTH PRODUCT** FREE-AIR TEMPERATURE f = 100 kHz $R_L = 10 \text{ k}\Omega$ C<sub>L</sub> = 100 pF $V_{CC\pm} = \pm 15 \text{ V}$

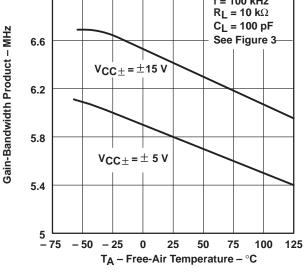


Figure 33

#### **PHASE MARGIN** vs FREE-AIR TEMPERATURE 78° $A_{VD} = 5$ $R_L = 10 \text{ k}\Omega$ $C_L = 100 pF$ 76° See Figure 3 φm – Phase Margin **74**° **72**° $V_{CC\pm} = \pm 5 V$ **70**° 68° $V_{CC\pm} = \pm 15 V$ 66° -75 -50 -25 0 25 75 100 50 125 $T_A$ – Free-Air Temperature – $^{\circ}$ C

Figure 35

#### APPLICATION INFORMATION

#### macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 36 and Figure 37 were generated using the TLE2161 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

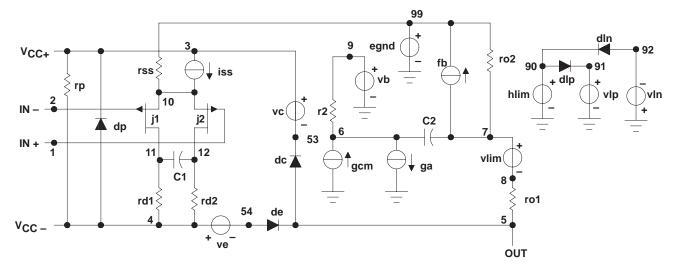


Figure 36. Boyle Macromodel

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

PSpice and Parts are trademark of MicroSim Corporation.



#### **APPLICATION INFORMATION**

#### macromodel information (continued)

```
.subckt TLE2161 1 2 3 4 5
      11 12 125.4E-14
c1
с2
       6
              5.000E-12
dc
         53
              dx
      54 5d x
de
dlp
      90 91 dx
dln
      92
          90
              dx
dp
       4
              dx
          0 poly(2) (3,0) (4,0) 0 .5 .5
egnd
      99
          99 poly(5) vb vc ve vlp vln 0 4.085E6 -4E6 4E6 4E6 -4E6
0 11 12 201.1E-6
       7
fb
              11 12 201.1E-6
ga
       6
          6 10 99 3.576E-9
gcm
       3 10 dc 45.00E-6
iss
hlim
      90
          0
              vlim 1K
          2 10 jx
j1
      11
          1
      12
              10 jx
j2
r2
       6
           9
              100.0E3
       4 11
              4.973E3
rd1
       4 12
rd2
              4.973E3
ro1
       8
          5
              280
       7
          99
ro2
              280
       3
              113.2E3
rp
      10 99
              4.444E6
rss
vb
       9
           0
              dc 0
          53
       3
              dc 2
VC
ve
      54
           4
              dc 2
vlim
           8
              dc 0
      91
              dc 50
vlp
          0
vln
       0 92 dc 50
.model dx
          D
             (Is=800.0E-18)
.model jx PJF (Is=1.000E-12 Beta=480E-6 Vto=-1)
```

Figure 37. Macromodel Subcircuit



#### **APPLICATION INFORMATION**

#### input characteristics

The TLE2161, TLE2161A and TLE2161B are specified with a minimum and a maximum input voltage that if exceeded at either input could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLE2161, TLE2161A, and TLE2161B are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 38). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

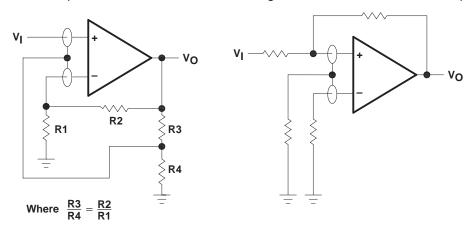


Figure 38. Use of Guard Rings

#### input offset voltage nulling

The TLE2161 series offers external null pins that can further reduce the input offset voltage. The circuit in Figure 39 can be connected as shown if the feature is desired. When external nulling is not needed, the null pins may be left disconnected.

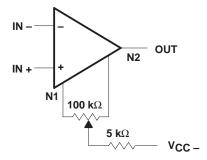


Figure 39. Input Offset Voltage Nulling







17-Dec-2015

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	_	Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	<b>Device Marking</b>	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
5962-9095801QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9095801QPA TLE2161M	Samples
5962-9095802QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9095802QPA TLE2161AM	Samples
5962-9095803QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9095803QPA TLE2161BM	Samples
TLE2161ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2161AC	Samples
TLE2161ACP	OBSOLETE	PDIP	Р	8		TBD	Call TI	Call TI	0 to 70		
TLE2161AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2161AI	Samples
TLE2161AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2161AI	Samples
TLE2161AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2161AI	Samples
TLE2161AIP	OBSOLETE	PDIP	Р	8		TBD	Call TI	Call TI			
TLE2161AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9095802QPA TLE2161AM	Samples
TLE2161BCP	OBSOLETE	PDIP	Р	8		TBD	Call TI	Call TI	0 to 70		
TLE2161BIP	OBSOLETE	PDIP	Р	8		TBD	Call TI	Call TI			
TLE2161BMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9095803QPA TLE2161BM	Samples
TLE2161BMP	OBSOLETE	PDIP	Р	8		TBD	Call TI	Call TI	-55 to 125		
TLE2161CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2161C	Samples
TLE2161CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2161C	Samples
TLE2161CP	OBSOLETE	PDIP	Р	8		TBD	Call TI	Call TI	0 to 70		
TLE2161ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		21611	Samples
TLE2161IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		21611	Samples



#### PACKAGE OPTION ADDENDUM

17-Dec-2015

Orderable Device		Package Type	Package Drawing	Pins	Package Qty		Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TLE2161IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		21611	Samples
TLE2161IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		21611	Samples
TLE2161IP	OBSOLETE	PDIP	Р	8		TBD	Call TI	Call TI			
TLE2161MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9095801QPA TLE2161M	Samples
TLE2161MP	OBSOLETE	PDIP	Р	8		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



#### **PACKAGE OPTION ADDENDUM**

17-Dec-2015

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#### OTHER QUALIFIED VERSIONS OF TLE2161, TLE2161A, TLE2161AM, TLE2161B, TLE2161BM, TLE2161M:

- Catalog: TLE2161A, TLE2161B, TLE2161
- Military: TLE2161M, TLE2161AM, TLE2161BM

NOTE: Qualified Version Definitions:

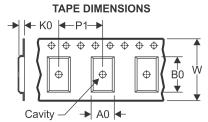
- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

### PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All difficulties are norminal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2161AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2161IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2161IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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\*All dimensions are nominal

7 till dillitoriolorio di o mominar							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2161AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2161IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2161IDR	SOIC	D	8	2500	367.0	367.0	38.0

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