TEXAS INSTRUMENTS

TSB82AA2B

1394b OHCI-Lynx ™ Controller

Data Manual

October 2011 *Connectivity Solutions*

SCPS172A

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1 Introduction

This chapter provides an overview of the Texas Instruments TSB82AA2B device and its features.

1.1 Description

The TSB82AA2B OHCI-Lynx™ controller is a discrete 1394b link-layer device, which has been designed to meet the demanding requirements of today's 1394 bus designs. The TSB82AA2B device is capable of exceptional 800M bit/s performance; thus, providing the throughput and bandwidth to move data efficiently and quickly between the PCI and 1394 buses. The TSB82AA2B device also provides outstanding ultra-low power operation and intelligent power management capabilities. The device provides the IEEE Std 1394 link function and is compatible with 100M bit/s, 200M bit/s, 400M bit/s, and 800M bit/s serial bus data rates.

TSB82AA2B improved throughput and increased bandwidth make it ideal for today's high-end PCs and open the door for the development of S800 RAID- and SAN-based peripherals.

The TSB82AA2B OHCI-Lynx controller operates as the interface between a 33-MHz/64-bit or 33-MHz/32-bit PCI local bus and a compatible 1394b physical layer (PHY) device (such as the TSB81BA3 device) that is capable of supporting serial data rates at 98.304M, 196.608M, 393.216M, or 786.432M bit/s (referred to as S100, S200, S400, or S800 speeds, respectively). When acting as a PCI bus master, the TSB82AA2B device is capable of multiple cacheline bursts of data, which can transfer at 264M bytes/s for 64-bit transfers or 132M bytes/s for 32-bit transfers after connecting to the memory controller.

Due to the high throughput potential of the TSB82AA2B, it possible to encounter large PCI and legacy 1394 bus latencies, which can cause the 1394 data to be overrun. To overcome this potential problem, the TSB82AA2B implements deep transmit and receive FIFOs (see Section 1.2, *Features*, for FIFO size information) to buffer the 1394 data, thus preventing possible problems due to bus latency. This also ensures that the device can transmit and receive sustained maximum size isochronous or asynchronous data payloads at S800.

The TSB82AA2B device implements other performance enhancements to improve overall performance of the device, such as: a highly tuned physical data path for enhanced SBP-2 performance, physical post writing buffers, multiple isochronous contexts, and advanced internal arbitration.

The TSB82AA2B also implements hardware enhancements to better support digital video (DV) and MPEG data stream reception and transmission. These enhancements are enabled through the isochronous receive digital video enhancements register at TI extension offset A80h (see Section 5.4, *Isochronous Receive Digital Video Enhancements Register*). These enhancements include automatic timestamp insertion for transmitted DV and MPEG-formatted streams and common isochronous packet (CIP) header stripping for received DV streams.

The CIP format is defined by the IEC 61883-1:1998 specification. The enhancements to the isochronous data contexts are implemented as hardware support for the synchronization timestamp for both DV and audio/video CIP formats. The TSB82AA2B device supports modification of the synchronization timestamp field to ensure that the value inserted via software is not stale — that is, less than the current cycle timer when the packet is transmitted.

The TSB82AA2B performance and enhanced throughput make it an excellent choice for today's 1394 PC market; however, the portable, mobile, and even today's desktop PCs power management schemes continue to require devices to use less and less power, and the TI 1394 OHCI-Lynx product line has continued to raise the bar by providing the lowest power 1394 link-layers in the industry. The TSB82AA2B represents the next evolution of TI commitment to meet the challenge of power-sensitive applications. The TSB82AA2B has ultra-low operational power requirements and intelligent power management capabilities that allow it to autonomously conserve power based on the device usage.

One of the key elements for reducing the TSB82AA2B operational power requirements is the TI advanced CMOS process and the implementation of an internal 1.8-V core, which is supplied by an improved integrated 3.3-V to 1.8-V voltage regulator. The TSB82AA2B implements a next-generation voltage regulator that is more efficient than its predecessors, thus providing an overall reduction in the device operational power requirements especially when operating in $D3_{cold}$ using auxiliary power. In fact, the TSB82AA2B device fully supports D0, D1, D2, and $D3_{hot/cold}$ power states as specified in the *PC 2001 Design Guide* requirements and the *PCI Power-Management Specification*. PME wake event support is subject to operating system support and implementation.

As required by the *1394 Open Host Controller Interface Specification* (OHCI) and IEEE Std 1394a-2000, internal control registers are memory mapped and nonprefetchable. The PCI configuration header is accessed through configuration cycles as specified by the *PCI Local Bus Specification*, and provides plug-and-play (PnP) compatibility. Furthermore, the TSB82AA2B device is fully compliant with the latest *PCI Local Bus Specification*, *PCI Bus Power-Management Interface Specification*, IEEE Draft Std 1394b, IEEE Std 1394a-2000, and *1394 Open Host Controller Interface Specification* (see Section 1.3, *Related Documents*, for a complete list).

1.2 Features

The TSB82AA2B device supports the following features:

- Single 3.3-V Supply (1.8-V Internal Core Voltage With Regulator)
- Available in Industrial (–40°C to 85°C) and Commercial (0°C to 70°C) Temperature Ranges
- 3.3-V and 5-V PCI Signaling Environments
- Serial Bus Data Rates of 100M bit/s, 200M bit/s, 400M bit/s, and 800M bit/s
- Physical Write Posting of up to Three Outstanding Transactions
- Serial ROM or Boot ROM Interface Supports 2-Wire Serial EEPROM Devices
- 33-MHz/64-Bit and 33-MHz/32-Bit Selectable PCI Interface
- Multifunction Terminal (MFUNC Terminal 1)
  - $\overline{\text{PCI\_CLKRUN}}$ Protocol Per *PCI Mobile Design Guide*
  - General-Purpose I/O (GPIO)
  - CYCLEIN/CYCLEOUT for External Cycle Timer Control for Customized Synchronization
- PCI Burst Transfers and Deep FIFOs to Tolerate Large Host Latency
  - Transmit FIFO — 5K Asynchronous
  - Transmit FIFO — 2K Isochronous
  - Receive FIFO — 2K Asynchronous
  - Receive FIFO — 2K Isochronous
- D0, D1, D2, and D3 Power States and $\overline{\text{PME}}$ Events Per *PCI Bus Power-Management Interface Specification*
- Programmable Asynchronous Transmit Threshold
- Isochronous Receive Dual-Buffer Mode
- Out-of-Order Pipelining for Asynchronous Transmit Requests
- Register Access Fail Interrupt When PHY SYSCLK Is Not Active
- Initial Bandwidth Available and Initial Channels Available Registers
- Digital Video and Audio Performance Enhancements
- Fabricated in Advanced Low-Power CMOS Process
- Packaged in 144-Terminal LQFP (PGE)

1.3 Related Documents

- *1394 Open Host Controller Interface Specification* (Revision 1.2)
- *IEEE Standard for a High-Performance Serial Bus* (IEEE Std 1394-1995)
- *IEEE Standard for a High-Performance Serial Bus — Amendment 1* (IEEE Std 1394a-2000)
- *P1394b Draft Standard for High-Performance Serial Bus* (Supplement)
- *PC 2001 Design Guide*
- *PCI Bus Power-Management Interface Specification* (Revision 1.1)
- *PCI Local Bus Specification* (Revision 2.3)
- *Serial Bus Protocol 2* (SBP−2)
- *Microsoft Windows™ Logo Program System and Device Requirements* (Version 0.5)
- *Microsoft Windows™ Logo Program Desktop and Mobile PC Requirements* (Version 1.1)
- *Digital Interface for Consumer Electronic Audio/Video Equipment Draft* (Version 2.1) (IEC 61883)

1.4 Trademarks

OHCI-Lynx is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

1.5 Ordering Information

ORDERING NUMBER	NAME	PACKAGE	COMMENT
TSB82AA2BPGE	OHCI-Lynx™ PCI-Based IEEE 1394 Host Controller	144-PQFP	Lead-free (Pb-free) device with RoHS
TSB82AA2BIPGE	OHCI-Lynx™ PCI-Based IEEE 1394 Host Controller	144-PQFP	Lead-free (Pb-free) device with RoHS

1.6 TSB82AA2B Data Manual Document History

DATE	REVISION	PAGE	PARAGRAPH	DESCRIPTION
12/2006	Initial release			
9/2008	A	1−3, 8−2		TSB82AA2BI added
10−2011	A	1−2	Features	last item, deleted “0r 176−ball.....package)”
10−2011	A	1−3	Trademarks	deleted “MicroStar BGA and” from first trademark
10−2011	A	9−2		deleted this page

2 Terminal Descriptions

This section provides the terminal descriptions for the TSB82AA2B device. Figure 2–1 and Figure 2–2 show the signal assigned to each terminal in the PGE and GGW packages, respectively. Table 2–1, Table 2–2, and Table 2–3 provide a cross-reference between each terminal number and the name of the signal on that terminal. Table 2–1 is arranged in terminal number order for the PGE package, Table 2–2 is arranged in terminal number order for the GGW package, and Table 2–3 lists the signals in alphanumerical order.

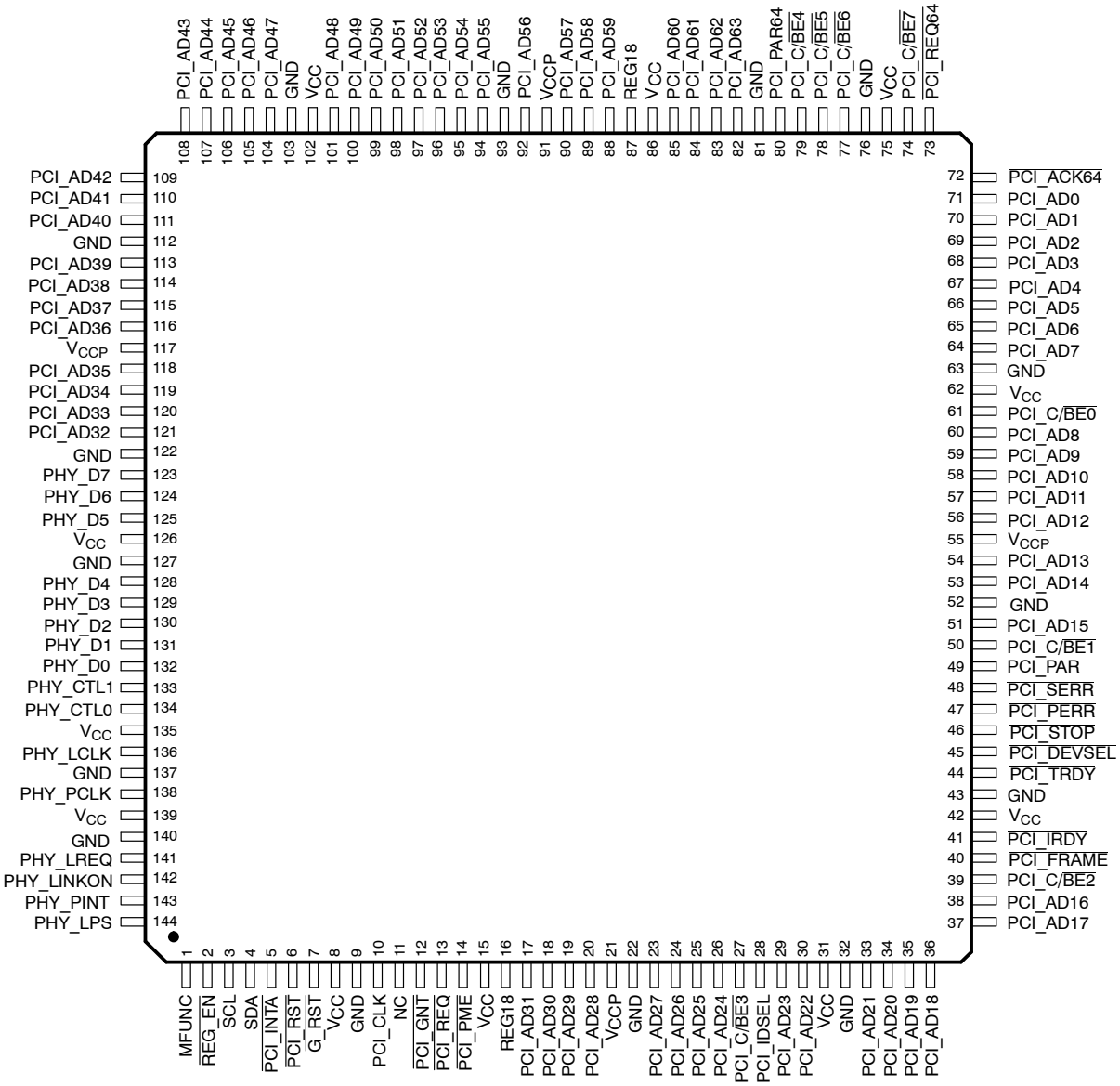


Figure 2–1. PGE Package Terminal Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
U		NC	PCI_AD16	PCI_IRDY	NC	PCI_DEVSEL	PCI_SERR	PCI_PAR	PCI_AD15	VCCP	PCI_AD9	NC	PCI_AD7	PCI_AD4	PCI_AD1	PCI_ACK64	
T	NC		PCI_AD17	PCI_FRAME	NC	PCI_TRDY	PCI_PERR	NC	PCI_AD13	PCI_AD12	PCI_AD8	NC	PCI_AD6	PCI_AD3	PCI_AD0		NC
R	PCI_AD18	NC		PCI_C/BE2	VCC	GND	NC	NC	PCI_AD14	PCI_AD10	PCI_C/BE0	GND	PCI_AD5	PCI_AD2		PCI_REQ64	PCI_C/BE7
P	PCI_AD21	PCI_AD20	PCI_AD19				PCI_STOP	PCI_C/BE1	GND	PCI_AD11	VCC				VCC	NC	NC
N	VCC	NC	GND												GND	PCI_C/BE6	PCI_C/BE5
M	PCI_IDSEL	PCI_AD23	PCI_AD22												PCI_C/BE4	NC	PCI_PAR64
L	PCI_AD26	PCI_AD25	PCI_AD24	PCI_C/BE3										GND	PCI_AD63	PCI_AD62	PCI_AD61
K	VCCP	NC	PCI_AD27	GND										VCC	REG18	PCI_AD59	PCI_AD60
J	PCI_AD30	PCI_AD28	NC	PCI_AD29										PCI_AD57	NC	NC	PCI_AD58
H	PCI_PME	PCI_AD31	REG18	VCC										GND	PCI_AD55	PCI_AD56	VCCP
G	PCI_REQ	PCI_GNT	PCI_CLK	GND										PCI_AD51	PCI_AD52	PCI_AD53	PCI_AD54
F	NC	NC	VCC												PCI_AD48	PCI_AD49	PCI_AD50
E	G_RST	PCI_RST	PCI_INTA												GND	NC	VCC
D	SDA	SCL	REG_EN				VCC	PHY_D0	GND	PHY_D7	PCI_AD35				PCI_AD45	PCI_AD46	PCI_AD47
C	MFUNC	NC		PHY_LINKON	VCC	GND	NC	NC	PHY_D4	PHY_D6	PCI_AD34	PCI_AD37	GND	PCI_AD42		PCI_AD43	PCI_AD44
B	NC		PHY_LPS	PHY_LREQ	NC	NC	PHY_CTL0	PHY_D1	PHY_D3	PHY_D5	PCI_AD33	PCI_AD36	PCI_AD39	PCI_AD41	NC		NC
A		NC	PHY_PINT	GND	PHY_PCLK	PHY_LCLK	PHY_CTL1	PHY_D2	VCC	GND	PCI_AD32	VCCP	PCI_AD38	PCI_AD40	NC	NC	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

Figure 2–2. GGW Package Terminal Diagram

Table 2–1. Signal Names Sorted by PGE Terminal Numbers

NO.	TERMINAL NAME	NO.	TERMINAL NAME	NO.	TERMINAL NAME	NO.	TERMINAL NAME
1	MFUNC	37	PCI_AD17	73	$\overline{\text{PCI\_REQ64}}$	109	PCI_AD42
2	$\overline{\text{REG\_EN}}$	38	PCI_AD16	74	PCI_C/$\overline{\text{BE7}}$	110	PCI_AD41
3	SCL	39	PCI_C/$\overline{\text{BE2}}$	75	V_{CC}	111	PCI_AD40
4	SDA	40	$\overline{\text{PCI\_FRAME}}$	76	GND	112	GND
5	$\overline{\text{PCI\_INTA}}$	41	$\overline{\text{PCI\_IRDY}}$	77	PCI_C/$\overline{\text{BE6}}$	113	PCI_AD39
6	$\overline{\text{PCI\_RST}}$	42	V_{CC}	78	PCI_C/$\overline{\text{BE5}}$	114	PCI_AD38
7	$\overline{\text{G\_RST}}$	43	GND	79	PCI_C/$\overline{\text{BE4}}$	115	PCI_AD37
8	V_{CC}	44	$\overline{\text{PCI\_TRDY}}$	80	PCI_PAR64	116	PCI_AD36
9	GND	45	$\overline{\text{PCI\_DEVSEL}}$	81	GND	117	V_{CCP}
10	PCI_CLK	46	$\overline{\text{PCI\_STOP}}$	82	PCI_AD63	118	PCI_AD35
11	NC	47	$\overline{\text{PCI\_PERR}}$	83	PCI_AD62	119	PCI_AD34
12	$\overline{\text{PCI\_GNT}}$	48	$\overline{\text{PCI\_SERR}}$	84	PCI_AD61	120	PCI_AD33
13	$\overline{\text{PCI\_REQ}}$	49	PCI_PAR	85	PCI_AD60	121	PCI_AD32
14	$\overline{\text{PCI\_PME}}$	50	PCI_C/$\overline{\text{BE1}}$	86	V_{CC}	122	GND
15	V_{CC}	51	PCI_AD15	87	REG18	123	PHY_D7
16	REG18	52	GND	88	PCI_AD59	124	PHY_D6
17	PCI_AD31	53	PCI_AD14	89	PCI_AD58	125	PHY_D5
18	PCI_AD30	54	PCI_AD13	90	PCI_AD57	126	V_{CC}
19	PCI_AD29	55	V_{CCP}	91	V_{CCP}	127	GND
20	PCI_AD28	56	PCI_AD12	92	PCI_AD56	128	PHY_D4
21	V_{CCP}	57	PCI_AD11	93	GND	129	PHY_D3
22	GND	58	PCI_AD10	94	PCI_AD55	130	PHY_D2
23	PCI_AD27	59	PCI_AD9	95	PCI_AD54	131	PHY_D1
24	PCI_AD26	60	PCI_AD8	96	PCI_AD53	132	PHY_D0
25	PCI_AD25	61	PCI_C/$\overline{\text{BE0}}$	97	PCI_AD52	133	PHY_CTL1
26	PCI_AD24	62	V_{CC}	98	PCI_AD51	134	PHY_CTL0
27	PCI_C/$\overline{\text{BE3}}$	63	GND	99	PCI_AD50	135	V_{CC}
28	PCI_IDSEL	64	PCI_AD7	100	PCI_AD49	136	PHY_LCLK
29	PCI_AD23	65	PCI_AD6	101	PCI_AD48	137	GND
30	PCI_AD22	66	PCI_AD5	102	V_{CC}	138	PHY_PCLK
31	V_{CC}	67	PCI_AD4	103	GND	139	V_{CC}
32	GND	68	PCI_AD3	104	PCI_AD47	140	GND
33	PCI_AD21	69	PCI_AD2	105	PCI_AD46	141	PHY_LREQ
34	PCI_AD20	70	PCI_AD1	106	PCI_AD45	142	PHY_LINKON
35	PCI_AD19	71	PCI_AD0	107	PCI_AD44	143	PHY_PINT
36	PCI_AD18	72	$\overline{\text{PCI\_ACK64}}$	108	PCI_AD43	144	PHY_LPS

Table 2–2. Signal Names Sorted by GGW Terminal Numbers

TERMINAL NO.	SIGNAL NAME	TERMINAL NO.	SIGNAL NAME	TERMINAL NO.	SIGNAL NAME	TERMINAL NO.	SIGNAL NAME
A02	NC	C17	PCI_AD44	J14	PCI_AD57	R02	NC
A03	PHY_PINT	D01	SDA	J15	NC	R04	PCI_C/$\overline{BE2}$
A04	GND	D02	SCL	J16	NC	R05	V_{CC}
A05	PHY_PCLK	D03	$\overline{REG\_EN}$	J17	PCI_AD58	R06	GND
A06	PHY_LCLK	D07	V_{CC}	K01	V_{CCP}	R07	NC
A07	PHY_CTL1	D08	PHY_D0	K02	NC	R08	NC
A08	PHY_D2	D09	GND	K03	PCI_AD27	R09	PCI_AD14
A09	V_{CC}	D10	PHY_D7	K04	GND	R10	PCI_AD10
A10	GND	D11	PCI_AD35	K14	V_{CC}	R11	PCI_C/$\overline{BE0}$
A11	PCI_AD32	D15	PCI_AD45	K15	REG18	R12	GND
A12	V_{CCP}	D16	PCI_AD46	K16	PCI_AD59	R13	PCI_AD5
A13	PCI_AD38	D17	PCI_AD47	K17	PCI_AD60	R14	PCI_AD2
A14	PCI_AD40	E01	$\overline{G\_RST}$	L01	PCI_AD26	R16	$\overline{PCI\_REQ64}$
A15	NC	E02	$\overline{PCI\_RST}$	L02	PCI_AD25	R17	PCI_C/$\overline{BE7}$
A16	NC	E03	$\overline{PCI\_INTA}$	L03	PCI_AD24	T01	NC
B01	NC	E15	GND	L04	PCI_C/$\overline{BE3}$	T03	PCI_AD17
B03	PHY_LPS	E16	NC	L14	GND	T04	$\overline{PCI\_FRAME}$
B04	PHY_LREQ	E17	V_{CC}	L15	PCI_AD63	T05	NC
B05	NC	F01	NC	L16	PCI_AD62	T06	$\overline{PCI\_TRDY}$
B06	NC	F02	NC	L17	PCI_AD61	T07	$\overline{PCI\_PERR}$
B07	PHY_CTL0	F03	V_{CC}	M01	PCI_IDSEL	T08	NC
B08	PHY_D1	F15	PCI_AD48	M02	PCI_AD23	T09	PCI_AD13
B09	PHY_D3	F16	PCI_AD49	M03	PCI_AD22	T10	PCI_AD12
B10	PHY_D5	F17	PCI_AD50	M15	PCI_C/$\overline{BE4}$	T11	PCI_AD8
B11	PCI_AD33	G01	$\overline{PCI\_REQ}$	M16	NC	T12	NC
B12	PCI_AD36	G02	$\overline{PCI\_GNT}$	M17	PCI_PAR64	T13	PCI_AD6
B13	PCI_AD39	G03	PCI_CLK	N01	V_{CC}	T14	PCI_AD3
B14	PCI_AD41	G04	GND	N02	NC	T15	PCI_AD0
B15	NC	G14	PCI_AD51	N03	GND	T17	NC
B17	NC	G15	PCI_AD52	N15	GND	U02	NC
C01	MFUNC	G16	PCI_AD53	N16	PCI_C/$\overline{BE6}$	U03	PCI_AD16
C02	NC	G17	PCI_AD54	N17	PCI_C/$\overline{BE5}$	U04	$\overline{PCI\_IRDY}$
C04	PHY_LINKON	H01	$\overline{PCI\_PME}$	P01	PCI_AD21	U05	NC
C05	V_{CC}	H02	PCI_AD31	P02	PCI_AD20	U06	$\overline{PCI\_DEVSEL}$
C06	GND	H03	REG18	P03	PCI_AD19	U07	$\overline{PCI\_SERR}$
C07	NC	H04	V_{CC}	P07	$\overline{PCI\_STOP}$	U08	PCI_PAR
C08	NC	H14	GND	P08	PCI_C/$\overline{BE1}$	U09	PCI_AD15
C09	PHY_D4	H15	PCI_AD55	P09	GND	U10	V_{CCP}
C10	PHY_D6	H16	PCI_AD56	P10	PCI_AD11	U11	PCI_AD9
C11	PCI_AD34	H17	V_{CCP}	P11	V_{CC}	U12	NC
C12	PCI_AD37	J01	PCI_AD30	P15	V_{CC}	U13	PCI_AD7
C13	GND	J02	PCI_AD28	P16	NC	U14	PCI_AD4
C14	PCI_AD42	J03	NC	P17	NC	U15	PCI_AD1
C16	PCI_AD43	J04	PCI_AD29	R01	PCI_AD18	U16	$\overline{PCI\_ACK64}$

Table 2–3. Signal Names Sorted Alphanumerically to Terminal Number

TERMINAL NAME	NUMBER		TERMINAL NAME	NUMBER		TERMINAL NAME	NUMBER	
	PGE	GGW		PGE	GGW		PGE	GGW
GND	9	A04	PCI_AD17	37	T03	PCI_AD53	96	G16
GND	22	A10	PCI_AD18	36	R01	PCI_AD54	95	G17
GND	32	C06	PCI_AD19	35	P03	PCI_AD55	94	H15
GND	43	C13	PCI_AD20	34	P02	PCI_AD56	92	H16
GND	52	D09	PCI_AD21	33	P01	PCI_AD57	90	J14
GND	63	E15	PCI_AD22	30	M03	PCI_AD58	89	J17
GND	76	G04	PCI_AD23	29	M02	PCI_AD59	88	K16
GND	81	H14	PCI_AD24	26	L03	PCI_AD60	85	K17
GND	93	K04	PCI_AD25	25	L02	PCI_AD61	84	L17
GND	103	L14	PCI_AD26	24	L01	PCI_AD62	83	L16
GND	112	N03	PCI_AD27	23	K03	PCI_AD63	82	L15
GND	122	N15	PCI_AD28	20	J02	PCI_CLK	10	G03
GND	127	P09	PCI_AD29	19	J04	PCI_C/$\overline{BE0}$	61	R11
GND	137	R06	PCI_AD30	18	J01	PCI_C/$\overline{BE1}$	50	P08
GND	140	R12	PCI_AD31	17	H02	PCI_C/$\overline{BE2}$	39	R04
$\overline{G\_RST}$	7	E01	PCI_AD32	121	A11	PCI_C/$\overline{BE3}$	27	L04
MFUNC	1	C01	PCI_AD33	120	B11	PCI_C/$\overline{BE4}$	79	M15
NC	11	A02, A15, A16, B01, B05, B06, B15, B17, C02, C07, C08, E16, F01, F02, J03, J15, J16, K02, M16, N02, P16, P17, R02, R07, R08, T01, T05, T08, T12, T17, U02, U05, U12,	PCI_AD34	119	C11	PCI_C/$\overline{BE5}$	78	N17
$\overline{PCI\_ACK64}$	72	U16	PCI_AD35	118	D11	PCI_C/$\overline{BE6}$	77	N16
PCI_AD0	71	T15	PCI_AD36	116	B12	PCI_C/$\overline{BE7}$	74	R17
PCI_AD1	70	U15	PCI_AD37	115	C12	$\overline{PCI\_DEVSEL}$	45	U06
PCI_AD2	69	R14	PCI_AD38	114	A13	$\overline{PCI\_FRAME}$	40	T04
PCI_AD3	68	T14	PCI_AD39	113	B13	$\overline{PCI\_GNT}$	12	G02
PCI_AD4	67	U14	PCI_AD40	111	A14	PCI_IDSEL	28	M01
PCI_AD5	66	R13	PCI_AD41	110	B14	$\overline{PCI\_INTA}$	5	E03
PCI_AD6	65	T13	PCI_AD42	109	C14	$\overline{PCI\_IRDY}$	41	U04
PCI_AD7	64	U13	PCI_AD43	108	C16	PCI_PAR	49	U08
PCI_AD8	60	T11	PCI_AD44	107	C17	PCI_PAR64	80	M17
PCI_AD9	59	U11	PCI_AD45	106	D15	$\overline{PCI\_PERR}$	47	T07
PCI_AD10	58	R10	PCI_AD46	105	D16	$\overline{PCI\_PME}$	14	H01
PCI_AD11	57	P10	PCI_AD47	104	D17	$\overline{PCI\_REQ}$	13	G01
PCI_AD12	56	T10	PCI_AD48	101	F15	$\overline{PCI\_REQ64}$	73	R16
PCI_AD13	54	T09	PCI_AD49	100	F16	$\overline{PCI\_RST}$	6	E02
PCI_AD14	53	R09	PCI_AD50	99	F17	$\overline{PCI\_SERR}$	48	U07
PCI_AD15	51	U09	PCI_AD51	98	G14	$\overline{PCI\_STOP}$	46	P07
PCI_AD16	38	U03	PCI_AD52	97	G15	$\overline{PCI\_TRDY}$	44	T06

Table 2–3. Signal Names Sorted Alphanumerically to Terminal Number (Continued)

TERMINAL NAME	NUMBER		TERMINAL NAME	NUMBER		TERMINAL NAME	NUMBER	
	PGE	GGW		PGE	GGW		PGE	GGW
PHY_CTL0	134	B07	PHY_LPS	144	B03	V_{CC}	42	E17
PHY_CTL1	133	A07	PHY_LREQ	141	B04	V_{CC}	62	F03
PHY_D0	132	D08	PHY_PCLK	138	A05	V_{CC}	75	H04
PHY_D1	131	B08	PHY_PINT	143	A03	V_{CC}	86	K14
PHY_D2	130	A08	$\overline{\text{REG\_EN}}$	2	D03	V_{CC}	102	N01
PHY_D3	129	B09	REG18	16	H03	V_{CC}	126	P11
PHY_D4	128	C09	REG18	87	K15	V_{CC}	135	P15
PHY_D5	125	B10	SCL	3	D02	V_{CC}	139	R05
PHY_D6	124	C10	SDA	4	D01	V_{CCP}	21	A12
PHY_D7	123	D10	V_{CC}	8	A09	V_{CCP}	55	H17
PHY_LCLK	136	A06	V_{CC}	15	C05	V_{CCP}	91	K01
PHY_LINKON	142	C04	V_{CC}	31	D07	V_{CCP}	117	U10

The terminals are grouped in tables by functionality, such as PCI system function and power supply function (see Table 2–4 through Table 2–8). The terminal numbers are also listed for convenient reference.

Table 2–4. Power Supply Terminals

TERMINAL			I/O	DESCRIPTION
NAME	NUMBER			
	PGE	GGW		
GND	9, 22, 32, 43, 52, 63, 76, 81, 93, 103, 112, 122, 127, 137, 140	A04, A10, C06, C13, D09, E15, G04, H14, K04, L14, N03, N15, P09, R06, R12	–	Ground terminals. These terminals must be tied together to the low-impedance circuit board ground plane.
REG18	16 87	H03 K15	–	The REG18 terminals are connected to the internal 1.8-V core voltage. They provide a mechanism to provide local bypass for the internal core voltage or to externally provide the 1.8 V to the core if the internal regulator is disabled.
$\overline{\text{REG\_EN}}$	2	D03	I	Regulator enable. When this terminal is low, the internal regulator is enabled and generates the 1.8-V internal core voltage from the 3.3-V supply voltage. If it is disabled, 1.8 V must be provided to the REG18 terminals for normal operation.
V_{CC}	8, 15, 31, 42, 62, 75, 86, 102, 126, 135, 139	A09, C05, D07, E17, F03, H04, K14, N01, P11, P15, R05	–	3.3-V power supply terminals. A parallel combination of high frequency decoupling capacitors near each terminal is suggested, such as 0.1 μF and 0.001 μF. Lower frequency 10-μF filtering capacitors are also recommended. They must be tied to a low-impedance point on the circuit board.
V_{CCP}	21, 55, 91, 117	A12, H17, K01, U10	–	PCI signaling clamp voltage power input. PCI signals are clamped per the *PCI Local Bus Specification*. In addition, if a 5-V ROM is used, the V_{CCP} terminal must be connected to 5 V.

Table 2–5. Reset and Miscellaneous Terminals

TERMINAL NAME	TERMINAL NO. PGE	TERMINAL NO. GGW	I/O	DESCRIPTION
$\overline{\text{G\_RST}}$	7	E01	I	Global power reset. This reset brings all of the TSB82AA2B internal registers to their default states, including those registers not reset by $\overline{\text{PCI\_RST}}$. When $\overline{\text{G\_RST}}$ is asserted, the device is completely nonfunctional. Additionally, $\overline{\text{G\_RST}}$ must be asserted a minimum of 2 ms after both 3.3 V and 1.8 V are valid at the device. When implementing wake capabilities from the 1394 host controller, it is necessary to implement two resets to the TSB82AA2B device. $\overline{\text{G\_RST}}$ is designed to be a one-time power-on reset, and $\overline{\text{PCI\_RST}}$ must be connected to the PCI bus $\overline{\text{RST}}$.
MFUNC	1	C01	I/O	Multifunction terminal. MFUNC is a multifunction terminal whose function is selected via the multifunction select register: Bits 2–0 Function 000 General-purpose input/output (GPIO) 001 CYCLEIN 010 CYCLEOUT 011 $\overline{\text{PCI\_CLKRUN}}$ 100–111 Reserved
$\overline{\text{PCI\_RST}}$	6	E02	I	PCI reset. When this bus reset is asserted, the TSB82AA2B device places all output buffers in a high-impedance state and resets all internal registers except device power management context and vendor-specific bits initialized by host power-on software. When $\overline{\text{PCI\_RST}}$ is asserted, the device is completely nonfunctional. This terminal must be connected to PCI bus $\overline{\text{RST}}$.
SCL	3	D02	I/O	Serial clock. This terminal provides the SCL serial clock signaling. ROM is implemented: Connect terminal 3 to the SCL terminal on the ROM; the 2.7-kΩ resistor pulls this signal to the ROM V_{CC}. (SDA is implemented as open-drain.) ROM is not implemented. Connect terminal 3 to ground with a 220-Ω resistor.
SDA	4	D01	I/O	Serial data. This terminal provides the SDA serial data signaling. This terminal is sampled at $\overline{\text{G\_RST}}$ to determine if a serial ROM is implemented; thus if no ROM is implemented, this terminal must be connected to ground. ROM is implemented: Connect terminal 4 to the SDA terminal on the ROM; the 2.7-kΩ resistor pulls this signal to the ROM V_{CC}. (SDA is implemented as open-drain.) ROM is not implemented. Connect terminal 4 to ground with a 220-Ω resistor.

Table 2–6. 32-Bit PCI Bus Terminals

TERMINAL NAME	TERMINAL NO. PGE	TERMINAL NO. GGW	I/O	DESCRIPTION
PCI_AD31	17	H02	I/O	PCI address/data bus for the lower DWORD. These signals make up the multiplexed PCI address and data bus for the lower 32 bits on the PCI interface. During the address phase of a PCI cycle, AD31–AD0 contain a 32-bit address or other destination information. During the data phase, AD31–AD0 contain data.
PCI_AD30	18	J01		
PCI_AD29	19	J04		
PCI_AD28	20	J02		
PCI_AD27	23	K03		
PCI_AD26	24	L01		
PCI_AD25	25	L02		
PCI_AD24	26	L03		
PCI_AD23	29	M02		
PCI_AD22	30	M03		
PCI_AD21	33	P01		
PCI_AD20	34	P02		
PCI_AD19	35	P03		
PCI_AD18	36	R01		
PCI_AD17	37	T03		
PCI_AD16	38	U03		
PCI_AD15	51	U09		
PCI_AD14	53	R09		
PCI_AD13	54	T09		
PCI_AD12	56	T10		
PCI_AD11	57	P10		
PCI_AD10	58	R10		
PCI_AD9	59	U11		
PCI_AD8	60	T11		
PCI_AD7	64	U13		
PCI_AD6	65	T13		
PCI_AD5	66	R13		
PCI_AD4	67	U14		
PCI_AD3	68	T14		
PCI_AD2	69	R14		
PCI_AD1	70	U15		
PCI_AD0	71	T15		
PCI_C/$\overline{BE0}$	61	R11	I/O	PCI bus commands and byte enables for lower DWORD. The command and byte enable signals are multiplexed on the same PCI terminals. During the address phase of a bus cycle, PCI_C/$\overline{BE3}$–PCI_C/$\overline{BE0}$ define the bus command. During the data phase, this 4-bit bus is used as a byte enable for the lower 32 bits of data.
PCI_C/$\overline{BE1}$	50	P08		
PCI_C/$\overline{BE2}$	39	R04		
PCI_C/$\overline{BE3}$	27	L04		
PCI_CLK	10	G03	I	PCI bus clock. Provides timing for all transactions on the PCI bus. All PCI signals are sampled at the rising edge of PCI_CLK.
$\overline{PCI\_DEVSEL}$	45	U06	I/O	PCI device select. The TSB82AA2B device asserts this signal to claim a PCI cycle as the target device. As a PCI initiator, the TSB82AA2B device monitors this signal until a target responds. If no target responds before time-out occurs, the TSB82AA2B device terminates the cycle with an initiator abort.
$\overline{PCI\_FRAME}$	40	T04	I/O	PCI cycle frame. This signal is driven by the initiator of a PCI bus cycle. $\overline{PCI\_FRAME}$ is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When $\overline{PCI\_FRAME}$ is deasserted, the PCI bus transaction is in the final data phase.
$\overline{PCI\_GNT}$	12	G02	I	PCI bus grant. This signal is driven by the PCI bus arbiter to grant the TSB82AA2B device access to the PCI bus after the current data transaction has completed. This signal may or may not follow a PCI bus request, depending upon the PCI bus parking algorithm.
PCI_IDSEL	28	M01	I	Initialization device select. PCI_IDSEL selects the TSB82AA2B device during configuration space accesses. PCI_IDSEL can be connected to 1 of the upper 24 PCI address lines on the PCI bus.
$\overline{PCI\_INTA}$	5	E03	O	Interrupt signal. This output indicates interrupts from the TSB82AA2B device to the host. This terminal is implemented as open-drain.

Table 2–6. 32-Bit PCI Bus Terminals (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PGE	GGW		
PCI_IRDY	41	U04	I/O	PCI initiator ready. PCI_IRDY indicates the ability of the PCI bus initiator to complete the current data phase of the transaction. A data phase is completed upon a rising edge of PCI_CLK where both PCI_IRDY and PCI_TRDY are asserted.
PCI_PAR	49	U08	I/O	PCI parity. In all PCI bus read and write cycles, the TSB82AA2B device calculates even parity across the PCI_AD31–PCI_AD0 and PCI_C/BE0–PCI_C/BE3 buses. As an initiator during PCI cycles, the TSB82AA2B device outputs this parity indicator with a one-PCI_CLK delay. As a target during PCI cycles, the calculated parity is compared to the initiator parity indicator; a miscompare can result in a parity error assertion (PCI_PERR).
PCI_PERR	47	T07	I/O	PCI parity error indicator. This signal is driven by a PCI device to indicate that calculated parity does not match PCI_PAR and/or PCI_PAR64 when PERR_ENB (bit 6) is set to 1 in the command register at offset 04h in the PCI configuration space (see Section 3.4, *Command Register*).
PCI_PME	14	H01	O	This terminal indicates wake events to the host. It is an open-drain signal which is asserted when PME_STS is asserted and bit 8 (PME_ENB) in the PCI power management control and status register at offset 48h in the PCI configuration space (see Section 3.20, *Power Management Control and Status Register*) has been set. Bit 15 (PME_STS) in the PCI power management control and status register is set due to any unmasked interrupt in the D0 (active) or D1 power state, and on a PHY_LINKON indication in the D2, D3, or D0 (uninitialized) power state.
PCI_REQ	13	G01	O	PCI bus request. Asserted by the TSB82AA2B device to request access to the bus as an initiator. The host arbiter asserts PCI_GNT when the TSB82AA2B device has been granted access to the bus.
PCI_SERR	48	U07	O	PCI system error. When SERR_ENB (bit 8) in the command register at offset 04h in the PCI configuration space (see Section 3.4, *Command Register*) is set to 1, the output is pulsed, indicating an address parity error has occurred. The TSB82AA2B device need not be the target of the PCI cycle to assert this signal. This terminal is implemented as open-drain.
PCI_STOP	46	P07	I/O	PCI cycle stop signal. This signal is driven by a PCI target to request the initiator to stop the current PCI bus transaction. This signal is used for target disconnects, and is commonly asserted by target devices which do not support burst data transfers.
PCI_TRDY	44	T06	I/O	PCI target ready. PCI_TRDY indicates the ability of the PCI bus target to complete the current data phase of the transaction. A data phase is completed upon a rising edge of PCI_CLK where both PCI_IRDY and PCI_TRDY are asserted.

Table 2–7. PCI 64-Bit Bus Extension Terminals

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PGE	GGW		
PCI_ACK64	72	U16	I	PCI bus 64-bit transfer acknowledge. Asserted by a target if it is willing to accept a 64-bit data transfer when it positively decodes its address for a memory transaction and the master has requested a 64-bit data transfer by asserting PCI_REQ64. PCI_REQ64 has identical timing to PCI_DEVSEL. When the TSB82AA2B device is bus master, it monitors PCI_REQ64 when it has requested a 64-bit data transfer for the current transaction. If the target asserts PCI_REQ64 when it claims the cycle, the TSB82AA2B device transfers data using 64 bits. As a target, the TSB82AA2B does not support 64-bit data transfers and never asserts PCI_REQ64 when another master has requested 64-bit transfer.
PCI_AD63	82	L15	I/O	PCI address/data bus for the upper DWORD. These signals make up the multiplexed PCI address and data bus for the upper 32 bits of the PCI interface. During the address phase of a dual address command with PCI_REQ64 asserted, AD63–AD32 contain the upper 32 bits of a 64-bit address. During the data phase, AD63–AD32 contain data when a 64-bit transfer has been negotiated by the assertion of PCI_REQ64 by the master and PCI_ACK64 by the target. Note, the TSB82AA2B does not support the dual address command.
PCI_AD62	83	L16		
PCI_AD61	84	L17		
PCI_AD60	85	K17		
PCI_AD59	88	K16		
PCI_AD58	89	J17		
PCI_AD57	90	J14		
PCI_AD56	92	H16		
PCI_AD55	94	H15		
PCI_AD54	95	G17		
PCI_AD53	96	G16		
PCI_AD52	97	G15		
PCI_AD51	98	G14		
PCI_AD50	99	F17		
PCI_AD49	100	F16		
PCI_AD48	101	F15		
PCI_AD47	104	D17		
PCI_AD46	105	D16		
PCI_AD45	106	D15		
PCI_AD44	107	C17		
PCI_AD43	108	C16		
PCI_AD42	109	C14		
PCI_AD41	110	B14		
PCI_AD40	111	A14		
PCI_AD39	113	B13		
PCI_AD38	114	A13		
PCI_AD37	115	C12		
PCI_AD36	116	B12		
PCI_AD35	118	D11		
PCI_AD34	119	C11		
PCI_AD33	120	B11		
PCI_AD32	121	A11		
PCI_C/BE7	74	R17	I/O	PCI bus commands and byte enables for the upper DWORD. During the address phase of a bus cycle, PCI_C/BE7–PCI_C/BE4 are reserved and indeterminate since the TSB82AA2B does not support the dual address command. During the data phase, this 4-bit bus is used as a byte enable for the upper 32 bits when a 64-bit transfer has been negotiated by the assertion of PCI_REQ64 by the master and PCI_ACK64 by the target.
PCI_C/BE6	77	N16		
PCI_C/BE5	78	N17		
PCI_C/BE4	79	M15		
PCI_PAR64	80	M17	I	PCI parity for the upper DWORD. In all PCI bus read and write cycles, the TSB82AA2B device calculates even parity across the PCI_AD63–PCI_AD32 and PCI_C/BE4–PCI_C/BE7 buses. As an initiator during PCI cycles, the TSB82AA2B device outputs this parity indicator with a one-PCI_CLK delay. As a target during PCI cycles, the calculated parity is compared to the initiator parity indicator; a miscompare can result in a parity error assertion (PCI_PERR).
PCI_REQ64	73	R16	I	PCI bus request for 64-bit transfer. Asserted by a bus master to request a 64-bit transfer for a memory transaction. The timing of PCI_REQ64 is identical to PCI_FRAME. When the TSB82AA2B device is the bus master, it asserts PCI_REQ64 to request a 64-bit transfer on the current transaction. The TSB82AA2B device only requests a 64-bit transfer for a memory transaction. The target asserts PCI_ACK64 if it is willing to transfer data using 64 bits.

Table 2–8. PHY-Link Interface Terminals

TERMINAL			I/O	DESCRIPTION
NAME	NUMBER			
	PGE	GGW		
PHY_CTL1 PHY_CTL0	133 134	A07 B07	I/O	PHY-link interface control. These bidirectional control bus signals indicate the phase of operation of the PHY-link interface. Upon a reset of the interface, this bus is driven by the PHY. When driven by the PHY, information on PHY_CTL0 and PHY_CTL1 is synchronous to PHY_PCLK. When driven by the link, information on PHY_CTL0 and PHY_CTL1 is synchronous to PHY_LCLK.
PHY_D7 PHY_D6 PHY_D5 PHY_D4 PHY_D3 PHY_D2 PHY_D1 PHY_D0	123 124 125 128 129 130 131 132	D10 C10 B10 C09 B09 A08 B08 D08	I/O	PHY-link interface data. These bidirectional data bus signals carry 1394 packet data, packet speed, and grant type information between the PHY and the link. Upon a reset of the interface, this bus is driven by the PHY. When driven by the PHY, information on PHY_D7 through PHY_D0 is synchronous to PHY_PCLK. When driven by the link, information on PHY_D7 through PHY_D0 is synchronous to PHY_LCLK.
PHY_LINKON	142	C04	I/O	Link-on notification. PHY_LINKON is an input to the TSB82AA2B device from the PHY that is used to provide notification that a link-on packet has been received, or, if the PHY is configured properly, an event such as a port connection has occurred. This input only has meaning when LPS is disabled. This includes the D0 (uninitialized), D2, and D3 power states. If PHY_LINKON becomes active in the D0 (uninitialized), D2, or D3 power state, the TSB82AA2B device sets bit 15 (PME_STS) in the power management control and status register in the PCI configuration space at offset 48h (see Section 3.20, *Power Management Control and Status Register*).
PHY_LPS	144	B03	I/O	Link power status. PHY_LPS is an output from the TSB82AA2B device that, when active, indicates that the link is powered and capable of maintaining communications over the PHY-link interface. When this signal is inactive, it indicates that the link is not powered or that the link has not been initialized by software. This signal is active when bit 19 (LPS) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) has been set by software according to the initialization as specified in the *1394 Open Host Controller Interface* specification. When active, the signal is nominally a 2-MHz pulse.
PHY_LREQ	141	B04	O	Link request. PHY_LREQ is a serial output from the TSB82AA2B device to the PHY used to request packet transmissions, read and write PHY registers, and to indicate the occurrence of certain link events that are relevant to the PHY. Information encoded on PHY_LREQ is synchronous to PHY_LCLK.
PHY_LCLK	136	A06	O	Link clock. PHY_LCLK is an output from the TSB82AA2B device that is generated from the incoming PHY_PCLK signal. PHY_LCLK is freqency-locked to PHY_PCLK and synchronizes data and information generated by the link.
PHY_PCLK	138	A05	I	PHY clock. PHY_PCLK is an input to the TSB82AA2B device from the PHY that, when active, provides a nominal 98.304-MHz clock with a nominal 50% duty cycle.
PHY_PINT	143	A03	I	PHY interrupt. PHY_PINT is a serial input to the TSB82AA2B device from the PHY that is used to transfer status, register, interrupt, and other information to the link. Information encoded on PHY_PINT is synchronous to PHY_PCLK.

3 TSB82AA2B Controller Programming Model

This section describes the internal PCI configuration registers used to program the TSB82AA2B device. All registers are detailed in the same format – a brief description for each register, followed by the register offset and a bit table describing the reset state for each register.

A bit description table, typically included when the register contains bits of more than one type or purpose, indicates bit field names, field access tags that appear in the *type* column, and a detailed field description. Table 3–1 describes the field access tags.

Table 3–1. Bit Field Access Tag Descriptions

ACCESS TAG	NAME	MEANING
R	Read	Field can be read by software.
W	Write	Field can be written by software to any value.
S	Set	Field can be set by a write of 1. Writes of 0 have no effect.
C	Clear	Field can be cleared by a write of 1. Writes of 0 have no effect.
U	Update	Field can be autonomously updated by the TSB82AA2B device.

Figure 3–1 shows a simplified block diagram of the TSB82AA2B device.

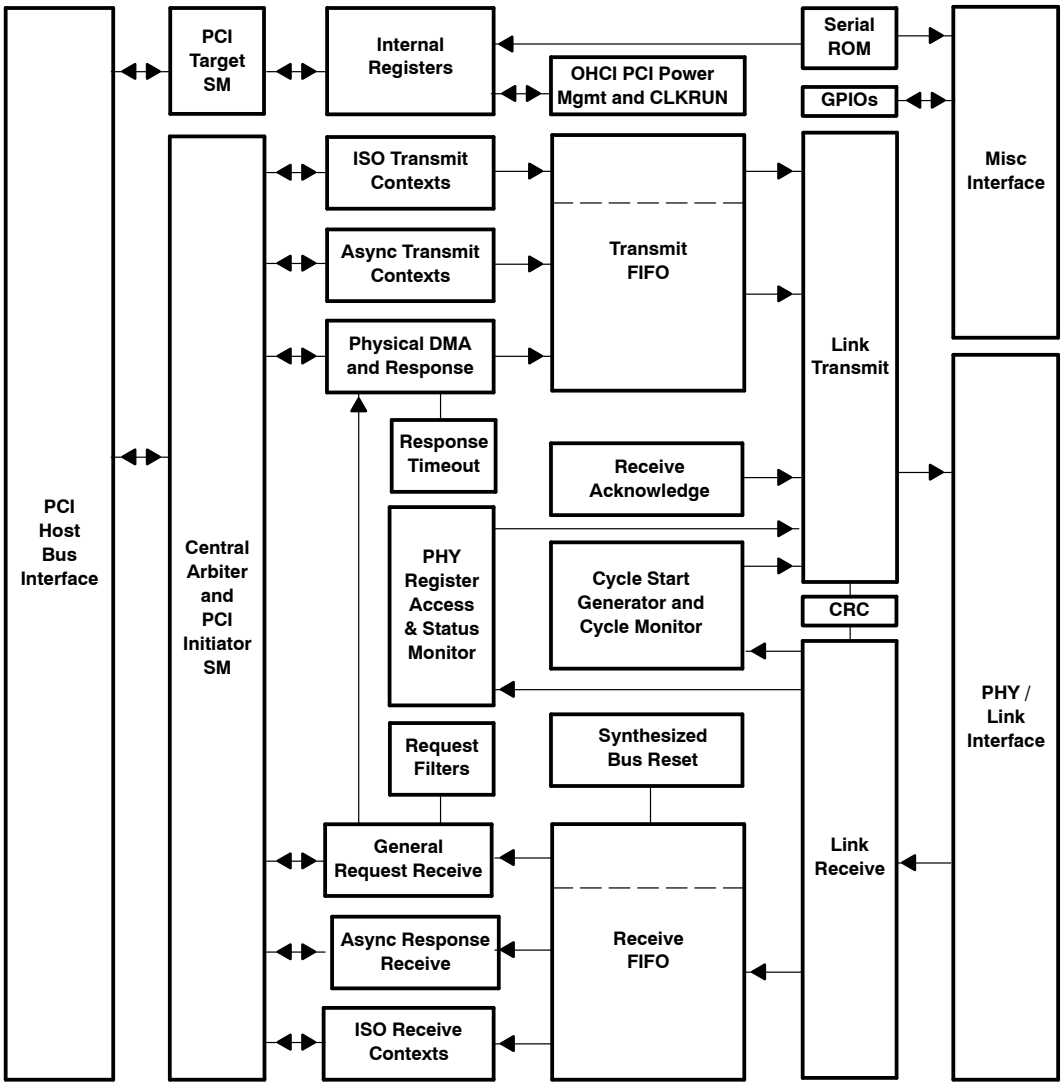


Figure 3–1. TSB82AA2B Block Diagram

3.1 PCI Configuration Registers

The TSB82AA2B device is a single-function PCI device. The configuration header is compliant with the *PCI Local Bus Specification* as a standard header. Table 3–2 illustrates the PCI configuration header that includes both the predefined portion of the configuration space and the user-definable registers.

Table 3–2. PCI Configuration Register Map

REGISTER NAME				OFFSET
Device ID		Vendor ID		00h
Status		Command		04h
Class code			Revision ID	08h
BIST	Header type	Latency timer	Cache line size	0Ch
OHCI base address				10h
TI extension base address				14h
CardBus CIS base address				18h
Reserved				1Ch–27h
CardBus CIS pointer				28h
Subsystem ID		Subsystem vendor ID		2Ch
Reserved				30h
Reserved			Power management capabilities pointer	34h
Reserved				38h
Maximum latency	Minimum grant	Interrupt pin	Interrupt line	3Ch
OHCI control				40h
Power management capabilities		Next item pointer	Capability ID	44h
Multifunction select	Power management extension	Power management control and status		48h
Reserved				4Ch–ECh
Miscellaneous configuration				F0h
Link enhancement control				F4h
Subsystem device ID alias		Subsystem vendor ID alias		F8h
GPI control		Reserved		FCh

3.2 Vendor ID Register

The vendor ID register contains a value allocated by the PCI SIG and identifies the manufacturer of the PCI device. The vendor ID assigned to TI is 104Ch.

Type: Read only
Offset: 00h
Default: 104Ch

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

3.3 Device ID Register

The device ID register contains a value assigned to the TSB82AA2B device by TI. The device ID for the TSB82AA2B device is 8025h.

Type: Read only
Offset: 02h
Default: 8025h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1

3.4 Command Register

The command register provides control over the TSB82AA2B interface to the PCI bus. All bit functions adhere to the definitions in the *PCI Local Bus Specification*, as seen in the following bit descriptions. See Table 3–3 for a complete description of the register contents.

Type: Read/Write, Read only
Offset: 04h
Default: 0000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–3. Command Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–11	RSVD	R	Reserved. Bits 15–11 return 0s when read.
10	INT_DISABLE	R/W	$\overline{\text{INTx}}$ disable. When set to 1, this bit disables the function from asserting interrupts on the $\overline{\text{INTx}}$ signals. 0 = $\overline{\text{INTx}}$ assertion is enabled (default). 1 = $\overline{\text{INTx}}$ assertion is disabled. This bit has been defined as part of the *PCI Local Bus Specification* (Revision 2.3).
9	FBB_ENB	R	Fast back-to-back enable. The TSB82AA2B device does not generate fast back-to-back transactions; therefore, bit 9 returns 0 when read.
8	SERR_ENB	R/W	$\overline{\text{PCI\_SERR}}$ enable. When bit 8 is set to 1, the TSB82AA2B $\overline{\text{PCI\_SERR}}$ driver is enabled. $\overline{\text{PCI\_SERR}}$ can be asserted after detecting an address parity error on the PCI bus.
7	STEP_ENB	R	Address/data stepping control. The TSB82AA2B device does not support address/data stepping; therefore, bit 7 is hardwired to 0.
6	PERR_ENB	R/W	Parity error enable. When bit 6 is set to 1, the TSB82AA2B device is enabled to drive $\overline{\text{PCI\_PERR}}$ response to parity errors through the $\overline{\text{PCI\_PERR}}$ signal.
5	VGA_ENB	R	VGA palette snoop enable. The TSB82AA2B device does not feature VGA palette snooping; therefore, bit 5 returns 0 when read.
4	MWI_ENB	R/W	Memory write and invalidate enable. When bit 4 is set to 1, the TSB82AA2B device is enabled to generate MWI PCI bus commands. If this bit is cleared, the TSB82AA2B device generates memory write commands instead.
3	SPECIAL	R	Special cycle enable. The TSB82AA2B function does not respond to special cycle transactions; therefore, bit 3 returns 0 when read.
2	MASTER_ENB	R/W	Bus master enable. When bit 2 is set to 1, the TSB82AA2B device is enabled to initiate cycles on the PCI bus.
1	MEMORY_ENB	R/W	Memory response enable. Setting bit 1 to 1 enables the TSB82AA2B device to respond to memory cycles on the PCI bus. This bit must be set to access OHCI registers.
0	IO_ENB	R	I/O space enable. The TSB82AA2B device does not implement any I/O-mapped functionality; therefore, bit 0 returns 0 when read.

3.5 Status Register

The status register provides status over the TSB82AA2B interface to the PCI bus. All bit functions adhere to the definitions in the *PCI Local Bus Specification*. See Table 3–4 for a complete description of the register contents.

Type: Read/Clear/Update, Read only
Offset: 06h
Default: 0210h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0

Table 3–4. Status Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. Bit 15 is set to 1 when either an address parity or data parity error is detected.
14	SYS_ERR	RCU	Signaled system error. Bit 14 is set to 1 when $\overline{\text{PCI\_SERR}}$ is enabled and the TSB82AA2B device has signaled a system error to the host.
13	MABORT	RCU	Received master abort. Bit 13 is set to 1 when a cycle initiated by the TSB82AA2B device on the PCI bus is terminated by a master abort.
12	TABORT_REC	RCU	Received target abort. Bit 12 is set to 1 when a cycle initiated by the TSB82AA2B device on the PCI bus is terminated by a target abort.
11	TABORT_SIG	RCU	Signaled target abort. Bit 11 is set to 1 by the TSB82AA2B device when it terminates a transaction on the PCI bus with a target abort.
10–9	PCI_SPEED	R	DEVSEL timing. Bits 10 and 9 encode the timing of $\overline{\text{PCI\_DEVSEL}}$ and are hardwired to 01b, indicating that the TSB82AA2B device asserts this signal at a medium speed on nonconfiguration cycle accesses.
8	DATAPAR	RCU	Data parity error detected. Bit 8 is set to 1 when the following conditions have been met: a. $\overline{\text{PCI\_PERR}}$ was asserted by any PCI device including the TSB82AA2B device. b. The TSB82AA2B device was the bus master during the data parity error. c. Bit 6 (PERR_ENB) in the command register at offset 04h in the PCI configuration space (see Section 3.4, *Command Register*) is set to 1.
7	FBB_CAP	R	Fast back-to-back capable. The TSB82AA2B device cannot accept fast back-to-back transactions; therefore, bit 7 is hardwired to 0.
6	UDF	R	User-definable features (UDF) supported. The TSB82AA2B device does not support the UDF; therefore, bit 6 is hardwired to 0.
5	66MHZ	R	66-MHz capable. The TSB82AA2B device operates at a maximum PCI_CLK frequency of 33 MHz; therefore, bit 5 is hardwired to 0.
4	CAPLIST	R	Capabilities list. Bit 4 returns 1 when read, indicating that capabilities additional to standard PCI are implemented. The linked list of PCI power-management capabilities is implemented in this function.
3	INT_STATUS	RU	Interrupt status. This bit reflects the interrupt status of the function. Only when bit 10 (INT_DISABLE) in the command register (PCI offset 04h, see Section 3.4) is a 0 and this bit is a 1 is the function's $\overline{\text{INTx}}$ signal asserted. Setting the INT_DISABLE bit to a 1 has no effect on the state of this bit. This bit has been defined as part of the *PCI Local Bus Specification* (Revision 2.3).
2–0	RSVD	R	Reserved. Bits 2–0 return 0s when read.

3.6 Class Code and Revision ID Register

The class code and revision ID register categorizes the TSB82AA2B device as a serial bus controller (0Ch), controlling an IEEE Std 1394 bus (00h), with an OHCI programming model (10h). Furthermore, the TI chip revision is indicated in the least significant byte. See Table 3–5 for a complete description of the register contents.

Type: Read only
Offset: 08h
Default: 0C00 1001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0

Table 3–5. Class Code and Revision ID Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–24	BASECLASS	R	Base class. This field returns 0Ch when read, which broadly classifies the function as a serial bus controller.
23–16	SUBCLASS	R	Subclass. This field returns 00h when read, which specifically classifies the function as controlling an IEEE Std 1394 serial bus.
15–8	PGMIF	R	Programming interface. This field returns 10h when read, which indicates that the programming model is compliant with the *1394 Open Host Controller Interface Specification*.
7–0	CHIPREV	R	Silicon revision. This field returns 10h when read, indicating the silicon revision of the TSB82AA2B device.

3.7 Latency Timer and Class Cache Line Size Register

The latency timer and class cache line size register is programmed by host BIOS to indicate system cache line size and the latency timer associated with the TSB82AA2B device. See Table 3–6 for a complete description of the register contents.

Type: Read/Write
Offset: 0Ch
Default: 0000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–6. Latency Timer and Class Cache Line Size Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	LATENCY_TIMER	R/W	PCI latency timer. The value in this register specifies the latency timer for the TSB82AA2B device, in units of PCI clock cycles. When the TSB82AA2B device is a PCI bus initiator and asserts $\overline{\text{PCI\_FRAME}}$, the latency timer begins counting from zero. If the latency timer expires before the TSB82AA2B transaction has terminated, the TSB82AA2B device terminates the transaction when its $\overline{\text{PCI\_GNT}}$ is deasserted.
7–0	CACHELINE_SZ	R/W	Cache line size. This value is used by the TSB82AA2B device during memory write and invalidate, memory-read line, and memory-read multiple transactions.

3.8 Header Type and BIST Registers

The header type and built-in self-test (BIST) registers indicate the TSB82AA2B PCI header type, and indicate no built-in self test. See Table 3–7 for a complete description of the register contents.

Type: Read only
Offset: 0Eh
Default: 0000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–7. Header Type and BIST Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	BIST	R	Built-in self test. The TSB82AA2B device does not include a BIST; therefore, this field returns 00h when read.
7–0	HEADER_TYPE	R	PCI header type. The TSB82AA2B device includes the standard PCI header, which is communicated by returning 00h when this field is read.

3.9 OHCI Base Address Register

The OHCI base address register is programmed with a base address referencing the memory-mapped OHCI control. When BIOS writes all 1s to this register, the value read back is FFFF F800h, indicating that at least 2K bytes of memory address space are required for the OHCI registers. See Table 3–8 for a complete description of the register contents.

Type: Read/Write, Read only
Offset: 10h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–8. OHCI Base Address Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–11	OHCIREG_PTR	R/W	OHCI register pointer. This field specifies the upper 21 bits of the 32-bit OHCI base address register.
10–4	OHCI_SZ	R	OHCI register size. This field returns 0s when read, indicating that the OHCI registers require a 2K-byte region of memory.
3	OHCI_PF	R	OHCI register prefetch. Bit 3 returns 0 when read, indicating that the OHCI registers are nonprefetchable.
2–1	OHCI_MEMTYPE	R	OHCI memory type. This field returns 0s when read, indicating that the OHCI base address register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
0	OHCI_MEM	R	OHCI memory indicator. Bit 0 returns 0 when read, indicating that the OHCI registers are mapped into system memory space.

3.10 TI Extension Base Address Register

The TI extension base address register is programmed with a base address referencing the memory-mapped TI extension registers. When BIOS writes all 1s to this register, the value read back is FFFF F800h, indicating that at least 2K bytes of memory address space are required for the TI registers. See Table 3–9 for a complete description of the register contents.

Type: Read/Write, Read only
Offset: 14h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–9. TI Base Address Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–11	TIREG_PTR	R/W	TI register pointer. This field specifies the upper 21 bits of the 32-bit TI base address register.
10–4	TI_SZ	R	TI register size. This field returns 0s when read, indicating that the TI registers require a 2K-byte region of memory.
3	TI_PF	R	TI register prefetch. Bit 3 returns 0 when read, indicating that the TI registers are nonprefetchable.
2–1	TI_MEMTYPE	R	TI memory type. This field returns 0s when read, indicating that the TI base address register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
0	TI_MEM	R	TI memory indicator. Bit 0 returns 0 when read, indicating that the TI registers are mapped into system memory space.

3.11 CardBus CIS Base Address Register

The TSB82AA2B device may be configured to support CardBus registers via bit 6 (CARDBUS) in the PCI miscellaneous configuration register at offset F0h in the PCI configuration space (see Section 3.23, *Miscellaneous Configuration Register*). If CARDBUS is low (default), this 32-bit register returns 0s when read. If CARDBUS is high, this register is to be programmed with a base address referencing the memory-mapped card information structure (CIS). This register must be programmed with a nonzero value before the CIS may be accessed. See Table 3–10 for a complete description of the register contents.

Type: Read/Write, Read only
Offset: 18h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–10. CardBus CIS Base Address Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–11	CIS_BASE	R/W	CIS base address. This field specifies the upper 21 bits of the 32-bit CIS base address. If $\overline{\text{CARDBUS}}$ is sampled high on a $\overline{\text{G\_RST}}$, this field is read-only, returning 0s when read.
10–4	CIS_SZ	R	CIS address space size. This field returns 0s when read, indicating that the CIS space requires a 2K-byte region of memory.
3	CIS_PF	R	CIS prefetch. Bit 3 returns 0 when read, indicating that the CIS is nonprefetchable. Furthermore, the CIS is a byte-accessible address space, and either a doubleword or 16-bit word access yields indeterminate results.
2–1	CIS_MEMTYPE	R	CIS memory type. This field returns 0s when read, indicating that the CardBus CIS base address register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
0	CIS_MEM	R	CIS memory indicator. This bit returns 0 when read, indicating that the CIS is mapped into system memory space.

3.12 CardBus CIS Pointer Register

The TSB82AA2B device may be configured to support CardBus registers via bit 6 (CARDBUS) in the PCI miscellaneous configuration register at offset F0h in the PCI configuration space (see Section 3.23, *Miscellaneous Configuration Register*). If CARDBUS is low (default), this register is read-only returning 0s when read. If CARDBUS is high, this register contains the pointer to the CardBus card information structure (CIS). See Table 3–11 for a complete description of the register contents.

Type: Read only
Offset: 28h
Default: 0000 000Xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X

Table 3–11. CardBus CIS Pointer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–28	ROM_IMAGE	R	Since the CIS is not implemented as a ROM image, this field returns 0s when read.
27–3	CIS_OFFSET	R	This field indicates the offset into the CIS address space where the CIS begins, and bits 7–3 are loaded from the serial EEPROM field CIS_Offset (7–3). This implementation allows the TSB82AA2B device to produce serial EEPROM addresses equal to the lower PCI address byte to acquire data from the serial EEPROM.
2–0	CIS_INDICATOR	R	This field indicates the address space where the CIS resides and returns 011b if bit 6 (CARDBUS) in the PCI miscellaneous configuration register is high, 011b indicates that CardBus CIS base address register at offset 18h in the PCI configuration header contains the CIS base address. If CARDBUS is low, this field returns 000b when read.

3.13 Subsystem ID Registers

The subsystem ID registers are used for system and option card identification purposes. These registers can be initialized from the serial EEPROM or programmed via the subsystem access register at offset F8h in the PCI configuration space (see Section 3.25, *Subsystem Access Register*). See Table 3–12 for a complete description of register contents.

Type: Read/Update
Offset: 2Ch
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–12. Subsystem ID Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	OHCI_SSID	RU	Subsystem device ID. This field indicates the subsystem device ID.
15–0	OHCI_SSVID	RU	Subsystem vendor ID. This field indicates the subsystem vendor ID.

3.14 Power Management Capabilities Pointer Register

The power management capabilities pointer register provides a pointer into the PCI configuration header where the power-management register block resides. The TSB82AA2B configuration header doublewords at offsets 44h and 48h provide the power management registers. This register is read only and returns 44h when read.

Type: Read only
Offset: 34h
Default: 44h

Bit	7	6	5	4	3	2	1	0
Default	0	1	0	0	0	1	0	0

3.15 Interrupt Line and Interrupt Pin Registers

The interrupt line and interrupt pin registers communicate interrupt line routing information. See Table 3–13 for a complete description of the register contents.

Type: Read/Write, Read only
Offset: 3Ch
Default: 0100h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Table 3–13. Interrupt Line and Interrupt Pin Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	INTR_PIN	R	Interrupt pin. Returns 01h when read, indicating that the TSB82AA2B PCI function signals interrupts on the $\overline{\text{PCI\_INTA}}$ terminal.
7–0	INTR_LINE	R/W	Interrupt line. This field is programmed by the system and indicates to software which interrupt line the TSB82AA2B $\overline{\text{PCI\_INTA}}$ is connected to.

3.16 Minimum Grant and Maximum Latency Registers

The minimum grant and maximum latency registers communicate to the system the desired setting of bits 15–8 in the latency timer and class cache line size register at offset 0Ch in the PCI configuration space (see Section 3.7, *Latency Timer and Class Cache Line Size Register*). If a serial EEPROM is detected, the contents of these registers are loaded through the serial EEPROM interface after a $\overline{\text{PCI\_RST}}$. If no serial EEPROM is detected, these registers return a default value that corresponds to the MIN_GNT = 2, MAX_LAT = 4. See Table 3–14 for a complete description of the register contents.

Type: Read/Update
Offset: 3Eh
Default: 0402h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Table 3–14. Minimum Grant and Maximum Latency Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	MAX_LAT	RU	Maximum latency. The contents of this field may be used by host BIOS to assign an arbitration priority level to the TSB82AA2B device. The default for this field indicates that the TSB82AA2B device may need to access the PCI bus as often as every 0.25 μs; thus, an extremely high priority level is requested. The contents of this field may also be loaded through the serial EEPROM.
7–0	MIN_GNT	RU	Minimum grant. The contents of this field may be used by host BIOS to assign a latency timer register value to the TSB82AA2B device. The default for this field indicates that the TSB82AA2B device may need to sustain burst transfers for nearly 64 μs and, thus, request a large value be programmed in bits 15–8 of the TSB82AA2B latency timer and class cache line size register at offset 0Ch in the PCI configuration space (see Section 3.7, *Latency Timer and Class Cache Line Size Register*).

3.17 OHCI Control Register

The OHCI control register is defined by the *1394 Open Host Controller Interface Specification* and provides a bit for big endian PCI support. See Table 3–15 for a complete description of the register contents.

Type: Read/Write
Offset: 40h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–15. OHCI Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–1	RSVD	R	Reserved. Bits 31–1 return 0s when read.
0	GLOBAL_SWAP	R/W	When bit 0 is set to 1, all quadlets read from and written to the PCI interface are byte swapped (big endian). This bit is loaded from serial EEPROM and must be cleared to 0 for normal operation.

3.18 Capability ID and Next Item Pointer Register

The capability ID and next item pointer register identifies the linked-list capability item and provides a pointer to the next capability item, respectively. See Table 3–16 for a complete description of the register contents.

Type: Read only
Offset: 44h
Default: 0001h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 3–16. Capability ID and Next Item Pointer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	NEXT_ITEM	R	Next item pointer. The TSB82AA2B device supports only one additional capability that is communicated to the system through the extended capabilities list; therefore, this field returns 00h when read.
7–0	CAPABILITY_ID	R	Capability identification. This field returns 01h when read, which is the unique ID assigned by the PCI SIG for PCI power-management capability.

3.19 Power Management Capabilities Register

The power management capabilities register indicates the capabilities of the TSB82AA2B device related to PCI power management. See Table 3–17 for a complete description of the register contents.

Type: Read/Update, Read only
Offset: 46h
Default: 7E02h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0

Table 3–17. Power Management Capabilities Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PME_D3COLD	RU	$\overline{\text{PCI\_PME}}$ support from $D3_{cold}$. This bit can be set to 1 or cleared to 0 via bit 15 (PME_D3COLD) in the miscellaneous configuration register at offset F0h in the PCI configuration space (see Section 3.23, *Miscellaneous Configuration Register*). The miscellaneous configuration register is loaded from ROM. When this bit is set to 1, it indicates that the TSB82AA2B device is capable of generating a $\overline{\text{PCI\_PME}}$ wake event from $D3_{cold}$. This bit state is dependent upon the TSB82AA2B V_{AUX} implementation and may be configured by using bit 15 (PME_D3COLD) in the miscellaneous configuration register (see Section 3.23).
14–11	PME_SUPPORT	R	$\overline{\text{PCI\_PME}}$ support. This 4-bit field indicates the power states from which the TSB82AA2B device may assert $\overline{\text{PCI\_PME}}$. This field returns a value of 1111b, indicating that $\overline{\text{PCI\_PME}}$ may be asserted from the $D3_{hot}$, D2, D1, and D0 power states. Bit 14 contains the value 1 to indicate that the $\overline{\text{PCI\_PME}}$ signal can be asserted from the $D3_{hot}$ state. Bit 13 contains the value 1 to indicate that the $\overline{\text{PCI\_PME}}$ signal can be asserted from the D2 state. Bit 12 contains the value 1 to indicate that the $\overline{\text{PCI\_PME}}$ signal can be asserted from the D1 state. Bit 11 contains the value 1 to indicate that the $\overline{\text{PCI\_PME}}$ signal can be asserted from the D0 state.
10	D2_SUPPORT	R	D2 support. Bit 10 is hardwired to 1, indicating that the function supports the D2 device power state.
9	D1_SUPPORT	R	D1 support. Bit 9 is hardwired to 1, indicating that the TSB82AA2B device supports the D1 power state.
8–6	AUX_CURRENT	R	Auxiliary current. This 3-bit field reports the 3.3-V_{AUX} auxiliary current requirements. When bit 15 (PME_D3COLD) is cleared, this field returns 000b; otherwise, it returns 001b. 000b = Self powered 001b = 55 mA (3.3-V_{AUX} maximum current required)
5	DSI	R	Device-specific initialization. Bit 5 returns 0 when read, indicating that the TSB82AA2B device does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	R	Reserved. Bit 4 returns 0 when read.
3	PME_CLK	R	$\overline{\text{PME}}$ clock. Bit 3 returns 0 when read, indicating that no host bus clock is required for the TSB82AA2B device to generate $\overline{\text{PCI\_PME}}$.
2–0	PM_VERSION	R	Power-management version. This field returns 010b when read, indicating that the TSB82AA2B device is compatible with the registers described in the *PCI Bus Power Management Interface Specification* (Revision 1.1).

3.20 Power Management Control and Status Register

The power management control and status register implements the control and status of the PCI power management function. This register is not affected by the internally generated reset caused by the transition from the $D3_{hot}$ to D0 state. See Table 3–18 for a complete description of the register contents.

Type: Read/Clear, Read/Write, Read only
Offset: 48h
Default: 0000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–18. Power Management Control and Status Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PME_STS	RC	Bit 15 is set to 1 when the TSB82AA2B device normally asserts the $\overline{PME}$ signal, independent of the state of bit 8 (PME_ENB). This bit is cleared by a writeback of 1, which also clears the $\overline{PCI\_PME}$ signal driven by the TSB82AA2B device. Writing a 0 to this bit has no effect.
14–9	RSVD	R	Reserved. Bits 14–9 return 0s when read.
8	PME_ENB	R/W	When bit 8 is set to 1, $\overline{PME}$ assertion is enabled. When bit 8 is cleared, $\overline{PME}$ assertion is disabled. This bit defaults to 0 if the function does not support $\overline{PME}$ generation from $D3_{cold}$. If the function supports $\overline{PME}$ from $D3_{cold}$, then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded. Functions that do not support $\overline{PME}$ generation from any D-state[(that is, bits 15–11 in the power management capabilities register at offset 46h in the PCI configuration space (see Section 3.19, *Power Management Capabilities Register*) equal 00000b], may hardwire this bit to be read only, always returning a 0 when read by system software.
7–2	RSVD	R	Reserved. Bits 7–2 return 0s when read.
1–0	PWR_STATE	R/W	Power state. This 2-bit field is used to set the TSB82AA2B device power state and is encoded as follows: 00 = Current power state is D0. 01 = Current power state is D1. 10 = Current power state is D2. 11 = Current power state is D3.

3.21 Power Management Extension Register

The power management extension register provides extended power-management features not applicable to the TSB82AA2B device; thus, it is read only and returns 0s when read. See Table 3–19 for a complete description of the register contents.

Type: Read only
Offset: 4Ah
Default: 0000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–19. Power Management Extension Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–0	RSVD	R	Reserved. Bits 15–0 return 0s when read.

3.22 Multifunction Select Register

The multifunction select register provides a method. See Table 3–20 for a complete description of the register contents.

Type: Read/Write/Update, Read only
Offset: E8h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–20. Multifunction Select Register

BIT	FIELD NAME	TYPE	DESCRIPTION
31–8	RSVD	R	Reserved. Bits 31–8 return 0s when read.
7	RSVD	R	Reserved. This read-only bit is for internal use only.
6–4	RSVD	R	Reserved. Bits 6–4 return 0s when read.
3–0	MFUNC_SEL	R/W/U	Power state. This 2-bit field is used to set the TSB82AA2B device power state and is encoded as follows: 000 = General-purpose input/output 001 = CYCLEIN 010 = CYCLEOUT 011 = $\overline{\text{PCI\_CLKRUN}}$ 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved

3.23 Miscellaneous Configuration Register

The miscellaneous configuration register provides miscellaneous PCI-related configuration. See Table 3–21 for a complete description of the register contents.

Type: Read/Write, Read only
Offset: F0h
Default: 0000 0010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 3–21. Miscellaneous Configuration Register

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0s when read.
15	PME_D3COLD	R/W	$\overline{\text{PCI\_PME}}$ support from $D3_{cold}$. This bit programs bit 15 (PME_D3COLD) in the power management capabilities register at offset 46h in the PCI configuration space (see Section 3.19, *Power Management Capabilities Register*).
14–11	RSVD	R	Reserved. Bits 14–11 return 0s when read.
10	Ignore IntMask.masterInt Enable_for_pme	R/W	Ignore IntMask.masterIntEnable for PME generation. When set to 1, this bit causes PME generation behavior to be changed. Also, when set to 1, this bit causes bit 26 of the OHCI vendor ID register at OHCI offset 40h to read 1; otherwise, bit 26 reads 0. 0 = PME behavior generated from unmasked interrupt bits and bit 31 (masterIntEnable) in the interrupt mask register at OHCI offset 88h (see Section 4.22, *Interrupt Mask Register*) (default) 1 = PME behavior does not depend on the value of bit 31 (masterIntEnable).
9–8	MR_ENHANCE	R/W	This field selects the read command behavior of the PCI master. 00 = Memory read line (default) 01 = Memory read 10 = Memory read multiple 11 = Reserved
7	RSVD	R	Reserved. Bit 7 returns 0 when read.
6	CARDBUS	R/W	CardBus. When bit 6 is set to 1, CardBus register support is enabled, that is, the CardBus base register and CardBus CIS pointer are valid. Bit 6 is only set if a serial EEPROM is present and contains a valid CIS. If bit 6 is set to 1, a valid CIS must be implemented in the EEPROM at an offset pointed to in EEPROM word 0x14, bits 7–3.
5	RSVD	R	Reserved. Bit 5 returns 0 when read.
4	DIS_TGT_ABT	R/W	Bit 4 defaults to 1 disabling the target abort behavior when accesses are made to PHY clock domain registers when no clock is present. Bit 4 can be set to 0 to provide OHCI-Lynx™ –compatible target abort signaling. When this bit is set to 1, it enables the no-target-abort mode, in which the TSB82AA2B device returns indeterminate data instead of signaling target abort. The TSB82AA2B LLC is divided into the PCI_CLK and SCLK domains. If software tries to access registers in the link that are not active because the SCLK is disabled, a target abort is issued by the link. On some systems, this can cause a problem resulting in a fatal system error. Enabling this bit allows the link to respond to these types of requests by returning FFh. It is recommended that this bit be set to 1.
3	RSVD	R	Reserved. Bit 3 returns 0 when read.
2	DISABLE_SCLKGATE	R/W	When bit 2 is set to 1, the internal SCLK runs identically with the chip input. This is a test feature only and must be cleared to 0 (all applications).
1	DISABLE_PCIGATE	R/W	When bit 1 is set to 1, the internal PCI clock runs identically with the chip input. This is a test feature only and must be cleared to 0 (all applications).
0	KEEP_PCLK	R/W	When bit 0 is set to 1, the PCI clock always is kept running through the $\overline{\text{PCI\_CLKRUN}}$ protocol. When this bit is cleared, the PCI clock can be stopped using $\overline{\text{PCI\_CLKRUN}}$.

3.24 Link Enhancement Control Register

The link enhancement control register implements TI proprietary bits that are initialized by software or by a serial EEPROM, if present. After these bits are set to 1, their functionality is enabled only if bit 22 (aPhyEnhanceEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1. See Table 3–22 for a complete description of the register contents.

Type: Read/Write, Read only
Offset: F4h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–22. Link Enhancement Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0s when read.
15	DisableATPipelining	R/W	Disable AT pipelining. When bit 15 is set to 1, out-of-order AT pipelining is disabled.
14	EnableDraft	R/W	Enable OHCI 1.2 draft features. When bit 14 is set to 1, it enables some features beyond the OHCI 1.1 specification. Specifically, this enables HCControl.LPS to be cleared by writing a 1 to the HCControlClear.LPS bit and enables the link to set bit 9 in the xferStatus field of AR and IR ContextControl registers.
13–12	atx_thresh	R/W	This field sets the initial AT threshold value, which is used until the AT FIFO is underrun. When the TSB82AA2B device retries the packet, it uses a 2K-byte threshold resulting in a store-and-forward operation. 00 = Threshold ~4K bytes resulting in a store-and-forward operation (default) 01 = Threshold ~1.7K bytes 10 = Threshold ~1K bytes 11 = Threshold ~512 bytes These bits fine tune the asynchronous transmit threshold. Changing this value may increase or decrease the 1394 latency depending on the average PCI bus latency. Setting the AT threshold to 1.7K, 1K, or 512 bytes results in data being transmitted at these thresholds or when an entire packet has been checked into the FIFO. If the packet to be transmitted is larger than the AT threshold, the remaining data must be received before the AT FIFO is emptied; otherwise, an underrun condition occurs, resulting in a packet error at the receiving node. As a result, the link then commences store-and-forward operation—that is, wait until it has the complete packet in the FIFO before retransmitting it on the second attempt, to ensure delivery. An AT threshold of 4K results in store-and-forward operation, which means that asynchronous data is not transmitted until an end-of-packet token is received. Restated, setting the AT threshold to 4K results in only complete packets being transmitted. Note that this device always uses store-and-forward when the asynchronous transmit retries register at OHCI offset 08h (see Section 4.3, *Asynchronous Transmit Retries Register*) is cleared.
11–10	RSVD	R	Reserved. Bits 11–10 return 0s when read.
9	enab_aud_ts	R/W	Enable audio/music CIP timestamp enhancement. When bit 9 is set to 1, the enhancement is enabled for audio/music CIP transmit streams (FMT = 10h).
8	enab_dv_ts	R/W	Enable DV CIP timestamp enhancement. When bit 8 is set to 1, the enhancement is enabled for DV CIP transmit streams (FMT = 00h).
7	enab_unfair	R/W	Enable asynchronous priority requests (OHCI-Lynx compatible). Setting bit 7 to 1 enables the link to respond to requests with priority arbitration. It is recommended that this bit be set to 1.
6	RSVD	R	Bit 6 is not assigned in the TSB82AA2B follow-on products since this location, which is loaded by the serial EEPROM from the enhancements field, corresponds to bit 23 (programPhyEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*).

Table 3–22. Link Enhancement Control Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
5–3	RSVD	R	Reserved. Bits 5–3 return 0s when read.
2	enab_insert_idle	R/W	Enable insert idle (OHCI-Lynx compatible). When the PHY device has control of the PHY_CTL0–PHY_CTL1 control lines and PHY_DATA0–PHY_DATA7 data lines and the link requests control, the PHY device drives 11b on the PHY_CTL0–PHY_CTL1 lines. The link can then start driving these lines immediately. Setting bit 2 to 1 inserts an idle state, so the link waits one clock cycle before it starts driving the lines (turnaround time).
1	enab_accel	R/W	Enable acceleration enhancements (OHCI-Lynx compatible). When bit 1 is set to 1, the PHY device is notified that the link supports the IEEE Std 1394a-2000 acceleration enhancements, that is, ack-accelerated, fly-by concatenation, etc. It is recommended that bit 1 be set to 1.
0	RSVD	R	Reserved. Bit 0 returns 0 when read.

3.25 Subsystem Access Registers

Write access to the subsystem access registers updates the subsystem ID registers identically to OHCI-Lynx controller. The system ID value written to these registers may also be read back from these registers. See Table 3–23 for a complete description of the register contents.

Type: Read/Write
Offset: F8h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–23. Subsystem Access Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	SUBDEV_ID	R/W	Subsystem device ID alias. This field indicates the subsystem device ID.
15–0	SUBVEN_ID	R/W	Subsystem vendor ID alias. This field indicates the subsystem vendor ID.

3.26 GPIO Control Register

The GPIO control register has the control and status bits for the GPIO2 and GPIO3 ports. See Table 3–24 for a complete description of the register contents.

Type: Read/Write/Update, Read/Write, Read only
Offset: FCh
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3–24. GPIO Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–24	RSVD	R	Reserved. Bits 31–24 return 0s when read.
23	INT_EN	R/W	When bit 23 is set to 1, a TSB82AA2B general-purpose interrupt event occurs on a level change of the GPIO input. This event may generate an interrupt, with mask and event status reported through the interrupt mask register at OHCI offset 88h/8Ch (see Section 4.22, *Interrupt Mask Register*) and the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*).
22	RSVD	R	Reserved. Bit 22 returns 0 when read.
21	GPIO_INV	R/W	GPIO polarity invert. When bit 21 is set to 1, the polarity of GPIO is inverted.
20	GPIO_ENB	R/W	GPIO enable control. When bit 20 is set to 1, the output is enabled. Otherwise, the output is high impedance.
19–17	RSVD	R	Reserved. Bits 19–17 return 0s when read.
16	GPIO_DATA	RWU	GPIO data. Reads from bit 16 return the logical value of the input to GPIO. Writes to this bit update the value to drive to GPIO when the output is enabled.
15–0	RSVD	R	Reserved. Bits 15–0 return 0s when read.

4 OHCI Registers

The OHCI registers defined by the *1394 Open Host Controller Interface Specification* are memory mapped into a 2K-byte region of memory pointed to by the OHCI base address register at offset 10h in PCI configuration space (see Section 3.9, *OHCI Base Address Register*). These registers are the primary interface for controlling the TSB82AA2B IEEE Std 1394 link function.

This section provides the register interface and bit descriptions. Several set/clear register pairs in this programming model are implemented to solve various issues with typical read-modify-write control registers. There are two addresses for a set/clear register — RegisterSet and RegisterClear (see Table 4–1 for register listings). A 1 bit written to RegisterSet causes the corresponding bit in the set/clear register to be set to 1; a 0 bit leaves the corresponding bit unaffected. A 1 bit written to RegisterClear causes the corresponding bit in the set/clear register to be cleared; a 0 bit leaves the corresponding bit in the set/clear register unaffected.

Typically, a read from either RegisterSet or RegisterClear returns the contents of the set or clear register, respectively. However, sometimes reading the RegisterClear provides a masked version of the set or clear register. The interrupt event register is an example of this behavior.

Table 4–1. OHCI Register Map

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
—	OHCI version	Version	00h
	GUID ROM	GUID_ROM	04h
	Asynchronous transmit retries	ATRetries	08h
	CSR data	CSRData	0Ch
	CSR compare	CSRCompareData	10h
	CSR control	CSRControl	14h
	Configuration ROM header	ConfigROMhdr	18h
	Bus ID	BusID	1Ch
	Bus options	BusOptions	20h
	GUID high	GUIDHi	24h
	GUID low	GUIDLo	28h
	Reserved	—	2Ch–30h
	Configuration ROM mapping	ConfigROMmap	34h
	Posted write address low	PostedWriteAddressLo	38h
	Posted write address high	PostedWriteAddressHi	3Ch
	Vendor ID	VendorID	40h
	Reserved	—	44h–4Ch
	Host controller control	HCControlSet	50h
		HCControlClr	54h
	Reserved	—	58h–5Ch

Table 4–1. OHCI Register Map (Continued)

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
Self ID	Reserved	—	60h
	Self–ID buffer	SelfIDBuffer	64h
	Self–ID count	SelfIDCount	68h
	Reserved	—	6Ch
—	Isochronous receive channel mask high	IRChannelMaskHiSet	70h
		IRChannelMaskHiClear	74h
	Isochronous receive channel mask low	IRChannelMaskLoSet	78h
		IRChannelMaskLoClear	7Ch
	Interrupt event	IntEventSet	80h
		IntEventClear	84h
	Interrupt mask	IntMaskSet	88h
		IntMaskClear	8Ch
	Isochronous transmit interrupt event	IsoXmitIntEventSet	90h
		IsoXmitIntEventClear	94h
	Isochronous transmit interrupt mask	IsoXmitIntMaskSet	98h
		IsoXmitIntMaskClear	9Ch
—	Isochronous receive interrupt event	IsoRecvIntEventSet	A0h
		IsoRecvIntEventClear	A4h
	Isochronous receive interrupt mask	IsoRecvIntMaskSet	A8h
		IsoRecvIntMaskClear	ACh
	Initial bandwidth available	IntBandwidthAvailable	B0h
	Initial channels available high	IntChannelHiAvailable	B4h
	Initial channels available low	IntChannelLoAvailable	B8h
	Reserved	—	BCh–D8h
	Fairness control	FairnessControl	DCh
	Link control	LinkControlSet	E0h
		LinkControlClear	E4h
	Node ID	NodeID	E8h
	PHY control	PhyControl	ECh
	Isochronous cycle timer	Isocyctimer	F0h
	Reserved	—	F4h–FCh
	Asynchronous request filter high	AsyncRequestFilterHiSet	100h
		AsyncRequestFilterHiClear	104h
	Asynchronous request filter low	AsyncRequestFilterLoSet	108h
		AsyncRequestFilterloClear	10Ch
	Physical request filter high	PhysicalRequestFilterHiSet	110h
		PhysicalRequestFilterHiClear	114h
	Physical request filter low	PhysicalRequestFilterLoSet	118h
		PhysicalRequestFilterloClear	11Ch
	Physical upper bound	PhysicalUpperBound	120h
	Reserved	—	124h–17Ch

Table 4–1. OHCI Register Map (Continued)

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
Asychronous request transmit (ATRQ)	Asynchronous context control	ContextControlSet	180h
		ContextControlClear	184h
	Reserved	—	188h
	Asynchronous context command pointer	CommandPtr	18Ch
	Reserved	—	190h–19Ch
Asychronous response transmit (ATRS)	Asynchronous context control	ContextControlSet	1A0h
		ContextControlClear	1A4h
	Reserved	—	1A8h
	Asynchronous context command pointer	CommandPtr	1ACh
	Reserved	—	1B0h–1BCh
Asychronous request receive (ARRQ)	Asynchronous context control	ContextControlSet	1C0h
		ContextControlClear	1C4h
	Reserved	—	1C8h
	Asynchronous context command pointer	CommandPtr	1CCh
	Reserved	—	1D0h–1DCh
Asychronous response receive (ARRS)	Asynchronous context control	ContextControlSet	1E0h
		ContextControlClear	1E4h
	Reserved	—	1E8h
	Asynchronous context command pointer	CommandPtr	1ECh
	Reserved	—	1F0h–1FCh
Isochronous transmit context n (n = 0, 1, 2, 3, …, 7)	Isochronous transmit context control	ContextControlSet	200h + 16*n
		ContextControlClear	204h + 16*n
	Reserved	—	208h + 16*n
	Isochronous transmit context command pointer	CommandPtr	20Ch + 16*n
	Reserved	—	280h–3FCh
Isochronous receive context n (n = 0, 1, 2, 3)	Isochronous receive context control	ContextControlSet	400h + 32*n
		ContextControlClear	404h + 32*n
	Reserved	—	408h + 32*n
	Isochronous receive context command pointer	CommandPtr	40Ch + 32*n
	Isochronous receive context match	ContextMatch	410h + 32*n

4.1 OHCI Version Register

The OHCI version register indicates the OHCI version support and whether or not the serial EEPROM is present. See Table 4–2 for a complete description of the register contents.

Type: Read only
Offset: 00h
Default: 0X01 0010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	X	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 4–2. OHCI Version Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–25	RSVD	R	Reserved. Bits 31–25 return 0s when read.
24	GUID_ROM	R	The TSB82AA2B device sets bit 24 to 1 if the serial EEPROM is detected. If the serial EEPROM is present, the Bus_Info_Block is automatically loaded on system (hardware) reset.
23–16	version	R	Major version of the OHCI. The TSB82AA2B device is compliant with the *1394 Open Host Controller Interface Specification* (Revision 1.1); thus, this field reads 01h.
15–8	RSVD	R	Reserved. Bits 15–8 return 0s when read.
7–0	revision	R	Minor version of the OHCI. The TSB82AA2B device is compliant with the *1394 Open Host Controller Interface Specification* (Revision 1.1); thus, this field reads 10h.

4.2 GUID ROM Register

The GUID ROM register accesses the serial EEPROM and is only applicable if bit 24 (GUID_ROM) in the OHCI version register at OHCI offset 00h (see Section 4.1, *OHCI Version Register*) is set to 1. See Table 4–3 for a complete description of the register contents.

Type: Read/Set/Update, Read/Update, Read only
Offset: 04h
Default: 00XX 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–3. GUID ROM Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	addrReset	RSU	Software sets bit 31 to 1 to reset the GUID ROM address to 0. When the TSB82AA2B device completes the reset, it clears this bit. The TSB82AA2B device does not automatically fill bits 23–16 (rdData field) with the 0 byte.
30–26	RSVD	R	Reserved. Bits 30–26 return 0s when read.
25	rdStart	RSU	A read of the currently addressed byte is started when bit 25 is set to 1. This bit is automatically cleared when the TSB82AA2B device completes the read of the currently addressed GUID ROM byte.
24	RSVD	R	Reserved. Bit 24 returns 0 when read.
23–16	rdData	RU	This field represents the data read from the GUID ROM.
15–8	RSVD	R	Reserved. Bits 15–8 return 0s when read.
7–0	miniROM	R	Mini ROM. The TSB82AA2B device uses bits 7–0 to indicate the first byte location of the mini-ROM image in the GUID ROM. A value of 00h in this field indicates that no mini ROM is implemented.

4.3 Asynchronous Transmit Retries Register

The asynchronous transmit retries register indicates the number of times the TSB82AA2B device attempts a retry for asynchronous DMA request transmit and for asynchronous physical and DMA response transmit. See Table 4–4 for a complete description of the register contents.

Type: Read/Write, Read only
Offset: 08h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–4. Asynchronous Transmit Retries Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–29	secondLimit	R	The second limit field returns 0s when read, because outbound dual-phase retry is not implemented.
28–16	cycleLimit	R	The cycle limit field returns 0s when read, because outbound dual-phase retry is not implemented.
15–12	RSVD	R	Reserved. Bits 15–12 return 0s when read.
11–8	maxPhysRespRetries	R/W	This field tells the physical response unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node.
7–4	maxATRespRetries	R/W	This field tells the asynchronous transmit response unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node.
3–0	maxATReqRetries	R/W	This field tells the asynchronous transmit DMA request unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node.

4.4 CSR Data Register

The CSR data register accesses the bus management CSR registers from the host through compare-swap operations. This register contains the data to be stored in a CSR if the compare is successful.

Type: Read only
Offset: 0Ch
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

4.5 CSR Compare Register

The CSR compare register accesses the bus management CSR registers from the host through compare-swap operations. This register contains the data to be compared with the existing value of the CSR resource.

Type: Read only
Offset: 10h
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

4.6 CSR Control Register

The CSR control register accesses the bus management CSR registers from the host through compare-swap operations. This register controls the compare-swap operation and selects the CSR resource. See Table 4–5 for a complete description of the register contents.

Type: Read/Write, Read/Update, Read only
Offset: 14h
Default: 8000 000Xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X

Table 4–5. CSR Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	csrDone	RU	Bit 31 is set to 1 by the TSB82AA2B device when a compare-swap operation is complete. It is cleared whenever this register is written.
30–2	RSVD	R	Reserved. Bits 30–2 return 0s when read.
1–0	csrSel	R/W	This field selects the CSR resource as follows: 00 = BUS_MANAGER_ID 01 = BANDWIDTH_AVAILABLE 10 = CHANNELS_AVAILABLE_HI 11 = CHANNELS_AVAILABLE_LO

4.7 Configuration ROM Header Register

The configuration ROM header register externally maps to the first quadlet of the 1394 configuration ROM, offset FFFF F000 0400h. See Table 4–6 for a complete description of the register contents.

Type: Read/Write
Offset: 18h
Default: 0000 XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 4–6. Configuration ROM Header Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–24	info_length	R/W	IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1.
23–16	crc_length	R/W	IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1.
15–0	rom_crc_value	R/W	IEEE Std 1394 bus-management field. Must be valid at any time bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1. The reset value is undefined if no serial EEPROM is present. If a serial EEPROM is present, this field is loaded from the serial EEPROM.

4.8 Bus ID Register

The bus ID register externally maps to the first quadlet in the Bus_Info_Block and contains the constant 3133 3934h, which is the ASCII value of 1394.

Type: Read only
Offset: 1Ch
Default: 3133 3934h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	1	1	0	0	0	1	0	0	1	1	0	0	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	0

4.9 Bus Options Register

The bus options register externally maps to the second quadlet of the Bus_Info_Block. See Table 4–7 for a complete description of the register contents.

Type: Read/Write, Read only
Offset: 20h
Default: X0XX B0X2h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	0	0	0	0	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	1	0	1	1	0	0	0	0	X	X	0	0	0	0	1	0

Table 4–7. Bus Options Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	irmc	R/W	Isochronous resource-manager capable. IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1.
30	cmc	R/W	Cycle master capable. IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1.
29	isc	R/W	Isochronous support capable. IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1.
28	bmc	R/W	Bus manager capable. IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1.
27	pmc	R/W	Power-management capable. IEEE Std 1394 bus-management field. When bit 27 is set to 1, this indicates that the node is power-management capable. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1.
26–24	RSVD	R	Reserved. Bits 26–24 return 0s when read.
23–16	cyc_clk_acc	R/W	Cycle master clock accuracy, in parts per million. IEEE Std 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1.
15–12	max_rec	R/W	Maximum request. IEEE Std 1394 bus-management field. Hardware initializes this field to indicate the maximum number of bytes in a block request packet that is supported by the implementation. This value, max_rec_bytes must be 512 or greater, and is calculated by 2^(max_rec + 1). Software may change this field; however, this field must be valid at any time bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1. A received block write request packet with a length greater than max_rec_bytes may generate an ack_type_error. This field is not affected by a software reset, and defaults to a value indicating 4096 bytes on a system (hardware) reset.
11–8	RSVD	R	Reserved. Bits 11–8 return 0s when read.
7–6	g	R/W	Generation counter. This field is incremented if any portion of the configuration ROM has been incremented since the prior bus reset.
5–3	RSVD	R	Reserved. Bits 5–3 return 0s when read.
2–0	Lnk_spd	R	Link speed. This field returns 010, indicating that the link speeds of 100M bit/s, 200M bit/s, and 400M bit/s are supported.

4.10 GUID High Register

The GUID high register represents the upper quadlet in a 64-bit global unique ID (GUID), which maps to the third quadlet in the Bus_Info_Block. This register contains node_vendor_ID and chip_ID_hi fields. This register initializes to 0s on a system (hardware) reset, which is an illegal GUID value. If a serial EEPROM is detected, the contents of this register are loaded through the serial EEPROM interface after a $\overline{\text{G\_RST}}$. At that point, the contents of this register cannot be changed. If no serial EEPROM is detected, the contents of this register are loaded by the BIOS. At that point, the contents of this register cannot be changed. All bits in this register are reset by $\overline{\text{G\_RST}}$ only.

Type: Read only
Offset: 24h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.11 GUID Low Register

The GUID low register represents the lower quadlet in a 64-bit GUID, which maps to chip_ID_lo in the Bus_Info_Block. This register initializes to 0s on a system (hardware) reset and behaves identically to the GUID high register at OHCI offset 24h (see Section 4.10, *GUID High Register*).

Type: Read only
Offset: 28h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.12 Configuration ROM Mapping Register

The configuration ROM mapping register contains the start address within system memory that maps to the start address of 1394 configuration ROM for this node. See Table 4–8 for a complete description of the register contents.

Type: Read/Write, Read-only
Offset: 34h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–8. Configuration ROM Mapping Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–10	configROMaddr	R/W	If a quadlet read request to 1394 offset FFFF F000 0400h through offset FFFF F000 07FFh is received, then the low-order 10 bits of the offset are added to this register to determine the host memory address of the read request.
9–0	RSVD	R	Reserved. Bits 9–0 return 0s when read.

4.13 Posted Write Address Low Register

The posted write address low register communicates error information if a write request is posted and an error occurs while writing the posted data packet. See Table 4–9 for a complete description of the register contents.

Type: Read/Update
Offset: 38h
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 4–9. Posted Write Address Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–0	offsetLo	RU	Lower 32 bits of the 1394 destination offset of the write request that failed

4.14 Posted Write Address High Register

The posted write address high register communicates error information if a write request is posted and an error occurs while writing the posted data packet. See Table 4–10 for a complete description of the register contents.

Type: Read/Update
Offset: 3Ch
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 4–10. Posted Write Address High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	sourceID	RU	This field is the 10-bit bus number (bits 31–22) and 6-bit node number (bits 21–16) of the node that issued the write request that failed.
15–0	offsetHi	RU	Upper 16 bits of the 1394 destination offset of the write request that failed

4.15 Vendor ID Register

The vendor ID register provides the company ID of an organization that specifies any vendor-unique registers or features. The TSB82AA2B device implements several unique features with regards to OHCI. Therefore, bits 23–0 are programmed with TI OUI, 0X08 0028.

Type: Read/Update, Read only
Offset: 40h
Default: 0X08 0028h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	X	X	0	0	0	0	0	1	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0

Table 4–11. Vendor ID Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–27	RSVD	R	Reserved. Bits 31–27 return 0s when read.
26	PME_Enhance	RU	PME enhance. Bit 26 is conditionally set based on the value of bit 10 (Ignore IntMask.masterIntEnable_for_pme) in the miscellaneous configuration register at offset F0h in the PCI configuration space (see Section 3.23, *Miscellaneous Configuration Register*). If bit 10 is set to 1, bit 26 is set to 1 to indicate that the device supports the generation of $\overline{\text{PME}}$, regardless of the status of bit 31 (masterIntEnable) in the interrupt mask register at OHCI offset 88h (see Section 4.22, *Interrupt Mask Register*). If bit 10 is not set, bit 26 returns 0.
25	OHCI12_draft	RU	OHCI 1.2 draft features. Bit 25 is conditionally set based on the value of bit 14 (EnableDraft) in the link enhancement control register at offset F4h in the PCI configuration space (see Section 3.24, *Link Enhancement Control Register*). If bit 14 is set to 1, bit 25 is set to 1 to indicate that the device supports some features which have been defined in the OHCI 1.2 specification draft. If bit 14 is not set, bit 25 returns 0.
24	Iso_enhancements	R	Isochronous enhancements. Bit 24 is set to 1 indicating that it supports the isochronous enhancements defined in Sections 4.4 and 4.5.
23–0	vendorCompanyID	R	Vendor company organizational unique ID. This field returns TI OUI, 24'h080028, indicating that the device supports unique features defined by TI.

4.16 Host Controller Control Register

The host controller control set/clear register pair provides flags for controlling the TSB82AA2B device. See Table 4–12 for a complete description of the register contents.

Type: Read/Set/Clear/Update, Read/Set/Clear, Read/Clear, Read only
Offset: 50h set register
54h clear register
Default: X00X 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	X	0	0	0	0	0	0	0	0	0	0	0	X	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–12. Host Controller Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	BIBimageValid	RSU	When bit 31 is set to 1, the TSB82AA2B physical response unit is enabled to respond to block read requests to host configuration ROM and to the mechanism for atomically updating configuration ROM. Software creates a valid image of the bus_info_block in host configuration ROM before setting this bit. When this bit is cleared, the TSB82AA2B device returns ack_type_error on block read requests to host configuration ROM. Also, when this bit is cleared and a 1394 bus reset occurs, the configuration ROM mapping register at OHCI offset 34h (see Section 4.12, *Configuration ROM Mapping Register*), configuration ROM header register at OHCI offset 18h (see Section 4.7, *Configuration ROM Header Register*), and bus options register at OHCI offset 20h (see Section 4.9, *Bus Options Register*) are not updated. Software can set this bit only when bit 17 (linkEnable) is 0. Once bit 31 is set to 1, it can be cleared by a system (hardware) reset, a software reset, or if a fetch error occurs when the TSB82AA2B device loads bus_info_block registers from host memory.
30	noByteSwapData	RSC	Bit 30 controls whether physical accesses to locations outside the TSB82AA2B device itself, as well as any other DMA data accesses, are byte swapped.
29	ack_Tardy_enable	RSC	Bit 29 controls the acknowledgement of ack_tardy. When bit 29 is set to 1, ack_tardy may be returned as an acknowledgment to configuration ROM accesses from 1394 to the TSB82AA2B device, including accesses to the bus_info_block. The TSB82AA2B device returns ack_tardy to all other asynchronous packets addressed to the TSB82AA2B node. When the TSB82AA2B device sends ack_tardy, bit 27 (ack_tardy) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) is set to 1 to indicate the attempted asynchronous access. Software ensures that bit 27 (ack_tardy) in the interrupt event register is 0. Software also unmasks wake-up interrupt events such as bit 19 (phy) and bit 27 (ack_tardy) in the interrupt event register before placing the device into D1. Software does not set this bit if the TSB82AA2B node is the 1394 bus manager.
28–24	RSVD	R	Reserved. Bits 28–24 return 0s when read.
23	programPhyEnable	RC	Bit 23 informs upper-level software that lower-level software has consistently configured the IEEE 1394a-2000 enhancements in the link and PHY devices. When this bit is 1, generic software such as the OHCI driver is responsible for configuring IEEE Std 1394a-2000 enhancements in the PHY device and bit 22 (aPhyEnhanceEnable) in the TSB82AA2B device. When this bit is 0, the generic software may not modify the IEEE Std 1394a-2000 enhancements in the TSB82AA2B or PHY device and cannot interpret the setting of bit 22 (aPhyEnhanceEnable). This bit is initialized from the serial EEPROM.
22	aPhyEnhanceEnable	RSC	When bits 23 (programPhyEnable) and 17 (linkEnable) are 1, the OHCI driver can set bit 22 to 1 to use all IEEE Std 1394a-2000 enhancements. When bit 23 (programPhyEnable) is cleared to 0, the software does not change PHY enhancements or this bit.
21–20	RSVD	R	Reserved. Bits 21–20 return 0s when read.

Table 4–12. Host Controller Control Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
19	LPS	RSC	Bit 19 controls the link power status. Software must set this bit to 1 to permit link-PHY communication. A 0 prevents link-PHY communication. The OHCI-link is divided into two clock domains (PCI_CLK and PHY_SCLK). If software tries to access any register in the PHY_SCLK domain while the PHY_SCLK is disabled, a target abort is issued by the link. This problem can be avoided by setting bit 4 (DIS_TGT_ABT) in the miscellaneous configuration register at offset F0h in the PCI configuration space (see Section 3.23, *Miscellaneous Configuration Register*). This allows the link to respond to these types of request by returning all Fs (hex). OHCI registers at offsets DCh–F0h and 100h–11Ch are in the PHY_SCLK domain. After setting LPS, software must wait approximately 10 ms before attempting to access any of the OHCI registers. This gives the PHY_SCLK time to stabilize.
18	postedWriteEnable	RSC	Bit 18 enables (1) or disables (0) posted writes. Software changes this bit only when bit 17 (linkEnable) is 0.
17	linkEnable	RSC	Bit 17 is cleared to 0 by either a system (hardware) or software reset. Software must set this bit to 1 when the system is ready to begin operation and then force a bus reset. This bit is necessary to keep other nodes from sending transactions before the local system is ready. When this bit is cleared, the TSB82AA2B device is logically and immediately disconnected from the 1394 bus, no packets are received or processed, nor are packets transmitted.
16	SoftReset	RSCU	When bit 16 is set to 1, all TSB82AA2B states are reset, all FIFOs are flushed, and all OHCI registers are set to their system (hardware) reset values, unless otherwise specified. PCI registers are not affected by this bit. This bit remains set to 1 while the software reset is in progress and reverts back to 0 when the reset has completed.
15–0	RSVD	R	Reserved. Bits 15–0 return 0s when read.

4.17 Self-ID Buffer Register

The self-ID buffer register points to the 2K-byte aligned base address of the buffer in host memory where the self-ID packets are stored during bus initialization. Bits 31–11 are read/write accessible. Bits 10–0 are reserved, and return 0s when read.

Type: Read/Write, Read only
Offset: 64h
Default: XXXX XX00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0

4.18 Self-ID Count Register

The self-ID count register keeps a count of the number of times the bus self-ID process has occurred, flags self-ID packet errors, and keeps a count of the self-ID data in the self-ID buffer. See Table 4–13 for a complete description of the register contents.

Type: Read/Update, Read only
Offset: 68h
Default: X0XX 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–13. Self-ID Count Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	selfIDError	RU	When bit 31 is set to 1, an error was detected during the most recent self-ID packet reception. The contents of the self-ID buffer are undefined. This bit is cleared after a self-ID reception in which no errors are detected. Note that an error can be a hardware error or a host bus write error.
30–24	RSVD	R	Reserved. Bits 30–24 return 0s when read.
23–16	selfIDGeneration	RU	The value in this field increments each time a bus reset is detected. This field rolls over to 0 after reaching 255.
15–11	RSVD	R	Reserved. Bits 15–11 return 0s when read.
10–2	selfIDSize	RU	This field indicates the number of quadlets that have been written into the self-ID buffer for the current bits 23–16 (selfIDGeneration field). This includes the header quadlet and the self-ID data. This field is cleared to 0s when the self-ID reception begins.
1–0	RSVD	R	Reserved. Bits 1–0 return 0s when read.

4.19 Isochronous Receive Channel Mask High Register

The isochronous receive channel mask high set/clear register enables packet receives from the upper 32 isochronous data channels. A read from either the set register or clear register returns the content of the isochronous receive channel mask high register. See Table 4–14 for a complete description of the register contents.

Type: Read/Set/Clear
Offset: 70h set register
74h clear register
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 4–14. Isochronous Receive Channel Mask High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	isoChannel63	RSC	When bit 31 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 63.
30	isoChannel62	RSC	When bit 30 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 62.
29	isoChannel61	RSC	When bit 29 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 61.
28	isoChannel60	RSC	When bit 28 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 60.
27	isoChannel59	RSC	When bit 27 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 59.
26	isoChannel58	RSC	When bit 26 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 58.
25	isoChannel57	RSC	When bit 25 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 57.
24	isoChannel56	RSC	When bit 24 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 56.
23	isoChannel55	RSC	When bit 23 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 55.
22	isoChannel54	RSC	When bit 22 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 54.
21	isoChannel53	RSC	When bit 21 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 53.
20	isoChannel52	RSC	When bit 20 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 52.
19	isoChannel51	RSC	When bit 19 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 51.
18	isoChannel50	RSC	When bit 18 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 50.
17	isoChannel49	RSC	When bit 17 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 49.
16	isoChannel48	RSC	When bit 16 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 48.
15	isoChannel47	RSC	When bit 15 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 47.
14	isoChannel46	RSC	When bit 14 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 46.
13	isoChannel45	RSC	When bit 13 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 45.
12	isoChannel44	RSC	When bit 12 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 44.
11	isoChannel43	RSC	When bit 11 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 43.
10	isoChannel42	RSC	When bit 10 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 42.
9	isoChannel41	RSC	When bit 9 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 41.
8	isoChannel40	RSC	When bit 8 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 40.
7	isoChannel39	RSC	When bit 7 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 39.
6	isoChannel38	RSC	When bit 6 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 38.
5	isoChannel37	RSC	When bit 5 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 37.
4	isoChannel36	RSC	When bit 4 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 36.
3	isoChannel35	RSC	When bit 3 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 35.
2	isoChannel34	RSC	When bit 2 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 34.
1	isoChannel33	RSC	When bit 1 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 33.
0	isoChannel32	RSC	When bit 0 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 32.

4.20 Isochronous Receive Channel Mask Low Register

The isochronous receive channel mask low set/clear register enables packet receives from the lower 32 isochronous data channels. See Table 4–15 for a complete description of the register contents.

Type: Read/Set/Clear
Offset: 78h set register
7Ch clear register
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 4–15. Isochronous Receive Channel Mask Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	isoChannel31	RSC	When bit 31 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 31.
30	isoChannel30	RSC	When bit 30 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 30.
29–2	isoChanneln	RSC	Bits 29 through 2 (isoChanneln, where n = 29, 28, 27, …, 2) follow the same pattern as bits 31 and 30.
1	isoChannel1	RSC	When bit 1 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 1.
0	isoChannel0	RSC	When bit 0 is set to 1, the TSB82AA2B device is enabled to receive from isochronous channel number 0.

4.21 Interrupt Event Register

The interrupt event set/clear register reflects the state of the various TSB82AA2B interrupt sources. The interrupt bits are set to 1 by an asserting edge of the corresponding interrupt signal or by writing a 1 in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1 to the corresponding bit in the clear register.

This register is fully compliant with *1394 Open Host Controller Interface Specification*, and the TSB82AA2B device adds a vendor-specific interrupt function to bit 30. When the interrupt event register is read, the return value is the bit-wise AND function of the interrupt event and interrupt mask registers. See Table 4–16 for a complete description of the register contents.

Type: Read/Set/Clear/Update, Read/Set/Clear, Read/Update, Read only
Offset: 80h set register
84h clear register [returns the content of the interrupt event register bit-wise ANDed with the interrupt mask register when read]
Default: XXXX 0XXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	X	0	0	0	X	X	X	X	X	X	X	X	0	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X

Table 4–16. Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	RSVD	R	Reserved. Bit 31 returns 0 when read.
30	vendorSpecific	RSC	This vendor-specific interrupt event is reported when either of the general-purpose interrupts are asserted. The general-purpose interrupts are enabled by setting the corresponding bits INT_3EN and INT_2EN (bits 31 and 23, respectively) to 1 in the GPIO control register at offset FCh in the PCI configuration space (see Section 3.26, *GPIO Control Register*).
29	SoftInterrupt	RSC	Software interrupt. Bit 29 is used by software to generate a TSB82AA2B interrupt for its own use.
28	RSVD	R	Reserved. Bit 28 returns 0 when read.
27	ack_Tardy	RSCU	Bit 27 is set to 1 when bit 29 (ack_Tardy_enable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1 and any of the following conditions occur: a. Data is present in the receive FIFO that is to be delivered to the host. b. The physical response unit is busy processing requests or sending responses. c. The TSB82AA2B device sent an ack_tardy acknowledgement.
26	phyRegRcvd	RSCU	The TSB82AA2B device has received a PHY register data byte which can be read from bits 23–16 in the PHY layer control register at OHCI offset ECh (see Section 4.33, *PHY Layer Control Register*).
25	cycleTooLong	RSCU	If bit 21 (cycleMaster) in the link control register at OHCI offset E0h/E4h (see Section 4.31, *Link Control Register*) is set to 1, this indicates that over 125 μs have elapsed between the start of sending a cycle start packet and the end of a subaction gap. Bit 21 (cycleMaster) in the link control register is cleared by this event.
24	unrecoverableError	RSCU	This event occurs when the TSB82AA2B device encounters any error that forces it to stop operations on any or all of its subunits, for example, when a DMA context sets its dead bit to 1. While bit 24 is set to 1, all normal interrupts for the context(s) that caused this interrupt are blocked from being set to 1.
23	cycleInconsistent	RSCU	A cycle start was received that had values for cycleSeconds and cycleCount fields that are different from the values in bits 31–25 (cycleSeconds field) and bits 24–12 (cycleCount field) in the isochronous cycle timer register at OHCI offset F0h (see Section 4.34, *Isochronous Cycle Timer Register*).

Table 4–16. Interrupt Event Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
22	cycleLost	RSCU	A lost cycle is indicated when no cycle_start packet is sent or received between two successive cycleSynch events. A lost cycle can be predicted when a cycle_start packet does not immediately follow the first subaction gap after the cycleSynch event or if an arbitration reset gap is detected after a cycleSynch event without an intervening cycle start. Bit 22 may be set either when a lost cycle occurs or when logic predicts that one will occur.
21	cycle64Seconds	RSCU	Indicates that the 7th bit of the cycle second counter has changed.
20	cycleSynch	RSCU	Indicates that a new isochronous cycle has started. Bit 20 is set to 1 when the low-order bit of the cycle count toggles.
19	phy	RSCU	Indicates that the PHY device requests an interrupt through a status transfer.
18	regAccessFail	RSCU	Indicates that a TSB82AA2B register access has failed due to a missing SCLK clock signal from the PHY device. When a register access fails, bit 18 is set to 1 before the next register access.
17	busReset	RSCU	Indicates that the PHY device has entered bus reset mode.
16	selfIDcomplete	RSCU	A self-ID packet stream has been received. It is generated at the end of the bus initialization process. Bit 16 is turned off simultaneously when bit 17 (busReset) is turned on.
15	selfIDcomplete2	RSCU	Secondary indication of the end of a self-ID packet stream. Bit 15 is set to 1 by the TSB82AA2B device when it sets bit 16 (selfIDcomplete), and retains its state, independent of bit 17 (busReset).
14–10	RSVD	R	Reserved. Bits 14–10 return 0s when read.
9	lockRespErr	RSCU	Indicates that the TSB82AA2B device sent a lock response for a lock request to a serial bus register, but did not receive an ack_complete
8	postedWriteErr	RSCU	Indicates that a host bus error occurred while the TSB82AA2B device was trying to write a 1394 write request, which had already been given an ack_complete, into system memory
7	isochRx	RU	Isochronous receive DMA interrupt. Indicates that one or more isochronous receive contexts have generated an interrupt. This is not a latched event; it is the logical OR of all bits in the isochronous receive interrupt event register at OHCI offset A0h/A4h (see Section 4.25, *Isochronous Receive Interrupt Event Register*) and isochronous receive interrupt mask register at OHCI offset A8h/ACh (see Section 4.26, *Isochronous Receive Interrupt Mask Register*). The isochronous receive interrupt event register indicates which contexts have been interrupted.
6	isochTx	RU	Isochronous transmit DMA interrupt. Indicates that one or more isochronous transmit contexts have generated an interrupt. This is not a latched event; it is the logical OR of all bits in the isochronous transmit interrupt event register at OHCI offset 90h/94h (see Section 4.23, *Isochronous Transmit Interrupt Event Register*) and isochronous transmit interrupt mask register at OHCI offset 98h/9Ch (see Section 4.24, *Isochronous Transmit Interrupt Mask Register*). The isochronous transmit interrupt event register indicates which contexts have been interrupted.
5	RSPkt	RSCU	Indicates that a packet was sent to an asynchronous receive response context buffer and the descriptor's xferStatus and resCount fields have been updated
4	RQPkt	RSCU	Indicates that a packet was sent to an asynchronous receive request context buffer and the descriptor's xferStatus and resCount fields have been updated
3	ARRS	RSCU	Asynchronous receive response DMA interrupt. Bit 3 is conditionally set to 1 upon completion of an ARRS DMA context command descriptor.
2	ARRQ	RSCU	Asynchronous receive request DMA interrupt. Bit 2 is conditionally set to 1 upon completion of an ARRQ DMA context command descriptor.
1	respTxComplete	RSCU	Asynchronous response transmit DMA interrupt. Bit 1 is conditionally set to upon completion of an ATRS DMA command.
0	reqTxComplete	RSCU	Asynchronous request transmit DMA interrupt. Bit 0 is conditionally set to 1 upon completion of an ATRQ DMA command.

4.22 Interrupt Mask Register

The interrupt mask set/clear register enables the various TSB82AA2B interrupt sources. Reads from either the set register or the clear register always return the contents of the interrupt mask register. In all cases, except bit 31 (masterIntEnable) and bit 30 (VendorSpecific), the enables for each interrupt event align with the interrupt event register bits detailed in Table 4–16.

This register is fully compliant with *1394 Open Host Controller Interface Specification*, and the TSB82AA2B device adds a vendor-specific interrupt function to bit 30. See Table 4–17 for a description of bits 31 and 30.

Type: Read/Set/Clear/Update, Read/Set/Clear, Read/Update, Read only
Offset: 88h set register
8Ch clear register
Default: XXXX 0XXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	0	0	0	X	X	X	X	X	X	X	X	0	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X

Table 4–17. Interrupt Mask Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	masterIntEnable	RSCU	Master interrupt enable. If bit 31 is set to 1, the external interrupts are generated in accordance with the interrupt mask register. If bit 31 is cleared, the external interrupts are not generated regardless of the interrupt mask register settings.
30	VendorSpecific	RSC	When this bit and bit 30 (vendorSpecific) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this vendor-specific interrupt mask enables interrupt generation.
29	SoftInterrupt	RSC	When this bit and bit 29 (SoftInterrupt) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this soft-interrupt mask enables interrupt generation.
28	RSVD	R	Reserved. Bit 28 returns 0 when read.
27	ack_tardy	RSC	When this bit and bit 27 (ack_tardy) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this acknowledge-tardy interrupt mask enables interrupt generation.
26	phyRegRcvd	RSC	When this bit and bit 26 (phyRegRcvd) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this PHY-register interrupt mask enables interrupt generation.
25	cycleTooLong	RSC	When this bit and bit 25 (cycleTooLong) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this cycle-too-long interrupt mask enables interrupt generation.
24	unrecoverableError	RSC	When this bit and bit 24 (unrecoverableError) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this unrecoverable-error interrupt mask enables interrupt generation.
23	cycleInconsistent	RSC	When this bit and bit 23 (cycleInconsistent) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this inconsistent-cycle interrupt mask enables interrupt generation.
22	cycleLost	RSC	When this bit and bit 22 (cycleLost) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this lost-cycle interrupt mask enables interrupt generation.
21	cycle64Seconds	RSC	When this bit and bit 21 (cycle64Seconds) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this 64-second-cycle interrupt mask enables interrupt generation.

Table 4–17. Interrupt Mask Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
20	cycleSynch	RSC	When this bit and bit 20 (cycleSynch) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this isochronous-cycle interrupt mask enables interrupt generation.
19	phy	RSC	When this bit and bit 19 (phy) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this PHY-status-transfer interrupt mask enables interrupt generation.
18	regAccessFail	RSC	When this bit and bit 18 (regAccessFail) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this register-access-failed interrupt mask enables interrupt generation.
17	busReset	RSC	When this bit and bit 17 (busReset) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this bus-reset interrupt mask enables interrupt generation.
16	selfIDcomplete	RSC	When this bit and bit 16 (selfIDcomplete) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this self-ID-complete interrupt mask enables interrupt generation.
15	selfIDcomplete2	RSC	When this bit and bit 15 (selfIDcomplete2) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this second-self-ID-complete interrupt mask enables interrupt generation.
14–10	RSVD	R	Reserved. Bits 14–10 return 0s when read.
9	lockRespErr	RSC	When this bit and bit 9 (lockRespErr) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this lock-response-error interrupt mask enables interrupt generation.
8	postedWriteErr	RSC	When this bit and bit 8 (postedWriteErr) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this posted-write-error interrupt mask enables interrupt generation.
7	isochRx	RSC	When this bit and bit 7 (isochRx) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this isochronous-receive-DMA interrupt mask enables interrupt generation.
6	isochTx	RSC	When this bit and bit 6 (isochTx) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this isochronous-transmit-DMA interrupt mask enables interrupt generation.
5	RSPkt	RSC	When this bit and bit 5 (RSPkt) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this receive-response-packet interrupt mask enables interrupt generation.
4	RQPkt	RSC	When this bit and bit 4 (RQPkt) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this receive-request-packet interrupt mask enables interrupt generation.
3	ARRS	RSC	When this bit and bit 3 (ARRS) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this asynchronous-receive-response-DMA interrupt mask enables interrupt generation.
2	ARRQ	RSC	When this bit and bit 2 (ARRQ) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this asynchronous-receive-request-DMA interrupt mask enables interrupt generation.
1	respTxComplete	RSC	When this bit and bit 1 (respTxComplete) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this response-transmit-complete interrupt mask enables interrupt generation.
0	reqTxComplete	RSC	When this bit and bit 0 (reqTxComplete) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) are set to 1, this request-transmit-complete interrupt mask enables interrupt generation.

4.23 Isochronous Transmit Interrupt Event Register

The isochronous transmit interrupt event set/clear register reflects the interrupt state of the isochronous transmit contexts. An interrupt is generated on behalf of an isochronous transmit context if an OUTPUT_LAST* command completes and its interrupt bits are set to 1. Upon determining that the isochTx (bit 6) interrupt has occurred in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*), software can check this register to determine which context(s) caused the interrupt. The interrupt bits are set to 1 by an asserting edge of the corresponding interrupt signal, or by writing a 1 in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1 to the corresponding bit in the clear register. See Table 4–18 for a complete description of the register contents.

Type: Read/Set/Clear, Read only
Offset: 90h set register
94h clear register (returns the contents of the isochronous transmit interrupt event register bit-wise ANDed with the isochronous transmit interrupt mask register when read**)**
Default: 0000 00XXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

Table 4–18. Isochronous Transmit Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–8	RSVD	R	Reserved. Bits 31–8 return 0s when read.
7	isoXmit7	RSC	Isochronous transmit channel 7 caused the interrupt event register bit 6 (isochTx) interrupt.
6	isoXmit6	RSC	Isochronous transmit channel 6 caused the interrupt event register bit 6 (isochTx) interrupt.
5	isoXmit5	RSC	Isochronous transmit channel 5 caused the interrupt event register bit 6 (isochTx) interrupt.
4	isoXmit4	RSC	Isochronous transmit channel 4 caused the interrupt event register bit 6 (isochTx) interrupt.
3	isoXmit3	RSC	Isochronous transmit channel 3 caused the interrupt event register bit 6 (isochTx) interrupt.
2	isoXmit2	RSC	Isochronous transmit channel 2 caused the interrupt event register bit 6 (isochTx) interrupt.
1	isoXmit1	RSC	Isochronous transmit channel 1 caused the interrupt event register bit 6 (isochTx) interrupt.
0	isoXmit0	RSC	Isochronous transmit channel 0 caused the interrupt event register bit 6 (isochTx) interrupt.

4.24 Isochronous Transmit Interrupt Mask Register

The isochronous transmit interrupt mask set/clear register enables the isochTx interrupt source on a per-channel basis. Reads from either the set register or the clear register always return the contents of the isochronous transmit interrupt mask register. In all cases, the enables for each interrupt event align with the event register bits detailed in Table 4–18.

Type: Read/Set/Clear, Read only
Offset: 98h set register
9Ch clear register
Default: 0000 00XXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

4.25 Isochronous Receive Interrupt Event Register

The isochronous receive interrupt event set/clear register reflects the interrupt state of the isochronous receive contexts. An interrupt is generated on behalf of an isochronous receive context if an INPUT_* command completes and its interrupt bits are set to 1. Upon determining that the isochRx (bit 7) interrupt in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) has occurred, software can check this register to determine which context(s) caused the interrupt. The interrupt bits are set to 1 by an asserting edge of the corresponding interrupt signal, or by writing a 1 in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1 to the corresponding bit in the clear register. See Table 4–19 for a complete description of the register contents.

Type: Read/Set/Clear, Read only
Offset: A0h set register
A4h clear register (returns the contents of isochronous receive interrupt event register bit-wise ANDed with the isochronous receive mask register when read)
Default: 0000 000Xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X

Table 4–19. Isochronous Receive Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–4	RSVD	R	Reserved. Bits 31–4 return 0s when read.
3	isoRecv3	RSC	Isochronous receive channel 3 caused the interrupt event register bit 7 (isochRx) interrupt.
2	isoRecv2	RSC	Isochronous receive channel 2 caused the interrupt event register bit 7 (isochRx) interrupt.
1	isoRecv1	RSC	Isochronous receive channel 1 caused the interrupt event register bit 7 (isochRx) interrupt.
0	isoRecv0	RSC	Isochronous receive channel 0 caused the interrupt event register bit 7 (isochRx) interrupt.

4.26 Isochronous Receive Interrupt Mask Register

The isochronous receive interrupt mask set/clear register enables the isochRx interrupt source on a per-channel basis. Reads from either the set register or the clear register always return the contents of the isochronous receive interrupt mask register. In all cases, the enables for each interrupt event align with the isochronous receive interrupt event register bits detailed in Table 4–19.

Type: Read/Set/Clear, Read only
Offset: A8h set register
ACh clear register
Default: 0000 000Xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X

4.27 Initial Bandwidth Available Register

The initial bandwidth available register value is loaded into the corresponding bus management CSR register on a system (hardware) or software reset. See Table 4–20 for a complete description of the register contents.

Type: Read/Write, Read only
Offset: B0h
Default: 0000 1333h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1

Table 4–20. Initial Bandwith Available Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–13	RSVD	R	Reserved. Bits 31–13 return 0s when read.
12–0	InitBWAvailable	R/W	This field is reset to 1333h on a system (hardware) or software reset, and is not affected by a 1394 bus reset. The value of this field is loaded into the BANDWIDTH_AVAILABLE CSR register upon a $\overline{\text{G\_RST}}$, $\overline{\text{PCI\_RST}}$, or a 1394 bus reset.

4.28 Initial Channels Available High Register

The initial channels available high register value is loaded into the corresponding bus management CSR register on a system (hardware) or software reset. See Table 4–21 for a complete description of the register contents.

Offset: B4h
Type: Read/Write
Default: FFFF FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 4–21. Initial Channels Available High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–0	InitChanAvailHi	R/W	This field is reset to FFFF_FFFFh on a system (hardware) or software reset, and is not affected by a 1394 bus reset. The value of this field is loaded into the CHANNELS_AVAILABLE_HI CSR register upon a $\overline{\text{G\_RST}}$, $\overline{\text{PCI\_RST}}$, or a 1394 bus reset.

4.29 Initial Channels Available Low Register

The initial channels available low register value is loaded into the corresponding bus management CSR register on a system (hardware) or software reset. See Table 4–22 for a complete description of the register contents.

Offset: B8h
Type: Read/Write
Default: FFFF FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 4–22. Initial Channels Available Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–0	InitChanAvailLo	R/W	This field is reset to FFFF_FFFFh on a system (hardware) or software reset, and is not affected by a 1394 bus reset. The value of this field is loaded into the CHANNELS_AVAILABLE_LO CSR register upon a $\overline{\text{G\_RST}}$, $\overline{\text{PCI\_RST}}$, or a 1394 bus reset.

4.30 Fairness Control Register

The fairness control register provides a mechanism by which software can direct the host controller to transmit multiple asynchronous requests during a fairness interval. See Table 4–23 for a complete description of the register contents.

Type: Read-only
Offset: DCh
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–23. Fairness Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–8	RSVD	R	Reserved. Bits 31–8 return 0s when read.
7–0	pri_req	R/W	This field specifies the maximum number of priority arbitration requests for asynchronous request packets that the link is permitted to make of the PHY device during a fairness interval.

4.31 Link Control Register

The link control set/clear register provides the control flags that enable and configure the link core protocol portions of the TSB82AA2B device. It contains controls for the receiver and cycle timer. See Table 4–24 for a complete description of the register contents.

Type: Read/Set/Clear/Update, Read/Set/Clear, Read/Set, Read only
Offset: E0h set register
E4h clear register
Default: 00X0 0X00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	X	X	X	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	X	X	0	0	0	0	0	0	0	0	0

Table 4–24. Link Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–23	RSVD	R	Reserved. Bits 31–23 return 0s when read.
22	cycleSource	RSC	When bit 22 is set to 1, the cycle timer uses an external source (CYCLEIN) to determine when to roll over the cycle timer. When this bit is cleared, the cycle timer rolls over when the timer reaches 3072 cycles of the 24.576-MHz clock (125 μs).
21	cycleMaster	RSCU	When bit 21 is set to 1 and the PHY device has notified the TSB82AA2B device that PHY device is root, the TSB82AA2B device generates a cycle start packet every time the cycle timer rolls over, based on the setting of bit 22 (cycleSource). When bit 21 is cleared, the OHCI-Lynx accepts received cycle start packets to maintain synchronization with the node which is sending them. Bit 21 is automatically cleared when bit 25 (cycleTooLong) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) is set to 1. Bit 21 cannot be set to 1 until bit 25 (cycleTooLong) is cleared.
20	CycleTimerEnable	RSC	When bit 20 is set to 1, the cycle timer offset counts cycles of the 24.576-MHz clock and rolls over at the appropriate time, based on the settings of the above bits. When this bit is cleared, the cycle timer offset does not count.
19–11	RSVD	R	Reserved. Bits 19–11 return 0s when read.
10	RcvPhyPkt	RSC	When bit 10 is set to 1, the receiver accepts incoming PHY packets into the AR request context if the AR request context is enabled. This bit does not control receipt of self-ID packets.
9	RcvSelfID	RSC	When bit 9 is set to 1, the receiver accepts incoming self-ID packets. Before setting this bit to 1, software must ensure that the self-ID buffer pointer register contains a valid address.
8–7	RSVD	R	Reserved. Bits 8–7 return 0s when read.
6	tag1SyncFilterLock	RS	When this bit is set to 1, bit 6 (tag1SyncFilter) in the isochronous receive context match register (see Section 4.46, *Isochronous Receive Context Match Register*) is set to 1 for all isochronous receive contexts. When this bit is cleared, bit 6 (tag1SyncFilter) in the isochronous receive context match register has Read/Write access. This bit is cleared when $\overline{\text{G\_RST}}$ is asserted.
5–0	RSVD	R	Reserved. Bits 5–0 return 0s when read.

4.32 Node ID Register

The node ID register contains the address of the node on which the OHCI-Lynx chip resides, and indicates the valid node number status. The 16-bit combination of the busNumber field (bits 15–6) and the NodeNumber field (bits 5–0) is referred to as the node ID. See Table 4–25 for a complete description of the register contents.

Type: Read/Write/Update, Read/Update, Read-only
Offset: E8h
Default: 0000 FFXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	1	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X

Table 4–25. Node ID Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	iDValid	RU	ID valid. Bit 31 indicates whether or not the TSB82AA2B device has a valid node number. It is cleared when a 1394 bus reset is detected, and set to 1 when the TSB82AA2B device receives a new node number from its PHY device.
30	root	RU	Root. Bit 30 is set to 1 during the bus reset process if the attached PHY device is root.
29–28	RSVD	R	Reserved. Bits 29–28 return 0s when read.
27	CPS	RU	Cable power status. Bit 27 is set to 1 if the PHY device is reporting that cable power status is OK.
26–16	RSVD	R	Reserved. Bits 26–16 return 0s when read.
15–6	BusNumber	RWU	Bus number. This field identifies the specific 1394 bus the TSB82AA2B device belongs to when multiple 1394-compatible buses are connected via a bridge.
5–0	NodeNumber	RU	Node number. This field is the physical node number established by the PHY device during self-ID. It is automatically set to the value received from the PHY device after the self-ID phase. If the PHY device sets the NodeNumber to 63, software must not set bit 15 (run) in the asynchronous context control register (see Section 4.40, *Asynchronous Context Control Register*) for either of the AT DMA contexts.

4.33 PHY Control Register

The PHY control register reads from or writes to a PHY register. See Table 4–26 for a complete description of the register contents.

Type: Read/Write/Update, Read/Write, Read/Update, Read only
Offset: ECh
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–26. PHY Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	rdDone	RU	Bit 31 is cleared to 0 by the TSB82AA2B device when either bit 15 (rdReg) or bit 14 (wrReg) is set to 1. This bit is set to 1 when a register transfer is received from the PHY device.
30–28	RSVD	R	Reserved. Bits 30–28 return 0s when read.
27–24	rdAddr	RU	This field is the address of the register most recently received from the PHY device.
23–16	rdData	RU	This field is the contents of a PHY register that has been read.
15	rdReg	RWU	Bit 15 is set to 1 by software to initiate a read request to a PHY register, and is cleared by hardware when the request has been sent. Bits 14 (wrReg) and 15 (rdReg) must not both be set to 1 simultaneously.
14	wrReg	RWU	Bit 14 is set to 1 by software to initiate a write request to a PHY register, and is cleared by hardware when the request has been sent. Bits 14 (wrReg) and 15 (rdReg) must not both be set to 1 simultaneously.
13–12	RSVD	R	Reserved. Bits 13–12 return 0s when read.
11–8	regAddr	R/W	This field is the address of the PHY register to be written or read.
7–0	wrData	R/W	This field is the data to be written to a PHY register and is ignored for reads.

4.34 Isochronous Cycle Timer Register

The isochronous cycle timer register indicates the current cycle number and offset. When the TSB82AA2B device is cycle master, this register is transmitted with the cycle start message. When the TSB82AA2B device is not cycle master, this register is loaded with the data field in an incoming cycle start. In the event that the cycle start message is not received, the fields can continue incrementing on their own (if programmed) to maintain a local time reference. See Table 4–27 for a complete description of the register contents.

Type: Read/Write/Update
Offset: F0h
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 4–27. Isochronous Cycle Timer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–25	cycleSeconds	RWU	This field counts seconds [rollovers from bits 24–12 (cycleCount field)] modulo 128.
24–12	cycleCount	RWU	This field counts cycles [rollovers from bits 11–0 (cycleOffset field)] modulo 8000.
11–0	cycleOffset	RWU	This field counts 24.576-MHz clocks modulo 3072, that is, 125 μs. If an external 8-kHz clock configuration is being used, this field must be cleared to 0s at each tick of the external clock.

4.35 Asynchronous Request Filter High Register

The asynchronous request filter high set/clear register enables asynchronous receive requests on a per-node basis, and handles the upper node IDs. When a packet is destined for either the physical request context or the ARRQ context, the source node ID is examined. If the bit corresponding to the node ID is not set to 1 in this register, then the packet is not acknowledged and the request is not queued. The node ID comparison is done if the source node is on the same bus as the TSB82AA2B device. Nonlocal bus-sourced packets are not acknowledged unless bit 31 in this register is set to 1. None of the bits in this register can be accessed while a bus reset interrupt is pending in the interrupt event register at 80h/84h. See Table 4–28 for a complete description of the register contents.

Type: Read/Set/Clear
Offset: 100h set register
104h clear register
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–28. Asynchronous Request Filter High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	asynReqAllBuses	RSC	If bit 31 is set to 1, all asynchronous requests received by the TSB82AA2B device from nonlocal bus nodes are accepted.
30	asynReqResource62	RSC	If bit 30 is set to 1 for local bus node number 62, asynchronous requests received by the TSB82AA2B device from that node are accepted.
29	asynReqResource61	RSC	If bit 29 is set to 1 for local bus node number 61, asynchronous requests received by the TSB82AA2B device from that node are accepted.
28	asynReqResource60	RSC	If bit 28 is set to 1 for local bus node number 60, asynchronous requests received by the TSB82AA2B device from that node are accepted.
27	asynReqResource59	RSC	If bit 27 is set to 1 for local bus node number 59, asynchronous requests received by the TSB82AA2B device from that node are accepted.
26	asynReqResource58	RSC	If bit 26 is set to 1 for local bus node number 58, asynchronous requests received by the TSB82AA2B device from that node are accepted.
25	asynReqResource57	RSC	If bit 25 is set to 1 for local bus node number 57, asynchronous requests received by the TSB82AA2B device from that node are accepted.
24	asynReqResource56	RSC	If bit 24 is set to 1 for local bus node number 56, asynchronous requests received by the TSB82AA2B device from that node are accepted.
23	asynReqResource55	RSC	If bit 23 is set to 1 for local bus node number 55, asynchronous requests received by the TSB82AA2B device from that node are accepted.
22	asynReqResource54	RSC	If bit 22 is set to 1 for local bus node number 54, asynchronous requests received by the TSB82AA2B device from that node are accepted.
21	asynReqResource53	RSC	If bit 21 is set to 1 for local bus node number 53, asynchronous requests received by the TSB82AA2B device from that node are accepted.
20	asynReqResource52	RSC	If bit 20 is set to 1 for local bus node number 52, asynchronous requests received by the TSB82AA2B device from that node are accepted.
19	asynReqResource51	RSC	If bit 19 is set to 1 for local bus node number 51, asynchronous requests received by the TSB82AA2B device from that node are accepted.
18	asynReqResource50	RSC	If bit 18 is set to 1 for local bus node number 50, asynchronous requests received by the TSB82AA2B device from that node are accepted.
17	asynReqResource49	RSC	If bit 17 is set to 1 for local bus node number 49, asynchronous requests received by the TSB82AA2B device from that node are accepted.

Table 4–28. Asynchronous Request Filter High Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
16	asynReqResource48	RSC	If bit 16 is set to 1 for local bus node number 48, asynchronous requests received by the TSB82AA2B device from that node are accepted.
15	asynReqResource47	RSC	If bit 15 is set to 1 for local bus node number 47, asynchronous requests received by the TSB82AA2B device from that node are accepted.
14	asynReqResource46	RSC	If bit 14 is set to 1 for local bus node number 46, asynchronous requests received by the TSB82AA2B device from that node are accepted.
13	asynReqResource45	RSC	If bit 13 is set to 1 for local bus node number 45, asynchronous requests received by the TSB82AA2B device from that node are accepted.
12	asynReqResource44	RSC	If bit 12 is set to 1 for local bus node number 44, asynchronous requests received by the TSB82AA2B device from that node are accepted.
11	asynReqResource43	RSC	If bit 11 is set to 1 for local bus node number 43, asynchronous requests received by the TSB82AA2B device from that node are accepted.
10	asynReqResource42	RSC	If bit 10 is set to 1 for local bus node number 42, asynchronous requests received by the TSB82AA2B device from that node are accepted.
9	asynReqResource41	RSC	If bit 9 is set to 1 for local bus node number 41, asynchronous requests received by the TSB82AA2B device from that node are accepted.
8	asynReqResource40	RSC	If bit 8 is set to 1 for local bus node number 40, asynchronous requests received by the TSB82AA2B device from that node are accepted.
7	asynReqResource39	RSC	If bit 7 is set to 1 for local bus node number 39, asynchronous requests received by the TSB82AA2B device from that node are accepted.
6	asynReqResource38	RSC	If bit 6 is set to 1 for local bus node number 38, asynchronous requests received by the TSB82AA2B device from that node are accepted.
5	asynReqResource37	RSC	If bit 5 is set to 1 for local bus node number 37, asynchronous requests received by the TSB82AA2B device from that node are accepted.
4	asynReqResource36	RSC	If bit 4 is set to 1 for local bus node number 36, asynchronous requests received by the TSB82AA2B device from that node are accepted.
3	asynReqResource35	RSC	If bit 3 is set to 1 for local bus node number 35, asynchronous requests received by the TSB82AA2B device from that node are accepted.
2	asynReqResource34	RSC	If bit 2 is set to 1 for local bus node number 34, asynchronous requests received by the TSB82AA2B device from that node are accepted.
1	asynReqResource33	RSC	If bit 1 is set to 1 for local bus node number 33, asynchronous requests received by the TSB82AA2B device from that node are accepted.
0	asynReqResource32	RSC	If bit 0 is set to 1 for local bus node number 32, asynchronous requests received by the TSB82AA2B device from that node are accepted.

4.36 Asynchronous Request Filter Low Register

The asynchronous request filter low set/clear register enables asynchronous receive requests on a per-node basis, and handles the lower node IDs. Other than filtering different node IDs, this register behaves identically to the asynchronous request filter high register. None of the bits in this register can be accessed while a bus reset interrupt is pending in the interrupt event register at 80h/84h. See Table 4–29 for a complete description of the register contents.

Type: Read/Set/Clear
Offset: 108h set register
10Ch clear register
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–29. Asynchronous Request Filter Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	asynReqResource31	RSC	If bit 31 is set to 1 for local bus node number 31, asynchronous requests received by the TSB82AA2B device from that node are accepted.
30	asynReqResource30	RSC	If bit 30 is set to 1 for local bus node number 30, asynchronous requests received by the TSB82AA2B device from that node are accepted.
29–2	asynReqResourcen	RSC	Bits 29 through 2 (asynReqResourcen, where n = 29, 28, 27, …, 2) follow the same pattern as bits 31 and 30.
1	asynReqResource1	RSC	If bit 1 is set to 1 for local bus node number 1, asynchronous requests received by the TSB82AA2B device from that node are accepted.
0	asynReqResource0	RSC	If bit 0 is set to 1 for local bus node number 0, asynchronous requests received by the TSB82AA2B device from that node are accepted.

4.37 Physical Request Filter High Register

The physical request filter high set/clear register enables physical receive requests on a per-node basis, and handles the upper node IDs. When a packet is destined for the physical request context and the node ID has been compared against the ARRQ registers, the comparison is done again with this register. If the bit corresponding to the node ID is not set to 1 in this register, the request is handled by the ARRQ context instead of the physical request context. The node ID comparison is done if the source node is on the same bus as the TSB82AA2B device. Nonlocal bus sourced packets are not acknowledged unless bit 31 in this register is set to 1. See Table 4–30 for a complete description of the register contents.

Type: Read/Set/Clear
Offset: 110h set register
114h clear register
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–30. Physical Request Filter High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	physReqAllBusses	RSC	If bit 31 is set to 1, all physical requests received by the TSB82AA2B device from nonlocal bus nodes are accepted. Bit 31 is not cleared by a $\overline{\text{PCI\_RST}}$.
30	physReqResource62	RSC	If bit 30 is set to 1 for local bus node number 62, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
29	physReqResource61	RSC	If bit 29 is set to 1 for local bus node number 61, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
28	physReqResource60	RSC	If bit 28 is set to 1 for local bus node number 60, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
27	physReqResource59	RSC	If bit 27 is set to 1 for local bus node number 59, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
26	physReqResource58	RSC	If bit 26 is set to 1 for local bus node number 58, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
25	physReqResource57	RSC	If bit 25 is set to 1 for local bus node number 57, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
24	physReqResource56	RSC	If bit 24 is set to 1 for local bus node number 56, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
23	physReqResource55	RSC	If bit 23 is set to 1 for local bus node number 55, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
22	physReqResource54	RSC	If bit 22 is set to 1 for local bus node number 54, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
21	physReqResource53	RSC	If bit 21 is set to 1 for local bus node number 53, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
20	physReqResource52	RSC	If bit 20 is set to 1 for local bus node number 52, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
19	physReqResource51	RSC	If bit 19 is set to 1 for local bus node number 51, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
18	physReqResource50	RSC	If bit 18 is set to 1 for local bus node number 50, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
17	physReqResource49	RSC	If bit 17 is set to 1 for local bus node number 49, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.

Table 4–30. Physical Request Filter High Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
16	physReqResource48	RSC	If bit 16 is set to 1 for local bus node number 48, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
15	physReqResource47	RSC	If bit 15 is set to 1 for local bus node number 47, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
14	physReqResource46	RSC	If bit 14 is set to 1 for local bus node number 46, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
13	physReqResource45	RSC	If bit 13 is set to 1 for local bus node number 45, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
12	physReqResource44	RSC	If bit 12 is set to 1 for local bus node number 44, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
11	physReqResource43	RSC	If bit 11 is set to 1 for local bus node number 43, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
10	physReqResource42	RSC	If bit 10 is set to 1 for local bus node number 42, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
9	physReqResource41	RSC	If bit 9 is set to 1 for local bus node number 41, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
8	physReqResource40	RSC	If bit 8 is set to 1 for local bus node number 40, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
7	physReqResource39	RSC	If bit 7 is set to 1 for local bus node number 39, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
6	physReqResource38	RSC	If bit 6 is set to 1 for local bus node number 38, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
5	physReqResource37	RSC	If bit 5 is set to 1 for local bus node number 37, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
4	physReqResource36	RSC	If bit 4 is set to 1 for local bus node number 36, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
3	physReqResource35	RSC	If bit 3 is set to 1 for local bus node number 35, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
2	physReqResource34	RSC	If bit 2 is set to 1 for local bus node number 34, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
1	physReqResource33	RSC	If bit 1 is set to 1 for local bus node number 33, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
0	physReqResource32	RSC	If bit 0 is set to 1 for local bus node number 32, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.

4.38 Physical Request Filter Low Register

The physical request filter low set/clear register enables physical receive requests on a per-node basis, and handles the lower node IDs. When a packet is destined for the physical request context and the node ID has been compared against the asynchronous request filter registers, the node ID comparison is done again with this register. If the bit corresponding to the node ID is not set to 1 in this register, the request is handled by the asynchronous request context instead of the physical request context. See Table 4–31 for a complete description of the register contents.

Type: Read/Set/Clear
Offset: 118h set register
11Ch clear register
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–31. Physical Request Filter Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	physReqResource31	RSC	If bit 31 is set to 1 for local bus node number 31, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
30	physReqResource30	RSC	If bit 30 is set to 1 for local bus node number 30, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
29–2	physReqResourcen	RSC	Bits 29 through 2 (physReqResourcen, where n = 29, 28, 27, …, 2) follow the same pattern as bits 31 and 30.
1	physReqResource1	RSC	If bit 1 is set to 1 for local bus node number 1, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.
0	physReqResource0	RSC	If bit 0 is set to 1 for local bus node number 0, physical requests received by the TSB82AA2B device from that node are handled through the physical request context.

4.39 Physical Upper Bound Register (Optional Register)

The physical upper bound register is an optional register and is not implemented. This register returns all 0s when read.

Type: Read only
Offset: 120h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.40 Asynchronous Context Control Register

The asynchronous context control set/clear register controls the state and indicates status of the DMA context. See Table 4–32 for a complete description of the register contents.

Type: Read/Set/Clear/Update, Read/Set/Update, Read/Update, Read only
Offset:
- 180h set register (ATRQ)
- 184h clear register (ATRQ)
- 1A0h set register (ATRS)
- 1A4h clear register (ATRS)
- 1C0h set register (ARRQ)
- 1C4h clear register (ARRQ)
- 1E0h set register (ARRS)
- 1E4h clear register (ARRS)

Default: 0000 X0XXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Table 4–32. Asynchronous Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0s when read.
15	run	RSCU	Bit 15 is set to 1 by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The TSB82AA2B device changes this bit only on a system (hardware) or software reset.
14–13	RSVD	R	Reserved. Bits 14–13 return 0s when read.
12	wake	RSU	Software sets bit 12 to 1 to cause the TSB82AA2B device to continue or resume descriptor processing. The TSB82AA2B device clears this bit on every descriptor fetch.
11	dead	RU	The TSB82AA2B device sets bit 11 when it encounters a fatal error, and clears the bit when software clears bit 15 (run). Asynchronous contexts supporting out-of-order pipelining provide unique contextControl.dead functionality. See Section 7.7 in the *1394 Open Host Controller Interface Specification* (Revision 1.1) for more information.
10	active	RU	The TSB82AA2B device sets bit 10 to 1 when it is processing descriptors.
9	betaFrame	RU	Bit 9 is set to 1 when the PHY indicates that the received packet is sent in beta format. A response to a request sent using beta format also uses beta format.
8	RSVD	R	Reserved. Bit 8 returns 0 when read.
7–5	spd	RU	This field indicates the speed at which a packet was received or transmitted and only contains meaningful information for receive contexts. This field is encoded as: 000 = 100M bit/s 001 = 200M bit/s 010 = 400M bit/s 011 = 800M bit/s All other values are reserved.
4–0	eventcode	RU	This field holds the acknowledge sent by the link core for this packet or holds an internally generated error code if the packet was not transferred successfully.

4.41 Asynchronous Context Command Pointer Register

The asynchronous context command pointer register contains a pointer to the address of the first descriptor block that the TSB82AA2B device accesses when software enables the context by setting bit 15 (run) of the asynchronous context control register (see Section 4.40, *Asynchronous Context Control Register*) to 1. See Table 4–33 for a complete description of the register contents.

Type: Read/Write/Update
Offset: 18Ch (ATRQ)
1ACh (ATRS)
1CCh (ArRQ)
1ECh (ArRS)
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 4–33. Asynchronous Context Command Pointer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–4	descriptorAddress	RWU	Contains the upper 28 bits of the address of a 16-byte aligned descriptor block
3–0	Z	RWU	Indicates the number of contiguous descriptors at the address pointed to by the descriptor address. If Z is 0, it indicates that the descriptorAddress field (bits 31–4) is not valid.

4.42 Isochronous Transmit Context Control Register

The isochronous transmit context control set/clear register controls options, state, and status for the isochronous transmit DMA contexts. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3, …, 7). See Table 4–34 for a complete description of the register contents.

Type: Read/Set/Clear/Update, Read/Set/Clear, Read/Update, Read only
Offset: 200h + (16 * n) set register
204h + (16 * n) clear register
Default: XXXX X0XXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Table 4–34. Isochronous Transmit Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	cycleMatchEnable	RSCU	When bit 31 is set to 1, processing occurs such that the packet described by the context first descriptor block is transmitted in the cycle whose number is specified in the cycleMatch field (bits 30–16). The cycleMatch field (bits 30–16) must match the low-order two bits of cycleSeconds and the 13-bit cycleCount field in the cycle start packet that is sent or received immediately before isochronous transmission begins. Since the isochronous transmit DMA controller may work ahead, the processing of the first descriptor block may begin slightly in advance of the actual cycle in which the first packet is transmitted. The effects of this bit, however, are impacted by the values of other bits in this register and are explained in the *1394 Open Host Controller Interface Specification.* Once the context has become active, hardware clears this bit.
30–16	cycleMatch	RSC	This field contains a 15-bit value, corresponding to the low-order two bits of the isochronous cycle timer register at OHCI offset F0h (see Section 4.34, *Isochronous Cycle Timer Register*) cycleSeconds field (bits 31–25) and the cycleCount field (bits 24–12). If bit 31 (cycleMatchEnable) is set to 1, then this isochronous transmit DMA context becomes enabled for transmits when the low-order two bits of the isochronous cycle timer register cycleSeconds field (bits 31–25) and the cycleCount field (bits 24–12) value equal this field (cycleMatch) value.
15	run	RSC	Bit 15 is set to 1 by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The TSB82AA2B device changes this bit only on a system (hardware) or software reset.
14–13	RSVD	R	Reserved. Bits 14–13 return 0s when read.
12	wake	RSU	Software sets bit 12 to 1 to cause the TSB82AA2B device to continue or resume descriptor processing. The TSB82AA2B device clears this bit on every descriptor fetch.
11	dead	RU	The TSB82AA2B device sets bit 11 to 1 when it encounters a fatal error, and clears the bit when software clears bit 15 (run) to 0.
10	active	RU	The TSB82AA2B device sets bit 10 to 1 when it is processing descriptors.
9–5	RSVD	R	Reserved. Bits 9–5 return 0s when read.
4–0	event code	RU	Following an OUTPUT_LAST* command, the error code is indicated in this field. Possible values are: ack_complete, evt_descriptor_read, evt_data_read, and evt_unknown.

† On an overflow for each running context, the isochronous transmit DMA supports up to seven cycle skips when the following are true:

1. Bit 11 (dead) in either the isochronous transmit or receive context control register is set to 1.
2. Bits 4–0 (eventcode field) in either the isochronous transmit or receive context control register is set to evt_timeout.
3. Bit 24 (unrecoverableError) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) is set to 1.

4.43 Isochronous Transmit Context Command Pointer Register

The isochronous transmit context command pointer register contains a pointer to the address of the first descriptor block that the TSB82AA2B device accesses when software enables an isochronous transmit context by setting bit 15 (run) in the isochronous transmit context control register (see Section 4.42, *Isochronous Transmit Context Control Register*) to 1. The isochronous transmit DMA context command pointer can be read when a context is active. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3, …, 7).

Type: Read only
Offset: 20Ch + (16 * n)
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

4.44 Isochronous Receive Context Control Register

The isochronous receive context control set/clear register controls options, state, and status for the isochronous receive DMA contexts. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3). See Table 4–35 for a complete description of the register contents.

Type: Read/Set/Clear/Update, Read/Set/Clear, Read/Update, Read only
Offset: 400h + (32 * n) set register
404h + (32 * n) clear register
Default: XX00 X0XXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Table 4–35. Isochronous Receive Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	bufferFill	RSC	When bit 31 is set to 1, received packets are placed back to back to completely fill each receive buffer. When this bit is cleared, each received packet is placed in a single buffer. If bit 28 (multiChanMode) is set to 1, this bit must also be set to 1. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1.
30	isochHeader	RSC	When bit 30 is set to 1, received isochronous packets include the complete 4-byte isochronous packet header seen by the link layer. The end of the packet is marked with xferStatus in the first doublet, and a 16-bit time stamp indicating the time of the most recently received (or sent) cycleStart packet. When this bit is cleared, the packet header is stripped from received isochronous packets. The packet header, if received, immediately precedes the packet payload. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1.
29	cycleMatchEnable	RSCU	When bit 29 is set to 1 and the 13-bit cycleMatch field (bits 24–12) in the isochronous receive context match register (see Section 4.46, *Isochronous Receive Context Match Register*) matches the 13-bit cycleCount field in the cycleStart packet, the context begins running. The effects of this bit, however, are impacted by the values of other bits in this register. Once the context has become active, hardware clears this bit. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1.

Table 4–35. Isochronous Receive Context Control Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
28	multiChanMode	RSC	When bit 28 is set to 1, the corresponding isochronous receive DMA context receives packets for all isochronous channels enabled in the isochronous receive channel mask high register at OHCI offset 70h/74h (see Section 4.19, *Isochronous Receive Channel Mask High*) and isochronous receive channel mask low register at OHCI offset 78h/7Ch (see Section 4.20, *Isochronous Receive Channel Mask Low*). The isochronous channel number specified in the isochronous receive context match register (see Section 4.46, *Isochronous Receive Context Match Register*) is ignored. When this bit is cleared, the isochronous receive DMA context receives packets for the single channel specified in the isochronous receive context match register (see Section 4.46, *Isochronous Receive Context Match Register*). Only one isochronous receive DMA context may use the isochronous receive channel mask registers (see Sections 4.19, *Isochronous Receive Channel Mask High Register*, and 4.20, *Isochronous Receive Channel Mask Low Register*). If more than one isochronous receive context control register has this bit set, the results are undefined. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1.
27	dualBufferMode	RSC	When bit 27 is set to 1, receive packets are separated into first and second payload and streamed independently to the firstBuffer series and secondBuffer series as described in Section 10.2.3 in the *1394 Open Host Controller Interface Specification*. Also, when bit 27 is set to 1, both bits 28 (multiChanMode) and 31 (bufferFill) are cleared to 0. The value of this bit does not change when either bit 10 (active) or bit 15 (run) is set to 1.
26–16	RSVD	R	Reserved. Bits 27–16 return 0s when read.
15	run	RSCU	Bit 15 is set to 1 by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The TSB82AA2B device changes this bit only on a system (hardware) or software reset.
14–13	RSVD	R	Reserved. Bits 14 and 13 return 0s when read.
12	wake	RSU	Software sets bit 12 to 1 to cause the TSB82AA2B device to continue or resume descriptor processing. The TSB82AA2B device clears this bit on every descriptor fetch.
11	dead	RU	The TSB82AA2B device sets bit 11 to 1 when it encounters a fatal error, and clears the bit when software clears bit 15 (run).
10	active	RU	The TSB82AA2B device sets bit 10 to 1 when it is processing descriptors.
9	betaFrame	RU	Bit 9 is set to 1 when the PHY indicates that the received packet is sent in beta format. A response to a request sent using beta format also uses beta format.
8	RSVD	R	Reserved. Bit 8 returns 0 when read.
7–5	spd	RU	This field indicates the speed at which the packet was received. 000 = 100M bit/s 001 = 200M bit/s 010 = 400M bit/s 011 = 800M bit/s All other values are reserved.
4–0	event code	RU	For bufferFill mode, possible values are: ack_complete, evt_descriptor_read, evt_data_write, and evt_unknown. Packets with data errors (either dataLength mismatches or dataCRC errors) and packets for which a FIFO overrun occurred are backed out. For packet-per-buffer mode, possible values are ack_complete, ack_data_error, evt_long_packet, evt_overrun, evt_descriptor_read, evt_data_write, and evt_unknown.

† On an overflow for each running context, the isochronous transmit DMA supports up to seven cycle skips when the following are true:

1. Bit 11 (dead) in either the isochronous transmit or receive context control register is set to 1.
2. Bits 4–0 (eventcode field) in either the isochronous transmit or receive context control register is set to evt_timeout.
3. Bit 24 (unrecoverableError) in the interrupt event register at OHCI offset 80h/84h (see Section 4.21, *Interrupt Event Register*) is set to 1.

4.45 Isochronous Receive Context Command Pointer Register

The isochronous receive context command pointer register contains a pointer to the address of the first descriptor block that the TSB82AA2B device accesses when software enables an isochronous receive context by setting bit 15 (run) in the isochronous receive context control register (see Section 4.44, *Isochronous Receive Context Control Register*) to 1. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3).

Type: Read only
Offset: 40Ch + (32 * n)
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

4.46 Isochronous Receive Context Match Register

The isochronous receive context match register starts an isochronous receive context running on a specified cycle number, filters incoming isochronous packets based on tag values, and waits for packets with a specified sync value. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3). See Table 4–36 for a complete description of the register contents.

Type: Read/Write, Read only
Offset: 410Ch + (32 * n)
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	0	0	0	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X

Table 4–36. Isochronous Receive Context Match Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	tag3	R/W	If bit 31 is set to 1, this context matches on isochronous receive packets with a tag field of 11b.
30	tag2	R/W	If bit 30 is set to 1, this context matches on isochronous receive packets with a tag field of 10b.
29	tag1	R/W	If bit 29 is set to 1, this context matches on isochronous receive packets with a tag field of 01b.
28	tag0	R/W	If bit 28 is set to 1, this context matches on isochronous receive packets with a tag field of 00b.
27	RSVD	R	Reserved. Bit 27 returns 0 when read.
26–12	cycleMatch	R/W	Contains a 15-bit value, corresponding to the low-order two bits of cycleSeconds and the 13-bit cycleCount field in the cycleStart packet. If bit 29 (cycleMatchEnable) in the isochronous receive context control register (see Section 4.44, *Isochronous Receive Context Control Register*) is set to 1, this context is enabled for receives when the two low-order bits of the bus isochronous cycle timer register at OHCI offset F0h (see Section 4.34, *Isochronous Cycle Timer Register*) cycleSeconds field (bits 31–25) and cycleCount field (bits 24–12) value equal this field (cycleMatch) value.
11–8	sync	R/W	This 4-bit field is compared to the sync field of each isochronous packet for this channel when the command descriptor w field is set to 11b.
7	RSVD	R	Reserved. Bit 7 returns 0 when read.
6	tag1SyncFilter	R/W	If bit 6 and bit 29 (tag1) are set to 1, packets with tag 01b are accepted into the context if the two most significant bits of the packet sync field are 00b. Packets with tag values other than 01b are filtered according to bit 28 (tag0), bit 30 (tag2), and bit 31 (tag3) without any additional restrictions. If this bit is cleared, this context matches on isochronous receive packets as specified in bits 28–31 (tag0–tag3) with no additional restrictions.
5–0	channelNumber	R/W	This 6-bit field indicates the isochronous channel number for which this isochronous receive DMA context accepts packets.

5 TI Extension Registers

The TI extension base address register provides a method of accessing memory-mapped TI extension registers. The TI extension base address register is programmed with a base address referencing the memory-mapped TI extension registers. See Section 3.10, *TI Extension Base Address Register*, for register bit field details. See Table 5–1 for the TI extension register listing.

Table 5–1. TI Extension Register Map

REGISTER NAME	OFFSET
Reserved	00h–A7Fh
Isochronous Receive Digital Video Enhancements Set	A80h
Isochronous Receive Digital Video Enhancements Clear	A84h
Link Enhancement Control Set	A88h
Link Enhancement Control Clear	A8Ch
Isochronous Transmit Context 0 Timestamp Offset	A90h
Isochronous Transmit Context 1 Timestamp Offset	A94h
Isochronous Transmit Context 2 Timestamp Offset	A98h
Isochronous Transmit Context 3 Timestamp Offset	A9Ch
Isochronous Transmit Context 4 Timestamp Offset	AA0h
Isochronous Transmit Context 5 Timestamp Offset	AA4h
Isochronous Transmit Context 6 Timestamp Offset	AA8h
Isochronous Transmit Context 7 Timestamp Offset	AA8h

5.1 Digital Video (DV) Timestamp Enhancements

The DV timestamp enhancements are enabled by bit 8 (enab_dv_ts) in the link enhancement control register located at PCI offset F4h, and are aliased in TI extension register space at offset A88 (set) and A8Ch (clear).

The DV and MPEG transmit enhancements are enabled separately by bits in the link enhancement control register located in PCI configuration space at PCI offset F4h. The link enhancement control register is also aliased as a set/clear register in TI extension space at offset A88h (set) and A8Ch (clear).

Bit 8 (enab_dv_ts) of the link enhancement control register enables DV timestamp support. When enabled, the link calculates a timestamp based on the cycle timer and the timestamp offset register and substitutes it in the SYT field of the CIP once per DV frame.

Bit 10 (enab_mpeg_ts) of the link enhancement control register enables MPEG timestamp support. Two MPEG timestamp modes are supported. The default mode calculates an initial delta that is added to the calculated timestamp in addition to a user-defined offset. The initial offset is calculated as the difference in the intended transmit cycle count and the cycle count field of the timestamp in the first TSP of the MPEG2 stream. The use of the initial delta can be controlled by bit 31 (DisableInitialOffset) in the timestamp offset register (see Section 5.6, *Timestamp Offset Register*).

5.2 MPEG2 Timestamp Procedure

The MPEG2 timestamp enhancements are enabled by bit 10 (enab_mpeg_ts) in the link enhancement control register located at PCI offset F4h, and aliased in TI extension register space at offset A88h (set) and A8Ch (clear).

When bit 10 (enab_mpeg_ts) is set to 1, the hardware applies the timestamp enhancements to isochronous transmit packets that have the tag field equal to 01b in the isochronous packet header and a FMT field equal to 10h.

5.3 Isochronous Receive DV Enhancements

The DV frame sync and branch enhancement provides a mechanism in buffer-fill mode to synchronize 1394 DV data that is received in the correct order to DV frame-sized data buffers described by several INPUT_MORE descriptors (see *1394 Open Host Controller Interface Specification*, Revision 1.1). This is accomplished by waiting for the start-of-frame packet in a DV stream before transferring the received isochronous stream into the memory buffer described by the INPUT_MORE descriptors. This can improve the DV capture application performance by reducing the amount of processing overhead required to strip the CIP header and copy the received packets into frame-sized buffers.

The start of a DV frame is represented in the 1394 packet as a 16-bit pattern of 1FX7h (first byte 1Fh and second byte X7h) received as the first two bytes of the third quadlet in a DV isochronous packet. The TSB12LV23 OHCI-Lynx uses a field match of 1F07h to sync the frame. However, this does not accommodate all camcorder cases. To accommodate these models, the TSB82AA2B uses the pattern 1FX7h.

5.4 Isochronous Receive Digital Video Enhancements Register

The isochronous receive digital video enhancements register enables the DV enhancements in the TSB82AA2B device. The bits in this register may only be modified when both the active (bit 10) and run (bit 15) bits of the corresponding context control register are 0. See Table 5–2 for a complete description of the register contents.

Offset: A80h set register
A84h clear register
Type: Read/Set/Clear, Read only
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–2. Isochronous Receive Digital Video Enhancements Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–14	RSVD	R	Reserved. Bits 31–14 return 0s when read.
13	DV_Branch3	RSC	When bit 13 is set to 1, the isochronous receive context 3 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b, and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is only interpreted when bit 12 (CIP_Strip3) is 1 and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 460h/464h (see Section 4.44, *Isochronous Receive Context Control Register*) is 0.
12	CIP_Strip3	RSC	When bit 12 is set to 1, the isochronous receive context 3 strips the first two quadlets of payload. This bit is only interpreted when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 460h/464h (see Section 4.44, *Isochronous Receive Context Control Register*) is 0.
11–10	RSVD	R	Reserved. Bits 11 and 10 return 0s when read.
9	DV_Branch2	RSC	When bit 9 is set to 1, the isochronous receive context 2 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b, and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is only interpreted when bit 8 (CIP_Strip2) is 1 and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 440h/444h (see Section 4.44, *Isochronous Receive Context Control Register*) is 0.
8	CIP_Strip2	RSC	When bit 8 is set to 1, the isochronous receive context 2 strips the first two quadlets of payload. This bit is only interpreted when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 440h/444h (see Section 4.44, *Isochronous Receive Context Control Register*) is 0.
7–6	RSVD	R	Reserved. Bits 7 and 6 return 0s when read.
5	DV_Branch1	RSC	When bit 5 is set to 1, the isochronous receive context 1 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b, and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is only interpreted when bit 4 (CIP_Strip1) is 1 and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 420h/424h (see Section 4.44, *Isochronous Receive Context Control Register*) is 0.

Table 5–2. Isochronous Receive Digital Video Enhancements Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
4	CIP_Strip1	RSC	When bit 4 is set to 1, the isochronous receive context 1 strips the first two quadlets of payload. This bit is only interpreted when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 420h/424h (see Section 4.44, *Isochronous Receive Context Control Register*) is 0.
3–2	RSVD	R	Reserved. Bits 3 and 2 return 0s when read.
1	DV_Branch0	RSC	When bit 1 is set to 1, the isochronous receive context 0 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is only interpreted when bit 0 (CIP_Strip0) is 1 and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 400h/404h (see Section 4.44, *Isochronous Receive Context Control Register*) is 0.
0	CIP_Strip0	RSC	When bit 0 is set to 1, the isochronous receive context 0 strips the first two quadlets of payload. This bit is only interpreted when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 400h/404h (see Section 4.44, *Isochronous Receive Context Control Register*) is 0.

5.5 Link Enhancement Control Register

This register is a memory-mapped set/clear register that is an alias of the link enhancement control register at PCI offset F4h. These bits may be initialized by software. Some of the bits may also be initialized by a serial EEPROM, if one is present, as noted in the bit descriptions below. If the bits are to be initialized by software, then the bits must be initialized prior to setting bit 19 (LPS) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*). See Table 5–3 for a complete description of the register contents.

Offset: A88h set register
A8Ch clear register
Type: Read/Set/Clear, Read/Write, Read only
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–3. Link Enhancement Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0s when read.
15	dis_at_pipeline	RSC	Disable AT pipelining. When bit 15 is set to 1, out-of-order AT pipelining is disabled.
14	RSVD	R	Reserved
13–12	atx_thresh	RSC	This field sets the initial AT threshold value, which is used until the AT FIFO is underrun. When the TSB82AA2B device retries the packet, it uses a 2-Kbyte threshold, resulting in a store-and-forward operation. 00 = Threshold ~4K bytes resulting in a store-and-forward operation (default) 01 = Threshold ~1.7K bytes 10 = Threshold ~1K bytes 11 = Threshold ~512 bytes These bits fine tune the asynchronous transmit threshold. For most applications, the 1.7-K threshold is optimal. Changing this value may increase or decrease the 1394 latency depending on the average PCI bus latency. Setting the AT threshold to 1.7K, 1K, or 512 bytes results in data being transmitted at these thresholds or when an entire packet has been checked into the FIFO. If the packet to be transmitted is larger than the AT threshold, the remaining data must be received before the AT FIFO is emptied; otherwise, an underrun condition occurs, resulting in a packet error at the receiving node. As a result, the link then commences store-and-forward operation — that is, wait until it has the complete packet in the FIFO before retransmitting it on the second attempt, to ensure delivery. An AT threshold of 4K results in store-and-forward operation, which means that asynchronous data is not transmitted until an end-of-packet token is received. Restated, setting the AT threshold to 4K results in only complete packets being transmitted. Note that this device always uses store-and-forward when the asynchronous transmit retries register at OHCI offset 08h (see Section 4.3, *Asynchronous Transmit Retries Register*) is cleared.
11	RSVD	R	Reserved. Bit 11 returns 0 when read.
10	RSVD	R	Reserved. Bit 10 returns 0 when read.
9	enab_aud_ts	R/W	Enable audio/music CIP timestamp enhancement. When bit 9 is set to 1, the enhancement is enabled for audio/music CIP transmit streams (FMT = 10h).
8	enab_dv_ts	RSC	Enable DV CIP timestamp enhancement. When bit 8 is set to 1, the enhancement is enabled for DV CIP transmit streams (FMT = 00h).
7	enab_unfair	RSC	Enable asynchronous priority requests (OHCI-Lynx compatible). Setting bit 7 to 1 enables the link to respond to requests with priority arbitration. It is recommended that this bit be set to 1.

Table 5–3. Link Enhancement Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
6	RSVD	R	This bit is not assigned in the TSB82AA2B follow-on products, since this bit location loaded by the serial EEPROM from the enhancements field corresponds to bit 23 (programPhyEnable) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*).
5–3	RSVD	R	Reserved. Bits 5–3 return 0s when read.
2	enab_insert_idle	RSC	Enable insert idle (OHCI-Lynx compatible). When the PHY layer has control of the PHY_CTL0–PHY_CTL1 internal control lines and PHY_DATA0–PHY_DATA7 internal data lines and the link requests control, the PHY drives 11b on the PHY_CTL0–PHY_CTL1 internal lines. The link can then start driving these lines immediately. Setting bit 2 to 1 inserts an idle state, so the link waits one clock cycle before it starts driving the lines (turnaround time).
1	enab_accel	RSC	Enable acceleration enhancements (OHCI-Lynx compatible). When bit 1 is set to 1, the PHY is notified that the link supports IEEE Std 1394a-2000 acceleration enhancements, that is, ack-accelerated, fly-by concatenation, etc. It is recommended that this bit be set to 1.
0	RSVD	R	Reserved. Bit 0 returns 0 when read.

5.6 Isochronous Transmit Context n Timestamp Offset Registers

The value of these registers is added as an offset to the cycle timer value when using the MPEG, DV, and CIP enhancements. A timestamp offset register is implemented per isochronous transmit context. The n value following the offset indicates the context number (n = 0, 1, 2, 3, …, 7). These registers are programmed by software as appropriate. See Table 5–4 for a complete description of the register contents.

Offset: A90h + (4*n)
Type: Read/Write, Read only
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–4. Isochronous Transmit Context n Timestamp Offset Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	DisableInitialOffset	R/W	Bit 31 disables the use of the initial timestamp offset when the MPEG2 enhancements are enabled. A value of 0 indicates the use of the initial offset; a value of 1 indicates that the initial offset must not be applied to the calculated timestamp. This bit has no meaning for the DV timestamp enhancements.
30–25	RSVD	R	Reserved. Bits 30–25 return 0s when read.
24–12	CycleCount	R/W	This field adds an offset to the cycle count field in the timestamp when the DV or MPEG2 enhancements are enabled. The cycle count field is incremented modulo 8000; therefore, values in this field must be limited between 0 and 7999.
11–0	CycleOffset	R/W	This field adds an offset to the cycle offset field in the timestamp when the DV or MPEG2 enhancements are enabled. The cycle offset field is incremented modulo 3072; therefore, values in this field must be limited between 0 and 3071.

6 General-Purpose Input/Output (GPIO) Interface

The GPIO interface consists of one GPIO port available via the MFUNC terminal by configuring the multifunction configuration register (PCI offset E8h). GPIO powers up as a general-purpose input and is programmable via the GPIO control register. Figure 6–1 shows the logic diagram for GPIO implementation.

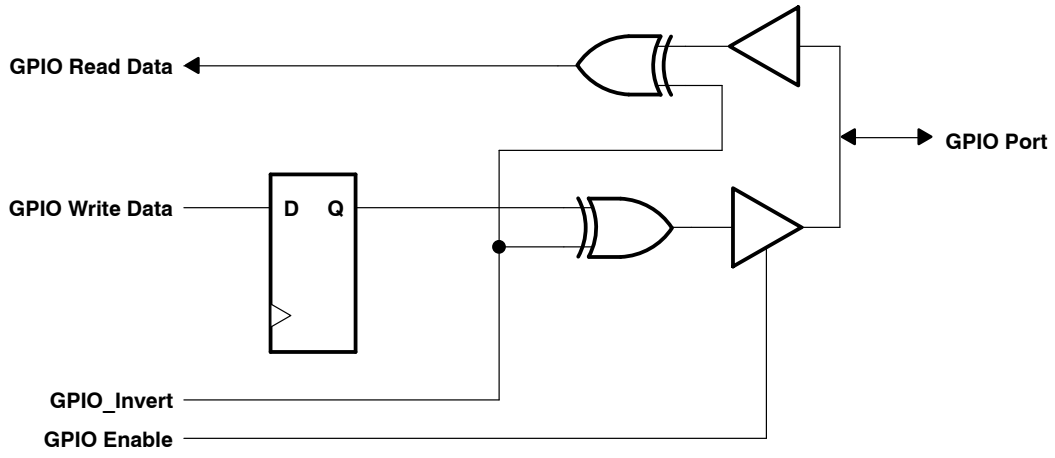


Figure 6–1. GPIO Logic Diagram

7 Serial EEPROM Interface

The TSB82AA2B device provides a serial bus interface to initialize the 1394 global unique ID register and a few PCI configuration registers through a serial EEPROM. The TSB82AA2B device communicates with the serial EEPROM via the 2-wire serial interface.

After power up, the serial interface initializes the locations listed in Table 7–1. While the TSB82AA2B device accesses the serial EEPROM, all incoming PCI slave accesses are terminated with retry status. Table 7–1 shows the serial EEPROM memory map required for initializing the TSB82AA2B registers.

> **NOTE:** If a ROM is implemented in the design, it must be programmed. An unprogrammed ROM defaults to all 1s, which could adversely impact device operation.

Table 7–1. Serial EEPROM Map

BYTE ADDRESS	BYTE DESCRIPTION							
00	PCI maximum latency (PCI offset 3Eh)					PCI minimum grant (PCI offset 3Fh)		
01	PCI subsystem vendor ID alias (lsbyte) (PCI offset F8h)							
02	PCI subsystem vendor ID alias (msbyte) (PCI offset F9h)							
03	PCI subsystem ID alias (lsbyte) (PCI offset FAh)							
04	PCI subsystem ID alias (msbyte) (PCI offset FBh)							
05	[7] Link_enhancement Control.enab_unfair (PCI offset F4h, bit 7)	[6] HCControl. ProgramPhy Enable (OHCI offset 50h, bit 23)	[5–3] RSVD			[2] Link_enhancement Control.enab_ insert_idle (PCI offset F4h, bit 2)	[1] Link_enhancement Control.enab_accel (PCI offset F4h, bit 1)	[0] RSVD
06	[7–6] RSVD		[5] † MiniRom enable (OHCI offset 04h, bit 5)		[4–0] RSVD			
07	1394 GUID high (lsbyte 0) (OHCI offset 24h)							
08	1394 GUID high (byte 1) (OHCI offset 25h)							
09	1394 GUID high (byte 2) (OHCI offset 26h)							
0A	1394 GUID high (msbyte 3) (OHCI offset 27h)							
0B	1394 GUID low (lsbyte 0) (OHCI offset 28h)							
0C	1394 GUID low (byte 1) (OHCI offset 29h)							
0D	1394 GUID low (byte 2) (OHCI offset 30h)							
0E	1394 GUID low (msbyte 3) (OHCI offset 31h)							
0F	Checksum							
10	[15] Link Enhancement.dis_ at_pipeline (PCI offset F4h, bit 15)	[14] Enab_draft (PCI offset F4h, bit 14)	[13–12] Link Enhancement.atx_ thresh (PCI offset F4h, bits 13–12)		[11–8] RSVD			
11	[7] RSVD	[6] MiscConfig. cardbus (PCI offset F0h, bit 6)	[5] RSVD	[4] MiscConfi g.dis_tgt_ abt (PCI offset F0h, bit 4	[3] RSVD	[2] MiscConfig.disable _sclkgate (PCI offset F0h, bit 2)	[1] MiscConfig.disable _pcigate (PCI offset F0h, bit 1)	[0] MiscConfi g.keep_pcl k (PCI offset F0h, bit 0)
12	[15] MiscConfig.PME_D 3cold (PCI offset F0h, bit 15)	[14–11] RSVD				[10] ignore_IntEvent. MasterIntEnable_ for_pme (PCI offset F0h, bit 10)	[9–8] MR_Enhance (PCI offset F0h, bits 9–8)	
13	[7–4] BusOptions.Max_Rec (OHCI offset 20h, bits 15–12)				[3–0] RSVD			
14	[7–3] CIS offset (PCI offset 28h, bits 7–3)					[2–0] RSVD		
15–16	[7–0] RSVD							
17	[7–3] RSVD					[2–0] MultifunctionSelect.MFunc_Sel (PCI offset E8h, bits 2–0)		
18–1F	RSVD							

† If bit 5 at EEPROM byte offset 06h is set, the mini-ROM is enabled and the starting address is 20h.

8 Electrical Characteristics

8.1 Absolute Maximum Ratings Over Operating Temperature Ranges†

Supply voltage range: V_{CC} . . . . . −0.5 V to 3.6 V

V_{CCP} . . . . . −0.5 V to 5.5 V

Input voltage range for PCI, V_I . . . . . −0.5 to V_{CCP} + 0.5 V

Input voltage range for PHY interface, V_I . . . . . −0.5 to V_{CC} + 0.5 V

Output voltage range for PCI, V_O . . . . . −0.5 to V_{CC} + 0.5 V

Output voltage range for PHY interface, V_O . . . . . −0.5 to V_{CC} + 0.5 V

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1) . . . . . ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 2) . . . . . ±20 mA

Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Applies to external input and bidirectional buffers. $V_I > V_{CCP}$.

2. Applies to external output and bidirectional buffers. $V_O > V_{CCP}$.

8.2 Recommended Operating Conditions

			OPERATION	MIN	NOM	MAX	UNIT
V_{CC}	Core voltage	Commercial	3.3 V	3	3.3	3.6	V
V_{CCP}	PCI I/O clamping voltage	Commercial	3.3 V	3	3.3	3.6	V
			5 V	4.5	5	5.5	
V_{IH}†	High-level input voltage	PCI	3.3 V	$0.475V_{CCP}$		V_{CCP}	V
			5 V	2		V_{CCP}	
		PHY interface		2		3.6	
V_{IL}†	Low-level input voltage	PCI	3.3 V	0		$0.325V_{CCP}$	V
			5 V	0		0.8	
		PHY interface		0		0.8	
V_I	Input voltage	PCI	3.3 V	0		V_{CCP}	V
		PHY interface		0		3.6	
V_O‡	Output voltage	PCI	3.3 V	0		V_{CCP}	V
		PHY interface		0		3.6	
t_t	Input transition time (t_r and t_f)	PCI		0		6	ns
T_A	Operating ambient temperature	TSB82AA2B		0	25	70	°C
		TSB82AA2BI		−40		85	
T_J§	Virtual junction temperature			0	25	115	°C

† Applies to external inputs and bidirectional buffers without hysteresis.
‡ Applies to external output buffers.
§ The junction temperatures reflect simulation conditions. Customer is responsible for verifying junction temperature.

8.3 Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

			OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	PCI		I_{OH} = – 0.5 mA	$0.9V_{CC}$		V
				I_{OH} = – 2 mA	2.4		
		PHY interface		I_{OH} = – 4 mA	2.8		
				I_{OH} = – 8 mA	V_{CC} – 0.6		
V_{OL}†	Low-level output voltage	PCI		I_{OL} = 1.5 mA		$0.1V_{CC}$	V
				I_{OL} = 6 mA		0.55	
		$\overline{\text{PCI\_PME}}$		I_{OL} = 4 mA		0.5	
		PHY interface		I_{OL} = 8 mA		0.5	
I_{OZ}	3-state output high impedance	Output terminals	3.6 V	$V_O = V_{CC}$ or GND		±20	µA
I_{IL}	Low-level input current	Input terminals	3.6 V	V_I = GND‡		±20	µA
		I/O terminals†	3.6 V	V_I = GND‡	±20		
I_{IH}	High-level input current	PCI†	3.6 V	$V_I = V_{CC}$‡		±20	µA
		Others†	3.6 V	$V_I = V_{CC}$‡	±20		

† For I/O terminals, input leakage (I_{IL} and I_{IH}) includes I_{OZ} of the disabled output.

8.4 Switching Characteristics for PCI Interface‡

PARAMETER		MIN	TYP	MAX	UNIT
t_{su}	Setup time before PCLK	7			ns
t_h	Hold time after PCLK	0			ns
t_{val}	Delay time, PCLK to data valid	2		11	ns

‡ These parameters are specified by design.

8.5 Switching Characteristics for PHY-Link Interface‡

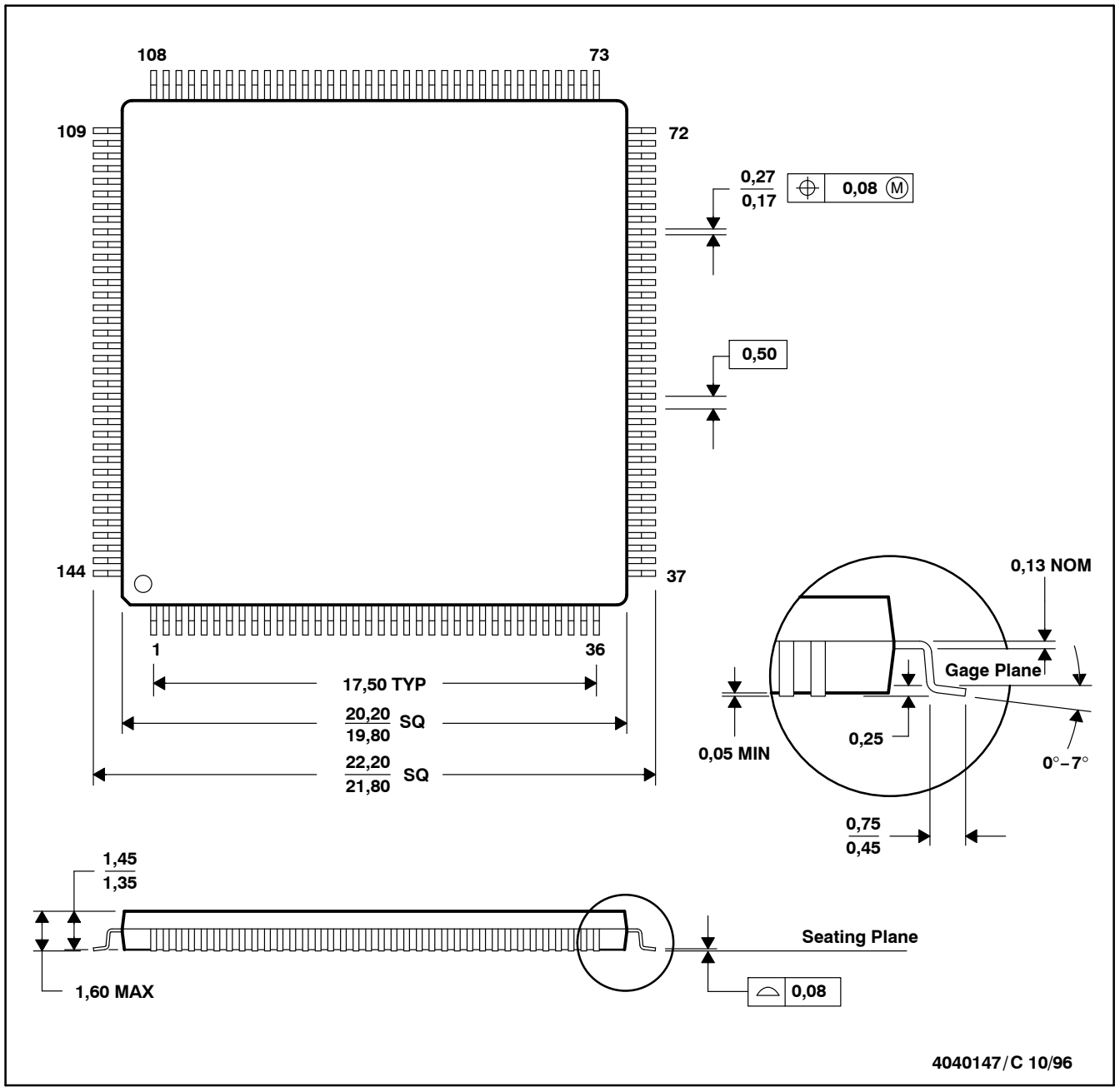
PARAMETER		MIN	TYP	MAX	UNIT
t_{su}	Setup time, Dn, CTLn, LREQ to PHY_CLK	6			ns
t_h	Hold time, Dn, CTLn, LREQ after PHY_CLK	0			ns
t_d	Delay time, PHY_CLK to Dn, CTLn	1		10	ns

‡ These parameters are specified by design.

9 Mechanical Information

The TSB82AA2B is packaged in a 144-terminal PGE and a 176-ball ZGW package. The following shows the mechanical dimensions for the PGE and ZGW packages.

PGE (S-PQFP-G144) Plastic Quad Flatpack



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSB82AA2BIPGE	ACTIVE	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TSB82AA2BI	Samples
TSB82AA2BPGE	ACTIVE	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TSB82AA2B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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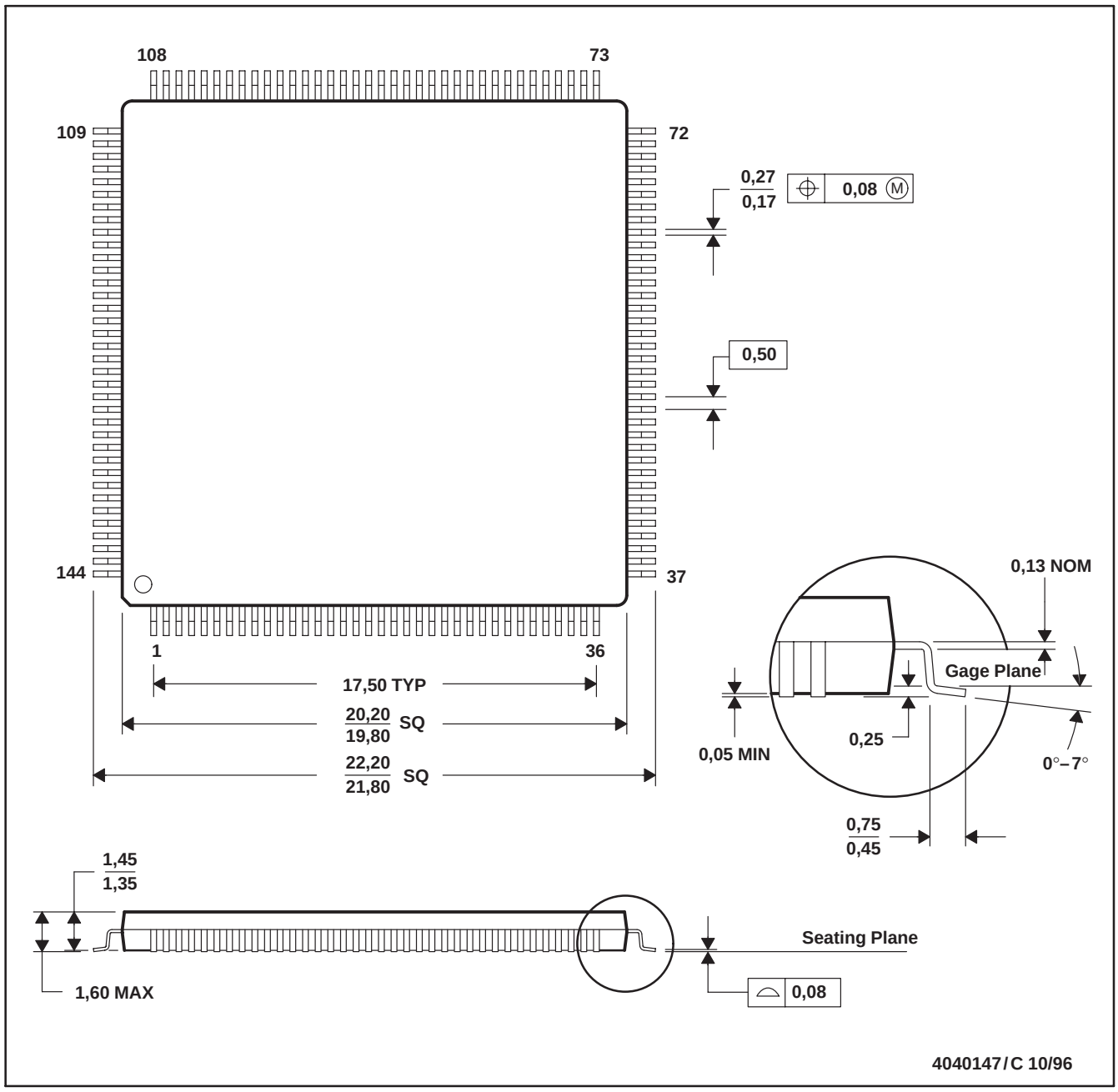

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