TSM104W, TSM104WA
QUAD OPERATIONAL AMPLIFIER AND PROGRAMMABLE VOLTAGE REFERENCE

SLOS478D – JULY 2005 – REVISED AUGUST 2006

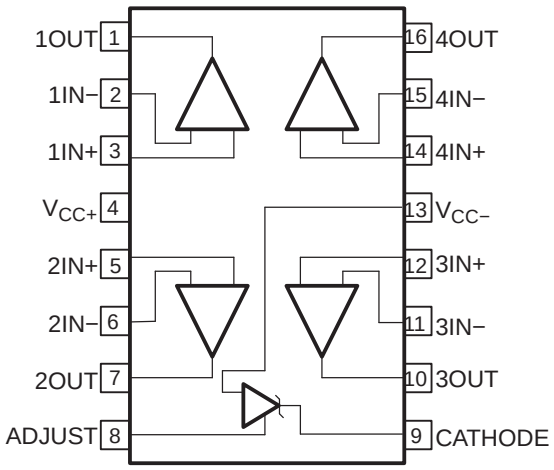
FEATURES

- **OPERATIONAL AMPLIFIER**
  - **Low Offset Voltage, Max of:**
    - **TSM104WA…3 mV (25°C) and 4 mV (Full Temperature)**
    - **TSM104W…5 mV (25°C) and 6 mV (Full Temperature)**
  - **Low Supply Current…375 μA/Channel Typ at V_{CC} = 5 V**
  - **Unity Gain Bandwidth…0.9 MHz Typ**
  - **Input Common-Mode Range Includes GND**
  - **Large Output-Voltage Swing…0 V to V_{CC} – 2 V**
  - **Wide Supply-Voltage Range…3 V to 30 V**
  - **2-kV ESD Protection (HBM)**
- **VOLTAGE REFERENCE**
  - **Adjustable Output Voltage…V_{REF} to 36 V**
  - **V_{REF} = 2.5 V With Tight Tolerance, Max of:**
    - **TSM104WA…0.4% (25°C) and 0.8% (Full Temperature)**
    - **TSM104W…1% (25°C) and 2% (Full Temperature)**
  - **Low Temperature Drift…7 mV Typ Over Operating Temperature Range**
  - **Wide Sink-Current Range…0.5 mA Typ to 100 mA**
  - **Output Impedance…0.2 Ω Typ**

TYPICAL APPLICATIONS

- **Battery Chargers**
- **Switch-Mode Power Supplies**
- **Linear Voltage Regulation**
- **Data-Acquisition Systems**

D (SOIC), N (PDIP), OR PW (TSSOP) PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TSM104W combines the building blocks of a quad operational amplifier and an adjustable voltage reference, both of which often are used in the control circuitry of switch-mode power supplies.

For the A grade, especially tight voltage regulation can be achieved through the low offset voltage for each operational amplifier (typically 0.5 mV) and tight tolerance for the voltage reference (0.4% at 25°C and 0.8% over operating temperature range).

The TSM104W and TSM104WA are characterized for operation from –40°C to 105°C.

ORDERING INFORMATION

T_A	MAX V_{IO} AND V_{REF} TOLERANCE (25°C)	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	A grade 3 mV, 0.4%	PDIP – N	Tube of 25	TSM104WAIN	PREVIEW
		SOIC – D	Tube of 75	TSM104WAID	TSM104WAI
			Reel of 2500	TSM104WAIDR	
		TSSOP – PW	Tube of 75	TSM104WAIPW	SM104AI
			Reel of 2000	TSM104WAIPWR	
	Standard grade 5 mV, 1%	PDIP – N	Tube of 25	TSM104WIN	PREVIEW
		SOIC – D	Tube of 75	TSM104WID	TSM104WI
			Reel of 2500	TSM104WIDR	
		TSSOP – PW	Tube of 75	TSM104WIPW	SM104I
			Reel of 2000	TSM104WIPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Absolute Maximum Ratings(1)

over free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage			36	V
V_{ID}	Operational amplifier input differential voltage			36	V
V_I	Operational amplifier input voltage range		–0.3	36	V
I_{KA}	Voltage reference cathode current			100	mA
θ_{JA}	Package thermal impedance(2)(3)	D package		73	°C/W
		N package		67	
		PW package		108	
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC+} – V_{CC–}$	Supply voltage	3	30	V
I_K	Cathode current	1	100	mA
T_A	Operating free-air temperature	–40	105	°C

Total Device Electrical Characteristics

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{CC}	Total supply current, excluding cathode-current reference	V_{CC+} = 5 V, No load	Full range		1.4	2.4	mA
		V_{CC+} = 30 V, No load				4	

Operational Amplifier Electrical Characteristics

V_{CC+} = 5 V, V_{CC-} = GND, V_O = 1.4 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TSM104W		25°C		1	5	mV
				Full range			6	
		TSM104WA		25°C		0.5	3	
				Full range			4	
αV_{IO}	Input offset voltage drift			25°C		7		µV/°C
I_{IO}	Input offset current			25°C		2	30	nA
				Full range			50	
I_{IB}	Input bias current			25°C		30	150	nA
				Full range			200	
A_{VD}	Large-signal voltage gain		V_{CC+} = 15 V, R_L = 2 kΩ, V_O = 1.4 V to 11.4 V	25°C	50	100		V/mV
				Full range	25			
k_{SVR}	Supply-voltage rejection ratio		V_{CC+} = 5 V to 30 V	25°C	65	100		dB
V_{ICR}	Input common-mode voltage range		V_{CC+} = 30 V(1)	25°C	0		V_{CC+} – 1.5	V
				Full range	0		V_{CC+} – 2	
CMRR	Common-mode rejection ratio			25°C	70	85		dB
				Full range	60			
I_{source}	Output source current		V_{CC+} = 15 V, V_O = 2 V, V_{id} = 1 V	25°C	20	40		mA
I_{SC}	Short circuit to GND		V_{CC+} = 15 V	25°C		40	60	mA
I_{sink}	Output sink current		V_{CC+} = 15 V, V_O = 2 V, V_{id} = –1 V	25°C	10	20		mA
V_{OH}	High-level output voltage		V_{CC+} = 30 V, R_L = 10 kΩ	25°C	27	28		V
				Full range	27			
V_{OL}	Low-level output voltage		R_L = 10 kΩ	25°C		5	20	mV
				Full range			20	
SR	Slew rate at unity gain		V_{CC+} = 15 V, C_L = 100 pF, R_L = 2 kΩ, V_I = 0.5 V to 3 V, unity gain	25°C	0.1	0.3		V/µs
GBW	Gain bandwidth product		V_{CC+} = 30 V, V_I = 10 mV, C_L = 100 pF, R_L = 2 kΩ, f = 100 kHz	25°C	0.5	0.9		MHz
THD	Total harmonic distortion		V_{CC+} = 30 V, V_O = 2 V_{pp}, C_L = 100 pF, R_L = 2 kΩ, f = 1 kHz, A_V = 20 dB	25°C		0.01		%
V_n	Equivalent input noise voltage		V_{CC} = 30 V, R_S = 100 Ω, f = 1 kHz	25°C		25		nV/√Hz
	Channel separation		1 kHz < f < 20 kHz	25°C		120		dB

(1) The input common-mode voltage of either input should not be allowed to go below –0.3 V. The upper end of the common-mode voltage range is V_{CC+} – 1.5 V, but either input can go to V_{CC+} + 0.3 V without damage (absolute maximum ratings still must be observed).

Voltage Reference Electrical Characteristics

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	TSM104W	I_K = 10 mA	25°C	2.475	2.5	2.525	V
				Full range	2.45		2.55	
		TSM104WA	I_K = 10 mA	25°C	2.49	2.5	2.51	
				Full range	2.48		2.52	
ΔV_{REF}	Reference input voltage deviation over temperature range		$V_{KA} = V_{REF}$, I_K = 10 mA	Full range		7	30	mV
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of change in reference voltage to change in cathode voltage		V_{KA} = 3 V to 36 V, I_K = 10 mA	25°C	–2	–1.1		mV/V
I_{REF}	Reference input current		I_K = 10 mA	25°C		1.5	2.5	µA
				Full range			3	
ΔI_{REF}	Reference input current deviation over temperature range			Full range		0.8	1.2	µA
I_{min}	Minimum cathode current for regulation		$V_{KA} = V_{REF}$	25°C		0.5	1	mA
$I_{K,OFF}$	Off-state cathode current			25°C		180	500	nA
$\lvert z_{ka} \rvert$	Dynamic impedance(1)		$V_{KA} = V_{REF}$, f < 1 kHz, ΔI_K = 1 mA to 100 mA	25°C		0.2	0.5	Ω

(1) The dynamic impedance is defined as $\lvert z_{ka} \rvert = \frac{\Delta V_{KA}}{\Delta I_K}$.

TYPICAL OPERATING CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

TOTAL HARMONIC DISTORTION (THD) vs FREQUENCY

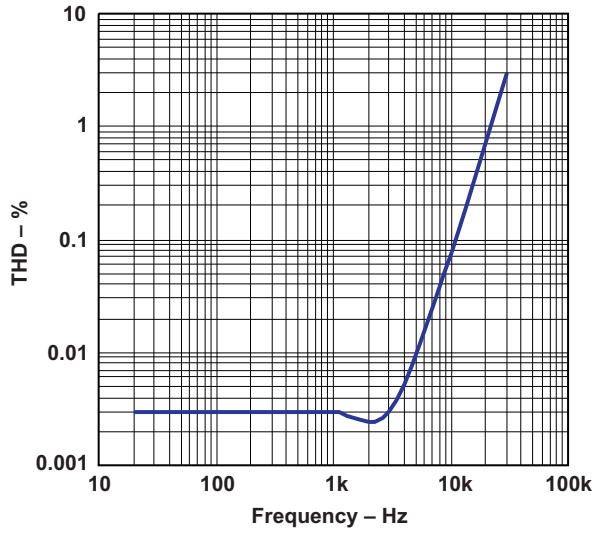


Figure 1.

AMPLIFIER NOISE VOLTAGE vs FREQUENCY

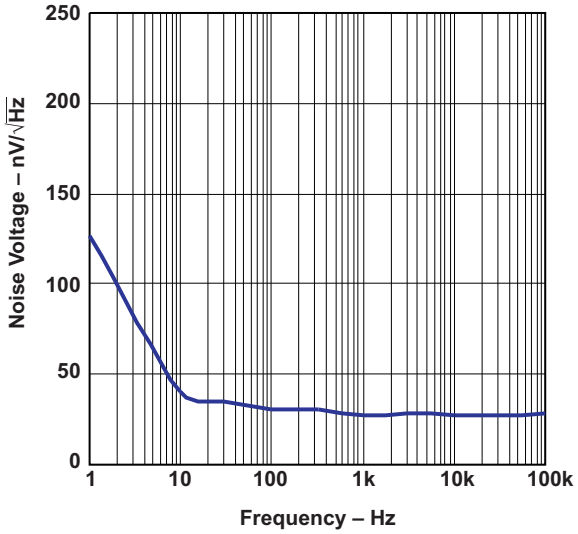


Figure 2.

I_K vs V_{REF}

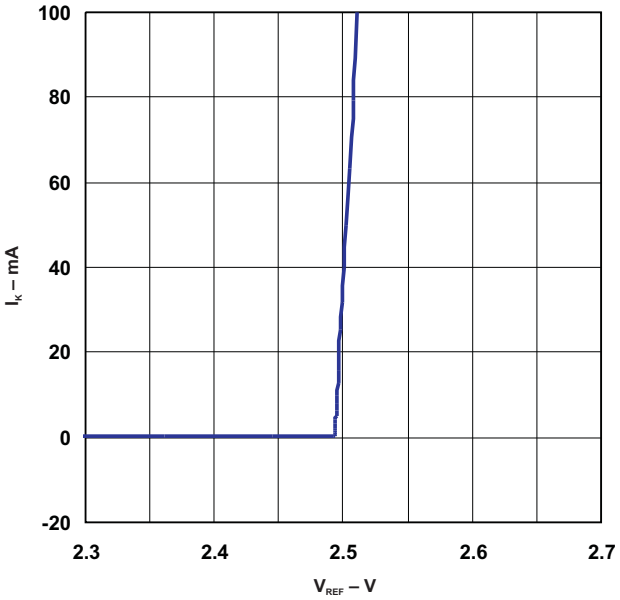


Figure 3.

V_{REF} STABILITY vs CAPACITANCE

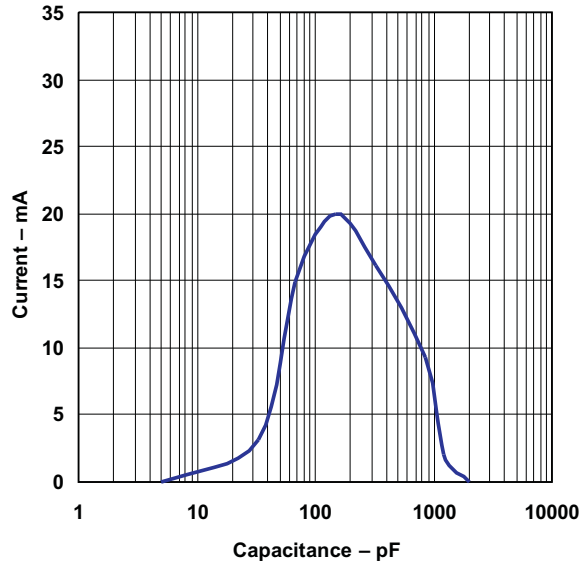


Figure 4.

TYPICAL OPERATING CHARACTERISTICS (continued)

T_A = 25°C (unless otherwise noted)

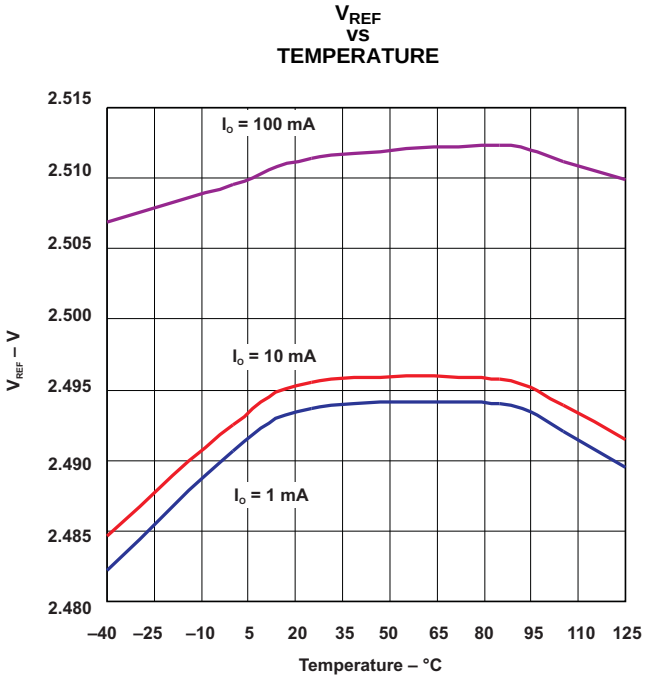


Figure 5.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSM104WAID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	TSM104WAI	Samples
TSM104WAIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	TSM104WAI	Samples
TSM104WAIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	SM104AI	Samples
TSM104WIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	TSM104WI	Samples
TSM104WIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	SM104I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

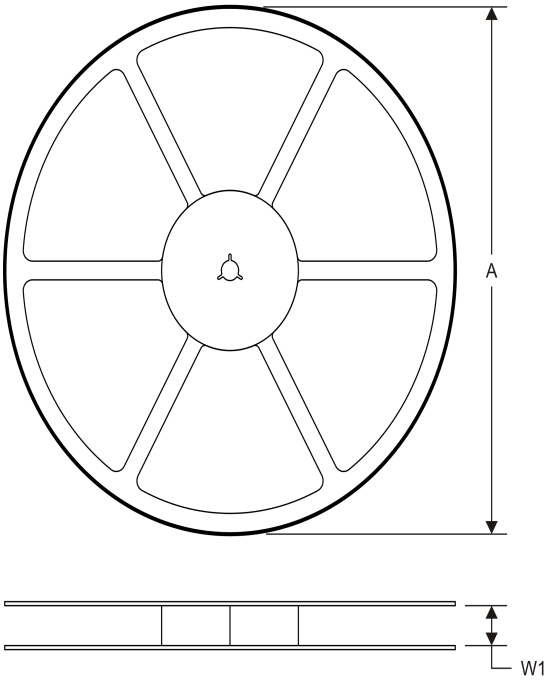
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

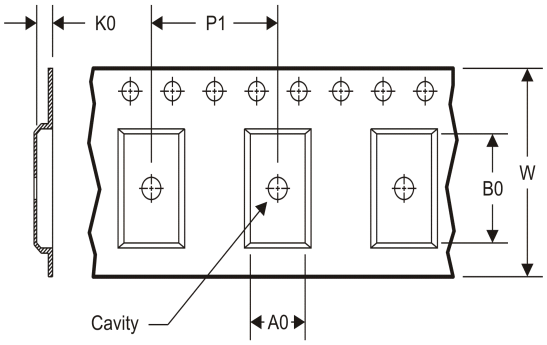
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



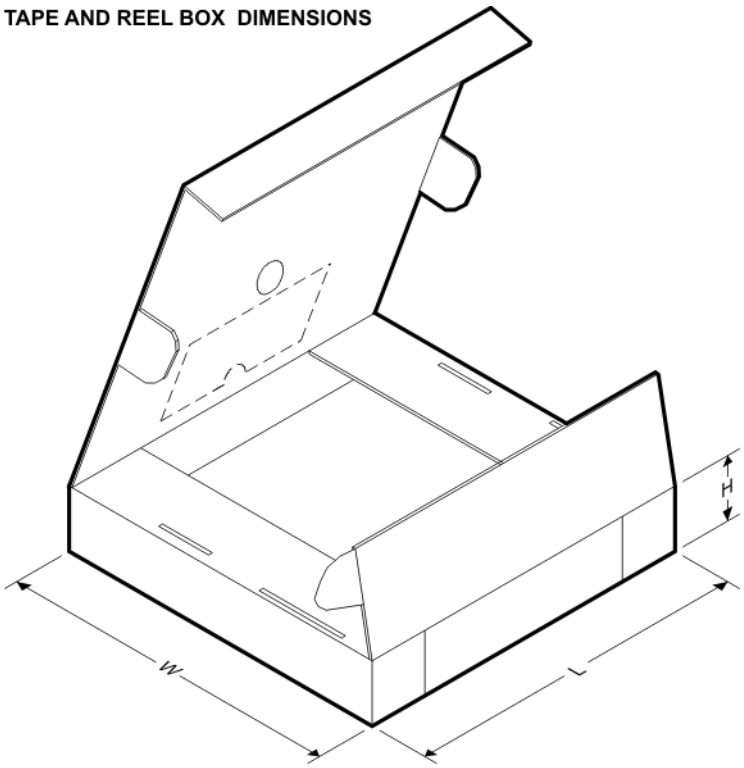
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSM104WAIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TSM104WAIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TSM104WIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TSM104WIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

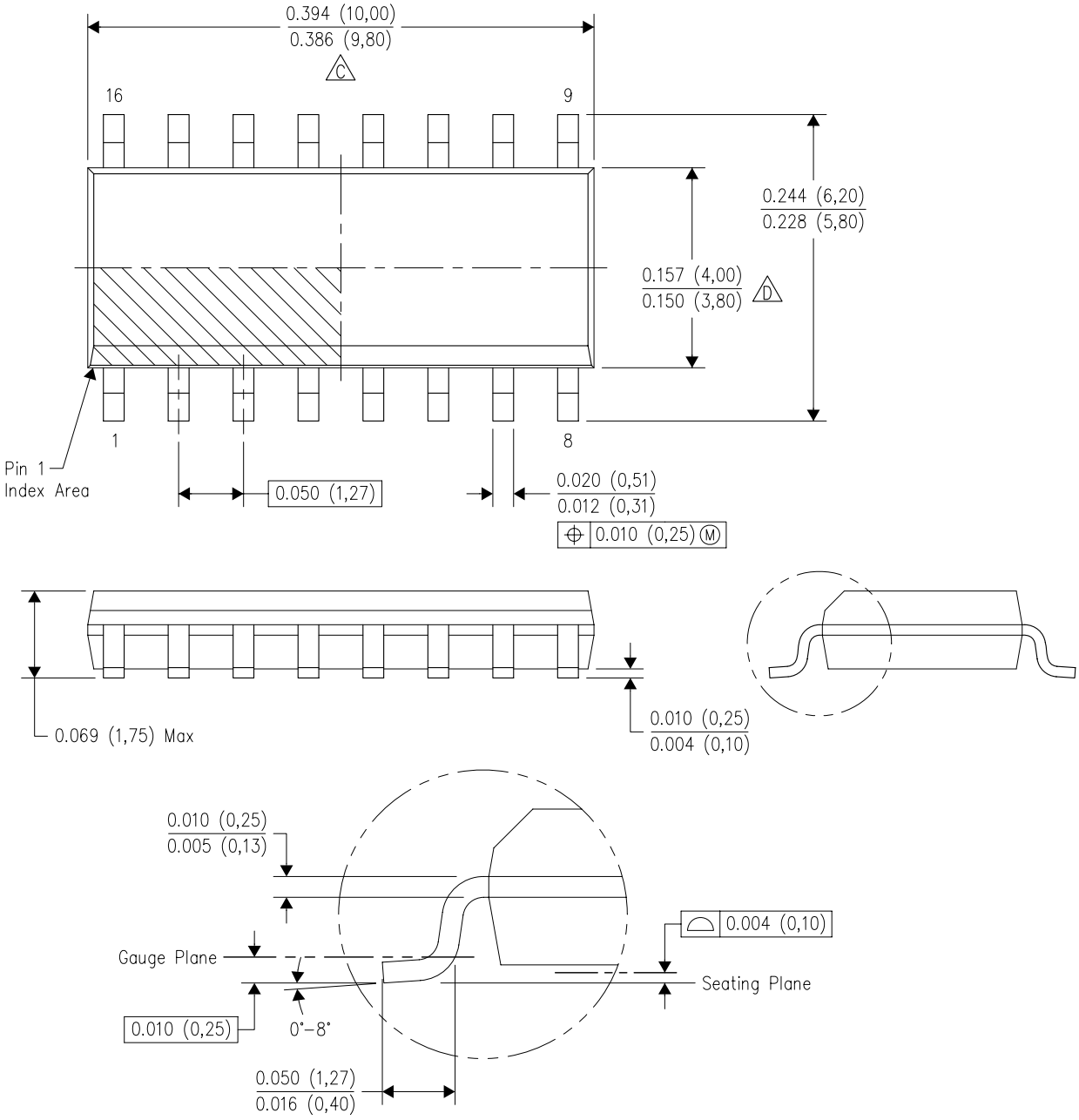
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

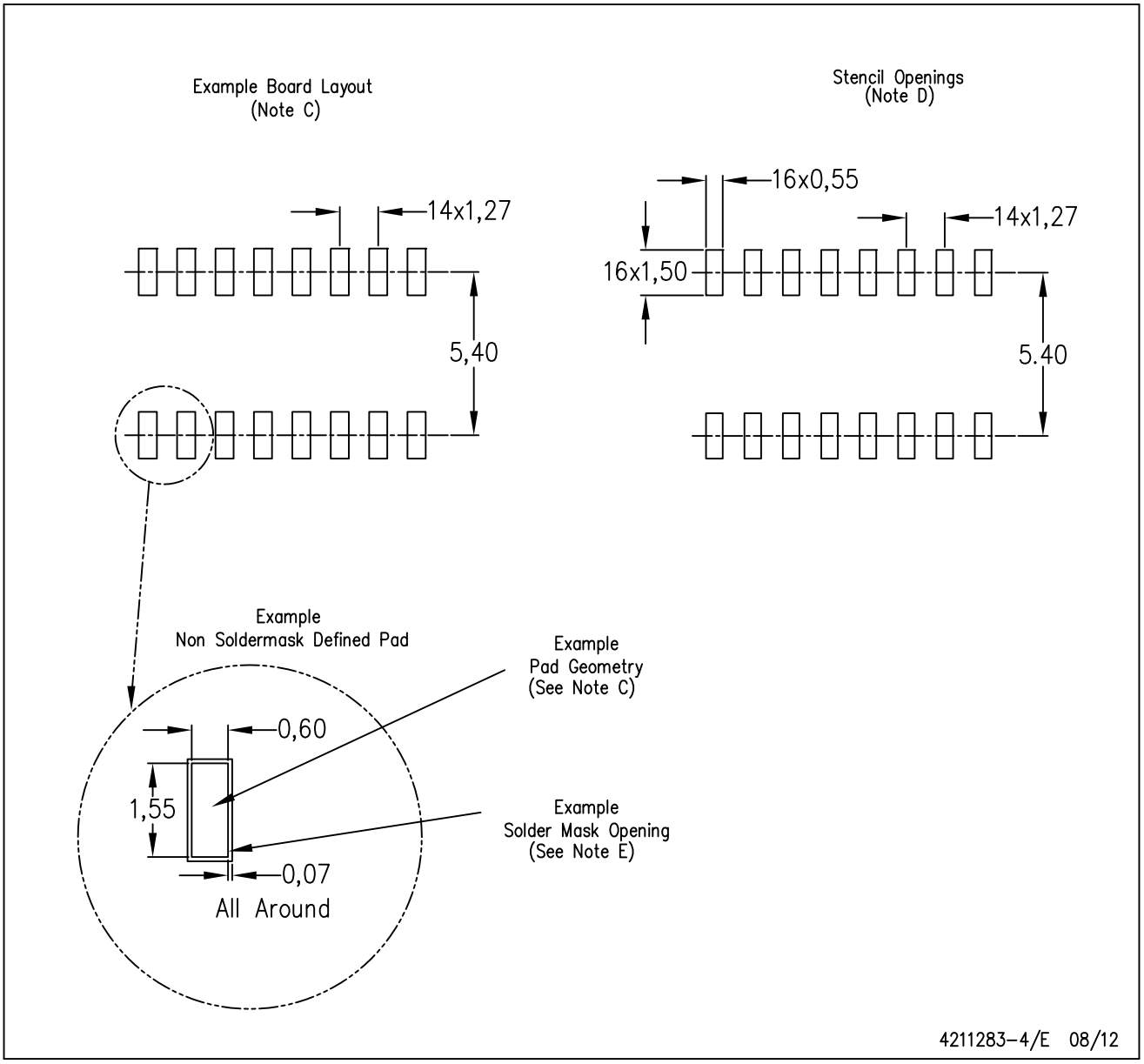
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSM104WAIDR	SOIC	D	16	2500	367.0	367.0	38.0
TSM104WAIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TSM104WIDR	SOIC	D	16	2500	367.0	367.0	38.0
TSM104WIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



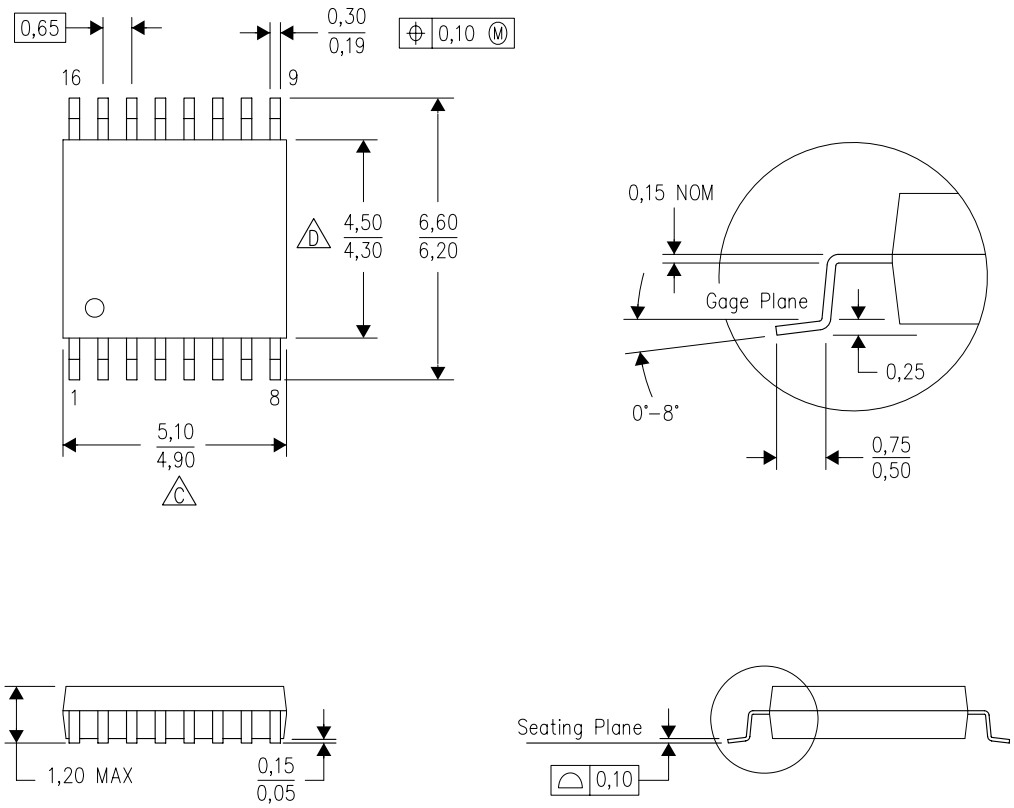
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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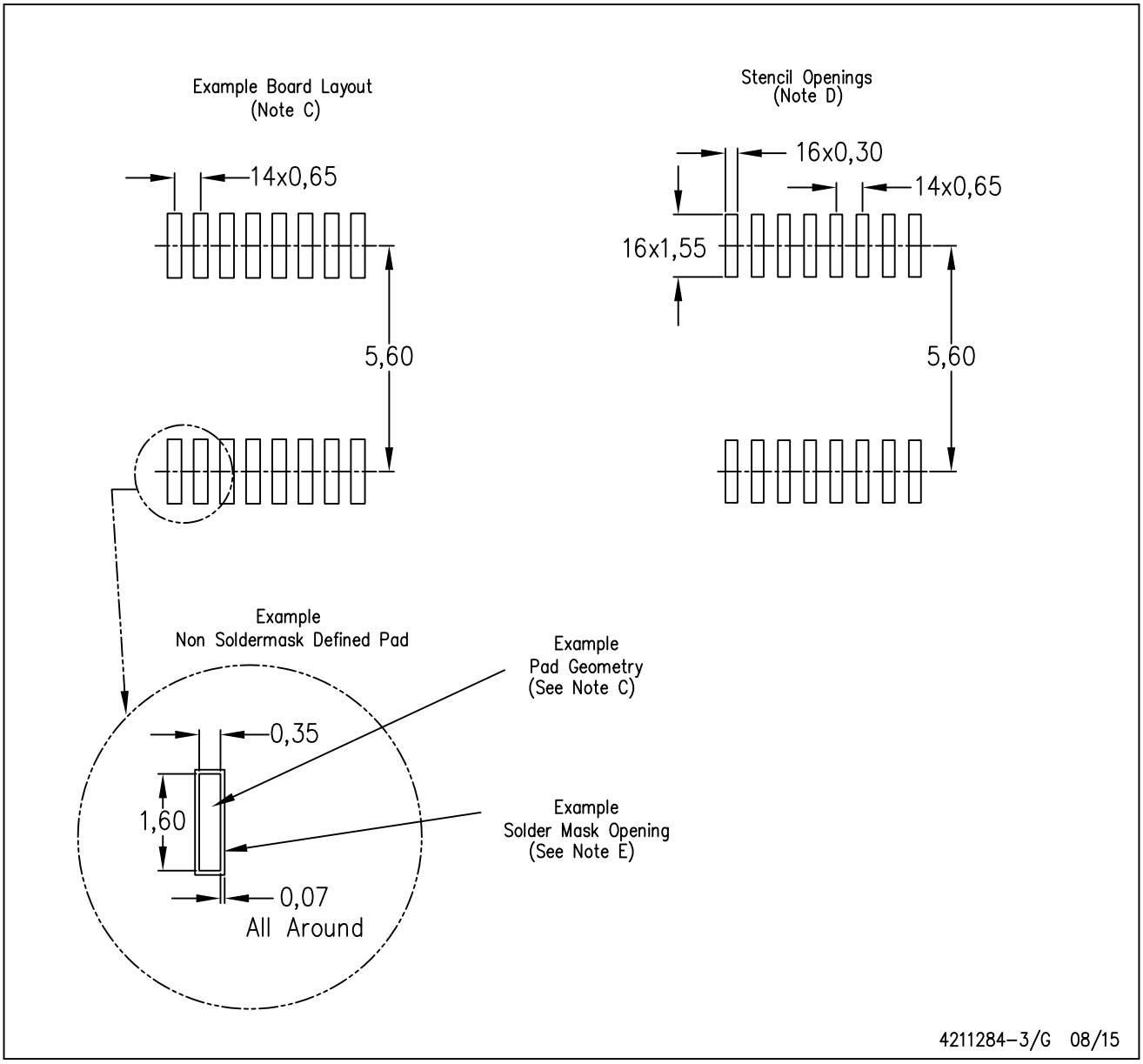
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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