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NC7ST86 TinyLogic® HST 2-Input Exclusive-OR Gate

General Description

Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak[™] leadless package
- High Speed; t_{PD} <8 ns typ, V_{CC} = 5V, C_L = 15 pF
- \blacksquare Low Quiescent Power; I_{CC} <1 μA typ, V_{CC} = 5.5V
- Balanced Output Drive; 2 mA I_{OL}, -2 mA I_{OH}
- TTL-compatible inputs

Ordering Code:

FAIRCHILD February 1997 SEMICONDUCTORIM Revised August 2004 NC7ST86 TinyLogic® HST 2-Input Exclusive-OR Gate										
General Do The NC7ST86 is Exclusive-OR Ga Silicon Gate CMC power circuit ope guard both inputs GND rails. High and reduced sen patible inputs fac Device performar output current dri	escription a single 2-Input te, with TTL-con DS fabrication as eration. ESD proc s and outputs with gain circuitry of sitivity to input of cilitate TTL to N noe is similar to I ve of HC/HCT.	high performand npatible inputs. A sures high spee- otection diodes i th respect to the fers high noise edge rate. The MOS/CMOS in MM74HCT but w	Features See CMOS Advanced d and low nherently VCc and immunity TTL-com- terfacing. Vith ½ the Features Space saving SOT23 or SC7 Ultra small MicroPak™ leadle High Speed; t _{PD} <8 ns typ, V Low Quiescent Power; I _{CC} < Balanced Output Drive; 2 mA	70 5-lead package ess package $t_{CC} = 5V$, $C_L = 15 \text{ pF}$ 1 μ A typ, $V_{CC} = 5.5V$ A t_{OL} , -2 mA t_{OH}	gic® HST 2-Input Exclus					
Ordering Code:										
Order	Package	Product Code	Package Description	Supplied As	0R					
NC7ST86M5X	MA05B	8S86	5-Lead SOT23, JEDEC MO-178, 1 6mm	3k Units on Tape and Reel	G					
NC7ST86P5X	MAA05A	T86	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel	ate					
NC7ST86L6X	MAC06A	D6	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel						

Logic Symbol



Pin Descriptions

Pin Names	Descriptions
А, В	Input
Y	Output
NC	No Connect

Function Table

	$\mathbf{Y} = \mathbf{A} \oplus \mathbf{B}$								
Γ	Inp	Output							
	Α	В	Y						
	L	L	L						
	L	Н	н						
	Н	L	н						
	Н	Н	L						



L = LOW Logic Level

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Pin Assignments for SOT23 and SC70

Connection Diagrams



Pad Assignments for MicroPak



(Top Thru View)

Absolute Maximum Ratings(Note 1)

Supply Voltage (V _{CC})	-0.5V to +7.0V	CO
DC Input Diode Current (IIK)		Sup
$V_{IN} < -0.5V$	–20 mA	Inpu
$V_{IN} \ge V_{CC} + 0.5V$	+20 mA	Outp
DC Input Voltage (V _{IN})	–0.5V to V _{CC} +0.5V	Ope
DC Output Diode Current (I _{OK})		Inpu
V _{OUT} < -0.5V	–20 mA	V
$V_{OUT} > V_{CC} + 0.5V$	+20 mA	The
Output Voltage (V _{OUT})	–0.5V to V _{CC} +0.5V	S
DC Output Source or Sink		S
Current (I _{OUT})	±12.5 mA	
DC V _{CC} or Ground Current per		
Supply Pin (I _{CC} or I _{GND})	±25 mA	
Storage Temperature (T _{STG})	$-65^{\circ}C$ to $+150^{\circ}C$	
Junction Temperature (T _J)	150°C	Note 1
Lead Temperature (T _L);		age to withou
(Soldering, 10 seconds)	260°C	power
Power Dissipation (P _D) @+85°C		tions.
SOT23-5	200 mW	Note 2
SC70-5	150 mW	

Recommended Operating Conditions (Note 2)

ply Voltage 4.5V to 5.5V ut Voltage (V_{IN}) 0V to V_{CC} 0V to V_{CC} put Voltage (V_{OUT}) $-40^\circ C$ to $+85^\circ C$ erating Temperature (T_A) ut Rise and Fall Time (t_r, t_f) _{CC} = 5.0V 0 to 500 ns ermal Resistance (θ_{JA}) 300°C/W OT23-5 C70-5 425°C/W

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside the databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC}	T _A = +25°C			$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Unite	Conditions	
Symbol	Falameter	(V)	Min	Тур	Max	Min	Max	Units	Conditions	
VIH	HIGH Level Input Voltage	4.5-5.5	2.0			2.0		V		
V _{IL}	LOW Level Input Voltage	4.5-5.5			0.8		0.8	V		
V _{OH}	HIGH Level Output Voltage	4.5	4.4	4.5		4.4		V	$I_{OH}=-20~\mu\text{A},~V_{IN}=V_{IL},$	
		4.5	4.18	4.35		4.13		V	$V_{IH} I_{OH} = -2 \text{ mA}$	
V _{OL}	LOW Level Output Voltage	4.5		0	0.1		0.1	V	$I_{OL}=20~\mu\text{A},~V_{IN}=V_{IL},$	
		4.5		0.10	0.26		0.33	V	$V_{IH} I_{OL} = 2 \text{ mA}$	
I _{IN}	Input Leakage Current	5.5			±0.1		±1.0	μΑ	$0 \le V_{IN} \le 5.5V$	
I _{CC}	Quiescent Supply Current	5.5			1.0		10.0	μA	$V_{IN} = V_{CC}$ or GND	
I _{CCT}	I _{CC} per Input	5.5			2.0		2.9	mA	One Input $V_{IN} = 0.5V$ or 2.4V,	
									Other Input V _{CC} or GND	

AC E	Electrical Characte	eristi	cs							
Cumhal	Devementer	V _{CC}		T _A = +25°C	;	$T_A = -40^\circ$	C to +85°C	Unite	Conditions	Figure
Symbol	Parameter	(V)	Min	Тур	Max	Min	Max	Units	Conditions	Number
t _{PLH} ,	Propagation Delay	FO		4.4	14			-	C _ 15 pF	
t _{PHL}		5.0		7.4	19			115	CL = 15 pr	
		4 5		6.6	18		22			Figures
		4.5		13.1	29		33		C 50 aF	1, 3
		E E		5.6	16		20	ns	$C_L = 50 \text{ pr}$	
		5.5		12.5	28		32			
t _{TLH} ,	Output Transition Time	5.0		4	10			ns	C _L = 15 pF	
t _{THL}		4.5		11	25		31	ns	C _L = 50 pF	Figures
		5.5		10	21		26			., 0
C _{IN}	Input Capacitance	Open		2	10			pF		
C _{PD}	Power Dissipation Capacitance	5.0		8				pF	(Note 3)	Figure 2

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by expression: $I_{CCD} = (C_{PD}) (V_{CC}) (f_{|N}) + (I_{CC} static).$

AC Loading and Waveforms



 C_L includes load and stray capacitance Input PRR = 1.0 MHz, t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveforms; PRR = Variable; Duty Cycle = 50% FIGURE 2. I_{CCD} Test Circuit



FIGURE 3. AC Waveforms

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