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August 2000

QFET™

FQS4900

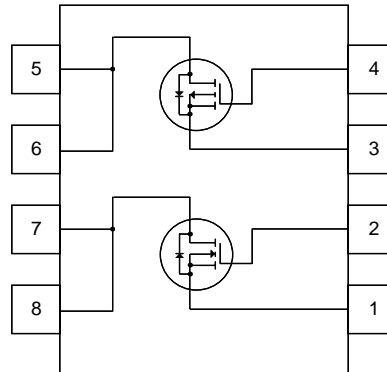
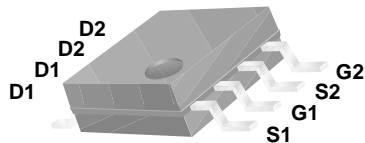
Dual N & P-Channel, Logic Level MOSFET

General Description

These dual N and P-channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. This device is well suited for high interface in telephone sets.

Features

- N-Channel 1.3A, 60V, $R_{DS(on)} = 0.55 \Omega @ V_{GS} = 10 V$
 $R_{DS(on)} = 0.65 \Omega @ V_{GS} = 5 V$
- P-Channel -0.3A, -300V, $R_{DS(on)} = 15.5 \Omega @ V_{GS} = -10 V$
 $R_{DS(on)} = 16 \Omega @ V_{GS} = -5 V$
- Low gate charge (typical N-Channel 1.6 nC)
 (typical P-Channel 3.6 nC)
- Fast switching
- Improved dv/dt capability



Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	60	-300	V
I_D	Drain Current - Continuous ($T_A = 25^\circ C$) - Continuous ($T_A = 70^\circ C$)	1.3	-0.3	A
		0.82	-0.19	A
I_{DM}	Drain Current - Pulsed (Note 1)	5.2	-1.2	A
V_{GSS}	Gate-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt (Note 2)	7.0	4.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ C$) ($T_A = 70^\circ C$)	2.0		W
		1.3		W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ C$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ C/W$

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	N-Ch	60	--	--	V
		$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	P-Ch	-300	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	N-Ch	--	--	1	μA
		$V_{DS} = 48\text{ V}, T_C = 55^\circ\text{C}$		--	--	10	μA
		$V_{DS} = -300\text{ V}, V_{GS} = 0\text{ V}$	P-Ch	--	--	-1	μA
		$V_{DS} = -240\text{ V}, T_C = 55^\circ\text{C}$		--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	All	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	All	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = 4\text{ V}, I_D = 20\text{ mA}$	N-Ch	1.0	--	1.95	V
		$V_{DS} = 4\text{ V}, I_D = -20\text{ mA}$	P-Ch	-1.0	--	-1.95	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.65\text{ A}$	N-Ch	--	0.39	0.55	Ω
		$V_{GS} = 5\text{ V}, I_D = 0.65\text{ A}$		--	0.46	0.65	Ω
		$V_{GS} = -10\text{ V}, I_D = -0.15\text{ A}$	P-CH	--	11.2	15.5	Ω
		$V_{GS} = -5\text{ V}, I_D = -0.15\text{ A}$		--	11.4	16	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 0.65\text{ A}$	N-CH	--	1.7	--	S
		$V_{DS} = -10\text{ V}, I_D = -0.15\text{ A}$	P-CH	--	0.6	--	S

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	N-Channel $V_{DD} = 30\text{ V}, I_D = 1.3\text{ A},$ $R_G = 25\ \Omega$	N-Ch	--	5.7	21	ns
			P-Ch	--	10	30	ns
t_r	Turn-On Rise Time	P-Channel $V_{DD} = -150\text{ V}, I_D = -0.3\text{ A},$ $R_G = 25\ \Omega$	N-Ch	--	21	50	ns
			P-Ch	--	25	60	ns
$t_{d(off)}$	Turn-Off Delay Time	N-Channel $V_{DS} = 48\text{ V}, I_D = 1.3\text{ A},$ $V_{GS} = 5\text{ V}$	N-Ch	--	11	32	ns
			P-Ch	--	35	80	ns
t_f	Turn-Off Fall Time	P-Channel $V_{DS} = -240\text{ V}, I_D = -0.3\text{ A},$ $V_{GS} = -5\text{ V}$	N-Ch	--	17	45	ns
			P-Ch	--	47	105	ns
Q_g	Total Gate Charge	N-Channel $V_{DS} = 48\text{ V}, I_D = 1.3\text{ A},$ $V_{GS} = 5\text{ V}$	N-Ch	--	1.6	2.1	nC
			P-Ch	--	3.6	4.7	nC
Q_{gs}	Gate-Source Charge	P-Channel $V_{DS} = -240\text{ V}, I_D = -0.3\text{ A},$ $V_{GS} = -5\text{ V}$	N-Ch	--	0.28	--	nC
			P-Ch	--	0.42	--	nC
Q_{gd}	Gate-Drain Charge	N-Channel $V_{DS} = 48\text{ V}, I_D = 1.3\text{ A},$ $V_{GS} = 5\text{ V}$	N-Ch	--	0.82	--	nC
			P-Ch	--	2.1	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	N-Ch	--	--	1.3	A	
		P-Ch	--	--	-0.3	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$	N-Ch	--	--	1.5	V
		$V_{GS} = 0\text{ V}, I_S = -0.3\text{ A}$	P-Ch	--	--	-4.0	V

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
3. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature

Typical Characteristics : N-Channel

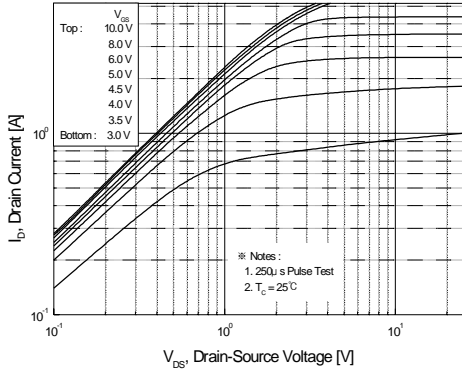


Figure 1. On-Region Characteristics

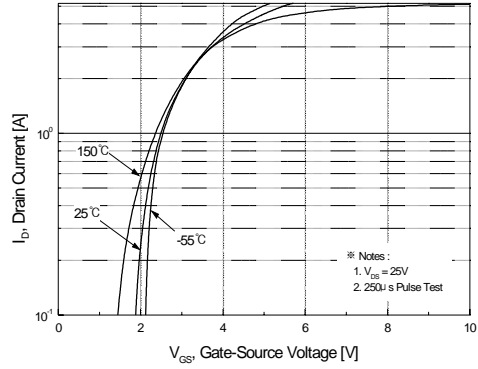


Figure 2. Transfer Characteristics

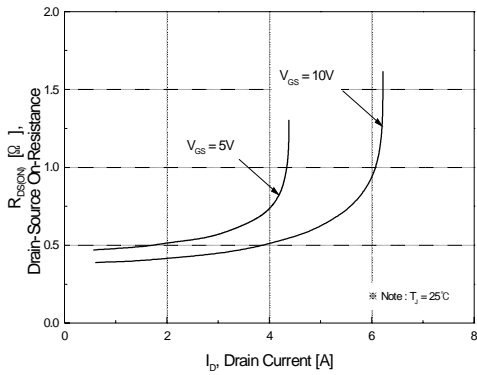


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

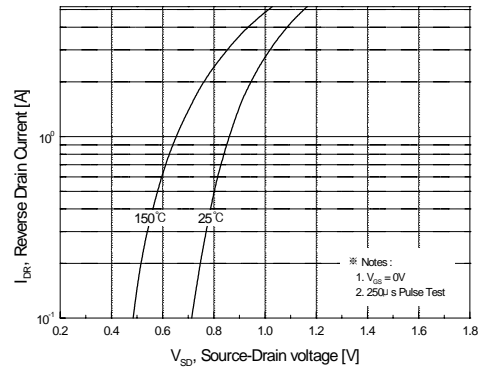


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

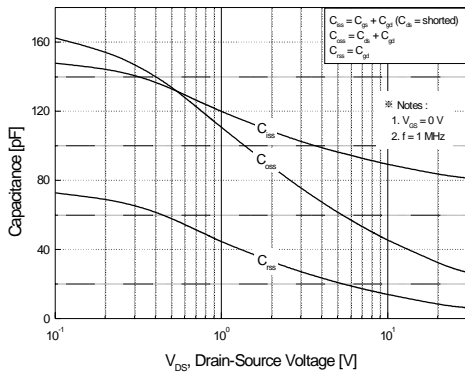


Figure 5. Capacitance Characteristics

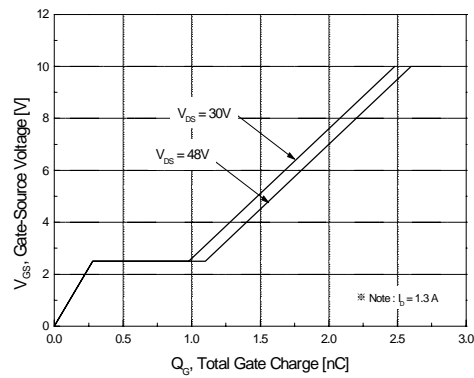


Figure 6. Gate Charge Characteristics

Typical Characteristics : N-Channel (Continued)

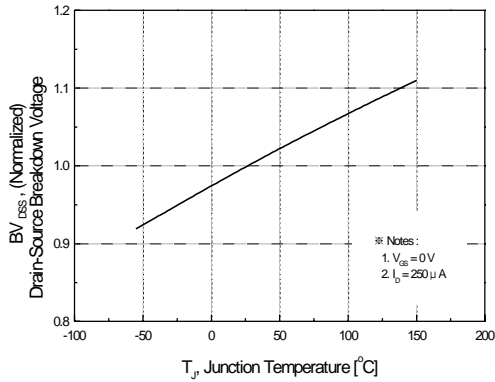


Figure 7. Breakdown Voltage Variation vs. Temperature

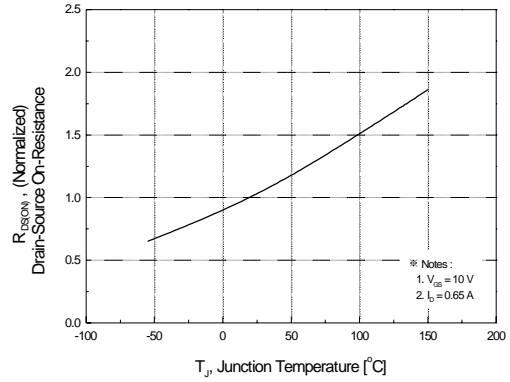


Figure 8. On-Resistance Variation vs. Temperature

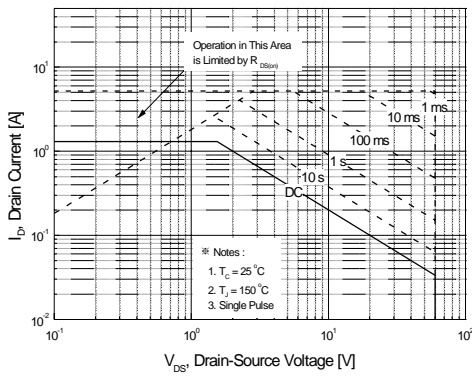


Figure 9. Maximum Safe Operating Area

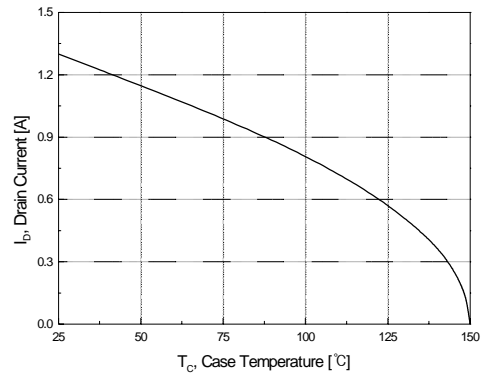


Figure 10. Maximum Drain Current vs. Case Temperature

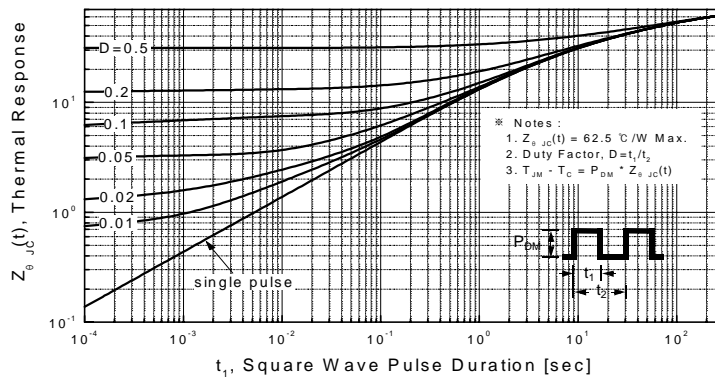


Figure 11. Transient Thermal Response Curve

Typical Characteristics : P-Channel (Continued)

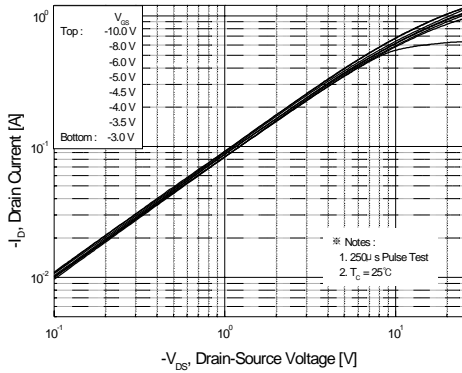


Figure 1. On-Region Characteristics

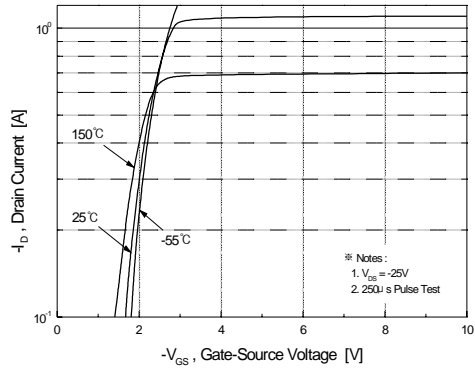


Figure 2. Transfer Characteristics

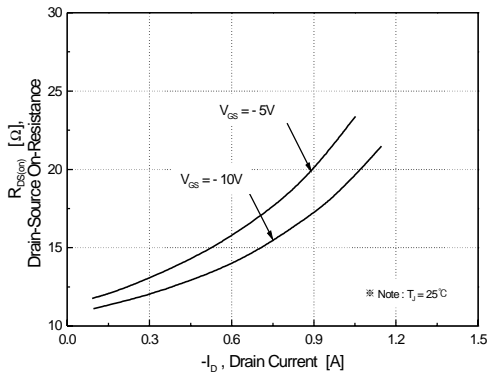


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

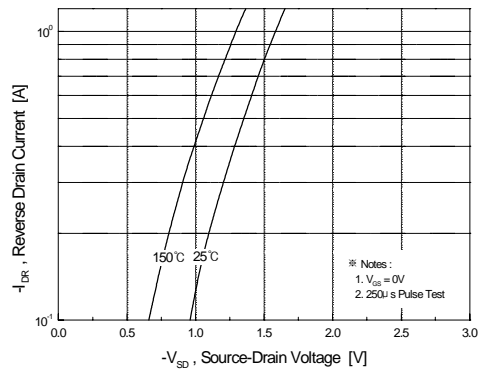


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

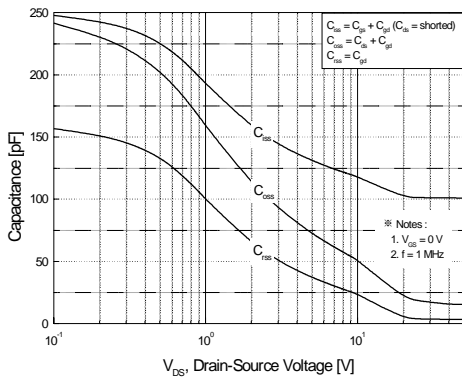


Figure 5. Capacitance Characteristics

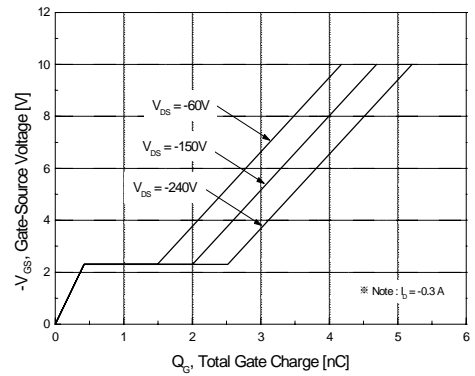


Figure 6. Gate Charge Characteristics

Typical Characteristics : P-Channel (Continued)

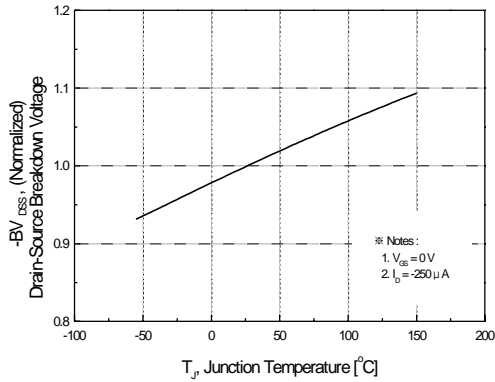


Figure 7. Breakdown Voltage Variation vs. Temperature

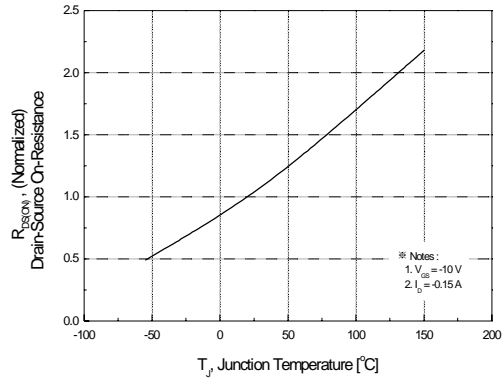


Figure 8. On-Resistance Variation vs. Temperature

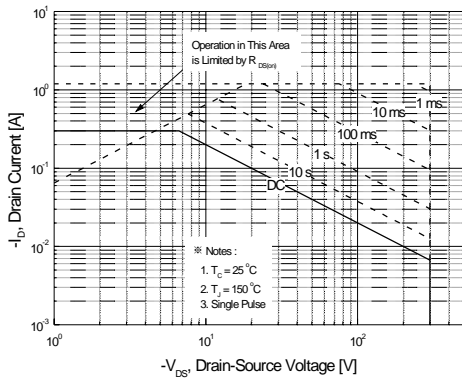


Figure 9. Maximum Safe Operating Area

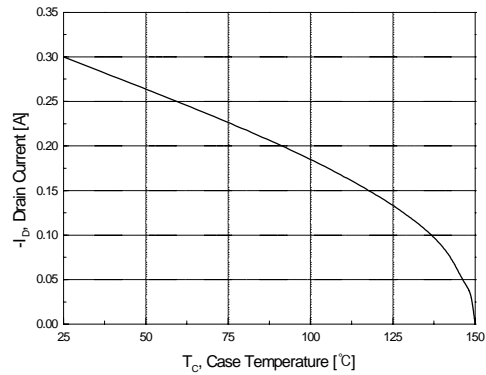


Figure 10. Maximum Drain Current vs. Case Temperature

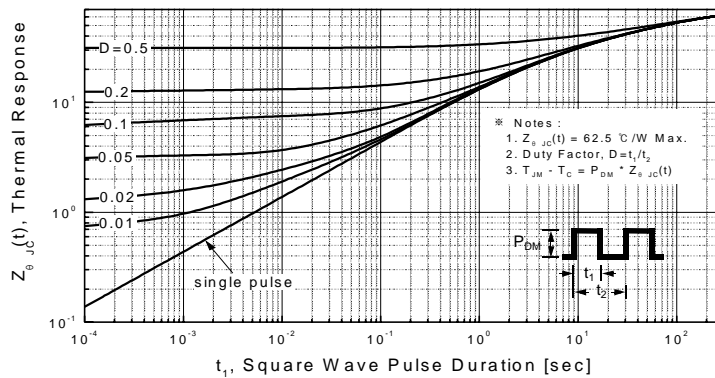
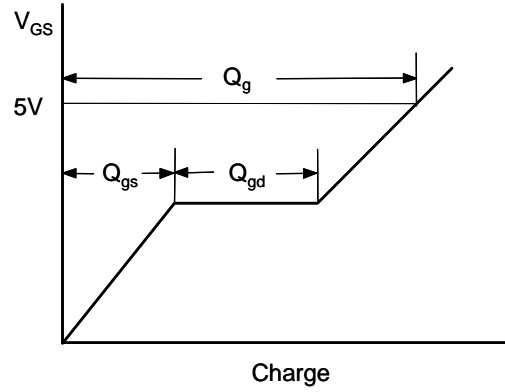
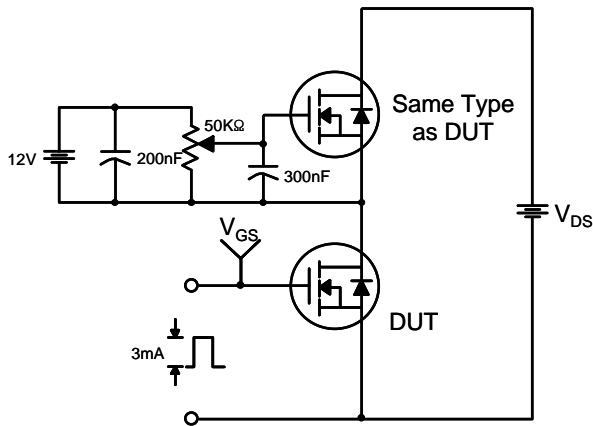
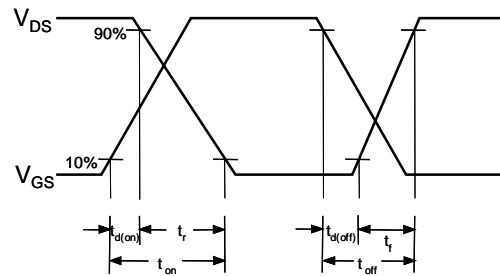
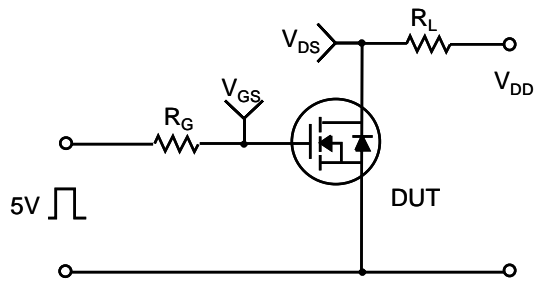


Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

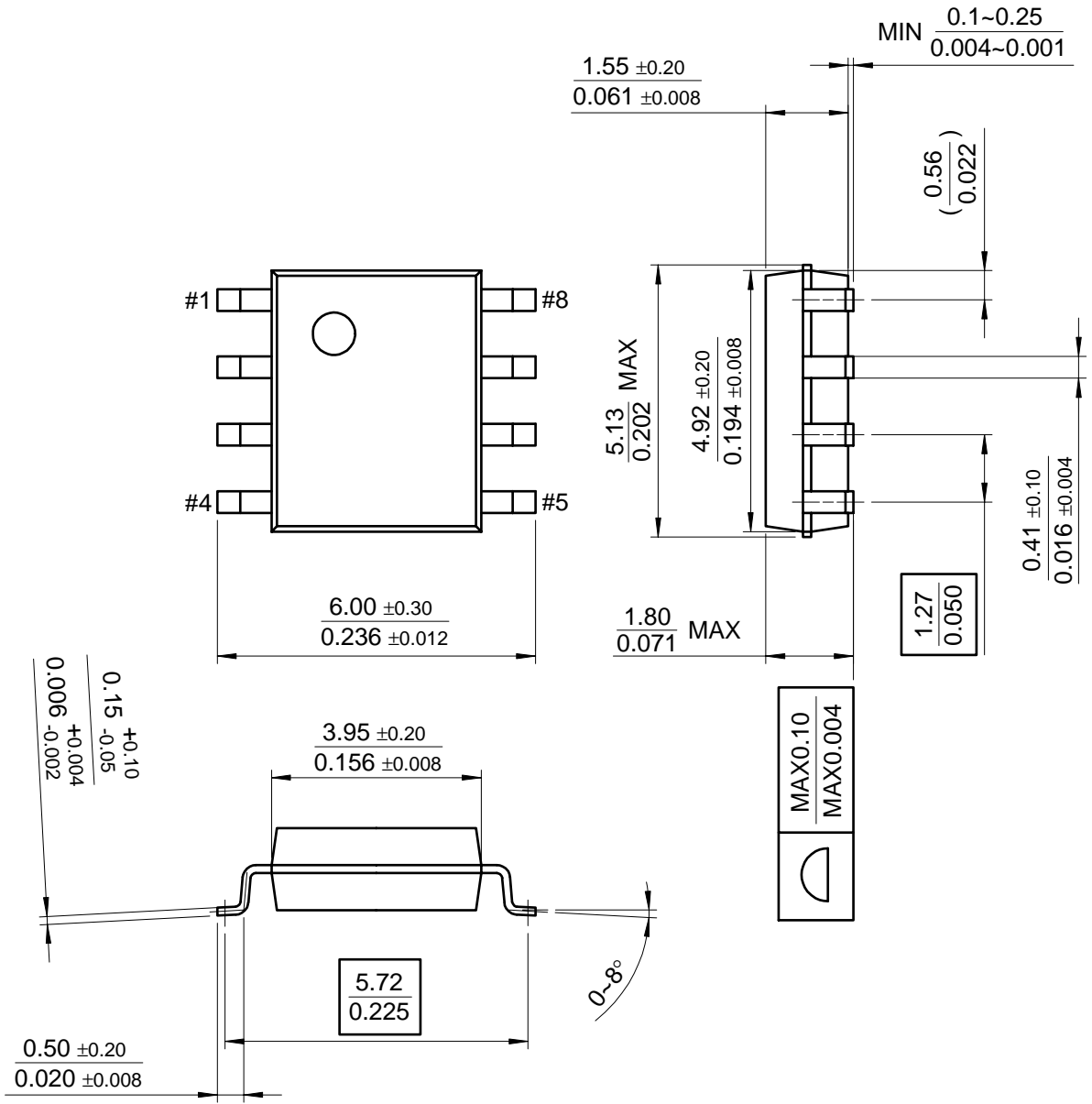


Resistive Switching Test Circuit & Waveforms



Package Dimensions

8-SOP



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