



Lattice USB Type-C Solution Data Sheet

Preliminary DS1052 Version 1.3, August 2015

General Description

The USB Type-C receptacle, plug and cable provide a smaller, thinner and more robust alternative to existing USB interconnects. The Lattice USB Type-C solution targets its use in a variety of platforms ranging from notebooks, PCs, Monitors, down to tablets and smart phones. These solutions are also implemented in Docking Stations, USB chargers and cables where cable detect (CD) electronic intelligence and power delivery (PD) protocols are implemented.

The Lattice solution is designed to support USB Type-C cable and Connector and USB Power Delivery specifications with programmable flexibility to support the new and evolving specifications as well as the various levels of complexities required by the end system in a cost effective manner.

Features

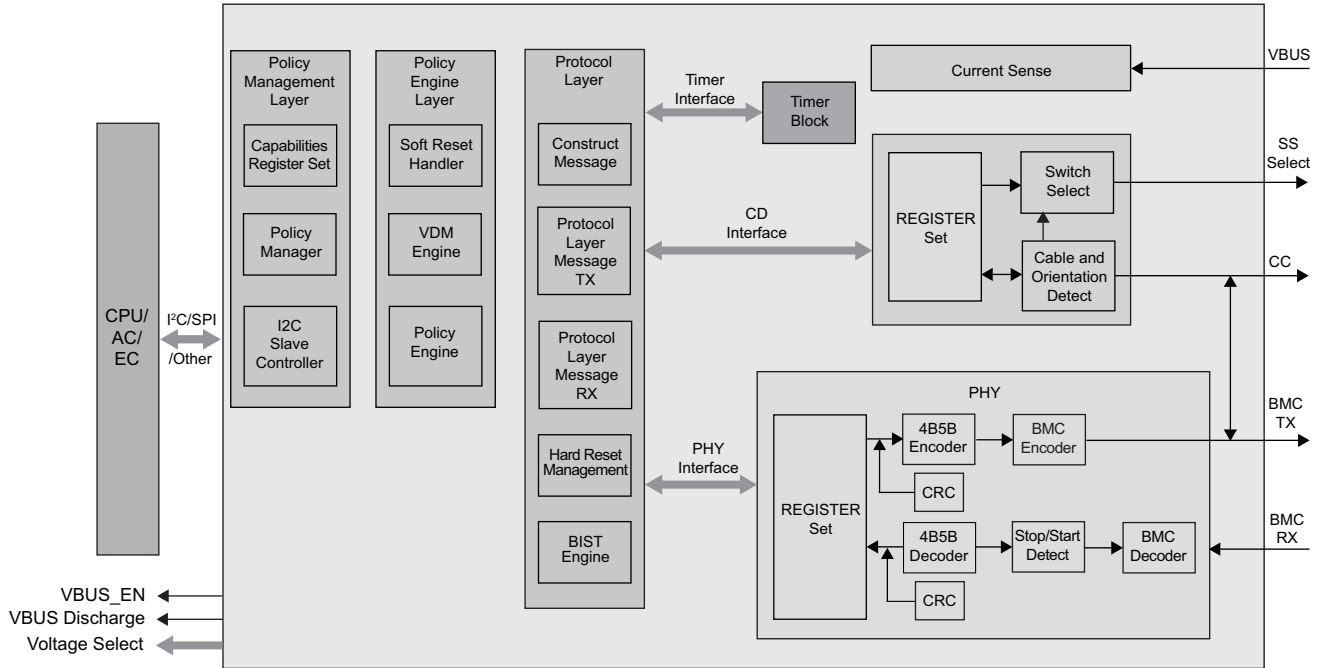
- **Four solutions cover majority of USB Type-C Power Delivery (PD) and Cable Detect (CD) Applications:**
 - CD/PD for Charger
 - CD/PD-Phy for hosts/devices
 - CD/PD for hosts/devices
 - CD/PD for Docks/Dockable Devices
- **Logic Based PHY Provides Fast Deterministic Response and Low Power**
 - Typical Solution Power 7 mW
- **Standby Power less than 100 uW**
- **Flexible 8-bit uC Policy Engine Enables Easy Modifications**
- **Supports Fast Development**
 - Industry Proven Solutions Reduce Design Risk
 - Schematics and BOMS available to minimize system design effort
- **Wide Range of Packages to Match PCB Technology**
 - 36 WLCSP
 - 48 QFN
 - 36 ucBGA
 - 81 ucBGA
- **Ultra-Small Form Factor**
 - As small as 2.078 mm x 2.078 mm
- **USB Type-C PHY**
- **USB Type-C Cable Detect (CD) support per USB Cable and Connector Specification v1.0**
- **USB Power Delivery (PD) support per Power Delivery Specification v2.0**
 - IO capability to drive LED indicator

Table 1-1. USB Type-C Device Table

Solution	Package, Ball Pitch, Dimension	Typical End Equipment	OPN
CD/PD for Charger	48 QFN, 0.50 mm, 7.00 mm x 7.00 mm	Charger	LIF-UC110-SG48I
CD/PD Phy for Hosts/Devices	36 WLCSP, 0.35 mm, 2.078 mm x 2.078 mm	Smartphone, Tablet	LIF-UC120-SWG36I
	36 ucBGA, 0.40 mm, 2.50 mm x 2.50 mm	Smartphone, Tablet	LIF-UC120-CM36I
CD/PD for Hosts/Devices	81 ucBGA, 0.40 mm, 4.00 mm x 4.00 mm	Tablet	LIF-UC140-CM81I

Architecture Overview

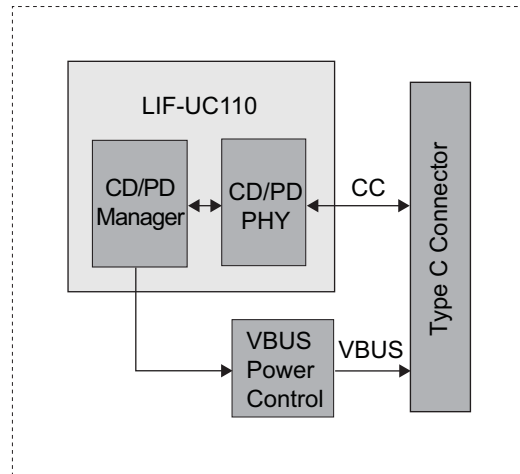
Figure 2-1. High-level Functional Block for USB Type-C Physical Layer and Power Detect Protocol



USB CD/PD Charger Solution (Captive Cable)

Block Diagram

Figure 2-2. USB CD/PD Charger Solution (Captive Cable) Block Diagram



CD = Cable Detect
PD = Power Delivery

Features Supported in Schematics

- Downstream Facing Port (DFP)
- USB Power Delivery Communication between Port partners
- Takes advantage of captive cable to minimize component count

Schematics

Figure 2-3. USB CD/PD Charger Solution (Captive Cable) Schematic Diagram

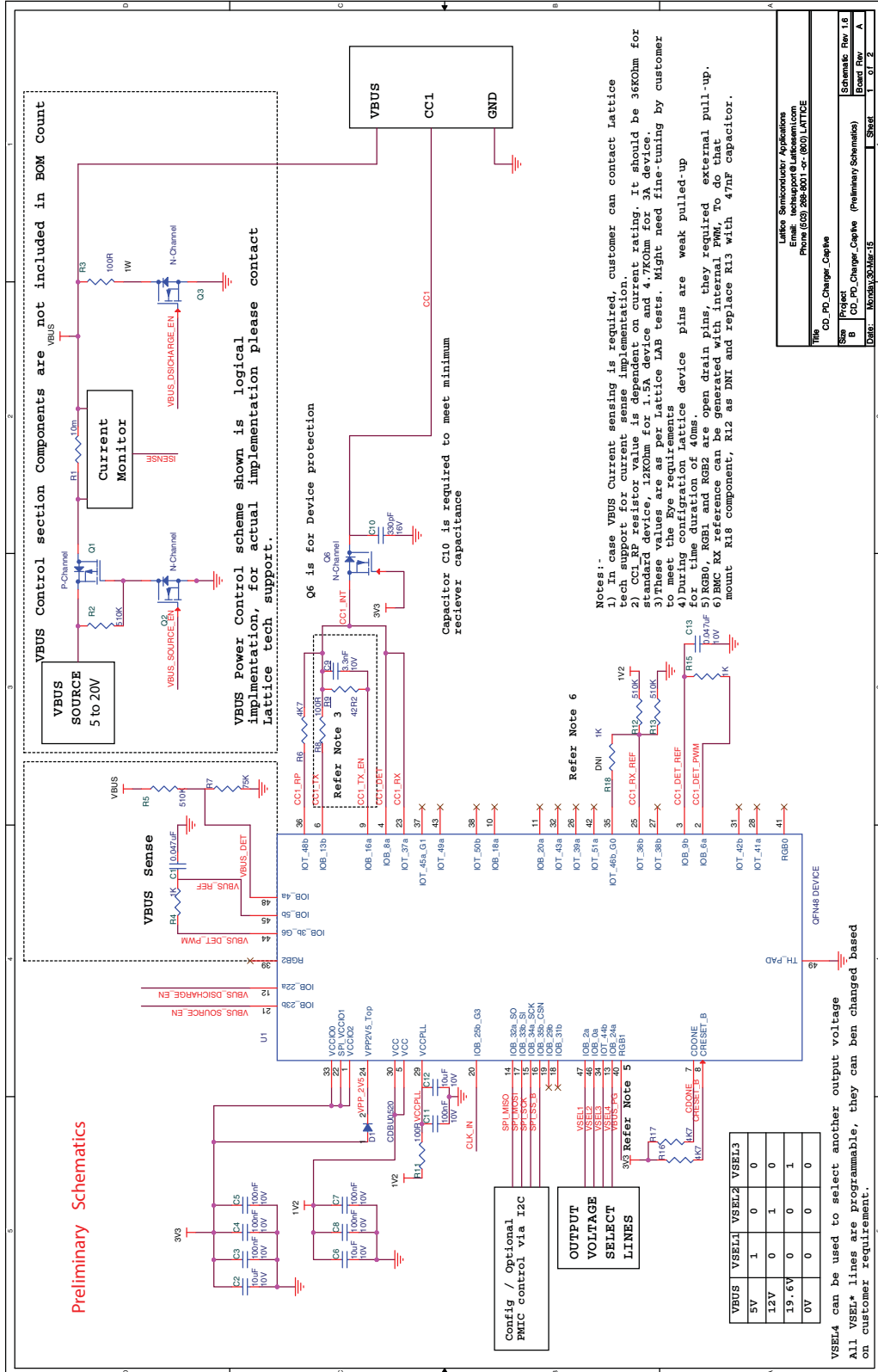


Table 2-1. USB CD/PD Mobile System Solution (Captive Cable) BOM

Item	Quantity	Reference	Part	DESCRIPTION
1	2	C1, C13	0.047 uF	CAP CER 0.047 uf 10 V 10% X5R 0402
2	3	C2, C6, C12	10 uF	CAP CER 10 uf 10 V 10% X5R 0805
3	6	C4, C5, C7, C3, C8, C11	100 nF	CAP CER 100 nf 10 V 10% X5R 0402
4	1	C9	3.3 nF	CAP CER 3300 pF 10 V 5% U2J 0402
5	1	C10	330 pF	CAP CER 330 pF 16 V 10% X7R 0402
6	1	D1	CDBU0520	DIODE SCHOTTKY 20 V 500 MA 0603
7	1	Q1	P-Channel	MOSFET P-CH 20 V 6 A SOT-23
8	1	Q3	N-Channel	MOSFET N-CH 20 V 6.3 A SOT-23
9	2	Q2, Q6	N-Channel	MOSFET N-CH 30 V 0.85 A SOT23
10	2	R4, R15	1K	RES 1 kOhm 1/16 W 5% 0402
11	4	R2, R5, R12, R13	510K	RES 510 kOhm 1/16 W 5% 0402
12	1	R8	100R	RES SMD 100 Ohm 1% 1/16 W 0402
13	3	R6, R16, R17	4K7	RES 150 Ohm 1/16 W 1% 0402 SMD
14	1	R11	100R	RES 100 Ohm 1/16 W 5% 0402
15	1	R9	42.2R	RES SMD 42.2 Ohm 1% 1/16 W 0402
16	1	R3	100R	RES SMD 100 Ohm 1% 1 W 2512
17	1	R7	75K	RES SMD 75 kOhm 5% 1/16 W 0402
18	1	R1	10m	RES 0.01 Ohm 1/2 W 1% 1206
19	1	U1	LIF-UC	LIF-UC 48-Pin Device

Table 2-2. USB CD/PD Mobile System Solution (Captive Cable) BOM Count^{1, 2}

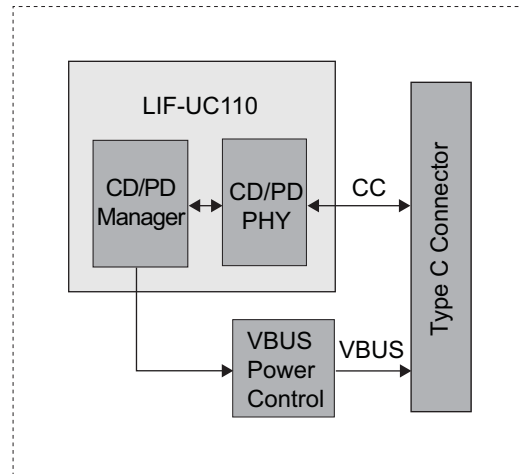
Item	Component	Count
1	Cap	13
2	FET	1
3	Resistor	12
4	Lattice LIF-UC	1

1. VBUS control section components are not included in the BOM count.
2. Diode D1 is not included in the BOM count. It is required only during onboard NVCM programming.

USB CD/PD Charger Solution (Non-Captive Cable)

Block Diagram

Figure 2-4. USB CD/PD Charger Solution (Non-Captive Cable) Block Diagram



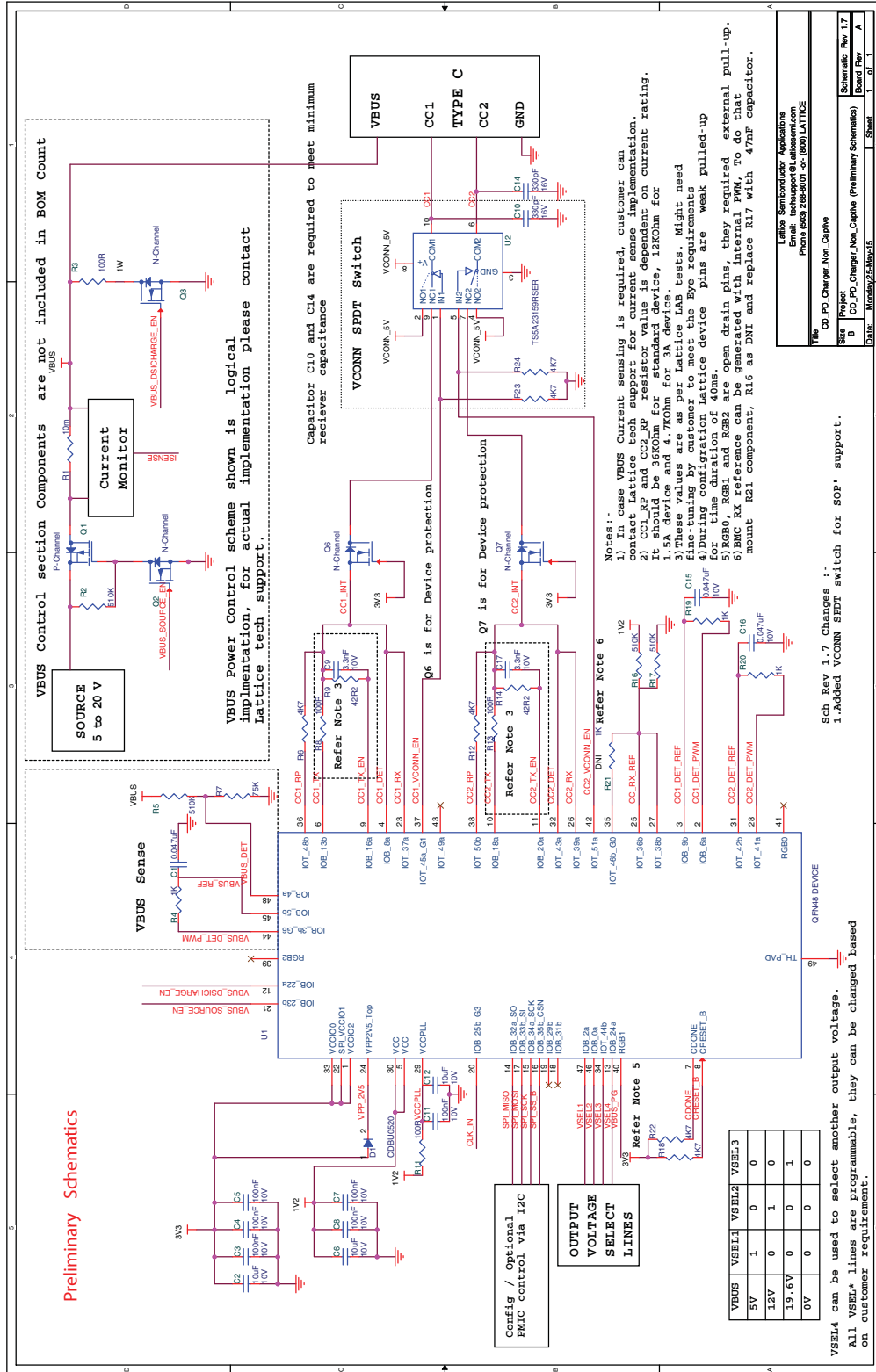
CD = Cable Detect
PD = Power Delivery

Features Supported in Schematics

- DFP
- USB Power Delivery Communication between Port partners
- Provides cable flip support needed in chargers with receptacles

Schematics

Figure 2-5. USB CD/PD Charger Solution (Non-Captive Cable) Schematic Diagram



BOM
Table 2-3. USB CD/PD Charger Solution (Non-Captive Cable) BOM

Item	Quantity	Reference	Part	DESCRIPTION
1	3	C1, C15, C16	0.047 uF	CAP CER 0.047 uf 10 V 10% X5R 0402
2	3	C2, C6, C12	10 uF	CAP CER 10 uf 10 V 10% X5R 0805
3	6	C4, C5, C7, C3, C8, C11	100 nF	CAP CER 100 nf 10 V 10% X5R 0402
4	2	C9, C17	3.3 nF	CAP CER 3300 pF 10.V 5% U2J 0402
5	2	C10, C14	330 pF	CAP CER 330 pF 16 V 10% X7R 0402
6	1	D1	CDBU0520	DIODE SCHOTTKY 20 V 500 MA
7	1	Q1	P-Channel	MOSFET P-CH 20 V 6 A SOT-23
8	1	Q3	N-Channel	MOSFET N-CH 20 V 6.3 A SOT-23
9	3	Q2, Q6, Q7	N-Channel	MOSFET N-CH 30 V 0.85 A SOT23
10	3	R4, R19, R20	1K	RES 1K Ohm 1/16 W 5% 0402
11	4	R2, R5, R16, R17	510K	RES 510K Ohm 1/16 W 5% 0402
12	6	R6, R12, R18, R22, R23, R24	4K7	RES 4.7K Ohm 1/16 W 5% 0402
13	2	R8, R13	100R	RES SMD 100 Ohm 1% 1/16 W 0402
14	2	R9, R14	42.2R	RES SMD 42.2 Ohm 1% 1/16 W 0402
15	1	R11	100R	RES 100 Ohm 1/16 W 5% 0402
16	1	R3	100R	RES SMD 100 Ohm 1% 1 W 2512
17	1	R7	75K	RES SMD 75 kOhm 5% 1/16 W 0402
18	1	R1	10m	RES 0.01 Ohm 1/2 W 1% 1206
19	1	U1	LIF-UC	LIF-UC 48-Pin Device
20	1	U2	TS5A23159RSER	Switch Dual SPDT

BOM Count
Table 2-4. USB CD/PD Charger Solution (Non-Captive Cable) BOM Count^{1, 2}

Item	Component	Count
1	Cap	16
2	FET	2
3	Resistor	18
4	Lattice LIF-UC	1
5	Dual SPDT	1

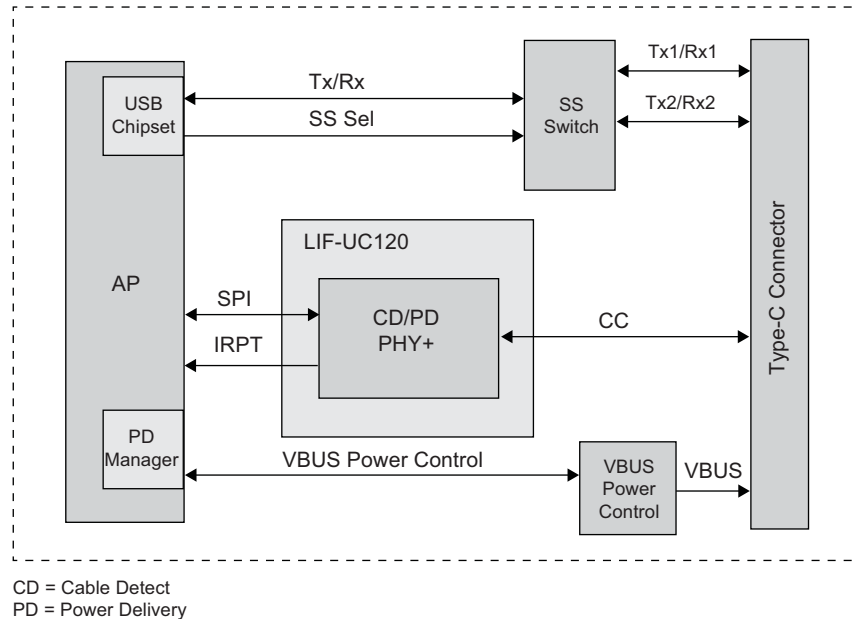
1. VBUS control section components are not included in the BOM count.

2. Diode D1 is not included in the BOM count. It is required only during onboard NVCM programming.

CD/PD PHY for Host/Devices

Block Diagram

Figure 2-6. CD/PD PHY for Host/Devices Block Diagram



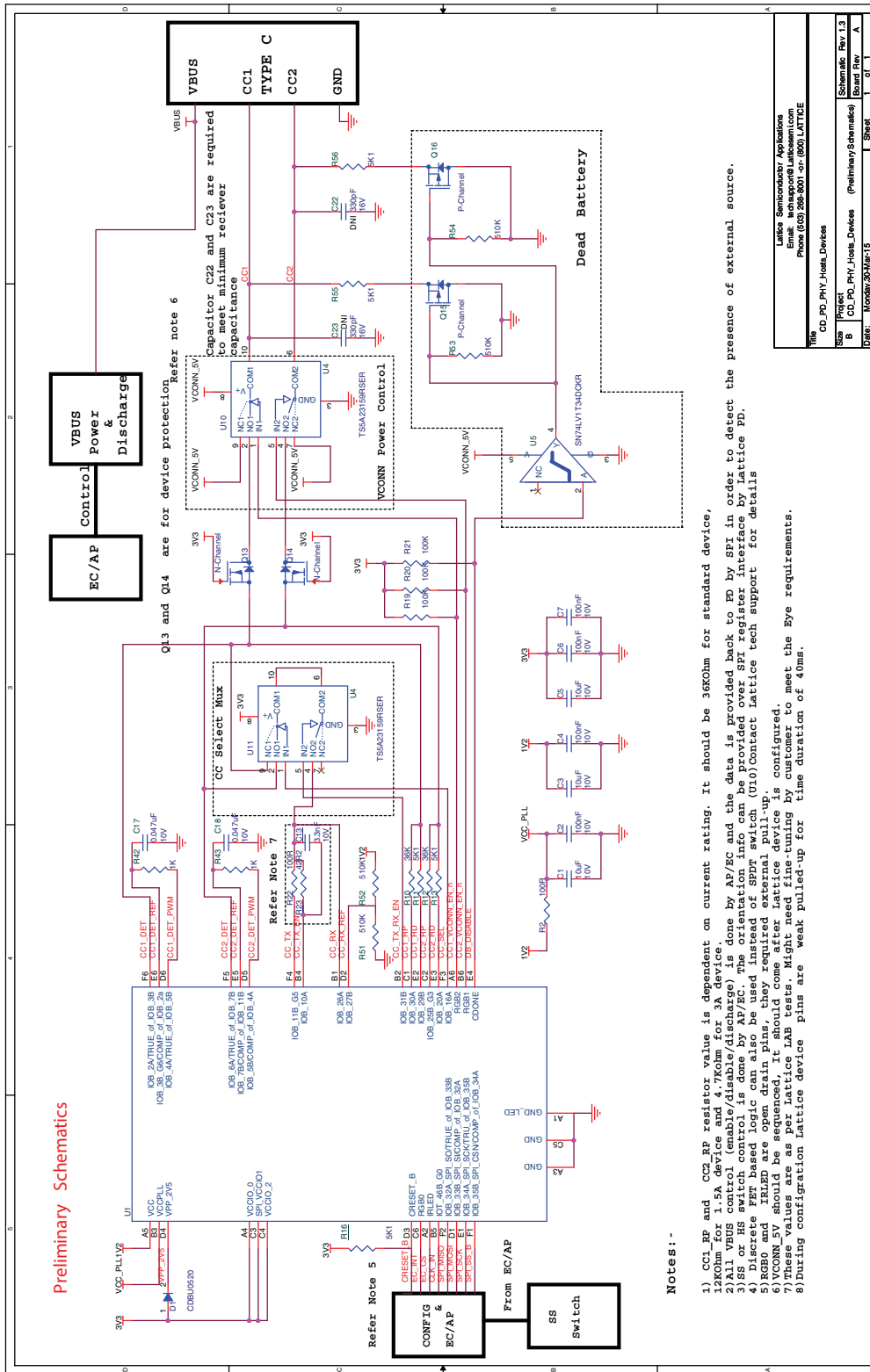
Features Supported in Schematics

- Dual Role Port (DRP)
- USB Power Delivery Communication between Port partners
- Dead Battery Support
- SPI Config interface is reused as SPI interface post configuration. SPI is used to interface PD to AP/Controller/Processor.

Note: VCONN supports up to 1 W power at 5 V supply.

Schematics

Figure 2-7. CD/PD Phy for Hosts/Devices Schematic Diagram



File	CD_PD_PHY_Hosts_Devices	Sheet	1
Project	CD_PD_PHY_Hosts_Devices (Preliminary Schematic)	Board Rev	A
Date	Monday, 23/11/15	Share	of 1

BOM
Table 2-5. CD/PD Phy for Hosts/Devices BOM

Item	Quantity	Reference	Part	Description	BOM_Note
1	3	C1, C3, C5	10 uF	CAP CER 10 uf 10 V 10% X5R 0805	
2	4	C2, C4, C6, C7	100 nF	CAP CER 100 nf 10 V 10% X5R 0402	
3	1	C13	3.3 nF	CAP CER 3300 pF 10 V 5% U2J 0402	
4	2	C17, C18	0.047 uF	CAP CER 0.047 uf 10 V 10% X5R 0402	
5	2	C22, C23	330 pF	CAP CER 330 pF 16 V 10% X7R 0402	DNI
6	1	D1	CDBU0520	DIODE SCHOTTKY 20 V 500 mA 0603	
7	2	Q13, Q14	N-Channel	MOSFET N-CH 30 V 0.85 A SOT23	
8	2	Q15, Q16	P-Channel	MOSFET P-CH 20 V 760 mA SOT-416	
9	1	R2	100R	RES 100 Ohm 1/16 W 5% 0402	
10	2	R10, R12	36K	RES 36K Ohm 1/16 W 5% 0402	
11	5	R11, R13, R16, R55, R56	5K1	RES 5.1K Ohm 1/16 W 5% 0402	
12	3	R19, R20, R21	100K	RES 100K Ohm 1/16 W 5% 0402	
13	1	R22	100R	RES SMD 100 Ohm 1% 1/16 W 0402	
14	1	R23	42R2	RES SMD 42.2 Ohm 1% 1/16 W 0402	
15	2	R42, R43	1K	RES 1 kOhm 1/16 W 5% 0402	
16	4	R51, R52, R53, R54	510K	RES 510 kOhm 1/16 W 5% 0402	
17	1	U1	LIF UC	LIF UC 36 Pin device	
18	1	U5	SN74LV1T34DCKR	IC BUFFER GATE SGL CMOS SC70-5	
19	2	U10, U11	TS5A23159RSER	SWITCH DUAL SPDT	

BOM Count
Table 2-6. CD/PD Phy for Hosts/Devices BOM Count¹

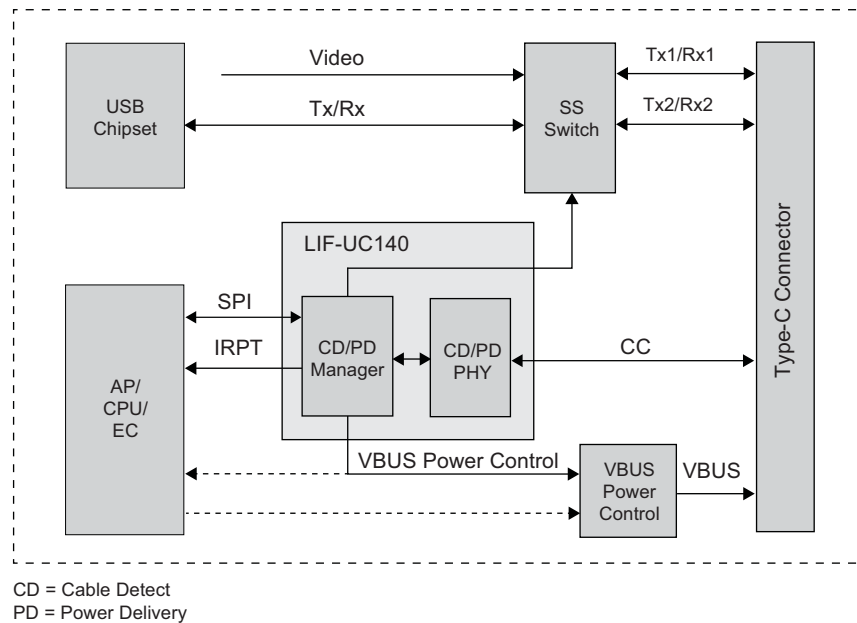
Item	Component	Count
1	Cap	12
2	FET	4
3	Resistor	19
4	Dual SPDT	2
5	Level Translator	1
6	Lattice LIF-UC	1

1. Diode D1 is not included in the BOM count. It is required only during onboard NVCM programming.

CD/PD for Hosts/Devices

Block Diagram

Figure 2-8. CD/PD for Hosts/Devices Block Diagram



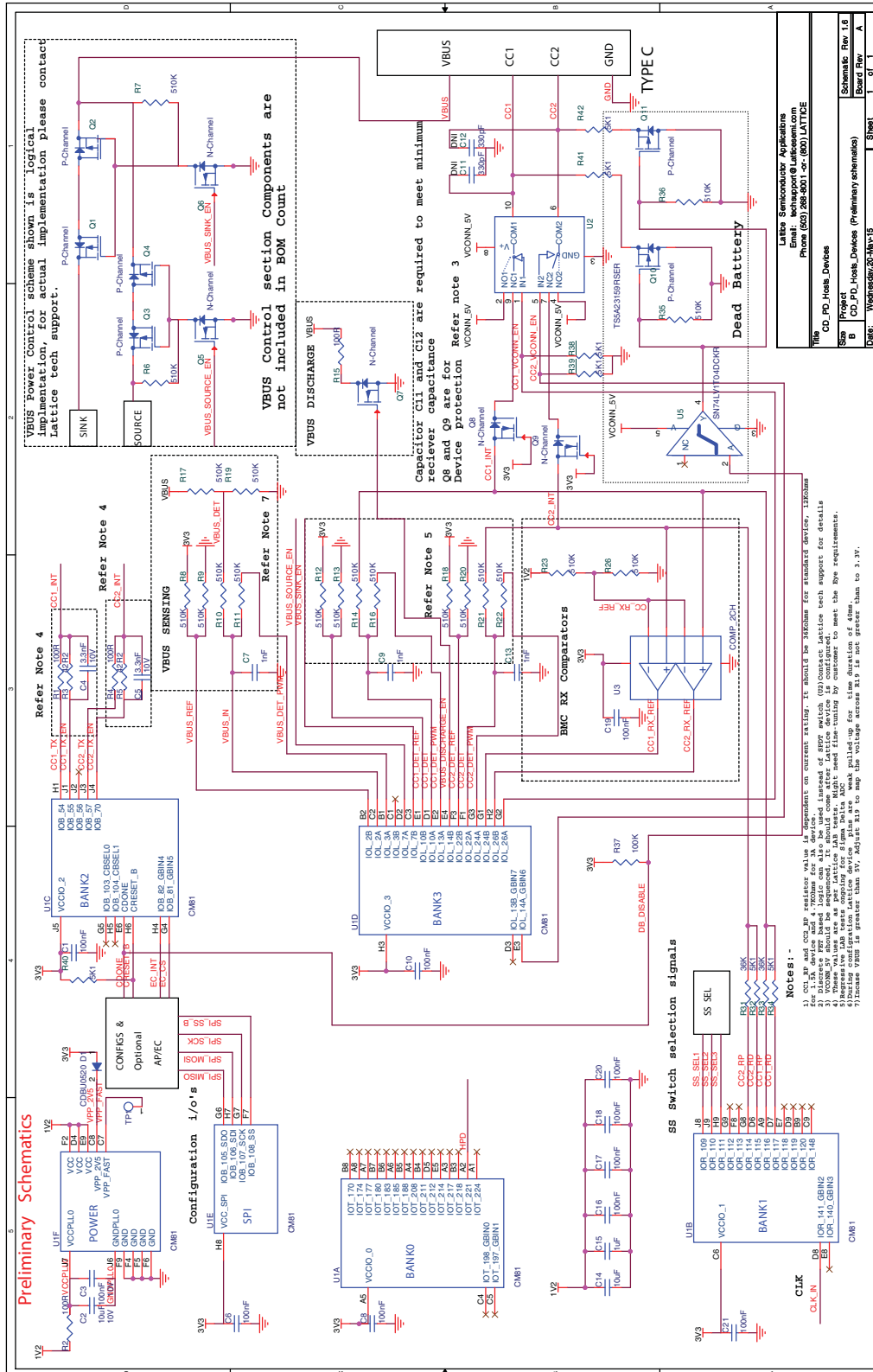
Features Supported in Schematics

- Dual Role Port (DRP)
- USB Power Delivery Communication between Port partners
- SS/HS switch control
- VBUS Source/Sink and Discharge Control signals
- Alternate mode support
- SPI Config interface is reused as SPI interface post configuration. SPI is used to interface PD to AP/Controller/Processor.

Note: VCONN supports up to 1 W power at 5 V supply.

Schematics

Figure 2-9. CD/PD for Hosts/Devices Schematic Diagram



BOM

Table 2-7. CD/PD for Hosts/Devices BOM

Item	Quantity	Reference	Part	DESCRIPTION
1	11	C1, C3, C6, C8, C10, C16, C17, C18, C19, C20, C21	100 nF	CAP CER 100 nf 10V 10% X5R 0402
2	2	C2, C14	10 uF	CAP CER 10 uf 10 V 10% X5R 0805
3	2	C4, C5	3.3 nF	CAP CER 3300 PF 10 V 5% U2J 0402
4	3	C7, C9, C13	1 nF	CAP CER 1000 PF 10 V 10% X5R 0402
5	2	C11, C12	330 pF	CAP CER 330 PF 16 V 10% X7R 0402
6	1	C15	1 uF	CAP CER 1 uf 10V 10% X5R 0402
7	1	D1	CDBU0520	DIODE SCHOTTKY 20 V 500 MA 0603
8	4	Q1, Q2, Q3, Q4	P-Channel	MOSFET P-CH 20 V 6 A SOT-23
9	4	Q5, Q6, Q8, Q9	N-Channel	MOSFET N-CH 30 V 0.85 A SOT23
10	1	Q7	N-Channel	MOSFET N-CH 20 V 6.3 A SOT-23
11	2	Q10, Q11	P-Channel	MOSFET P-CH 20 V 760 MA SOT-416
12	2	R1, R4	100R	RES SMD 100 Ohm 1% 1/16 W 0402
13	1	R2	100R	RES 100 OHM 1/16 W 5% 0402
14	2	R3, R5	42R2	RES SMD 42.2 Ohm 1% 1/16 W 0402
15	20	R6, R7, R8, R9, R10, R11, R12, R13, R14, R16, R17, R18, R19, R20, R21, R22, R23, R26, R35, R36	510K	RES 510K Ohm 1/16 W 5% 0402
16	1	R15	100R	RES SMD 100 Ohm 1% 1 W 2512
17	2	R31, R33	36K	RES 36K Ohm 1/16 W 5% 0402
18	7	R32, R34, R38, R39, R40, R41, R42	5K1	RES 5.1K Ohm 1/16 W 5% 0402
19	1	R37	100K	RES 100K Ohm M 1/16 W 5% 0402
20	1	U1	LIF-UC	LIF-UC 81 Pin Device
21	1	U2	TS5A23159RSER	SWITCH DUAL SPDT
22	1	U3	COMP_2CH	IC COMPARATR P-P NANOPWR SOT23-8
23	1	U5	SN74LV1T04DCKR	IC BUFFER GATE SGL CMOS SC70-5

BOM Count

Table 2-8. CD/PD for Hosts/Devices BOM Count^{1, 2}

Item	Component	Count
1	CAP	21
2	FET	4
3	Resistor	33
4	Dual SPDT	1
5	Level Translator	1
6	Comparator	1
6	Lattice LIF-UC	1

1. VBUS control section components are not Included in the BOM count.
2. Diode D1 is not included in the BOM count. It is required only during onboard NVCM programming.

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V_{CC}	-0.5 V to 1.42 V
Output Supply Voltage V_{CCIO}	-0.5 V to 3.60 V
NVCM Supply Voltage V_{PP_2V5}	-0.5 V to 3.60 V
PLL Supply Voltage V_{CCPLL}	-0.5 V to 1.42 V
I/O Tri-state Voltage Applied	-0.5 V to 3.60 V
Dedicated Input Voltage Applied	-0.5 V to 3.60 V
Storage Temperature (Ambient)	-65 °C to 150 °C
Junction Temperature (T_J)	-65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units		
V_{CC}^1	Core Supply Voltage	1.14	1.26	V		
V_{PP_2V5}	VPP_2V5 NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71	3.46	V	
		Master SPI Configuration	2.30	3.46	V	
		Configuration from NVCM	2.30	3.46	V	
		NVCM Programming	2.30	3.00	V	
$V_{CCIO}^{1, 2, 3}$	I/O Driver Supply Voltage	$V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}$		1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage	1.14	1.26	V		
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C		
t_{JIND}	Junction Temperature Industrial Operation	-40	100	°C		
t_{PROG}	Junction Temperature NVCM Programming	10.00	30.00	°C		

1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. Please refer to [Power-up Sequence](#) section. V_{CC} and V_{CCPLL} are not recommended to be tied together. Please refer to TN1252, [iCE40 Hardware Checklist](#).
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

Power Supply Ramp Rates^{1, 2}

Symbol	Parameter	Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.6	10	V/ms

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. Please refer to [Power-up Sequence](#) section.

Power-up Sequence

For all LIF-UC devices, it is required to have the V_{PP_2V5} to be powered up last among the supplies that are monitored by POR circuitry (V_{CC} , SPI_V_{CCIO1} , and V_{PP_2V5}). All supply voltages need to be powered up during configuration.

For the 36-pin WLCSP package (SWG36), the Power Up sequence is: V_{CC} and V_{CCPLL} , SPI_V_{CCIO1} , V_{PP_2V5} , V_{CCIO0} and V_{CCIO2} . Each supply has to wait until the previous supplies in the sequence have reached 0.5 V or higher.

There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are re-powered up again.

Power-On-Reset Voltage Levels¹

Symbol	Parameter	Min.	Max.	Units	
V_{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V_{CC} , SPI_V_{CCIO1} , V_{PP_2V5})	V_{CC}	0.62	0.92	V
		SPI_V_{CCIO1}	0.87	1.50	V
		V_{PP_2V5}	0.90	1.53	V
V_{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V_{CC} , SPI_V_{CCIO1} , V_{PP_2V5})	V_{CC}	—	0.79	V
		SPI_V_{CCIO1}	—	1.50	V
		V_{PP_2V5}	—	1.53	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL} , I_{IH} ^{1,3,4}	Input or I/O Leakage	$0V < V_{IN} < V_{CCIO} + 0.2 V$	—	—	+/-10	μA
C_1	I/O Capacitance, excluding LED Drivers ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = Typ., V_{IO} = 0 \text{ to } V_{CCIO} + 0.2 V$	—	6	—	pf
C_2	Global Input Buffer Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = Typ., V_{IO} = 0 \text{ to } V_{CCIO} + 0.2 V$	—	6	—	pf
C_3	RGB Pin Capacitance ²	$V_{CC} = Typ., V_{IO} = 0 \text{ to } 3.5 V$	—	15	—	pf
C_4	IRLED Pin Capacitance ²	$V_{CC} = Typ., V_{IO} = 0 \text{ to } 3.5 V$	—	53	—	pf
V_{HYST}	Input Hysteresis	$V_{CCIO} = 1.8 V, 2.5 V, 3.3 V$	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	$V_{CCIO} = 1.8 V, 0 \leq V_{IN} \leq 0.65 V_{CCIO}$	-3	—	-31	μA
		$V_{CCIO} = 2.5 V, 0 \leq V_{IN} \leq 0.65 V_{CCIO}$	-8	—	-72	μA
		$V_{CCIO} = 3.3 V, 0 \leq V_{IN} \leq 0.65 V_{CCIO}$	-11	—	-128	μA

- Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
- T_J 25 °C, $f = 1.0$ MHz.
- Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
- Some products are clamped to a diode when V_{IN} is larger than V_{CCIO} .

Supply Current ^{1, 2, 3, 4}

Symbol	Parameter	Typ. VCC = 1.2 V ⁴	Units
I _{CCSTDBY}	Core Power Supply Static Current	71	μA
I _{PP2V5STDBY}	VCC_V2P5 Power Supply Static Current	0.55	μA
I _{SPI_VCCIO1STDBY}	SPI_VCCIO1 Power Supply Static Current	0.5	μA
I _{CCIOSTDBY}	V _{CCIO} Power Supply Static Current	0.5	μA
I _{CCPEAK}	Core Power Supply Startup Peak Current	8.0	mA
I _{PP_2V5PEAK}	V _{PP_2V5} Power Supply Startup Peak Current	7.0	mA
I _{SPI_VCCIO1PEAK}	SPI_VCCIO1 Power Supply Startup Peak Current	9.0	mA
I _{CCIOPEAK}	V _{CCIO} Power Supply Startup Peak Current	7.5	mA

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. T_J = 25 °C, power supplies at nominal voltage, on devices processed in nominal process conditions.
4. Does not include pull-up.

User I²C Specifications

Parameter Symbol	Parameter Description	spec (STD Mode)			spec (FAST Mode)			Units
		Min	Typ	Max	Min	Typ	Max	
f _{SCL}	Maximum SCL clock frequency	—	—	100	—	—	400	kHz
t _{HI}	SCL clock HIGH Time	4	—	—	0.6	—	—	μs
t _{LO}	SCL clock LOW Time	4.7	—	—	1.3	—	—	μs
t _{SU,DAT}	Setup time (DATA)	250	—	—	100	—	—	ns
t _{HD,DAT}	Hold time (DATA)	0	—	—	0	—	—	ns
t _{SU,STA}	Setup time (START condition)	4.7	—	—	0.6	—	—	μs
t _{HD,STA}	Hold time (START condition)	4	—	—	0.6	—	—	μs
t _{SU,STO}	Setup time (STOP condition)	4	—	—	0.6	—	—	μs
t _{BUF}	Bus free time between STOP and START	4.7	—	—	1.3	—	—	μs
t _{CO,DAT}	SCL LOW to DATAOUT valid	—	—	3.4	—	—	0.9	μs

User SPI Specifications

Parameter Symbol	Parameter Description	Min	Typ	Max	Units
f _{MAX}	Maximum SCK clock frequency	—	—	45	MHz
t _{HI}	HIGH period of SCK clock	9	—	—	ns
t _{LO}	LOW period of SCK clock	9	—	—	ns
t _{SUmaster}	Setup time (master mode)	2	—	—	ns
t _{HOLDmaster}	Hold time (master mode)	5	—	—	ns
t _{SUslave}	Setup time (slave mode)	2	—	—	ns
t _{HOLDslave}	Hold time (slave mode)	5	—	—	ns
t _{SCK2OUT}	SCK to out (slave mode)	—	—	13.5	ns

Internal Oscillators (HFOSC, LFOSC)¹

Parameter		Parameter Description	Spec/Recommended			Units
Symbol	Conditions		Min	Typ	Max	
f _{CLKHF}	Commercial Temp	HFOSC clock frequency (t _J = 0 °C–85 °C)	–10%	48	10%	MHz
	Industrial Temp	HFOSC clock frequency (t _J = –40 °C–100 °C)	–20.00%	48	20.00%	MHz
f _{CLKLF}		LFOSC CLKK clock frequency	–10%	10	10%	kHz
DCH _{CLKHF}		HFOSC Duty Cycle (Clock High Period)	45	50	55	%
DCH _{CLKLF}		LFOSC Duty Cycle (Clock High Period)	45	50	55	%
Tsync_on		Oscillator output synchronizer delay	—	—	5	Cycles
Tsync_off		Oscillator output disable delay	—	—	5	Cycles

1. Glitchless enabling and disabling OSC clock outputs.

sysIO Recommended Operating Conditions

Standard	V _{CCIO} (V)		
	Min.	Typ.	Max.
LVC MOS 3.3	3.14	3.3	3.46
LVC MOS 2.5	2.37	2.5	2.62
LVC MOS 1.8	1.71	1.8	1.89

sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V _{IL}		V _{IH} ¹		V _{OL} Max. (V)	V _{OH} Min. (V)	I _{OL} Max. (mA)	I _{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVC MOS 3.3	–0.3	0.8	2.0	V _{CCIO} + 0.2V	0.4	V _{CCIO} – 0.5	8	–8
					0.2	V _{CCIO} – 0.2	0.1	–0.1
LVC MOS 2.5	–0.3	0.7	1.7	V _{CCIO} + 0.2V	0.4	V _{CCIO} – 0.5	6	–6
					0.2	V _{CCIO} – 0.2	0.1	–0.1
LVC MOS 1.8	–0.3	0.35V _{CCIO}	0.65V _{CCIO}	V _{CCIO} + 0.2V	0.4	V _{CCIO} – 0.4	4	–4
					0.2	V _{CCIO} – 0.2	0.1	–0.1

1. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.

Differential Comparator Electrical Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V _{INP} V _{INM}	Input Voltage	V _{CCIO} ¹ = 2.5	0	—	2.5	V
V _{THD}	Differential Input Threshold		250	350	450	mV
V _{CM}	Input Common Mode Voltage	V _{CCIO} ¹ = 2.5		V _{CCIO} /2		V
I _{IN}	Input Current	Power on	—	—	±10	µA

1. Typical.

Signal Descriptions

Signal Name	Function	I/O	Description
Power Supplies			
V _{CC}	Power	—	Core Power Supply
V _{CCIO_0} , SPI_V _{CCIO1} , V _{CCIO_2}	Power	—	Power for I/Os in Bank 0, 1, and 2.
V _{PP_2V5}	Power	—	Power for NVCM programming and operations
V _{CCPLL}	Power	—	Power for PLL.
GND	GROUND	—	Ground
Configuration			
CRESETB	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 k-Ohm pull-up to V _{CCIO_1}
CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to V _{CCIO_1}
	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
Config SPI			
SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pint outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external processor.
	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
SPI_SDO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pint outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the external processor.
	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pint receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the external processor.
	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function

SPI_CSN	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory. In Slave SPI mode, this pin inputs CSN from the external processor.
	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
CC1_RP		O	Enable signal to Connect RP to CC1 line 1:RP connected to CC1 line Z:RP not connected to CC1 line
CC1_TX		O	Configuration channel TX for CC1 line
CC1_TX_EN		O	Enable signal for CC1_TX 0:CC1_TX connected to CC1 line Z:CC1_TX not connected to CC1 line
CC1_DET		I	Cable detection on CC1 line
CC1_RX		I	Configuration channel RX for CC1 line
CC1_RD		O	Enable signal to Connect RD to CC1 line 0:RD connected to CC1 line Z:RD not connected to CC1 line
CC1_VCONN_EN		O	VCONN Enable 1:VCONN enabled on CC1 line 0:VCONN disabled on CC1 line
CC1_VCONN_EN_n		O	VCONN Enable 1:VCONN disabled on CC1 line 0:VCONN enabled on CC1 line
CC2_RP		O	Enable signal to Connect RP to CC2 line 1:RP connected to CC2 line Z:RP not connected to CC2 line
CC2_TX		O	Configuration channel TX for CC2 line
CC2_TX_EN		O	Enable signal for CC2_TX 0:CC2_TX connected to CC2 line Z:CC2_TX not connected to CC2 line
CC2_DET		I	Cable detection on CC2 line
CC2_RX		I	Configuration channel RX for CC2 line
CC2_RD		O	Enable signal to Connect RD to CC2 line 0:RD connected to CC2 line Z:RD not connected to CC2 line
CC2_VCONN_EN		O	VCONN Enable 1:VCONN enabled on CC2 line 0:VCONN disabled on CC2 line
CC2_VCONN_EN_n		O	VCONN Enable 1:VCONN disabled on CC2 line 0:VCONN enabled on CC2 line
CC_RX_REF		I	Reference Signal for CC1_RX and CC2_RX
CC1_DET_REF		I	Reference Signal for CC1_DET
CC1_DET_PWM		O	PWM signal to generate CC1_DET_REF
CC2_DET_REF		I	Reference Signal for CC2_DET

CC2_DET_PWM	O	PWM signal to generate CC2_DET_REF
DB_DISABLE	O	Disable signal to disable Dead battery MOSFET's
		1:Dead Battery MOSFE's disabled
		0:Dead Battery MOSFE's enabled
VBUS_SOURCE_EN	O	Enable Signal for VBUS Source
VBUS_SINK_EN	O	Enable Signal for VBUS Sink
VBUS_DSICHARGE_EN	O	Enable Signal for VBUS Discharge
		1:VBUS Discharge enabled
		0:VBUS Discharge disabled
VBUS_DET	I	VBUS detect and monitor signal
VBUS_REF	I	Reference signal for VBUS_DET
VBUS_DET_PWM		PWM signal to generate VBUS_REF
SS_SEL1, SS_SEL2, SS_SEL3	O	SS/HS Switch Control Signal
CLK_IN	I	4.8 MHz Clock or Even Multiples of 4.8 MHz such as 9.6 MHz or 19.2 MHz etc. LIF-UC110 and LIF-UC120 devices have an internal oscillator. It can also be used if the customer prefers not to use external clock source.
SPI_MISO	I/O	This pin is shared with device configuration and EC.After configuration. This pin is used SPI_MISO for EC.
SPI_MOSI	I/O	This pin is shared with device configuration and EC.After configuration. This pin is used SPI_MOSI for EC.
SPI_SCK	I/O	This pin is shared with device configuration and EC.After configuration. This pin is used SPI_SCK for EC.
SPI_SS_B	I	Chip select signal for Device configuration
EC_INT	O	Interrupt signal from FPGA to EC
EC_CS	I	Chip select signal from EC to FPGA
CDONE	I/O	Configuration Done. Includes a weak pull-up resistor to VCCIO_1
CRESETB	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10K-ohm pull-up to VCCIO_1
VSEL1,VSEL2,VSEL3,VSEL4	I/O	Voltage selection line 1 for selecting output voltage
VBUS_PG	O	VBUS power good signal
HPD	I/O	Hot Plug detect.
CC1_RX_REF	I	CC1 RX From external comparator
CC2_RX_REF	I	CC2 RX From external comparator
VBUS_IN	I	VBUS sense Input from the Connector
CC1_DET	I	CC1 input from the for cable detection
CC2_DET	I	CC2 input from the for cable detection



Lattice USB Type-C Solution Data Sheet Ordering Information

August 2015

Preliminary Data Sheet DS1052

Ordering Part Numbers

Part Number	Functional Description	Supply Voltage	Package	Pins	Temp.
LIF-UC110-SG48I	CD/PD for Charger	1.2 V	QFN	48	IND
LIF-UC120-SWG36I	CD/PD Phy for Hosts/Devices	1.2 V	WLCSP	36	IND
LIF-UC140-CM81I	CD/PD for Docks	1.2 V	CBGA	81	IND

Date	Version	Section	Change Summary
August 2015	1.3	Introduction	<p>Updated the Features section.</p> <ul style="list-style-type: none"> — Removed 81 caBGA under Wide Range of Packages to Match PCB Technology feature. — Updated Table 1-1, USB Type-C Device Table. <p>Revised heading to Package, Ball Pitch, Dimension and updated data. Removed the 81 BGA, 0.8 mm, 8 mm x 8 mm package.</p>
		Architecture	<p>Updated the Architecture Overview section. Revised Figure 2-1, High-level Functional Block for USB Type-C Physical Layer and Power Detect Protocol.</p>
			<p>Updated the USB CD/PD Charger Solution (Captive Cable) section. Revised Figure 2-2, USB CD/PD Charger Solution (Captive Cable) Block Diagram.</p>
			<p>Updated the USB CD/PD Charger Solution (Non-Captive Cable). Revised Figure 2-4, USB CD/PD Charger Solution (Non-Captive Cable) Block Diagram</p>
			<p>Updated the CD/PD PHY for Host/Devices. Revised Figure 2-6, CD/PD PHY for Host/Devices Block Diagram.</p>
<p>Updated the CD/PD for Hosts/Devices. Revised Figure 2-8, CD/PD for Host/Devices Block Diagram.</p>			
Ordering Information	<p>Updated Ordering Part Numbers section. Removed LIF-UC140-BG811 part number.</p>		
June 2015	1.2	Architecture	<p>Updated the USB CD/PD Charger Solution (Non-Captive Cable) section.</p> <ul style="list-style-type: none"> — Modified Figure 2-5, USB CD/PD Charger Solution (Non-Captive Cable) Schematic Diagram. Added VCONN switch for SOP support. — Updated Table 2-3, CD/PD for Hosts/Devices BOM. USB CD/PD Charger Solution (Non-Captive Cable) BOM. Revised Item 12. Added Item 20. — Updated Table 2-4, USB CD/PD Charger Solution (Non-Captive Cable) BOM Count. Revised Item 3. Added Item 5.
			<p>Updated the CD/PD PHY for Host/Devices section. Added note in supported features in schematics.</p>
			<p>Updated the CD/PD for Hosts/Devices section.</p> <ul style="list-style-type: none"> — Added note in supported features in schematics. — Modified Figure 2-9, CD/PD for Hosts/Devices Schematic Diagram. Changed R38 and R39 resistor values to 5.1 kOhm. — Updated Table 2-7, CD/PD for Hosts/Devices BOM. Revised Items 15 and 18.
March 2015	1.1	Architecture	<p>Updated the USB CD/PD Charger Solution (Captive Cable) section. Modified Figure 2-3, USB CD/PD Charger Solution (Captive Cable) Schematic Diagram.</p> <ul style="list-style-type: none"> — Updated BMX TX resistor values. — Added RC Circuit provision for BMC reference voltage. — Added pull-up resistors for CDONE. <p>Updated Table 2-1, USB CD/PD Mobile System Solution (Captive Cable) BOM and Table 2-2, USB CD/PD Mobile System Solution (Captive Cable) BOM Count.</p>

Date	Version	Section	Change Summary
			<p>Updated the USB CD/PD Charger Solution (Non-Captive Cable) section.</p> <p>Modified Figure 2-5, USB CD/PD Charger Solution (Non-Captive Cable) Schematic Diagram.</p> <ul style="list-style-type: none"> — Updated BMX TX resistor values. — Added RC Circuit provision for BMC reference voltage. — Added pull-up resistors for CDONE. <p>Updated Table 2-3, USB CD/PD Charger Solution (Non-Captive Cable) BOM and Table 2-4, USB CD/PD Charger Solution (Non-Captive Cable) BOM Count.</p> <hr/> <p>Updated the CD/PD PHY for Host/Devices section.</p> <p>Modified Figure 2-6, CD/PD Phy for Host/Devices Block Diagram.</p> <p>Removed items in Features Supported in Schematics.</p> <p>Modified Figure 2-7, CD/PD Phy for Hosts/Devices Schematic Diagram.</p> <ul style="list-style-type: none"> — Updated BMX TX resistor values. <p>Updated Table 2-5, CD/PD Phy for Hosts/Devices BOM and Table 2-6, CD/PD Phy for Hosts/Devices BOM Count.</p> <hr/> <p>Updated the CD/PD for Hosts/Devices section.</p> <p>Modified Figure 2-9, CD/PD for Hosts/Devices Schematic Diagram.</p> <ul style="list-style-type: none"> — Updated BMX TX resistor values. — Added dead battery circuit. — Moved DB-Disable signal to CDONE pin. — Changed Rx Comparator Power supply voltage to 3.3 V. <p>Added Table 2-7, CD/PD for Hosts/Devices BOM and Table 2-8, CD/PD for Hosts/Devices BOM Count.</p> <hr/> <p>Pinout Information</p> <p>Updated Signal Descriptions section.</p>
February 2015	1.0	All	Initial release.