SBAS224B – DECEMBER 2001 – REVISED MAY 2002

16-Bit, 500kSPS, *micro*Power Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH-SPEED PARALLEL INTERFACE
- 500kSPS SAMPLING RATE
- LOW POWER: 85mW at 500kSPS
- BIPOLAR INPUT RANGE
- TQFP-32 PACKAGE

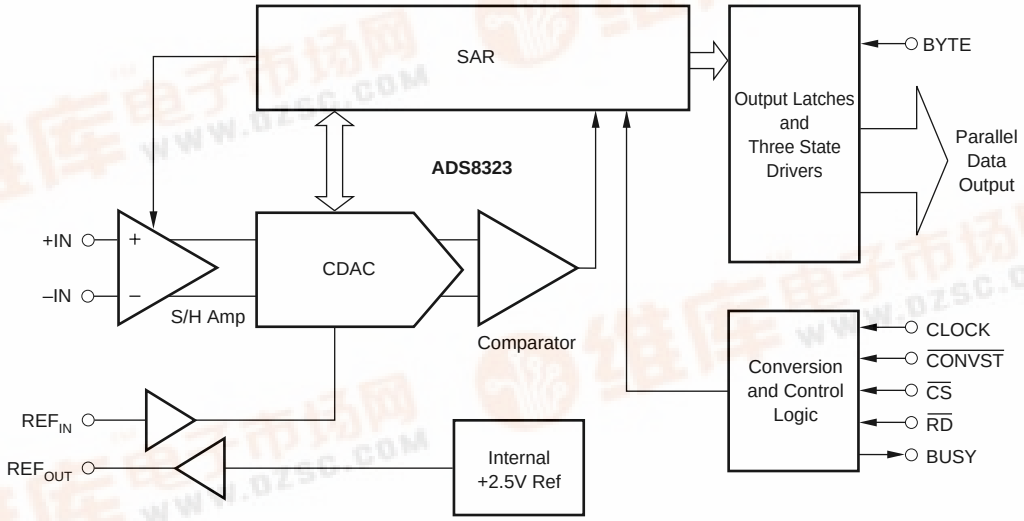
APPLICATIONS

- HIGH-SPEED DATA AQUISITION
- OPTICAL POWER MONITORING
- MOTOR CONTROL
- ATE

DESCRIPTION

The ADS8323 is a 16-bit, 500kSPS Analog-to-Digital Converter (ADC) with an internal 2.5V reference. The device includes a 16-bit capacitor-based SAR ADC with inherent sample-and-hold. The ADS8323 offers a full 16-bit interface, or an 8-bit option where data is read using two read cycles.

The ADS8323 is available in a TQFP-32 package and is specified over the industrial –40°C to +85°C temperature range.



PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	NO MISSING CODES ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS8323Y	±8	14	TQFP-32	PBS	–40°C to 85°C	ADS8323Y/250	Tape and Reel, 250
"	"	"	"	"	"	ADS8323Y/2K	Tape and Reel, 2000
ADS8323YB	±6	15	TQFP-32	PBS	–40°C to 85°C	ADS8323YB/250	Tape and Reel, 250
"	"	"	"	"	"	ADS8323YB/2K	Tape and Reel, 2000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings over operating free-air temperature (unless otherwise noted)(1)

Supply Voltage, DGND to DV_{DD}	–0.3V to 6V
Supply Voltage, AGND to AV_{DD}	–0.3V to 6V
Analog Input Voltage Range	AGND - 0.3V to AV_{DD} + 0.3V
Reference Input Voltage	AGND - 0.3V to AV_{DD} + 0.3V
Digital Input Voltage Range	DGND - 0.3V to DV_{DD} + 0.3V
Ground Voltage Differences, AGND to DGND	±0.3V
Voltage Differences, DV_{DD} to AGND	–0.3V to 6V
Power Dissipation	850mW
Operating Virtual Junction Temperature Range, T_J	–40°C to 150°C
Operating Free-Air Temperature Range, T_A	–40°C to 85°C
Storage Temperature Range, T_{STG}	–65°C to 150°C
Lead Temperature 1.6mm (1/16 inch) from Case for 10sec	260°C

NOTE: (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions of extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

RECOMMENDED OPERATING CONDITIONS

POWER SUPPLY		MIN	TYP	MAX	UNIT
Supply Voltage	AV_{DD}(1)	4.75	5.0	5.25	V
	DV_{DD}(1)	4.75	5.0	5.25	V
ANALOG/REFERENCE INPUTS					
Differential analog input voltage (IN+ to IN–)		$–REF_{IN}$		$+REF_{IN}$	V
External Reference Voltage		1.5	2.5	2.55	V

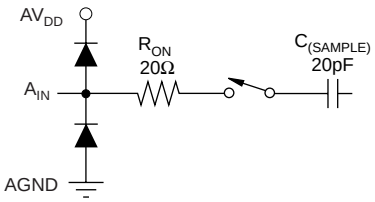
NOTE: (1) The voltage difference between AV_{DD} and DV_{DD} terminals cannot exceed 0.3V to maintain performance specifications.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$(1)	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
TQFP-32	1636mW	13.09mW/°C	1047mW	850mW

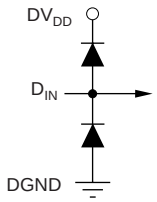
NOTE: (1) This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$). Thermal resistances are not production tested and are for informational purposes only.

EQUIVALENT INPUT CIRCUIT



Diode Turn-On Voltage: 0.35V

Equivalent Analog Input Circuit



Equivalent Digital Input Circuit

ELECTRICAL CHARACTERISTICS

At –40°C to +85°C, $+DV_{DD}$ = $+AV_{DD}$ = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 500kSPS, and f_{CLK} = 20 • f_{SAMPLE}, unless otherwise specified.

PARAMETER	CONDITIONS	ADS8323Y			ADS8323YB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
ANALOG INPUT								
Full-Scale Input Span[1]	+IN – (–IN)	$–V_{REF}$		$+V_{REF}$	*		*	V
Absolute Input Range	+IN	–0.3		AV_{DD} + 0.3	*		*	V
	–IN	–0.3		AV_{DD} + 0.3	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		nA
SYSTEM PERFORMANCE								
No Missing Codes		14			15			Bits
Integral Linearity Error			±4	±8		±3	±6	LSB[2]
Differential Linearity Error			±3			±1		LSB
Offset Error			±1	±2		±0.5	±1	mV
Gain Error[3]			±0.25	±0.5		±0.12	±0.25	% of FSR
Common-Mode Rejection Ratio	At DC		70			*		dB
	V_{IN} = 1Vp-p at 1MHz		50			*		dB
Noise			60			*		µVrms
Power-Supply Rejection	At $FFFF_H$ Output Code		±3			*		LSB
SAMPLING DYNAMICS								
Conversion Time		1.6			*			µs
Acquisition Time		0.4			*			µs
Throughput Rate				500			*	kSPS
Aperture Delay			10			*		ns
Aperture Jitter			30			*		ps
Small-Signal Bandwidth			20			*		MHz
Step Response			100			*		ns
Overvoltage Recovery			150			*		ns
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[4]	V_{IN} = 5Vp-p at 100kHz		–90			–93		dB
SINAD	V_{IN} = 5Vp-p at 100kHz		81			83		dB
Spurious-Free Dynamic Range	V_{IN} = 5Vp-p at 100kHz		94			96		dB
REFERENCE OUTPUT								
Voltage	I_{OUT} = 0	2.475	2.50	2.525	2.48	*	2.52	V
Source Current	Static Load			10			*	µA
Drift	I_{OUT} = 0		25			*		ppm/°C
Line Regulation	4.75V ≤ V_{CC} ≤ 5.25V		0.6			*		mV
REFERENCE INPUT								
Range		1.5		2.55	*		*	V
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels:								
V_{IH}	I_{IH} ≤ +5µA	3.0		$+DV_{DD}$	*		*	V
V_{IL}	I_{IL} ≤ –5µA	–0.3		0.8	*		*	V
V_{OH}	I_{OH} = –1.6mA	4.0			*			V
V_{OL}	I_{OL} = +1.6mA			0.4			*	V
Data Format		Binary Two's Complement					*	
POWER-SUPPLY REQUIREMENT								
Power-Supply Voltage								
$+AV_{DD}$		4.75	5	5.25	*	*	*	V
$+DV_{DD}$		4.75	5	5.25	*	*	*	V
Supply Current	f_{SAMPLE} = 500kSPS		17	25		*	*	mA
Power Dissipation	f_{SAMPLE} = 500kSPS		85	125		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Specifications same as ADS8323Y.

NOTES: (1) Ideal input span; does not include gain or offset error. (2) LSB means Least Signifcant Bit, with V_{REF} equal to +2.5V; 1LSB = 76µV. (3) Measured relative to an ideal, full-scale input (+In – (–In)) of 4.9999V. Thus, gain error includes the error of the internal voltage reference. (4) Calculated on the first nine harmonics of the input frequency.

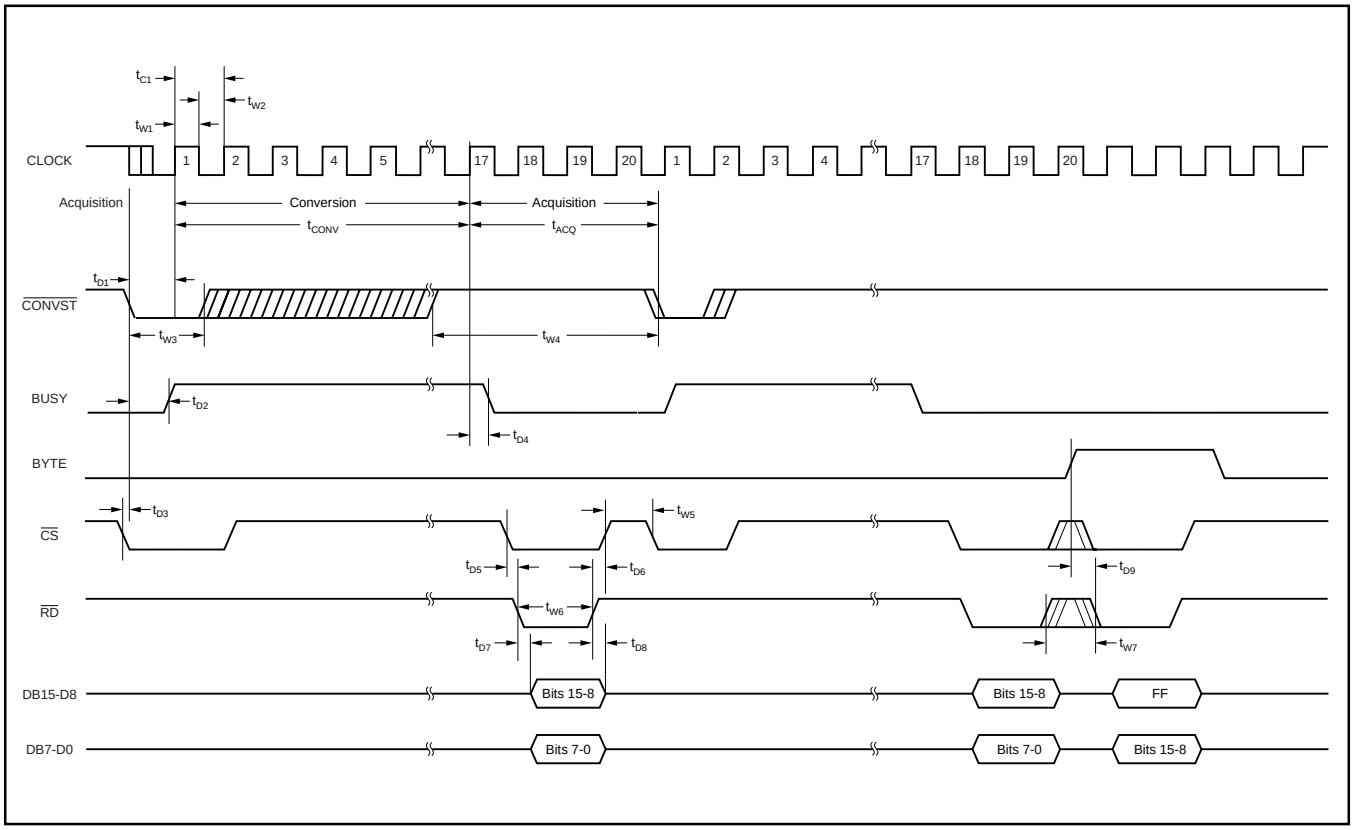
TIMING CHARACTERISTICS(1)(2)

All specifications typical at –40°C to +85°C, $+DV_{DD}$ = +5V.

PARAMETER	SYMBOL	ADS8323Y			ADS8323YB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Conversion Time	t_{CONV}			1.6			*	µs
Acquisition Time	t_{ACQ}			0.4			*	µs
CLOCK Period	t_{C1}	100			*			ns
CLOCK HIGH Time	t_{W1}	40			*			ns
CLOCK LOW Time	t_{W2}	40			*			ns
$\overline{CONVST}$ LOW to CLOCK HIGH	t_{D1}	10			*			ns
$\overline{CONVST}$ LOW Time	t_{W3}	20			*			ns
$\overline{CONVST}$ LOW to BUSY HIGH	t_{D2}			25			*	ns
$\overline{CS}$ LOW to $\overline{CONVST}$ LOW	t_{D3}	0			*			ns
$\overline{CONVST}$ HIGH	t_{W4}	20			*			ns
CLOCK HIGH to BUSY LOW	t_{D4}			25			*	ns
$\overline{CS}$ HIGH	t_{W5}	0			*			ns
$\overline{CS}$ LOW to $\overline{RD}$ LOW	t_{D5}	0			*			ns
$\overline{RD}$ HIGH to $\overline{CS}$ HIGH	t_{D6}	0			*			ns
$\overline{RD}$ LOW Time	t_{W6}	50			*			ns
$\overline{RD}$ LOW to Data Valid	t_{D7}	40			*			ns
Data Hold from $\overline{RD}$ HIGH	t_{D8}	5			*			ns
BYTE Change to $\overline{RD}$ LOW(3)	t_{D9}	0			*			ns
$\overline{RD}$ HIGH Time	t_{W7}	20			*			ns

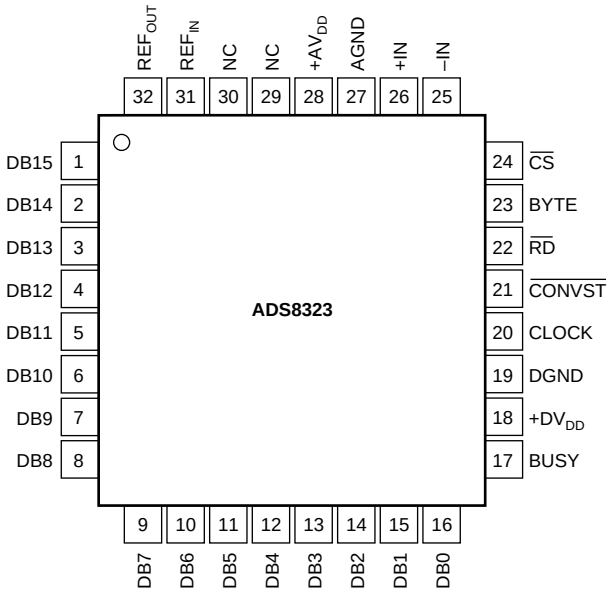
NOTES: (1) All input signals are specified with rise and fall times of 5ns, $t_R = t_F$ = 5ns (10% to 90% of DV_{DD}), and timed from a voltage level of $(V_{IL} + V_{IH})/2$. (2) See timing diagram, below. (3) BYTE is asynchronous; when BYTE is 0, bits 15 through 0 appear at DB15-DB0. When BYTE is 1, bits 15 through 8 appear on DB7-DB0. $\overline{RD}$ may remain LOW between changes in BYTE.

TIMING DIAGRAM



PIN CONFIGURATION

Top View **TQFP**



PIN ASSIGNMENTS

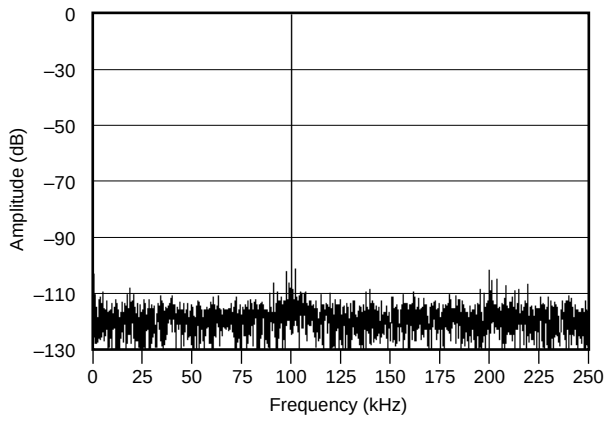
PIN	NAME	I/O	DESCRIPTION	PIN	NAME	I/O	DESCRIPTION
1	DB15	DO	Data Bit 15 - MSB	19	DGND	P	Digital Ground
2	DB14	DO	Data Bit 14	20	CLOCK	DI	An external CMOS compatible clock can be applied to the CLOCK input to synchronize the conversion process to an external source.
3	DB13	DO	Data Bit 13				
4	DB12	DO	Data Bit 12				
5	DB11	DO	Data Bit 11	21	$\overline{\text{CONVST}}$	DI	Convert Start, Active LOW.
6	DB10	DO	Data Bit 10	22	$\overline{\text{RD}}$	DI	Synchronization pulse for the parallel output, Active LOW.
3	DB9	DO	Data Bit 9				
8	DB8	DO	Data Bit 8	23	BYTE	DI	Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH). Data valid on pins 9-16.
9	DB7	DO	Data Bit 7				
10	DB6	DO	Data Bit 6	24	$\overline{\text{CS}}$	DI	Chip Select, Active LOW.
11	DB5	DO	Data Bit 5	25	–IN	AI	Inverting Input Channel
12	DB4	DO	Data Bit 4	26	+IN	AI	Noninverting Input Channel
13	DB3	DO	Data Bit 3	27	AGND	P	Analog Ground
14	DB2	DO	Data Bit 2	28	$+AV_{DD}$	P	Analog Power Supply, +5VDC.
15	DB1	DO	Data Bit 1	29	NC	—	No Connect
16	DB0	DO	Data Bit 0 - LSB	30	NC	—	No Connect
17	BUSY	DO	HIGH when a conversion is in progress.	31	REF_{IN}	AI	Reference Input. When using the internal 2.5V reference tie this pin directly to REF_{OUT}.
18	$+DV_{DD}$	P	Digital Power Supply, +5VDC.				
				32	REF_{OUT}	AO	Reference Output

NOTE: AI is Analog Input, AO is Analog Output, DI is Digital Input, DO is Digital Output, and P is Power-Supply Connection.

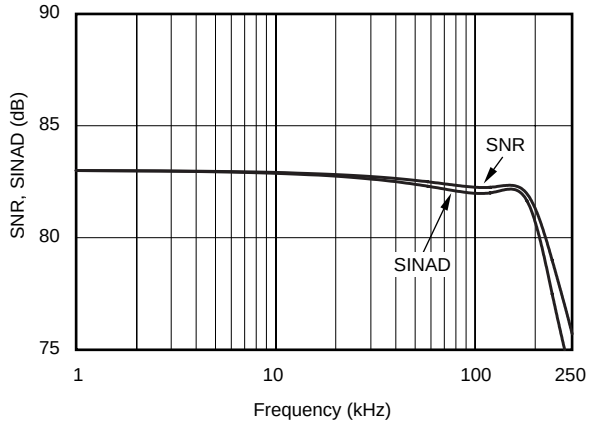
TYPICAL CHARACTERISTICS

At –40°C to +85°C, $+DV_{DD}$ = $+AV_{DD}$ = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 500kSPS, and f_{CLK} = 20 • f_{SAMPLE}, unless otherwise specified.

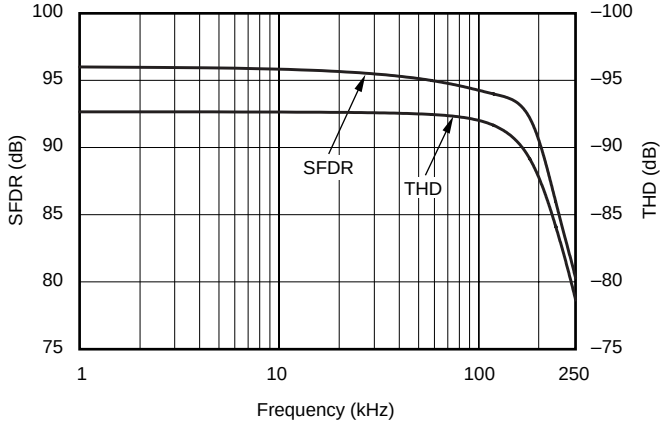
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 100.1kHz, –0.2dB)



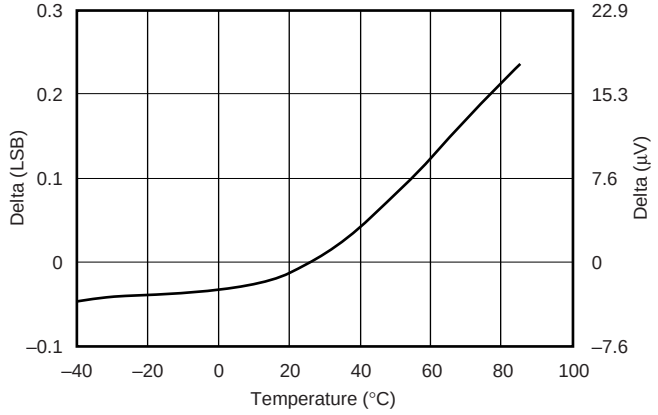
SIGNAL-TO-NOISE RATIO AND
SIGNAL-TO-(NOISE+DISTORTION)
vs INPUT FREQUENCY



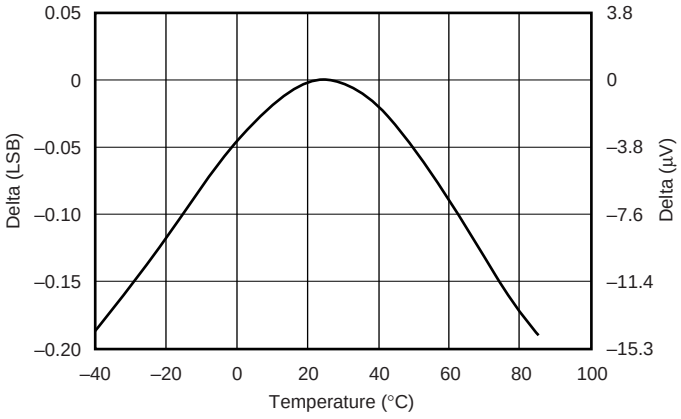
SPURIOUS-FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY



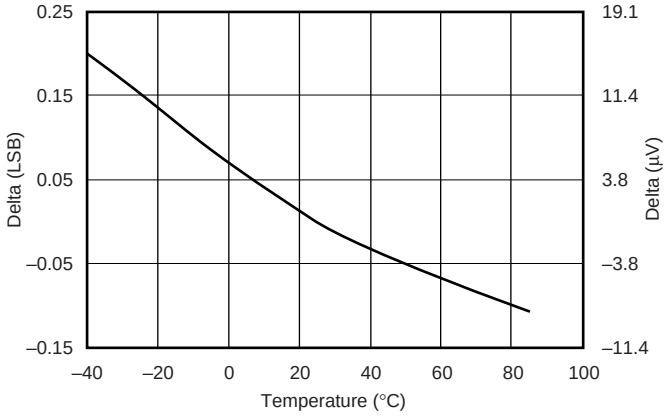
INL+ vs TEMPERATURE



INL– vs TEMPERATURE



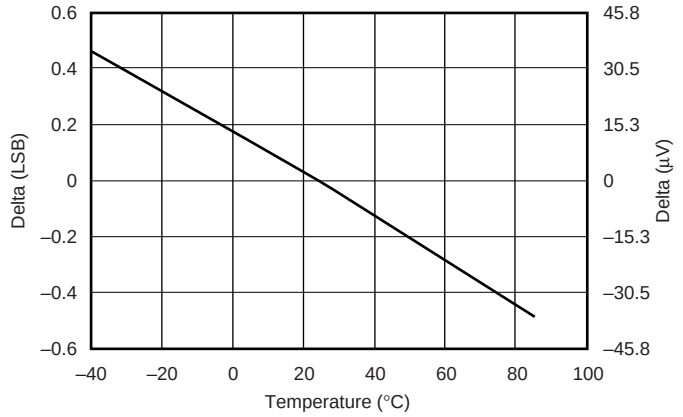
DNL+ vs TEMPERATURE



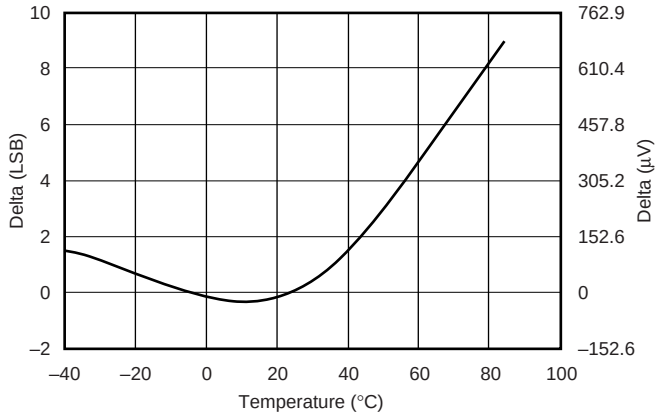
TYPICAL CHARACTERISTICS (Cont.)

At –40°C to +85°C, $+DV_{DD}$ = $+AV_{DD}$ = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 500kSPS, and f_{CLK} = 20 • f_{SAMPLE}, unless otherwise specified.

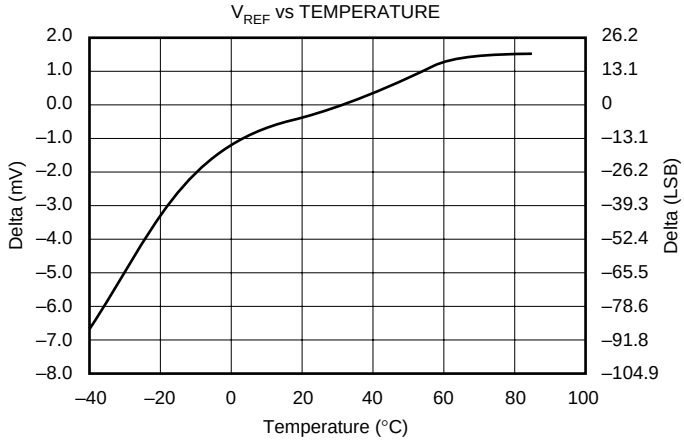
DNL– vs TEMPERATURE



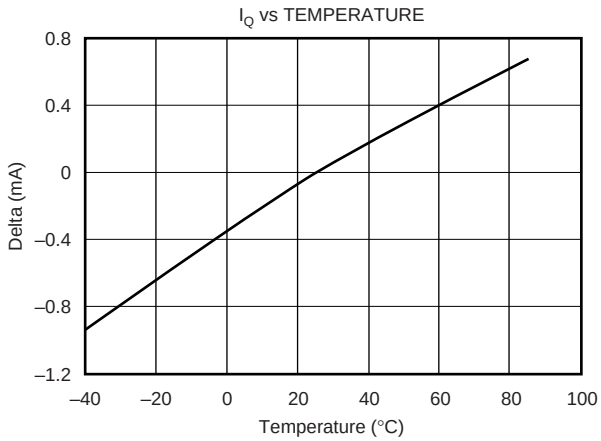
GAIN ERROR vs TEMPERATURE



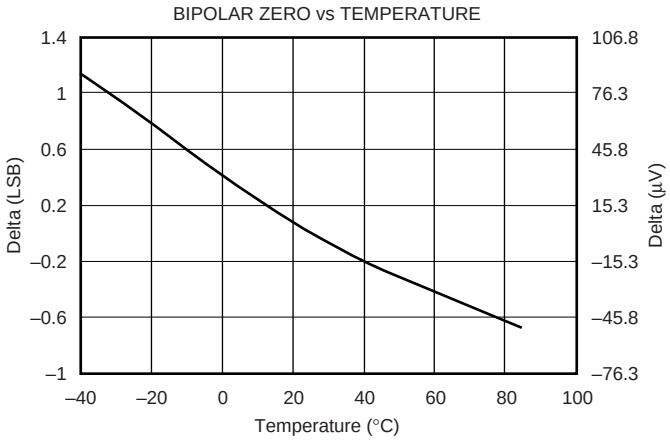
V_{REF} vs TEMPERATURE



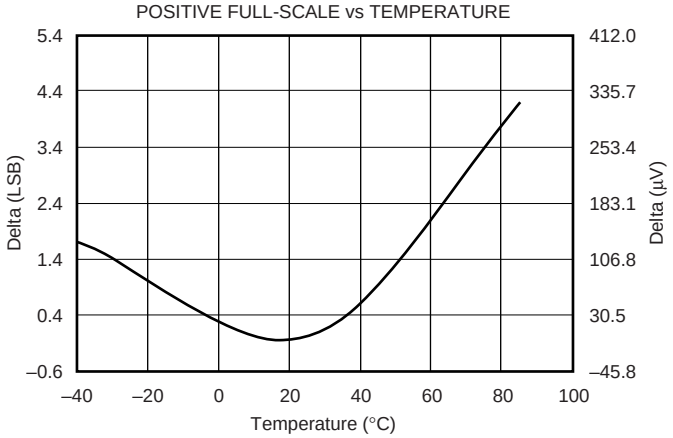
I_Q vs TEMPERATURE



BIPOLAR ZERO vs TEMPERATURE

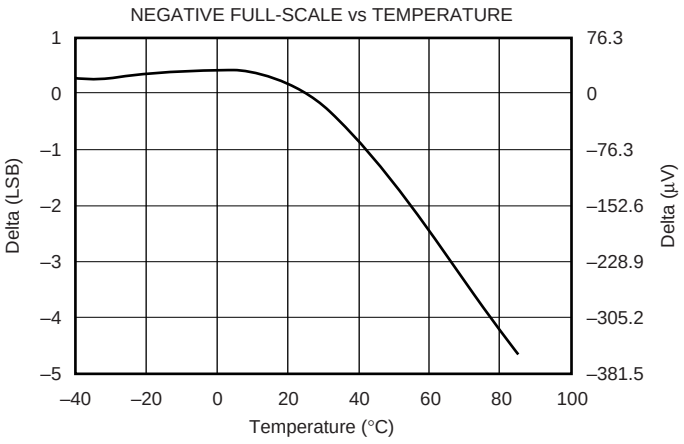


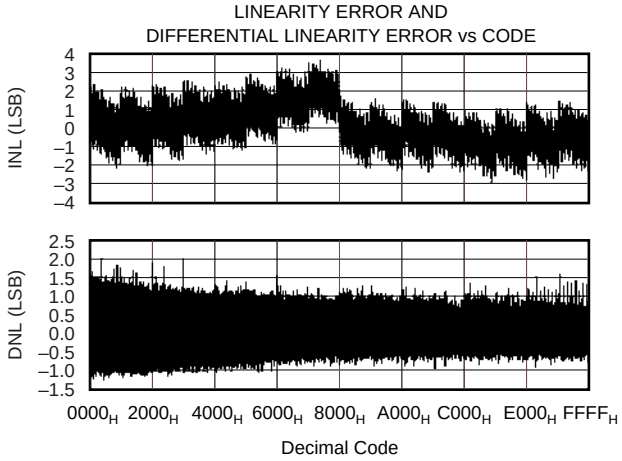
POSITIVE FULL-SCALE vs TEMPERATURE



TYPICAL CHARACTERISTICS (Cont.)

At –40°C to +85°C, $+DV_{DD}$ = $+AV_{DD}$ = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 500kSPS, and f_{CLK} = 20 • f_{SAMPLE}, unless otherwise specified.





THEORY OF OPERATION

The ADS8323 is a high-speed Successive Approximation Register (SAR) 16-bit ADC with an internal 2.5V bandgap reference that operates from a single +5V supply. The input is fully differential with a typical common-mode rejection of 70dB. The part accepts a differential analog input voltage in the range of $–V_{REF}$ to $+V_{REF}$, centered on the common-mode voltage (see the Analog Input section). The part will also accept bipolar input ranges when a level shift circuit is used at the front end (see Figure 7). See Figure 1 for the basic operating circuit for the ADS8323.

The ADS8323 requires an external clock to run the conversion process. This clock can vary between 25kHz (1.25kHz throughput) and 10MHz (500kSPS throughput). The duty cycle of the clock is unimportant as long as the minimum HIGH and LOW times are at least 40ns and the clock period is at least 100ns. The minimum clock frequency is governed by the parasitic leakage of the Capacitive Digital-to-Analog Converter (CDAC) capacitors internal to the ADS8323.

The analog input is provided to two input pins, +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. A conversion is initiated on the ADS8323 by bringing $\overline{\text{CONVST}}$ (pin 21) LOW for a minimum of 20ns. $\overline{\text{CONVST}}$ LOW places the sample-and-hold amplifier in the hold state and the conversion process is started. The BUSY output (pin 17) will go HIGH when the conversion begins and will stay HIGH during the conversion. While a conversion is in progress, both inputs are disconnected from any internal function. When the conversion result is latched into the output register, the BUSY signal will go LOW. The data can be read from the parallel output bus following the conversion by bringing both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ LOW.

NOTE: This mode of operation is described in more detail in the Timing and Control section of this data sheet.

SAMPLE-AND-HOLD SECTION

The sample-and-hold on the ADS8323 allow the ADC to accurately convert an input sine wave of full-scale amplitude to 16-bit resolution. The input bandwidth of the sample-and-hold is greater than the Nyquist rate (Nyquist equals one-half of the sampling rate) of the ADC even when the ADC is operated at its maximum throughput rate of 500kSPS. The typical small-signal bandwidth of the sample-and-hold amplifier is 20MHz. Typical aperture delay time, or the time it takes for the ADS8323 to switch from the sample to the hold mode following the negative edge of the $\overline{\text{CONVST}}$ signal, is 10ns. The average delta of repeated aperture delay values is typically 30ps (also known as aperture jitter). These specifications reflect the ability of the ADS8323 to capture AC input signals accurately at the exact same moment in time.

REFERENCE

If the internal reference is used, REF_{OUT} (pin 32) should be directly connected to REF_{IN} (pin 31). The ADS8323 can operate, however, with an external reference in the range of 1.5V to 2.55V for a corresponding full-scale range of 3.0V to 5.1V. The internal reference of the ADS8323 is double-buffered. If the internal reference is used to drive an external load, a buffer is provided between the reference and the load applied to REF_{OUT} (pin 32) (the internal reference can typically source or sink 10µA of current; compensation capacitance should be at least 0.1µF to minimize noise). If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of the CDAC during conversion.

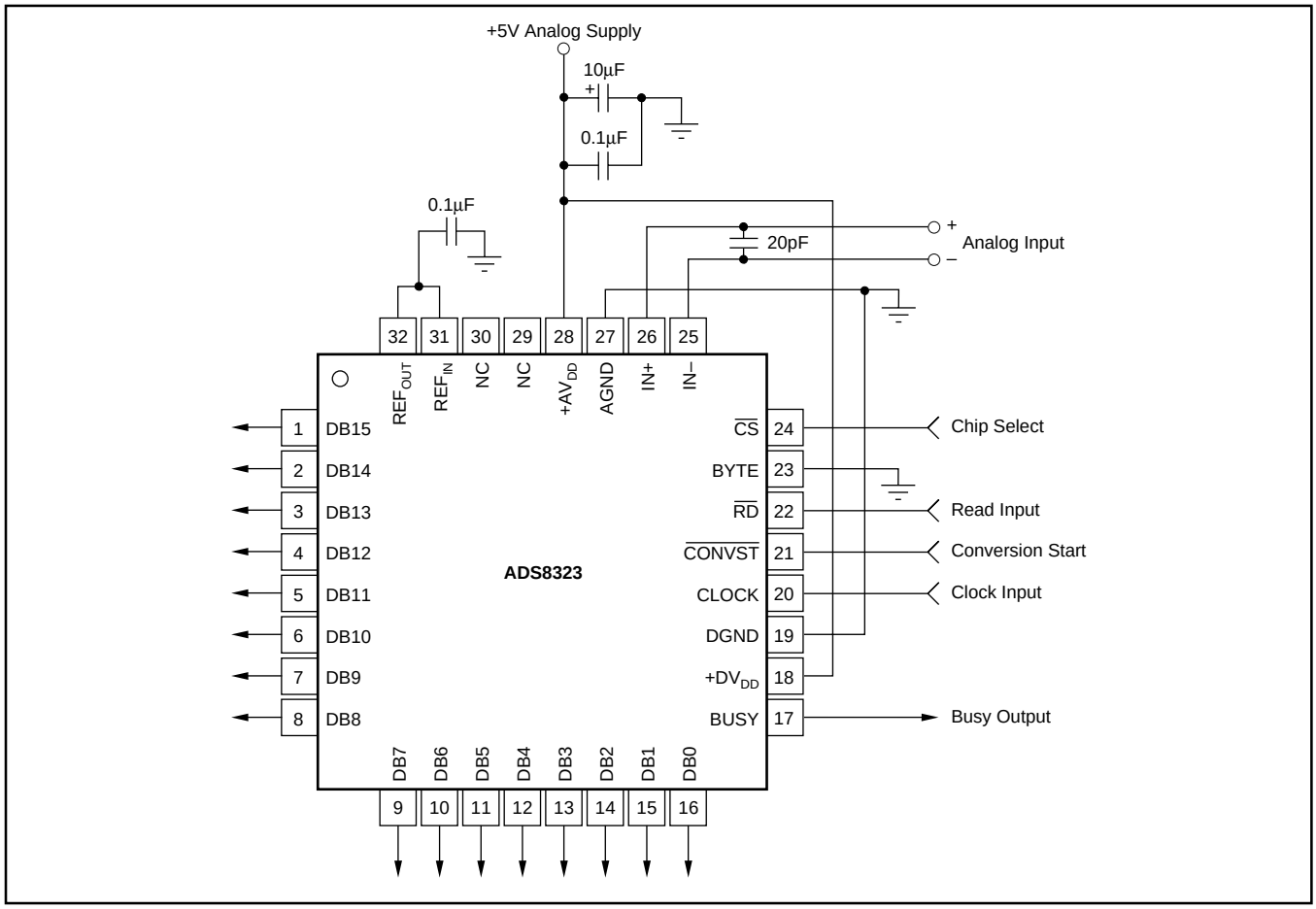


FIGURE 1. Typical Circuit Configuration.

ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS8323: single-ended or differential, as shown in Figures 2 and 3. When the input is single-ended, the –IN input is held at the common-mode voltage. The +IN input swings around the same common voltage and the peak-to-peak amplitude is the (common-mode + V_{REF}) and the (common-mode – V_{REF}). The value of V_{REF} determines the range over which the common-mode voltage may vary (see Figure 4).

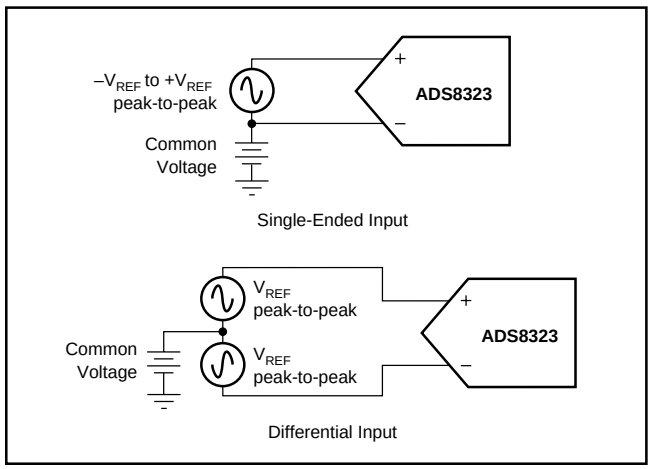


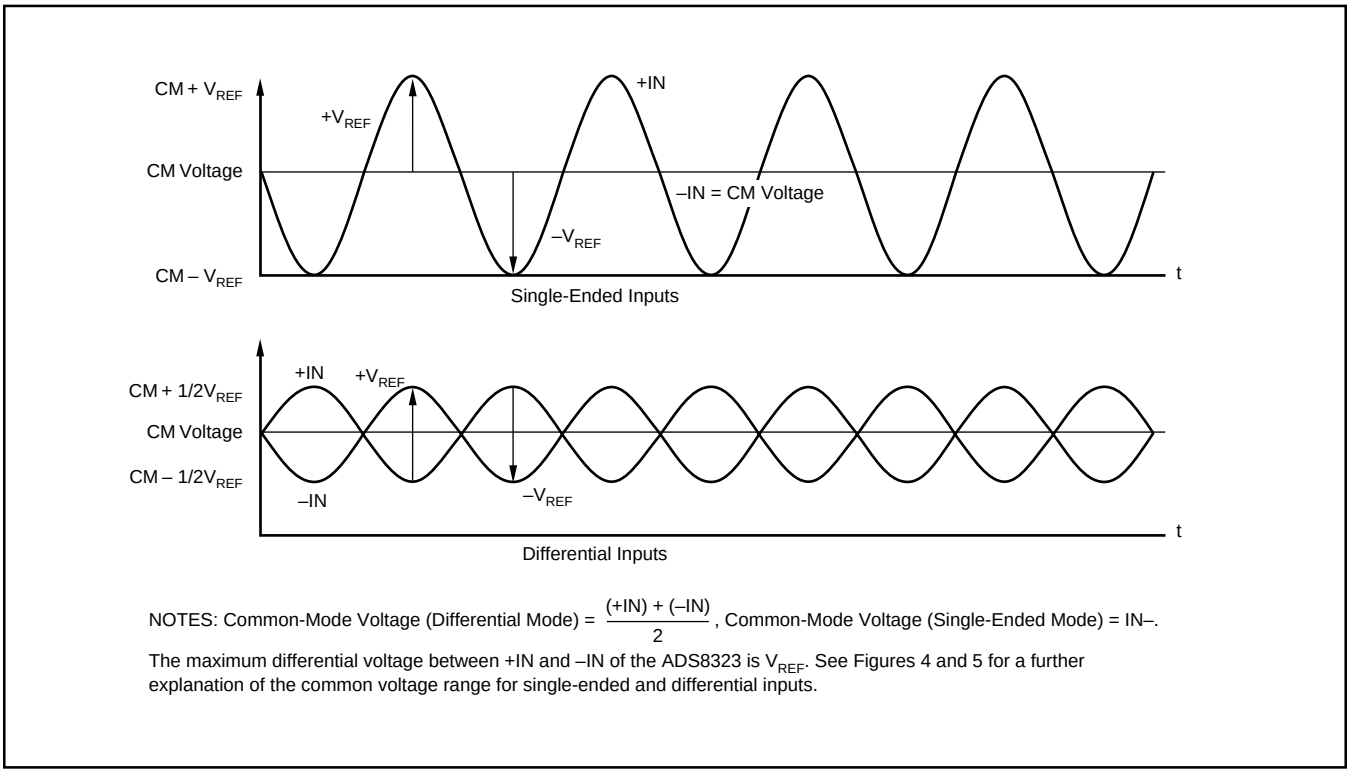
FIGURE 2. Methods of Driving the ADS8323 either Single-Ended or Differential.

When the input is differential, the amplitude of the input is the difference between the +IN and –IN input, or (+IN) – (–IN). The peak-to-peak amplitude of each input is $\pm 1/2V_{REF}$ around this common voltage. However, since the inputs are 180° out-of-phase, the peak-to-peak amplitude of the differential voltage is $+V_{REF}$ to $-V_{REF}$. The value of V_{REF} also determines the range of the voltage that may be common to both inputs (see Figure 5).

In each case, care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If matching is not observed, it may result in offset error, which changes with temperature. Often, a small capacitor (20pF) between the positive and negative inputs helps to match their impedance.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8323 charges the internal capacitor array during the sampling period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25pF) to a 16-bit settling level within 4 clock cycles (400ns), if the minimum acquisition time is used. When the converter goes into the hold mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. The +IN and –IN inputs should always remain within the range of AGND – 0.3V to AV_{DD} + 0.3V.



NOTES: Common-Mode Voltage (Differential Mode) = $\frac{(+IN) + (-IN)}{2}$, Common-Mode Voltage (Single-Ended Mode) = IN–.

The maximum differential voltage between +IN and –IN of the ADS8323 is V_{REF}. See Figures 4 and 5 for a further explanation of the common voltage range for single-ended and differential inputs.

FIGURE 3. Using the ADS8323 in the Single-Ended and Differential Input Modes.

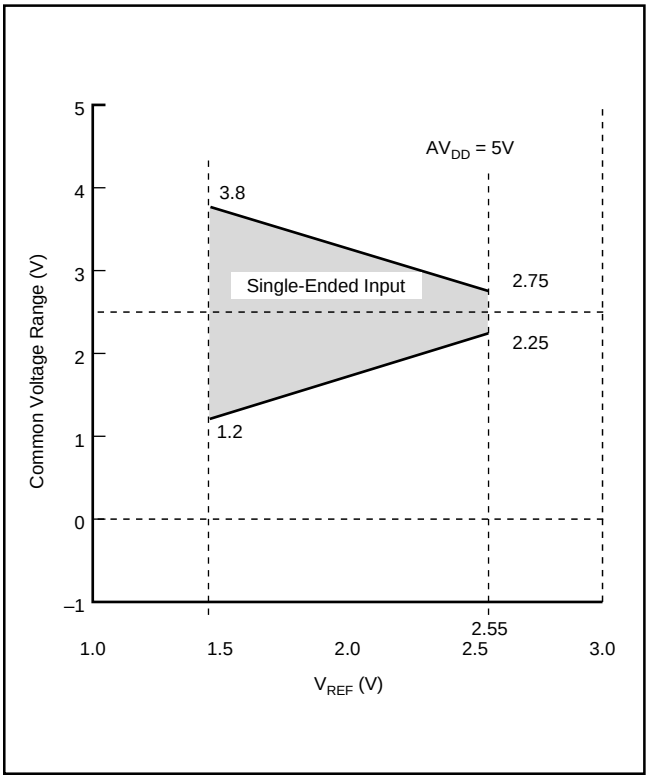


FIGURE 4. Single-Ended Input: Common-Mode Voltage Range vs V_{REF}.

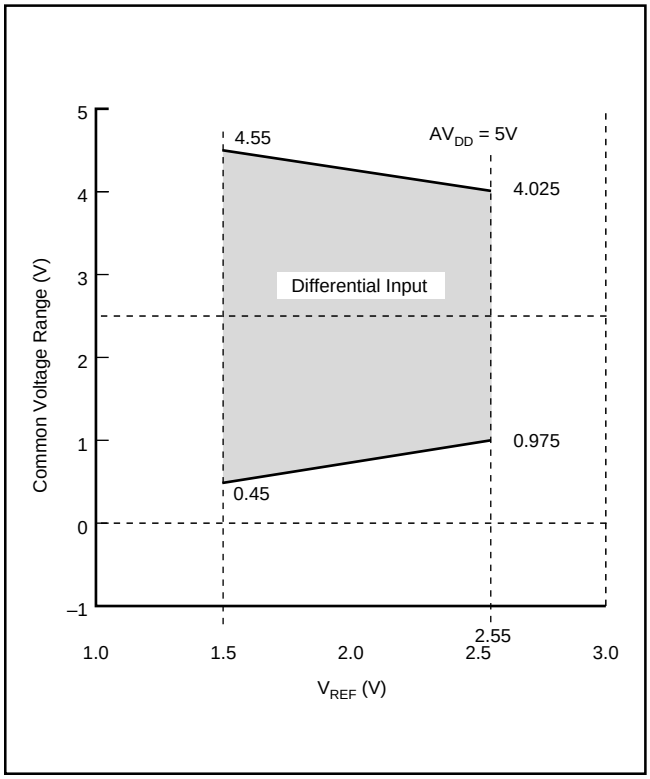


FIGURE 5. Differential Input: Common-Mode Voltage Range vs V_{REF}.

NOISE

Figure 6 shows the transition noise of the ADS8323. A low-level DC input was applied to the analog-input pins and the converter was put through 8192 conversions. The digital output of the ADC will vary in output code due to the internal noise of the ADS8323. This is true for all 16-bit SAR-type ADCs. The ADS8323, with five output codes for the σ distribution, will yield a < ±0.8LSB transition noise at 5V operation. Remember that to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be < 50µV.

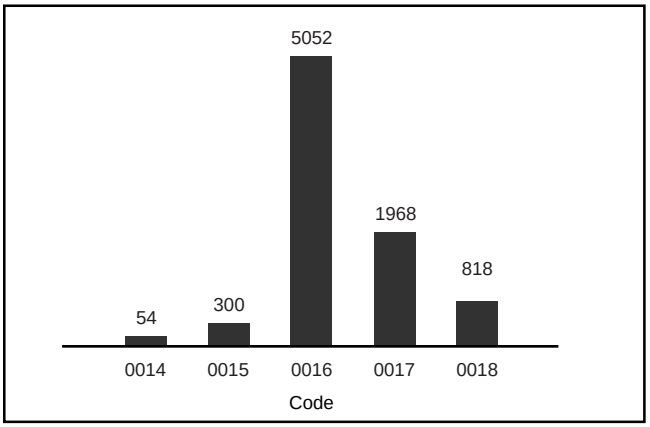


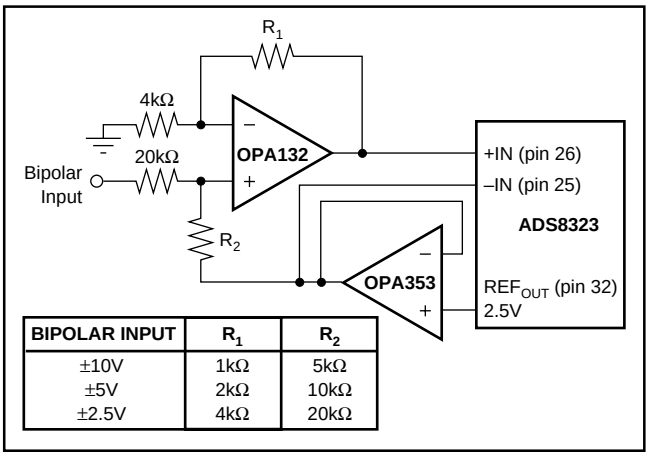
FIGURE 6. Histogram of 8192 Conversions of a Low-Level DC Input.

AVERAGING

Averaging the digital codes can compensate the noise of the ADC. By averaging conversion results, transition noise will be reduced by a factor of $1/\sqrt{n}$, where n is the number of averages. For example, averaging 4 conversion results will reduce the transition noise by 1/2 to ±0.4LSB. Averaging should only be used for input signals with frequencies near DC. For AC signals, a digital filter can be used to low-pass filter and decimate the output codes. This works in a similar manner to averaging—for every decimation by 2, the signal-to-noise ratio will improve 3dB.

BIPOLAR INPUTS

The differential inputs of the ADS8323 were designed to accept bipolar inputs ($-V_{REF}$ and $+V_{REF}$) around the common-mode voltage, which corresponds to a 0V to 5V input range with a 2.5V reference. By using a simple op amp circuit featuring four high-precision external resistors, the ADS8323 can be configured to accept bipolar inputs. The conventional ±2.5V, ±5V, and ±10V input ranges could be interfaced to the ADS8323 using the resistor values shown in Figure 7.



BIPOLAR INPUT	R_1	R_2
±10V	1kΩ	5kΩ
±5V	2kΩ	10kΩ
±2.5V	4kΩ	20kΩ

FIGURE 7. Level Shift Circuit for Bipolar Input Ranges.

DIGITAL INTERFACE

TIMING AND CONTROL

See the timing diagram in the Timing Characteristics section for detailed information on timing signals and their requirements.

The ADS8323 uses an external clock (CLOCK, pin 20) that controls the conversion rate of the CDAC. With a 10MHz external clock, the ADC sampling rate is 500kSPS that corresponds to a 2µs maximum throughput time.

EXPLANATION OF CLOCK, BUSY AND BYTE PINS

CLOCK—An external clock must be provided for the ADS8323. The maximum clock frequency is 10MHz and that provides 500kSPS throughput. The minimum clock frequency is 25kHz and that provides 1.25kHz throughput. The minimum clock cycle is 100ns (see Timing Diagram, t_{C1}), and CLOCK must remain HIGH (see Timing Diagram, t_{W1}) or LOW (see Timing Diagram, t_{W2}) for at least 40ns.

BUSY—Initially BUSY output is LOW. Reading data from output register or sampling the input analog signal will not affect the state of the BUSY signal. After the $\overline{\text{CONVST}}$ input goes LOW and conversion starts, a maximum of 25ns later the BUSY output will go HIGH. That signal will stay HIGH during conversion and will provide the status of the internal ADC to the DSP or uC. At the end of conversion, on the rising edge of 17th clock cycle, new data from the internal ADC is latched into the output registers. The BUSY signal will go LOW a maximum of 25ns later (see Timing Diagram, t_{D4}).

BYTE—The output data will appear as a full 16-bit word on DB15-DB0 (MSB-LSB or D15-D0) if BYTE is LOW. If there is only an 8-bit bus available on a board, the result may also be read on an 8-bit bus by using only DB7-DB0. In this case, two reads are necessary (see Timing Diagram). The first, as before, leaving BYTE LOW and reading the 8 least significant bits on DB7-DB0, then bringing BYTE HIGH. When BYTE is HIGH, the upper 8 bits (D15-D8) will appear on DB7-DB0.

START OF A CONVERSION AND READING DATA

By bringing the $\overline{\text{CONVST}}$ signal LOW, the input data is immediately placed in the hold mode (10ns). Although $\overline{\text{CS}}$ must be LOW when $\overline{\text{CONVST}}$ goes LOW to initiate a conversion. The conversion follows with the next rising edge of CLOCK. If it is important to detect a hold command during a certain clock cycle, then the falling edge of the $\overline{\text{CONVST}}$ signal must occur at least 10ns before the rising edge of CLOCK (see Timing Diagram, t_{D1}). The $\overline{\text{CONVST}}$ signal can remain LOW without initiating a new conversion. The $\overline{\text{CONVST}}$ signal must be HIGH for at least 20ns (see Timing Diagram, t_{W4}) before it is brought LOW again and $\overline{\text{CONVST}}$ must stay LOW for at least 20ns (see Timing Diagram, t_{W3}). Once a $\overline{\text{CONVST}}$ signal goes LOW, further impulses of this signal are ignored until the conversion is finished or the part is reset.

When the conversion is finished (after 16 clock cycles) the sampling switches will close and sample the new value. The start of the next conversion must be delayed to allow the input capacitor of the ADS8323 to be fully charged. This delay time depends on the driving amplifier, but should be at least 400ns. To gain acquisition time, the falling edge of $\overline{\text{CONVST}}$ must take place just before the rising edge of CLOCK (see Timing Diagram, t_{D1}). One conversion cycle requires 20 clock cycles. However, reading data during the conversion or on a falling hold edge might cause a loss in performance.

Reading Data ($\overline{\text{RD}}$, $\overline{\text{CS}}$)—In general, the data outputs are in tri-state. Both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ must be LOW to enable these outputs. $\overline{\text{RD}}$ and $\overline{\text{CS}}$ must stay LOW together for at least 40ns (see Timing Diagram, t_{D7}) before the output data is valid. $\overline{\text{RD}}$ must remain HIGH for at least 20ns (see Timing Diagram, t_{W7}) before bringing it back LOW for a subsequent read command. 16 clock-cycles after the start of a conversion (next rising edge of clock after the falling edge of $\overline{\text{CONVST}}$), the new data is latched into the output register and the reading process can start again.

$\overline{\text{CS}}$ being LOW tells the ADS8323 that the bus on the board is assigned to the ADS8323. If an ADC shares a bus with digital gates, there is a possibility that digital (high-frequency) noise gets coupled into the ADC. If the bus is just used by the ADS8323, $\overline{\text{CS}}$ can be hard-wired to ground. The output data should not be read 125ns prior to the falling edge of $\overline{\text{CONVST}}$ and 10ns after the falling edge.

The ADS8323's output is in Binary Two's Complement format (see Figure 8).

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
		BINARY CODE	HEX CODE
Full-Scale Range	$2 \cdot V_{REF}$		
Least Significant Bit (LSB)	$2 \cdot V_{REF}/65535$		
+Full Scale	$+V_{REF} - 1$ LSB	0111 1111 1111 1111	7FFF
Midscale	0V	0000 0000 0000 0000	0000
Midscale – 1LSB	0V – 1 LSB	1111 1111 1111 1111	FFFF
Zero	$-V_{REF}$	1000 0000 0000 0000	8000

TABLE I. Ideal Input Voltages and Output Codes.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8323 circuitry. This is particularly true if the CLOCK input is approaching the maximum throughput rate.

As the ADS8323 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high-power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. Their error can change if the external event changes in time with respect to the CLOCK input.

On average, the ADS8323 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1µF bypass capacitor is recommended from pin 31 directly to ground.

The AGND and DGND pins should be connected to a clean ground point. In all cases, this should be the "analog" ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power-supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

As with the GND connections, V_{DD} should be connected to a +5V power supply plane, or trace, that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8323 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor, or even a Pi filter made up of inductors and capacitors all designed to essentially low-pass filter the +5V supply, removing the high-frequency noise.

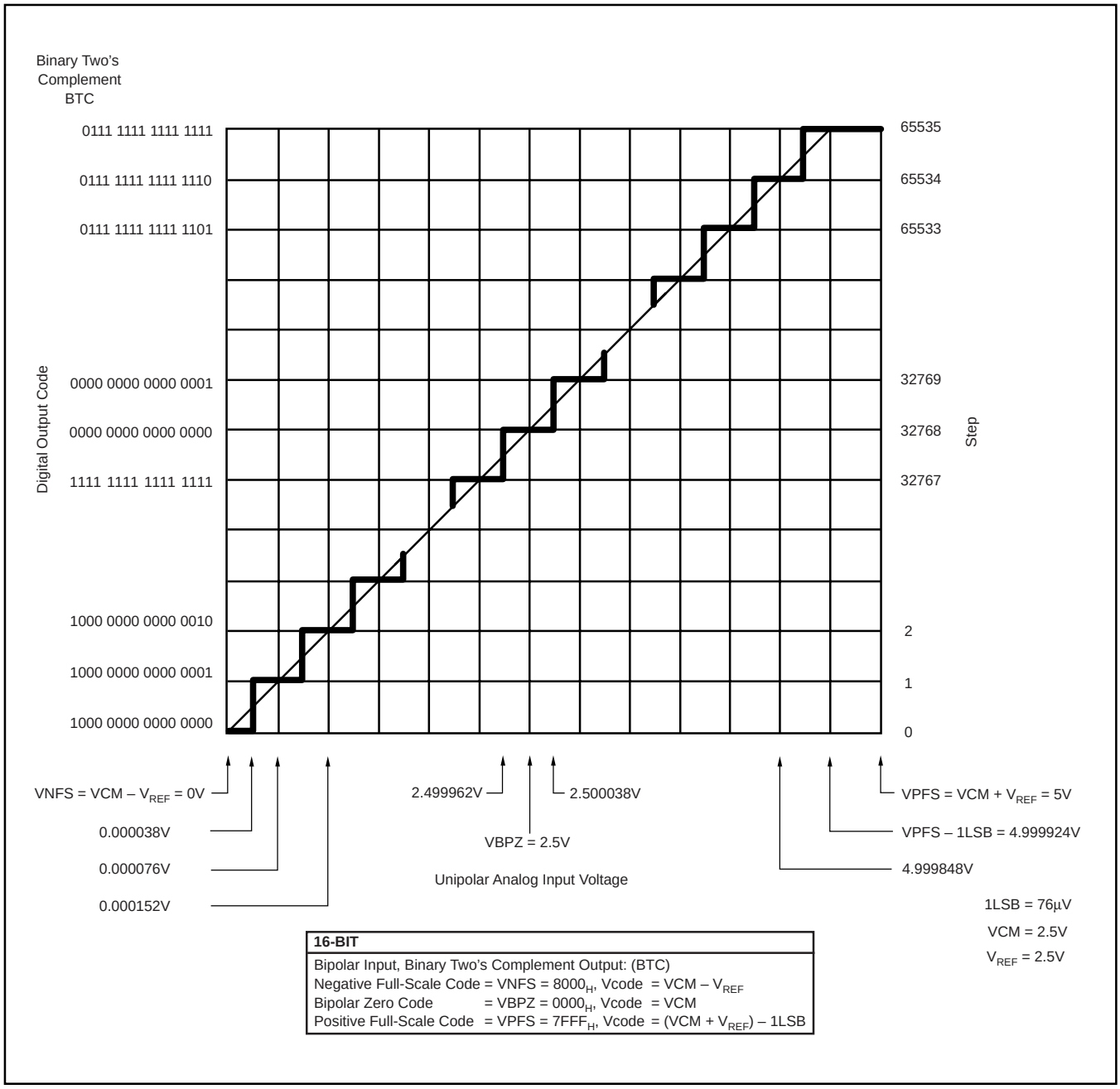
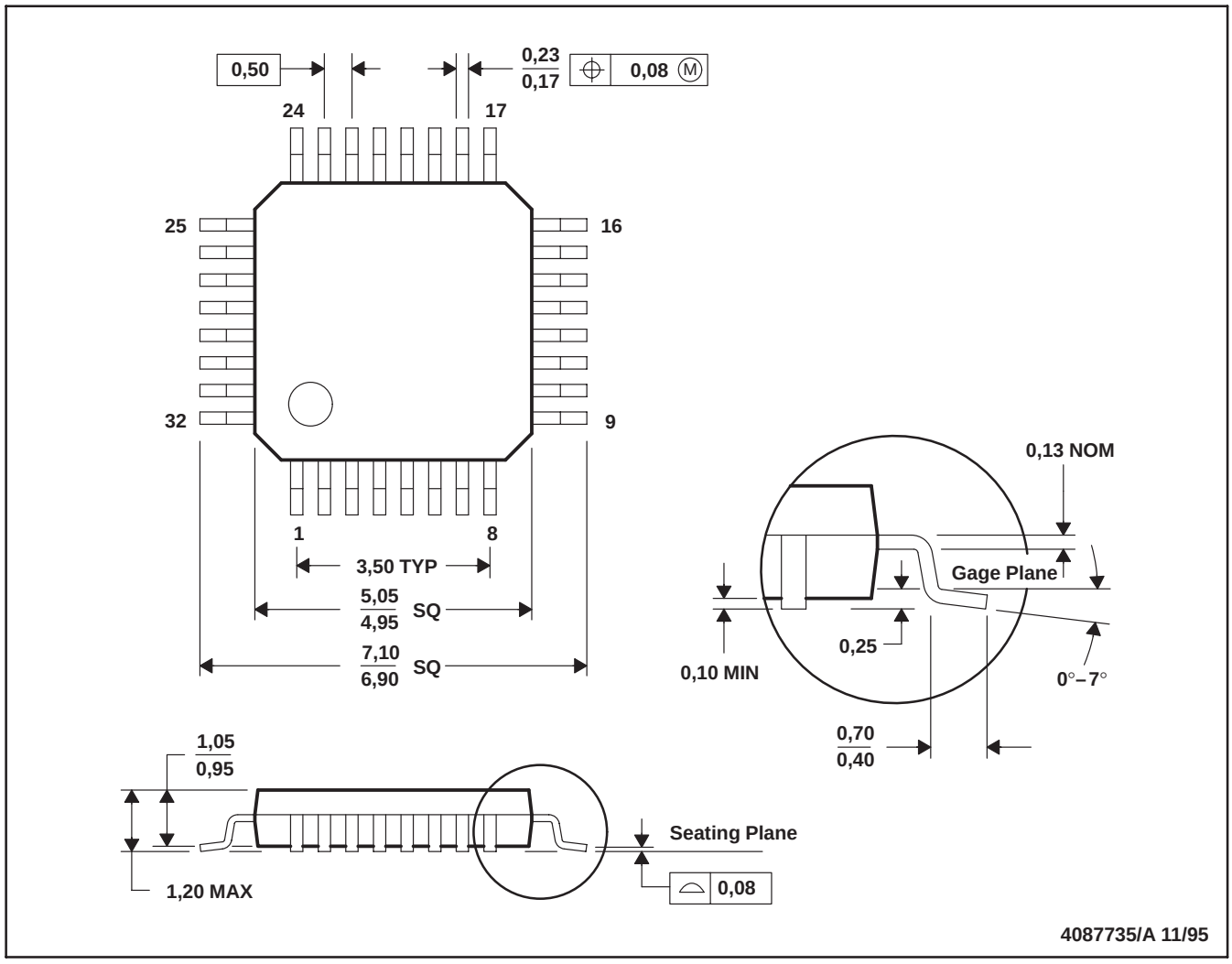


FIGURE 8. Ideal Conversion Characteristics (Condition: Single-Ended. VCM = IN– = 2.5V, V_{REF} = 2.5V).

PBS (S-PQFP-G32) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PACKAGE OPTION ADDENDUM

9-Dec-2004

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS8323Y/250	ACTIVE	TQFP	PBS	32	250	None	CU SNPB	Level-3-220C-168 HR
ADS8323Y/2K	ACTIVE	TQFP	PBS	32	2000	None	CU SNPB	Level-3-220C-168 HR
ADS8323YB/250	ACTIVE	TQFP	PBS	32	250	None	CU SNPB	Level-3-220C-168 HR
ADS8323YB/2K	ACTIVE	TQFP	PBS	32	2000	None	CU SNPB	Level-3-220C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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