24C04A

4K 5.0V I²C™ Serial EEPROM

FEATURES

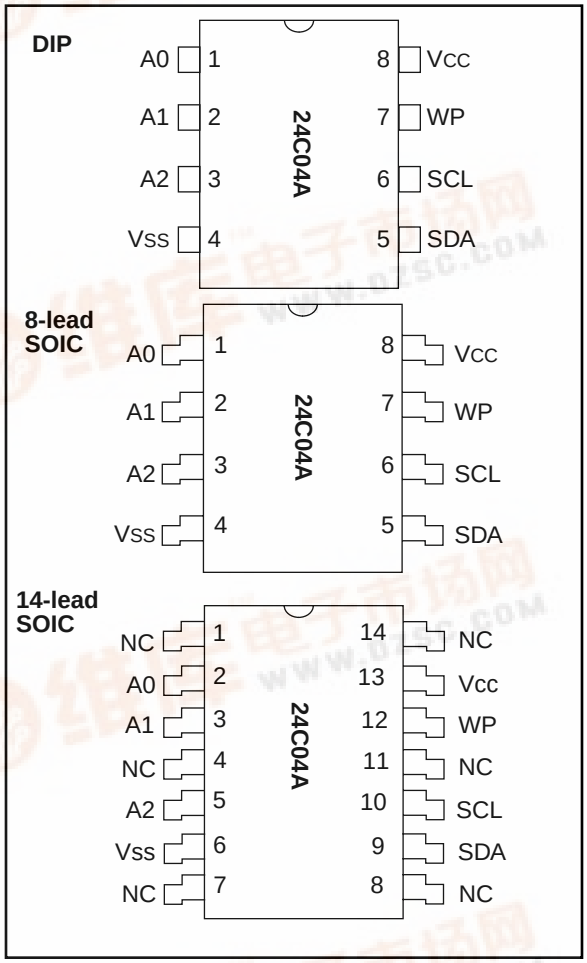
- Low power CMOS technology
- Hardware write protect
- Two wire serial interface bus, I²C™ compatible
- 5.0V only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer
- 1 ms write cycle time for single byte
- 1,000,000 Erase/Write cycles guaranteed
- Data retention >200 years
- 8-pin DIP/SOIC packages
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

DESCRIPTION

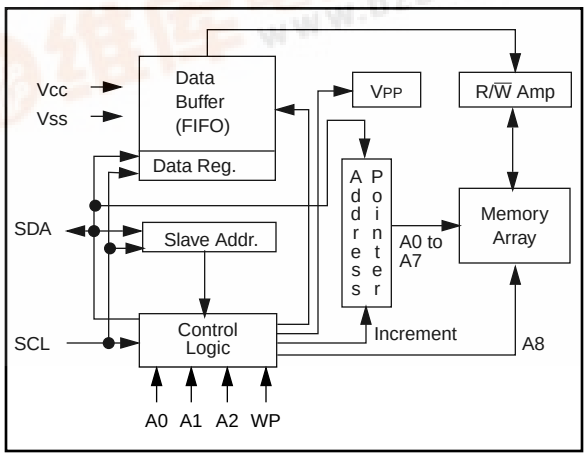
The Microchip Technology Inc. 24C04A is a 4K bit Electrically Erasable PROM. The device is organized as with a standard two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature provides hardware write protection for the upper half of the block. The 24C04A has a page write capability of up to eight bytes, and up to four 24C04A devices may be connected to the same two wire bus.

This device offers fast (1ms) byte write and extended (-40°C to 125°C) temperature operation. It is recommended that all other applications use Microchip's 24LC04B.

PACKAGE TYPES



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC}.....7.0V
All inputs and outputs w.r.t. V_{SS} ..... -0.6V to V_{CC} +1.0V
Storage temperature ..... -65˚C to +150˚C
Ambient temp. with power applied..... -65˚C to +125˚C
Soldering temperature of leads (10 seconds) ..... +300˚C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0	No Function - Must be connected to V_{CC} or V_{SS}
A1, A2	Chip Address Inputs
V_{SS}	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
V_{CC}	+5V Power Supply

TABLE 1-2: DC CHARACTERISTICS

V_{CC} = +5V (±10%)		Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to +125°C			
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
V_{CC} detector threshold	V_{TH}	2.8	4.5	V	
SCL and SDA pins: High level input voltage Low level input voltage Low level output voltage	 V_{IH} V_{IL} V_{OL}	 V_{CC} x 0.7 -0.3	 V_{CC} + 1 V_{CC} x 0.3 0.4	 V V V	 I_{OL} = 3.2 mA (SDA only)
A1 & A2 pins: High level input voltage Low level input voltage	 V_{IH} V_{IL}	 V_{CC} - 0.5 -0.3	 V_{CC} + 0.5 0.5	 V V	
Input leakage current	I_{LI}	—	10	µA	V_{IN} = 0V to V_{CC}
Output leakage current	I_{LO}	—	10	µA	V_{OUT} = 0V to V_{CC}
Pin capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	7.0	pF	V_{IN}/V_{OUT} = 0V (Note) Tamb = +25˚C, f = 1 MHz
Operating current	I_{CC} Write I_{CC} Write I_{CC} Read	— — —	3.5 4.25 750	mA mA µA	F_{CLK} = 100 kHz, program cycle time = 1 ms, Vcc = 5V, Tamb = 0˚C to +70˚C F_{CLK} = 100 kHz, program cycle time = 1 ms, Vcc = 5V, Tamb = (I) and (E) V_{CC} = 5V, Tamb= (C), (I) and (E)
Standby current	I_{CCS}	—	100	µA	SDA=SCL=V_{CC}=5V (no PROGRAM active) WP/TEST = V_{SS}, A0, A1, A2 = V_{SS}

Note: This parameter is periodically sampled and not 100% tested

FIGURE 1-1: BUS TIMING START/STOP

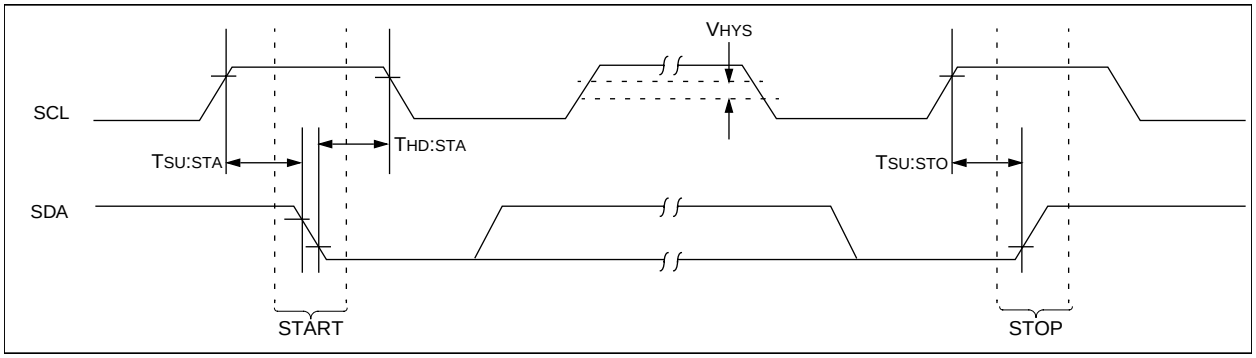


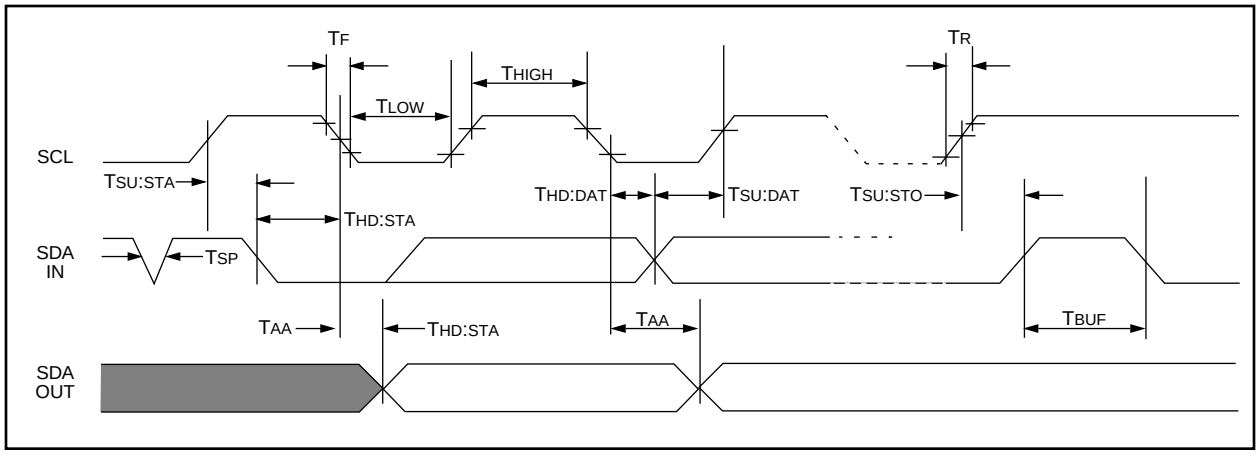
TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min.	Typ	Max.	Units	Remarks
Clock frequency	FCLK	—	—	100	kHz	
Clock high time	THIGH	4000	—	—	ns	
Clock low time	TLOW	4700	—	—	ns	
SDA and SCL rise time	TR	—	—	1000	ns	
SDA and SCL fall time	TF	—	—	300	ns	
START condition hold time	THD:STA	4000	—	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	—	ns	
Data input setup time	TSU:DAT	250	—	—	ns	
Data output delay time	TAA	300	—	3500		(Note 1)
STOP condition setup time	TSU:STO	4700	—	—	ns	
Bus free time	TBUF	4700	—	—	ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI	—	—	100	ns	
Program cycle time	TWC	—	.4 .4N	1 N	ms ms	Byte mode Page mode, N=# of bytes
Endurance	—	1M	—	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 2)

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24C04A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C04A works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to four 24C04As can be connected to the bus, selected by A1 and A2 chip address inputs. A0 must be tied to VCC or VSS.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

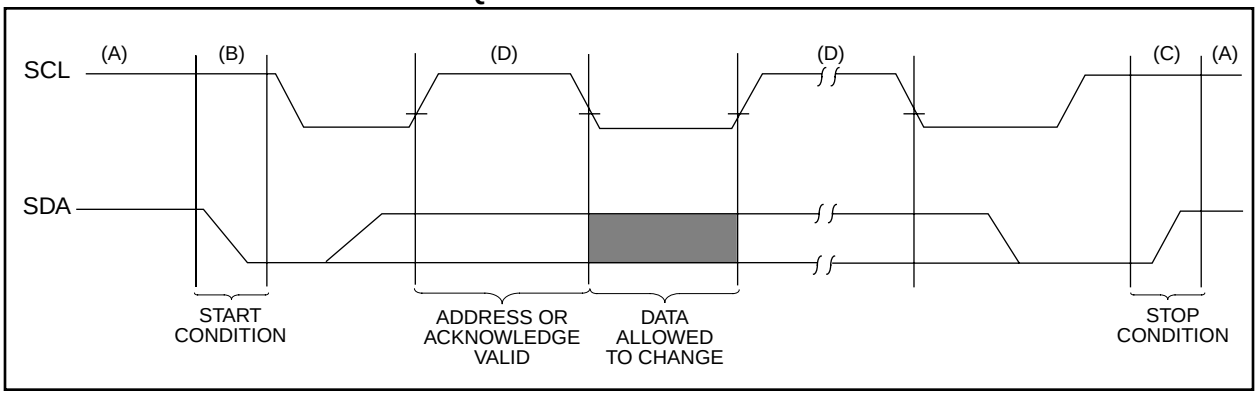
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24C04A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



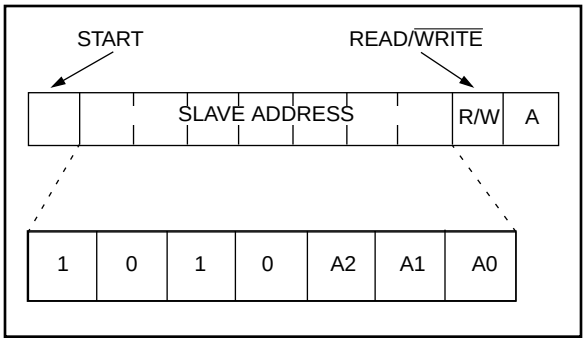
4.0 SLAVE ADDRESS

The chip address inputs A1 and A2 must be externally connected to either VCC or ground (VSS), thereby assigning a unique address to each device. A0 is not used on the 24C04A and must be connected to either VCC or VSS. Up to four 24C04A devices may be connected to the bus. Chip selection is then accomplished through software by setting the bits A1 and A2 of the slave address to the corresponding hard-wired logic levels of the selected 24C04A. After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010), followed by the chip address bits A0, A1 and A2. The seventh bit of that byte (A0) is used to select the upper block (addresses 100—1FF) or the lower block (addresses 000—0FF) of the array.

The eighth bit of the slave address determines if the master device wants to read or write to the 24C04A (Figure 4-1).

The 24C04A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 4-1: SLAVE ADDRESS ALLOCATION



5.0 BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 24C04A.

Following the START signal from the master, the device code (4-bits), the slave address (3-bits), and the R/$\overline{W}$ bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C04A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C04A. After receiving the acknowledge, the master device transmits the data word to be written into the addressed memory location. The 24C04A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle (Figure 6-1).

6.0 PAGE PROGRAM MODE

To program the master sends addresses and data to the 24C04A which is the slave (Figure 6-1 and Figure 6-2). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/$\overline{W}$ bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C04A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (The A0 bit transmitted with the slave address is the ninth bit of the address pointer). The 24C04A will generate an acknowledge after every 8-bits received and store them consecutively in a RAM (8 bytes maximum) buffer until a STOP condition is detected. This STOP condition initiates the internal programming cycle.. If more than 8 bytes are transmitted by the master, the 24C04A will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address registers bottom 3 bits to increment while the upper 5 bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 6-1), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received data bytes in the page buffer will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes.

FIGURE 6-1: BYTE WRITE

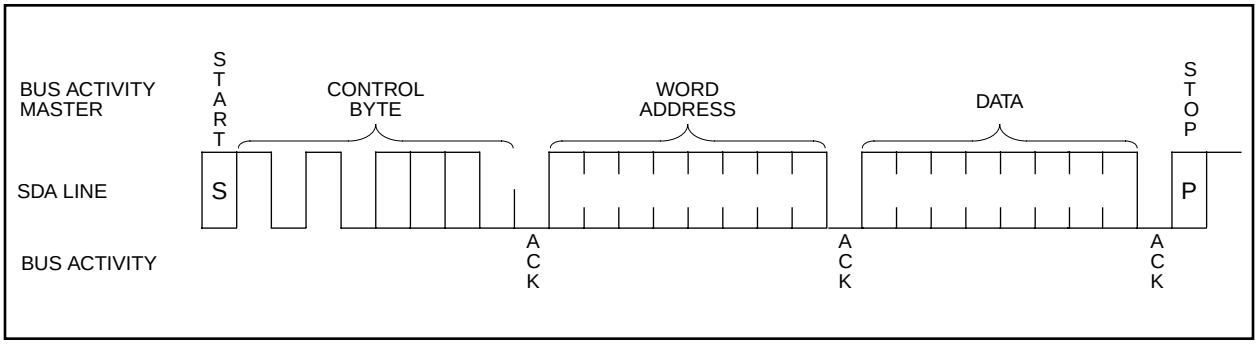
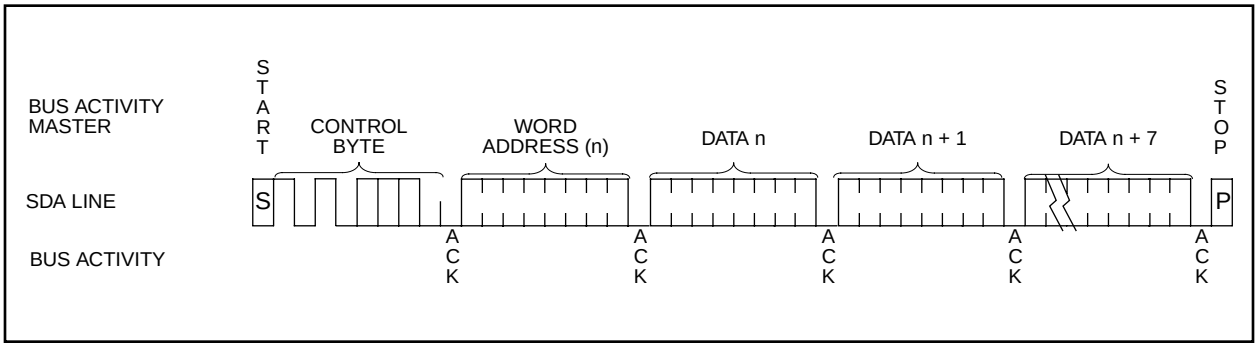


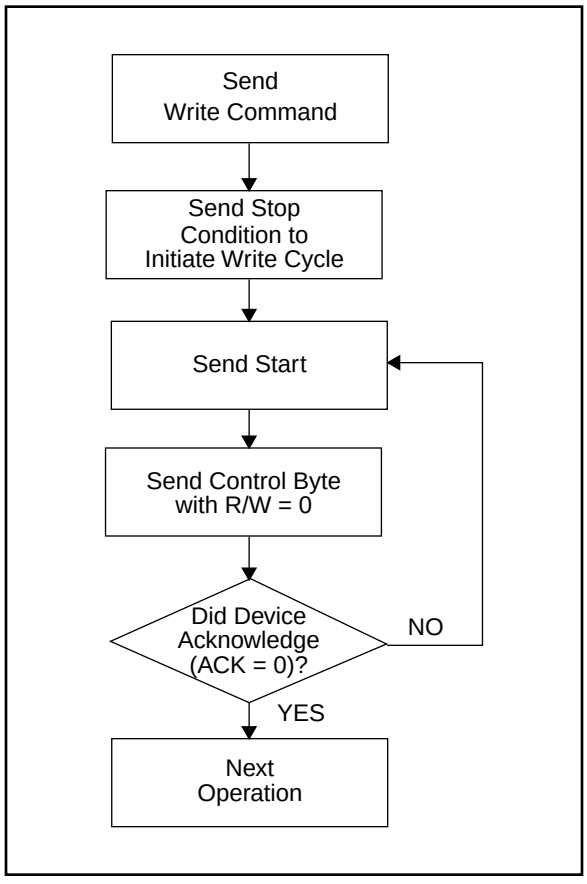
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin is connected to VCC (+5.0V). The device will accept slave and word addresses but if the memory accessed is write protected by the WP pin, the 24C04A will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the STOP condition is asserted.

9.0 READ MODE

In this mode the 24C04A transmits data to the master devide.

As can be seen from Figure 9-2 and Figure 9-3, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to). During this period the 24C04A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This auto-increment sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note 1: If the master knows where the address pointer is, it can begin the read sequence at the current address (Figure 9-1) and save time transmitting the slave and word addresses.

Note 2: In all modes, the address pointer will not increment through a block (256 byte) boundary, but will rotate back to the first location in that block.

FIGURE 9-1: CURRENT ADDRESS READ

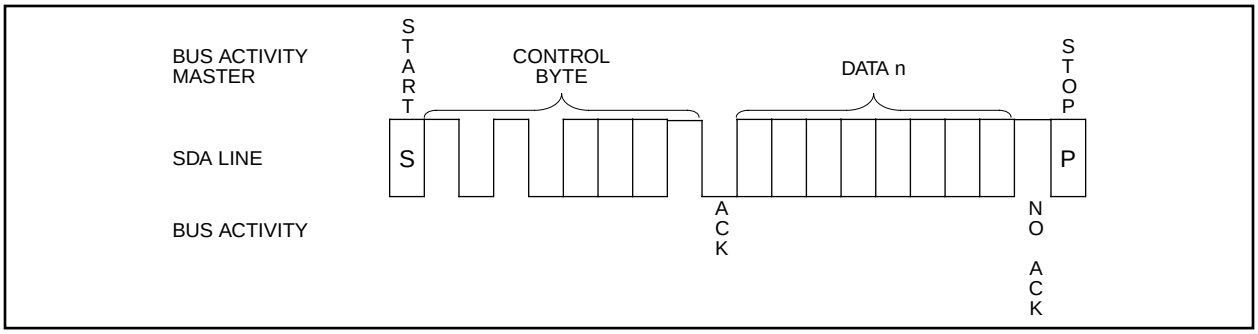


FIGURE 9-2: RANDOM READ

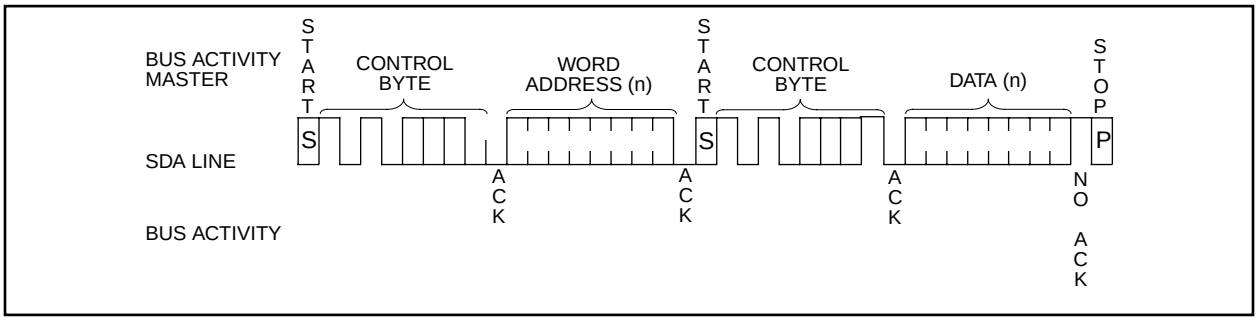
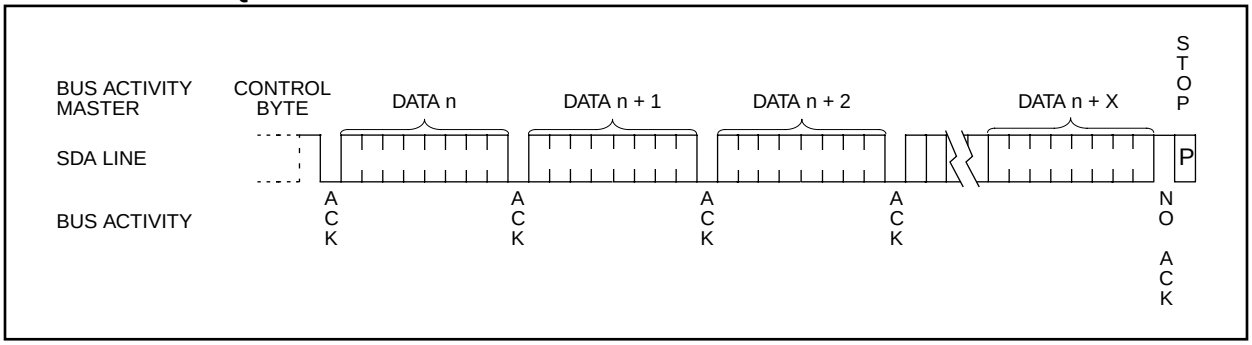


FIGURE 9-3: SEQUENTIAL READ



10.0 PIN DESCRIPTION

10.1 A0, A1, A2 Chip Address Inputs

A0 is not used as a chip select bit and must be tied to either Vss or Vcc. The levels on the remaining two address inputs(A1, A2) are compared with the corresponding bits in the slave address. The chip is selected if the compare is true. These inputs must be connected to either VSS or VCC.

These two address inputs allow up to four 24C04A's can be connected to the bus

10.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to VCC (typical 10KΩ).

For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

10.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

10.4 WP Write Protection

This pin must be connected to either VCC or VSS. If tied to VCC, write operations to the upper memory block will not be executed. Read operations are possible.

If tied to VSS, normal memory operation is enabled (read/write the entire memory).

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Note 1: A “page” is defined as the maximum number of bytes that can be programmed in a single write cycle. The 24C04A page is 8 bytes long.

Note 2: A “block” is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 24C04A has two blocks, 256 bytes each.

NOTES:

24C04A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24C04A - /P

Package:	P	= Plastic DIP
	SN	= Plastic SOIC (150 mil Body), 8-lead
	SM	= Plastic SOIC (207 mil Body), 8-lead
	SL	= Plastic SOIC (150 mil Body), 14-lead
Temperature Range:	Blank	= 0°C to +70°C
		= -40°C to +85°C
	E	= -40°C to +125°C
Device:	24C04A	4K I^2C Serial EEPROM
	24C04AT	4K I^2C Serial EEPROM (Tape and Reel)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

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