# TLV5626

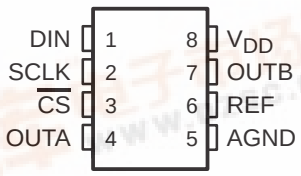
## 2.7 V TO 5.5 V LOW POWER DUAL 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

SLAS236 –JUNE 1999

### features

- Dual 8-Bit Voltage Output DAC
- Programmable Internal Reference
- Programmable Settling Time:
  0.8 μs in Fast Mode ,
  2.8 μs in Slow Mode
- Compatible With TMS320 and SPI™ Serial Ports
- Differential Nonlinearity <0.1 LSB Typ
- Monotonic Over Temperature

D PACKAGE
(TOP VIEW)




### applications

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

### description

The TLV5626 is a dual 8-bit voltage output DAC with a flexible 3-wire serial interface.The serial interface allows glueless interface to TMS320 and SPI™, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing 2 control and 8 data bits.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class AB output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows the designer to optimize speed versus power dissipation. With its on-chip programmable precision voltage reference, the TLV5626 simplifies overall system design.

Because of its ability to source up to 1 mA, the reference can also be used as a system reference. Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in an 8-pin SOIC package to reduce board space in standard commercial and industrial temperature ranges.

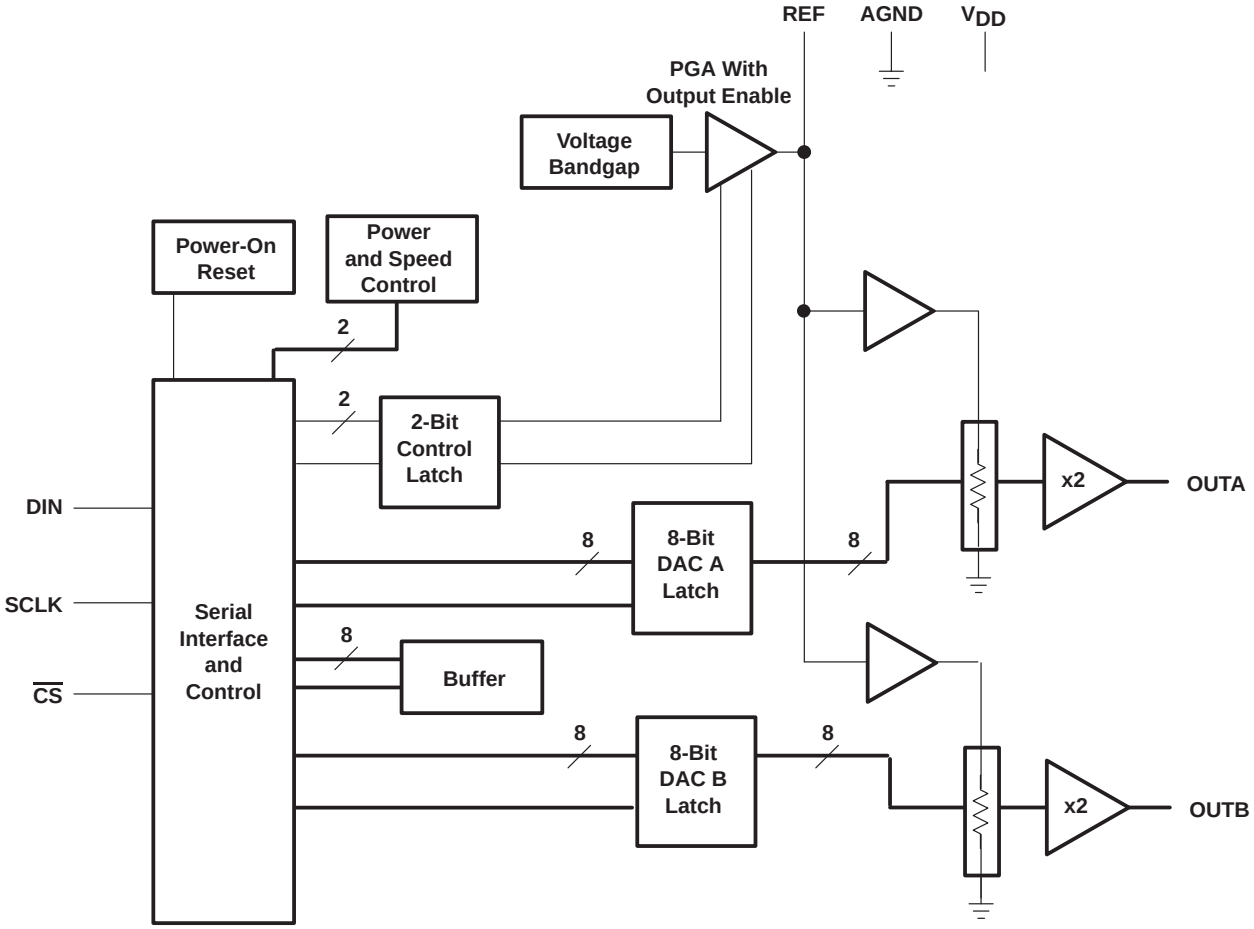
**AVAILABLE OPTIONS**

| $T_A$ | PACKAGE |
|---|---|
| | SOIC (D) |
| 0°C to 70°C | TLV5626CD |
| –40°C to 85°C | TLV5626ID |



SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corporation.

## functional block diagram




## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O/P | DESCRIPTION |
|---|---|---|---|
| AGND | 5 | P | Ground |
| $\overline{CS}$ | 3 | I | Chip select. Digital input active low, used to enable/disable inputs |
| DIN | 1 | I | Digital serial data input |
| OUTA | 4 | I | DAC A analog voltage output |
| OUTB | 7 | O | DAC B analog voltage output |
| REF | 6 | I/O | Analog reference voltage input/output |
| SCLK | 2 | I | Digital serial clock input |
| $V_{DD}$ | 8 | P | Positive power supply |

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage ($V_{DD}$ to AGND) . . . . . 7 V
Reference input voltage range . . . . . – 0.3 V to $V_{DD}$ + 0.3 V
Digital input voltage range . . . . . – 0.3 V to $V_{DD}$ + 0.3 V
Operating free-air temperature range, $T_A$: TLV5626C . . . . . 0°C to 70°C
TLV5626I . . . . . –40°C to 85°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | $V_{DD}$ = 5 V | 4.5 | 5 | 5.5 | V |
| | $V_{DD}$ = 3 V | 2.7 | 3 | 3.3 | V |
| Power on threshold voltage, POR | | 0.55 | | 2 | V |
| High-level digital input voltage, $V_{IH}$ | $V_{DD}$ = 2.7 V to 5.5 V | 2 | | | V |
| Low-level digital input voltage, $V_{IL}$ | $V_{DD}$ = 2.7 V to 5.5 V | | | 0.8 | V |
| Reference voltage, $V_{ref}$ to REF terminal | $V_{DD}$ = 5 V (see Note 1) | AGND | 2.048 | $V_{DD}$–1.5 | V |
| Reference voltage, $V_{ref}$ to REF terminal | $V_{DD}$ = 3 V (see Note 1) | AGND | 1.024 | $V_{DD}$–1.5 | V |
| Load resistance, $R_L$ | | 2 | | | kΩ |
| Load capacitance, $C_L$ | | | | 100 | pF |
| Clock frequency, $f_{CLK}$ | | | | 20 | MHz |
| Operating free-air temperature, $T_A$ | TLV5626C | 0 | | 70 | °C |
| | TLV5626I | –40 | | 85 | |

NOTE 1: Due to the x2 output buffer, a reference input voltage ≥ ($V_{DD}$ – 0.4 V)/2 causes clipping of the transfer function. The output buffer of the internal reference must be disabled, if an external reference is used.

## electrical characteristics over recommended operating conditions (unless otherwise noted)

### power supply

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Power supply current | No load, All inputs = AGND or $V_{DD}$, DAC latch = 0x800 | $V_{DD}$ = 5 V, Int. ref. | Fast | | 4.2 | 5 | mA |
| | | | | Slow | | 2 | 2.5 | mA |
| | | | $V_{DD}$ = 3 V, Int. ref. | Fast | | 3.7 | 4.6 | mA |
| | | | | Slow | | 1.7 | 2.2 | mA |
| | | | $V_{DD}$ = 5 V, Ext. ref. | Fast | | 3.8 | 4.6 | mA |
| | | | | Slow | | 1.7 | 2.1 | mA |
| | | | $V_{DD}$ = 3 V, Ext. ref. | Fast | | 3.4 | 4.2 | mA |
| | | | | Slow | | 1.4 | 1.8 | mA |
| | Power-down supply current | | | | | 1 | | µA |
| PSRR | Power supply rejection ratio | Zero scale, See Note 2 | | | | –65 | | dB |
| | | Full scale, See Note 3 | | | | –65 | | |

NOTES: 2. Power supply rejection ratio at zero scale is measured by varying $V_{DD}$ and is given by:
$PSRR = 20 \log [(E_{ZS}(V_{DD}max) – E_{ZS}(V_{DD}min))/V_{DD}max]$
3. Power supply rejection ratio at full scale is measured by varying $V_{DD}$ and is given by:
$PSRR = 20 \log [(E_G(V_{DD}max) – E_G(V_{DD}min))/V_{DD}max]$

### static DAC specifications

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Resolution | | 8 | | | bits |
| INL | Integral nonlinearity, end point adjusted | See Note 4 | | ±0.4 | ±1 | LSB |
| DNL | Differential nonlinearity | See Note 5 | | ±0.1 | ±0.5 | LSB |
| $E_{ZS}$ | Zero-scale error (offset error at zero scale) | See Note 6 | | | ±24 | mV |
| $E_{ZS}$ TC | Zero-scale-error temperature coefficient | See Note 7 | | 10 | | ppm/°C |
| $E_G$ | Gain error | See Note 8 | | | ±0.6 | % full scale V |
| $E_G$ $T_C$ | Gain error temperature coefficient | See Note 9 | | 10 | | ppm/°C |

NOTES: 4. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
5. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
7. Zero-scale-error temperature coefficient is given by: $E_{ZS}$ TC = $[E_{ZS}(T_{max}) – E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} – T_{min})$.
8. Gain error is the deviation from the ideal output ($2V_{ref}$ – 1 LSB) with an output load of 10 k excluding the effects of the zero-error.
9. Gain temperature coefficient is given by: $E_G$ TC = $[E_G(T_{max}) – E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} – T_{min})$.

### output specifications

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_O$ | Output voltage | $R_L$ = 10 kΩ | 0 | | $V_{DD}$–0.4 | V |
| | Output load regulation accuracy | $V_O$ = 4.096 V, 2.048 V, $R_L$ = 2 kΩ vs 10 k© | | | ±0.25 | % full scale V |

## electrical characteristics over recommended operating conditions (unless otherwise noted) (Continued)

### reference pin configured as output (REF)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{ref(OUTL)}$ | Low reference voltage | | 1.003 | 1.024 | 1.045 | V |
| $V_{ref(OUTH)}$ | High reference voltage | $V_{DD}$ > 4.75 V | 2.027 | 2.048 | 2.069 | V |
| $I_{ref(source)}$ | Output source current | | | | 1 | mA |
| $I_{ref(sink)}$ | Output sink current | | –1 | | | mA |
| | Load capacitance | | | | 100 | pF |
| PSRR | Power supply rejection ratio | | | –65 | | dB |

### reference pin configured as input (REF)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_I$ | Input voltage | | | 0 | | $V_{DD}$–1.5 | V |
| $R_I$ | Input resistance | | | | 10 | | MΩ |
| $C_I$ | Input capacitance | | | | 5 | | pF |
| | Reference input bandwidth | REF = 0.2 $V_{pp}$ + 1.024 V dc | Fast | | 1.3 | | MHz |
| | | | Slow | | 525 | | kHz |
| | Reference feedthrough | REF = 1 $V_{pp}$ at 1 kHz + 1.024 V dc (see Note 10) | | | –80 | | dB |

NOTE 10: Reference feedthrough is measured at the DAC output with an input code = 0x000.

### digital inputs

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{IH}$ | High-level digital input current | $V_I = V_{DD}$ | | | 1 | µA |
| $I_{IL}$ | Low-level digital input current | $V_I$ = 0 V | –1 | | | µA |
| $C_i$ | Input capacitance | | | 8 | | pF |

### analog output dynamic performance

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{s(FS)}$ | Output settling time, full scale | $R_L$ = 10 kΩ, $C_L$ = 100 pF, See Note 11 | Fast | | 0.8 | 2.4 | µs |
| | | | Slow | | 2.8 | 5.5 | |
| $t_{s(CC)}$ | Output settling time, code to code | $R_L$ = 10 kΩ, $C_L$ = 100 pF, See Note 12 | Fast | | 0.4 | 1.2 | µs |
| | | | Slow | | 0.8 | 1.6 | |
| SR | Slew rate | $R_L$ = 10 kΩ, $C_L$ = 100 pF, See Note 13 | Fast | | 12 | | V/µs |
| | | | Slow | | 1.8 | | |
| | Glitch energy | $\overline{DIN}$ = 0 to 1, $\overline{CS}$ = $V_{DD}$ $f_{CLK}$ = 100 kHz, | | | 5 | | nV–S |
| SNR | Signal-to-noise ratio | $f_S$ = 480 kSPS, $f_{out}$ = 1 kHz, $R_L$ = 10 kΩ, $C_L$ = 100 pF | | 53 | 57 | | dB |
| S/(N+D) | Signal-to-noise + distortion | | | 48 | 47 | | |
| THD | Total harmonic distortion | | | | –50 | –48 | |
| SFDR | Spurious free dynamic range | | | 50 | 62 | | |

NOTES: 11. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0xFD0 or 0xFD0 to 0x020 respectively. Not tested, assured by design.
12. Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count. Not tested, assured by design.
13. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

### digital input timing requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{su(CS–CK)}$ | Setup time, $\overline{CS}$ low before first negative SCLK edge | 10 | | | ns |
| $t_{su(C16-CS)}$ | Setup time, 16$^{th}$ negative SCLK edge (when D0 is sampled) before $\overline{CS}$ rising edge | 10 | | | ns |
| $t_{wH}$ | SCLK pulse width high | 25 | | | ns |
| $t_{wL}$ | SCLK pulse width low | 25 | | | ns |
| $t_{su(D)}$ | Setup time, data ready before SCLK falling edge | 10 | | | ns |
| $t_{h(D)}$ | Hold time, data held valid after SCLK falling edge | 5 | | | ns |

## PARAMETER MEASUREMENT INFORMATION

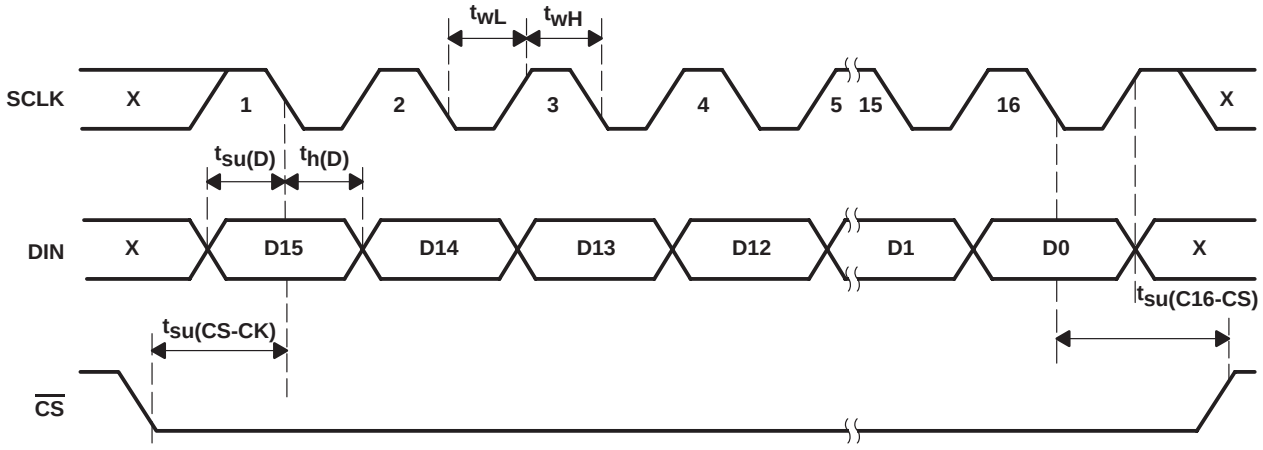



**Figure 1. Timing Diagram**

## TYPICAL CHARACTERISTICS

**SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

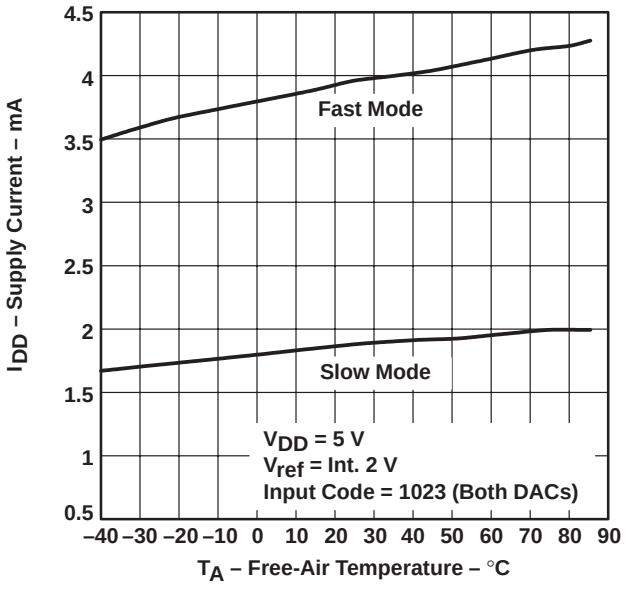



Figure 2

**SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

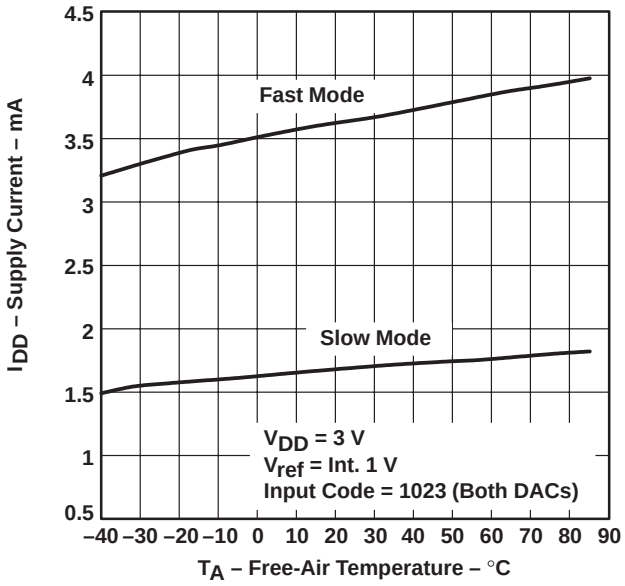



Figure 3

**POWER DOWN SUPPLY CURRENT
vs
TIME**

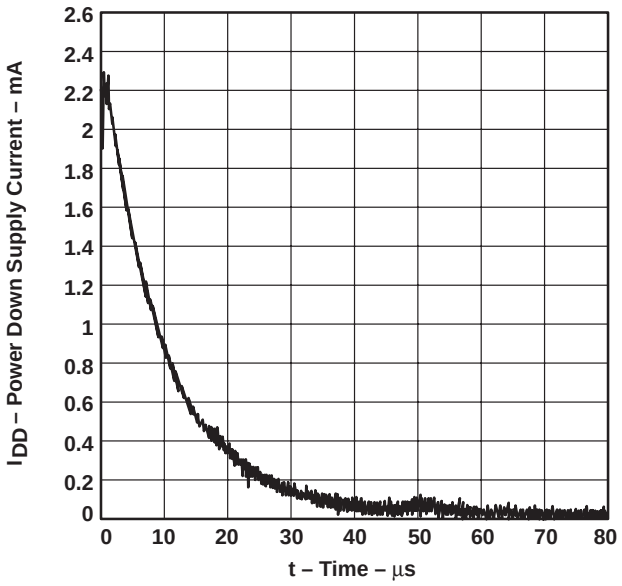



Figure 4

**OUTPUT VOLTAGE
vs
LOAD CURRENT**

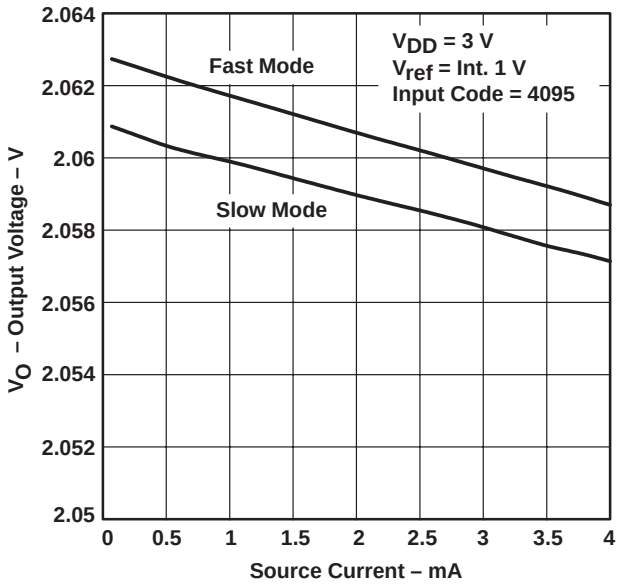



Figure 5

## TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
LOAD CURRENT

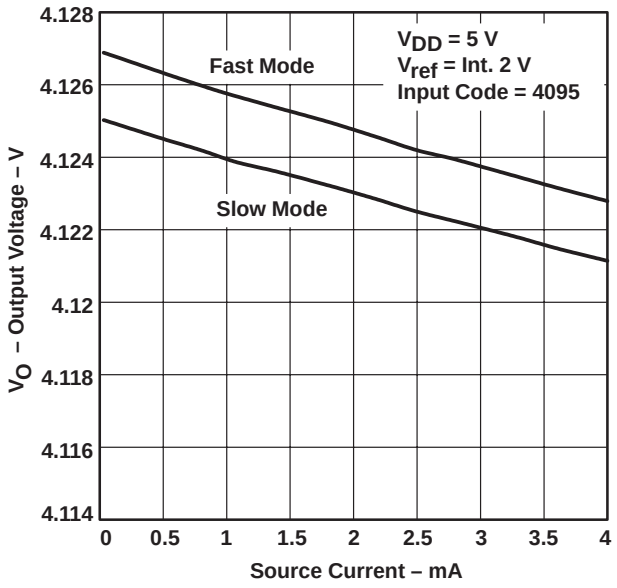



Figure 6

OUTPUT VOLTAGE
vs
LOAD CURRENT

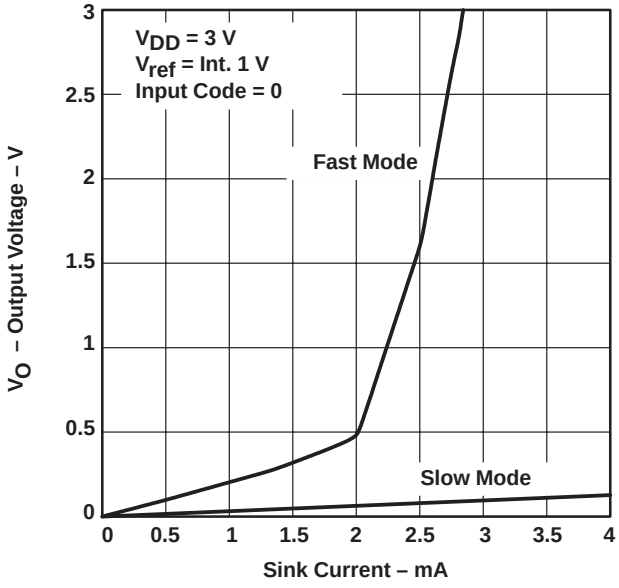



Figure 7

OUTPUT VOLTAGE
vs
LOAD CURRENT

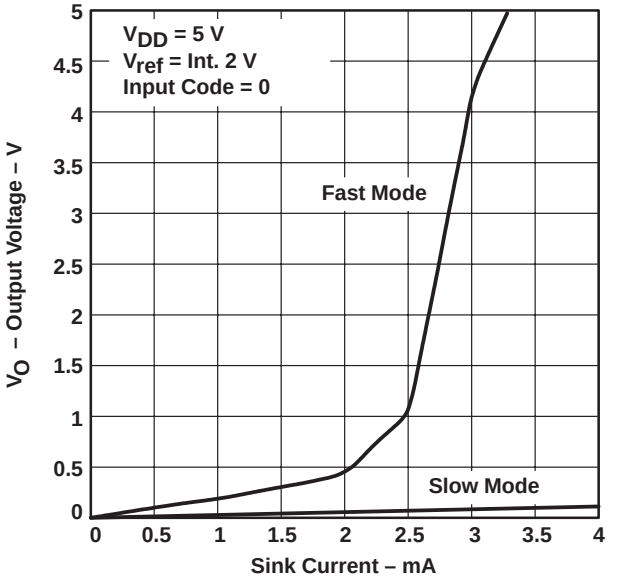



Figure 8

TOTAL HARMONIC DISTORTION AND NOISE
vs
FREQUENCY

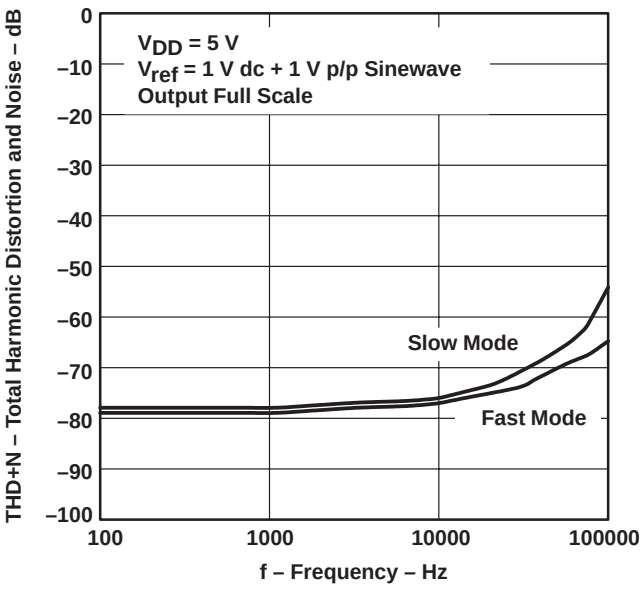



Figure 9

## TYPICAL CHARACTERISTICS

**TOTAL HARMONIC DISTORTION
vs
FREQUENCY**

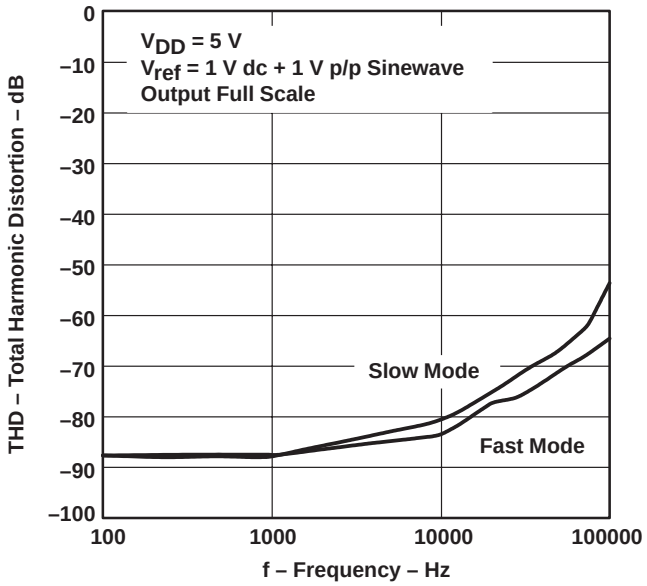



**Figure 10**

**DIFFERENTIAL NONLINEARITY
vs
DIGITAL OUTPUT CODE**

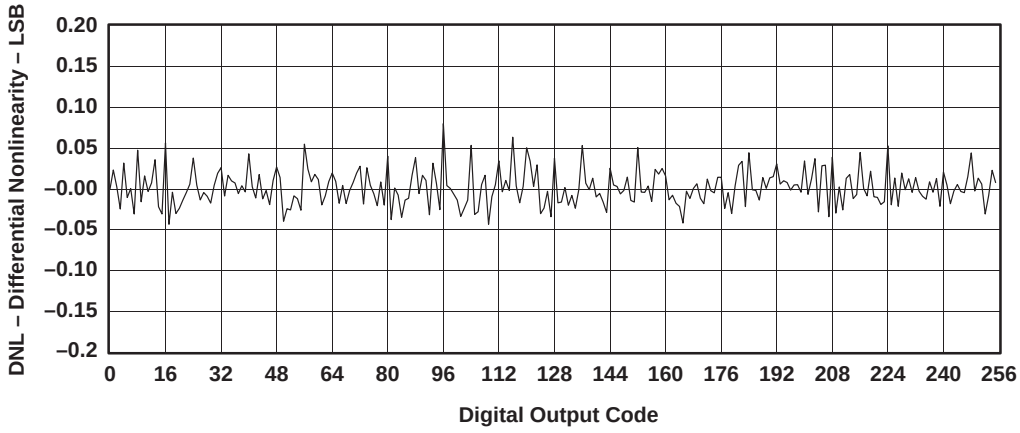



**Figure 11**

## TYPICAL CHARACTERISTICS

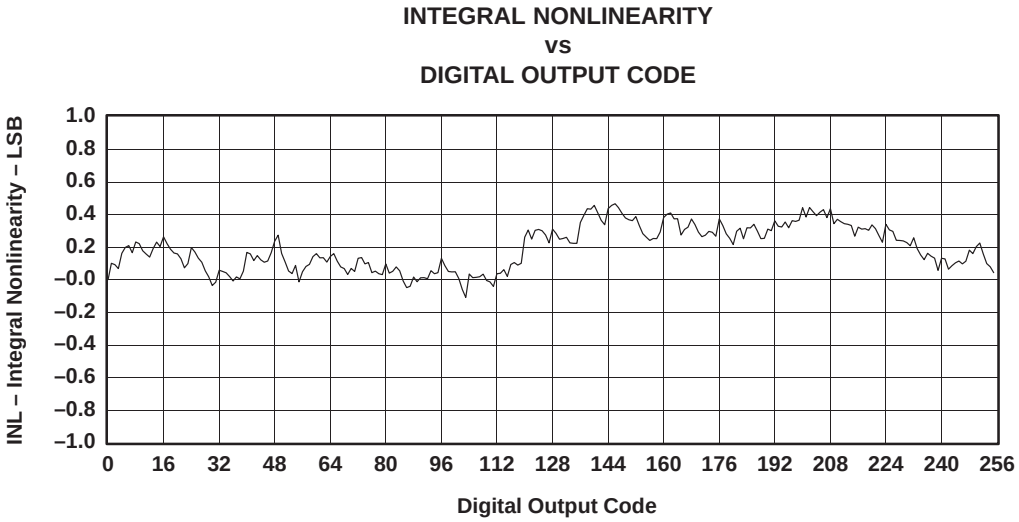



**Figure 12**

## APPLICATION INFORMATION

### general function

The TLV5626 is a dual 8-bit, single supply DAC, based on a resistor string architecture. It consists of a serial interface, a speed and power-down control logic, a programmable internal reference, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by reference) is given by:

$$2 \text{ REF } \frac{\text{CODE}}{\text{0x1000}} \text{ [V]}$$

Where REF is the reference voltage and CODE is the digital input value in the range 0x000 to 0xFF0.Bits 3 to 0 must be set to zero. A power on reset initially puts the internal latches to a defined state (all bits zero).

### serial interface

A falling edge of $\overline{CS}$ starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or $\overline{CS}$ rises, the content of the shift register is moved to the target latches (DAC A, DAC B, BUFFER, CONTROL), depending on the control bits within the data word.

Figure 13 shows examples of how to connect the TLV5626 to TMS320, SPI™, and Microwire™.

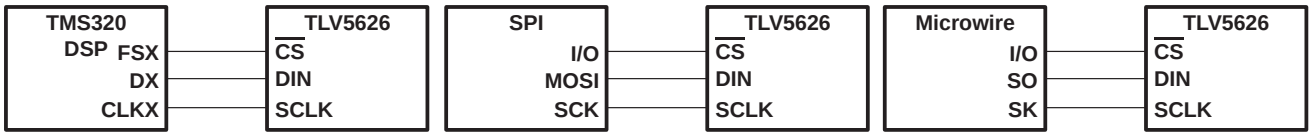



**Figure 13. Three-Wire Interface**

## APPLICATION INFORMATION

Notes on SPI™ and Microwire™: Before the controller starts the data transfer, the software has to generate a falling edge on the I/O pin connected to $\overline{CS}$. If the word width is 8 bits (SPI™ and Microwire™), two write operations must be performed to program the TLV5626. After the write operation(s), the holding registers or the control register are updated automatically on the 16$^{th}$ positive clock edge.

### serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{sclkmax} = \frac{1}{t_{whmin} + t_{wlmin}} = 20 \text{ MHz}$$

The maximum update rate is:

$$f_{updatemax} = \frac{1}{16\ (t_{whmin} + t_{wlmin})} = 1.25 \text{ MHz}$$

The maximum update rate is just a theoretical value for the serial interface, as the settling time of the TLV5626 has to be considered, too.

### data format

The 16-bit data word for the TLV5626 consists of two parts:

- Program bits (D15..D12)
- New data (D11..D0)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R1 | SPD | PWR | R0 | 12 Data bits | | | | | | | | | | | |

SPD: Speed control bit $1 \rightarrow$ fast mode $0 \rightarrow$ slow mode
PWR: Power control bit $1 \rightarrow$ power down $0 \rightarrow$ normal operation

The following table lists the possible combination of the register select bits:

**register select bits**

| R1 | R0 | REGISTER |
|---|---|---|
| 0 | 0 | Write data to DAC B and BUFFER |
| 0 | 1 | Write data to BUFFER |
| 1 | 0 | Write data to DAC A and update DAC B with BUFFER content |
| 1 | 1 | Write data to control register |

The meaning of the 12 data bits depends on the register. If one of the DAC registers or the BUFFER is selected, then the 12 data bits determine the new DAC value:

**data bits: DAC A, DAC B and BUFFER**

| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| New DAC Value | | | | | | | | 0 | 0 | 0 | 0 |

If control is selected, then D1, D0 of the 12 data bits are used to program the reference voltage:

## APPLICATION INFORMATION

**data bits: CONTROL**

| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X | REF1 | REF0 |

X: don't care

REF1 and REF0 determine the reference source and, if internal reference is selected, the reference voltage.

**reference bits**

| REF1 | REF0 | REFERENCE |
|---|---|---|
| 0 | 0 | External |
| 0 | 1 | 1.024 V |
| 1 | 0 | 2.048 V |
| 1 | 1 | External |

**CAUTION:**
**If external reference voltage is applied to the REF pin, external reference MUST be selected.**

### examples of operation:

- Set DAC A output, select fast mode, select internal reference at 2.048 V:

  1. Set reference voltage to 2.048 V (CONTROL register):

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

  2. Write new DAC A value and update DAC A output:

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | New DAC A output value | | | | | | | | 0 | 0 | 0 | 0 |

The DAC A output is updated on the rising clock edge after D0 is sampled.

To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

- Set DAC B output, select fast mode, select external reference:

  3. Select external reference (CONTROL register):

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

  4. Write new DAC B value to BUFFER and update DAC B output:

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | New BUFFER content and DAC B output value | | | | | | | | 0 | 0 | 0 | 0 |

X = Don't care

The DAC A output is updated on the rising clock edge after D0 is sampled.

To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

## APPLICATION INFORMATION

### examples of operation: (continued)

- Set DAC A value, set DAC B value, update both simultaneously, select slow mode, select internal reference at 1.024 V:

  1. Set reference voltage to 1.024 V (CONTROL register):

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

  2. Write data for DAC B to BUFFER:

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | New DAC B value | | | | | | | | 0 | 0 | 0 | 0 |

X = Don't care

  3. Write new DAC A value and update DAC A and B simultaneously:

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | New DAC A value | | | | | | | | 0 | 0 | 0 | 0 |

X = Don't care

Both outputs are updated on the rising clock edge after D0 from the DAC A data word is sampled.

- Set power-down mode:

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X |

X = Don't care

### linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 14.

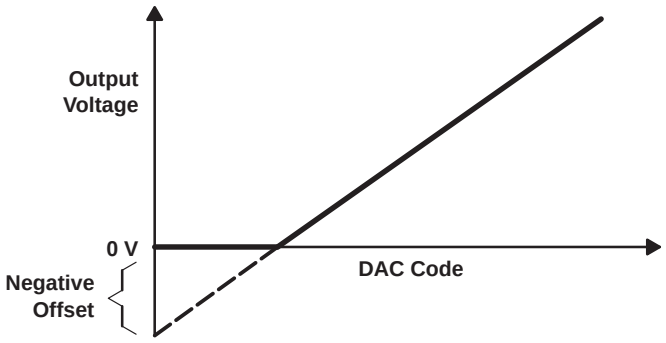



**Figure 14. Effect of Negative Offset (single supply)**

## APPLICATION INFORMATION

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

### definitions of specifications and terminology

**integral nonlinearity (INL)**

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

**differential nonlinearity (DNL)**

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

**zero-scale error ($E_{ZS}$)**

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

**gain error ($E_G$)**

Gain error is the error in slope of the DAC transfer function.

**signal-to-noise ratio + distortion (S/N+D)**

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

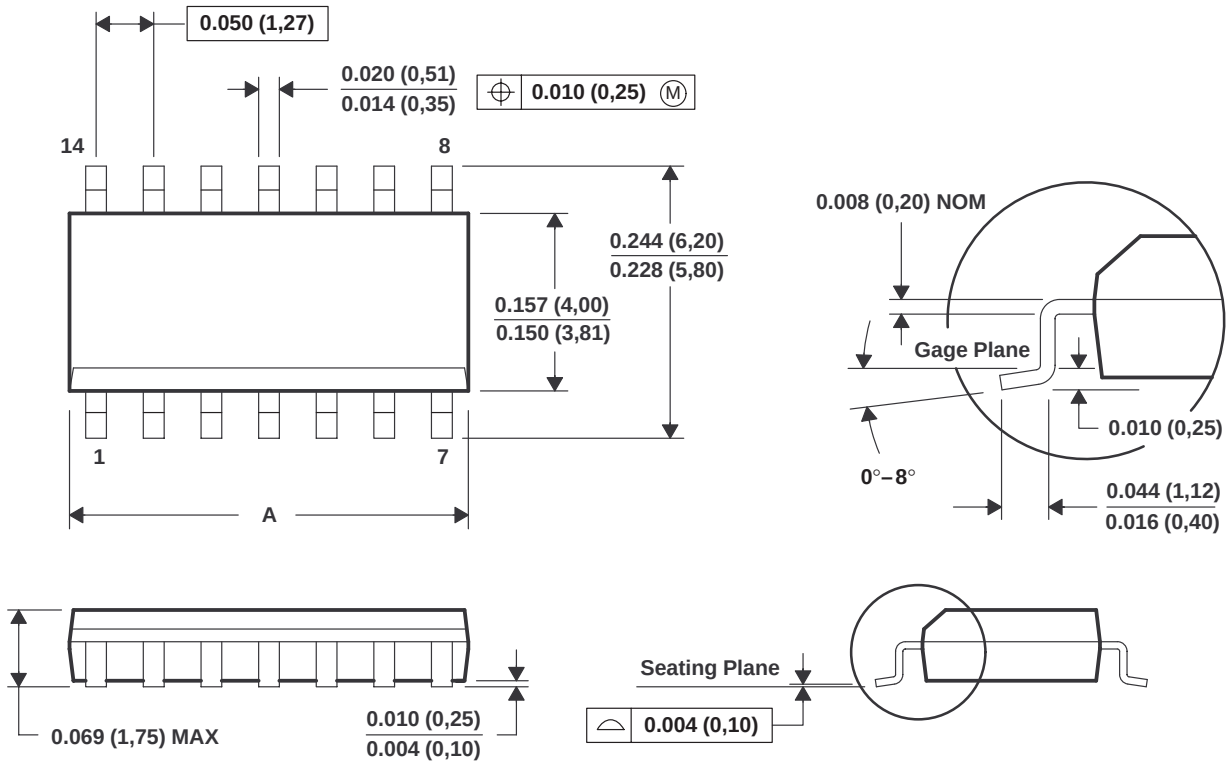
**spurious free dynamic range (SFDR)**

Spurious free dynamic range is the difference between the rms value of the output signal and the rms value of the spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

## MECHANICAL DATA

**D (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 |
|---|---|---|---|
| A MAX | 0.197 (5,00) | 0.344 (8,75) | 0.394 (10,00) |
| A MIN | 0.189 (4,80) | 0.337 (8,55) | 0.386 (9,80) |

**4040047/D 10/96**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.