



3.3V CMOS QUADRUPLE 2-INPUT POSITIVE-OR GATE WITH 5 VOLT TOLERANT I/O

IDT74LVC32A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels ($0.4\mu W$ typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs, and I/Os are 5V tolerant
- Supports hot insertion
- Available in SOIC, SSOP, and TSSOP packages

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

DESCRIPTION:

The LVC32A quadruple 2-input positive -OR gate is built using advanced dual metal CMOS technology. The LVC32A device performs the Boolean function $Y = A + B$ or $Y = \bar{A} \cdot \bar{B}$ in positive logic.

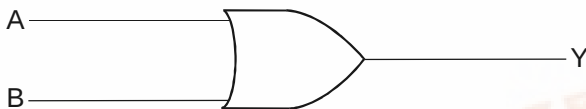
Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

The LVC32A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

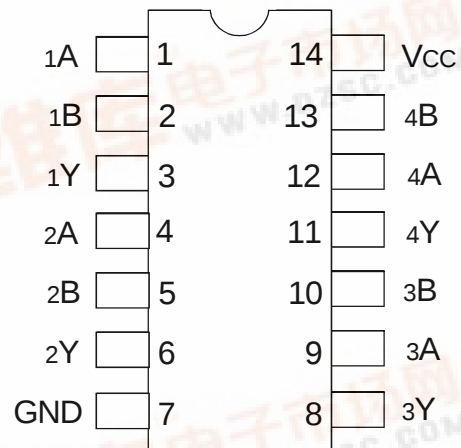
APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ SSOP/ TSSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xA, xB	Inputs
xY	Outputs

FUNCTION TABLE (EACH GATE)⁽¹⁾

Inputs		Output
xA	xB	xy
H	X	H
X	H	H
L	L	L

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care



IDT74LVC32A
3.3V CMOS QUADRUPLE 2-INPUT POSITIVE-OR GATE
INDUSTRIAL TEMPERATURE RANGE
ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to +6.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	−50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

NOTE:

- As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = −40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = −18mA		—	−0.7	−1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V, V _{IN} = GND or V _{CC}		—	—	10	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	500	μA

NOTE:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	IOH = – 6mA	2	—	
		VCC = 2.3V	IOH = – 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = – 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3V	IOL = 24mA	—	0.55	

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range.
TA = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per Gate	CL = 0pF, f = 10MHz	10.6	12.5	pF

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	VCC = 2.5V ± 0.2V		VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH	Propagation Delay	1	5.4	—	4.4	1.5	3.8	ns
tPHL	xA, xB to xY							
tsk(0)	Output Skew ⁽²⁾	—	—	—	—	—	1	ns

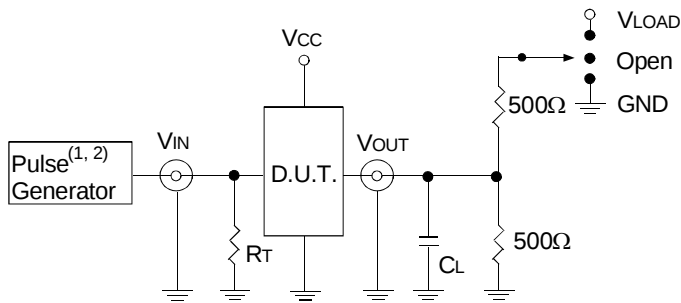
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. TA = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 2.5V \pm 0.2V$	$V_{CC}^{(2)} = 3.3V \pm 0.3V \text{ \& } 2.7V$	Unit
V_{LOAD}	$2 \times V_{CC}$	6	V
V_{IH}	V_{CC}	2.7	V
V_T	$V_{CC} / 2$	1.5	V
V_{LZ}	150	300	mV
V_{HZ}	150	300	mV
CL	30	50	pF



Test Circuit for All Outputs

LVC QUAD Link

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

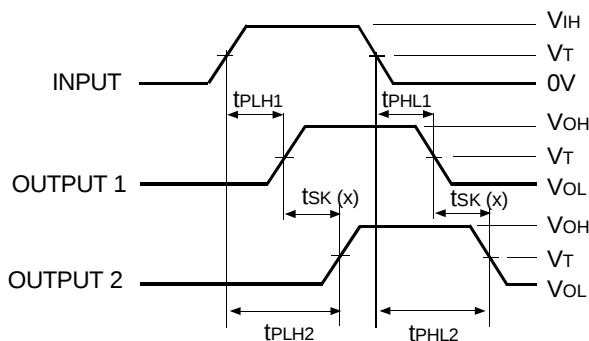
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_r \leq 2\text{ns}$; $t_f \leq 2\text{ns}$.
2. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open



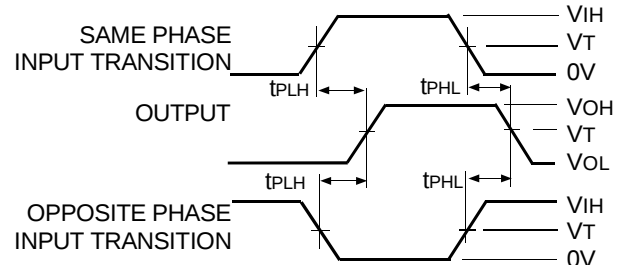
$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

LVC QUAD Link

Output Skew - $tsk(x)$

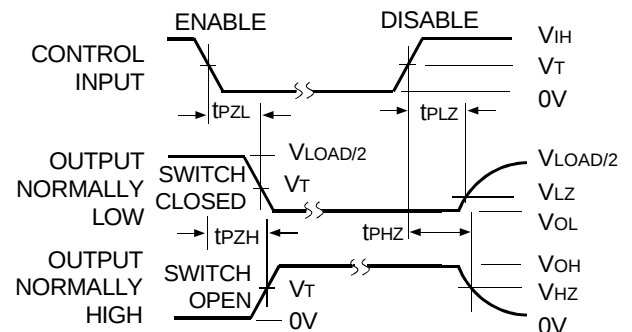
NOTES:

1. For $tsk(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $tsk(b)$ OUTPUT1 and OUTPUT2 are in the same bank.



LVC QUAD Link

Propagation Delay

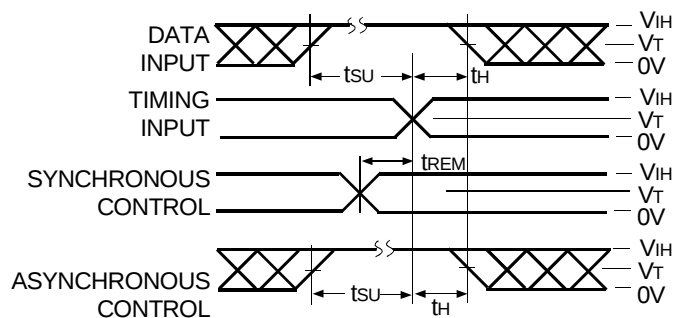


LVC QUAD Link

NOTE:

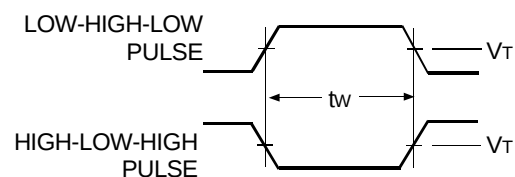
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times



LVC QUAD Link

Set-up, Hold, and Release Times



LVC QUAD Link

Pulse Width

ORDERING INFORMATION

IDT	XX	LVC	XXXX	XX	
Temp. Range		Device Type		Package	
				DC	Small Outline IC
				PY	Shrink Small Outline Package
				PG	Thin Shrink Small Outline Package
				32A	Quadruple 2-Input Positive-OR Gate, $\pm 24\text{mA}$
				74	-40°C to +85°C



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