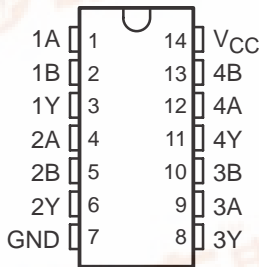
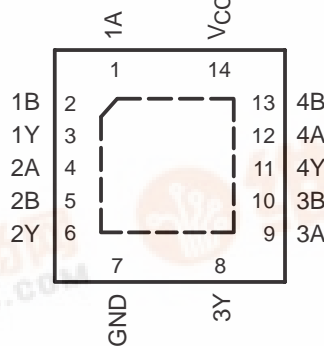


- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

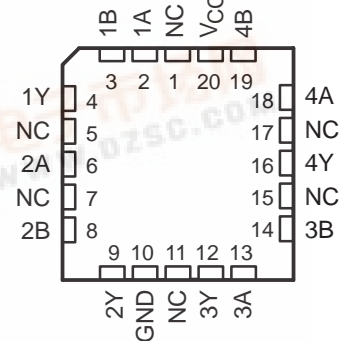
SN54LV32A ... J OR W PACKAGE
 SN74LV32A ... D, DB, DGV, NS,
 OR PW PACKAGE
 (TOP VIEW)



SN74LV32A ... RGY PACKAGE
 (TOP VIEW)



SN54LV32A ... FK PACKAGE
 (TOP VIEW)



NC – No internal connection

description/ordering information

These quadruple 2-input positive-OR gates are designed for 2-V to 5.5-V V_{CC} operation.

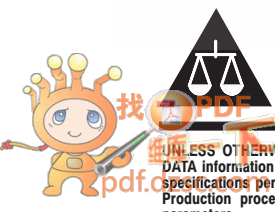
The 'LV32A devices perform the Boolean function $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|--------------|---------------|-----------------------|------------------|
| -40°C to 85°C | QFN – RGY | Reel of 1000 | SN74LV32ARGYR | LV32A |
| | SOIC – D | Tube of 50 | SN74LV32AD | LV32A |
| | | Reel of 2500 | SN74LV32ADR | |
| | SOP – NS | Reel of 2000 | SN74LV32ANSR | 74LV32A |
| | SSOP – DB | Reel of 2000 | SN74LV32ADBR | LV32A |
| | TSSOP – PW | Tube of 90 | SN74LV32APW | LV32A |
| | | Reel of 2000 | SN74LV32APWR | |
| Reel of 250 | | SN74LV32APWT | | |
| TVSOP – DGV | Reel of 2000 | SN74LV32ADGVR | LV32A | |
| -55°C to 125°C | CDIP – J | Tube of 25 | SNJ54LV32AJ | SNJ54LV32AJ |
| | CFP – W | Tube of 150 | SNJ54LV32AW | SNJ54LV32AW |
| | LCCC – FK | Tube of 55 | SNJ54LV32AFK | SNJ54LV32AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



SN54LV32A, SN74LV32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

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description/ordering information (continued)

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 7 V |
| Output voltage range, V_O (see Notes 1 and 2) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –20 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): D package | 86°C/W |
| (see Note 3): DB package | 96°C/W |
| (see Note 3): DGV package | 127°C/W |
| (see Note 3): NS package | 76°C/W |
| (see Note 3): PW package | 113°C/W |
| (see Note 4): RGY package | 47°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LV32A, SN74LV32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

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recommended operating conditions (see Note 5)

| | | SN54LV32A | | SN74LV32A | | UNIT |
|-----------------|------------------------------------|----------------------------------|-----------------------|-----------------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 2 | 5.5 | 2 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | 1.5 | | V |
| | | V _{CC} = 2.3 V to 2.7 V | V _{CC} × 0.7 | V _{CC} × 0.7 | | |
| | | V _{CC} = 3 V to 3.6 V | V _{CC} × 0.7 | V _{CC} × 0.7 | | |
| | | V _{CC} = 4.5 V to 5.5 V | V _{CC} × 0.7 | V _{CC} × 0.7 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | 0.5 | 0.5 | V |
| | | V _{CC} = 2.3 V to 2.7 V | V _{CC} × 0.3 | V _{CC} × 0.3 | | |
| | | V _{CC} = 3 V to 3.6 V | V _{CC} × 0.3 | V _{CC} × 0.3 | | |
| | | V _{CC} = 4.5 V to 5.5 V | V _{CC} × 0.3 | V _{CC} × 0.3 | | |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 2 V | | -50 | -50 | μA |
| | | V _{CC} = 2.3 V to 2.7 V | | -2 | -2 | mA |
| | | V _{CC} = 3 V to 3.6 V | | -6 | -6 | |
| | | V _{CC} = 4.5 V to 5.5 V | | -12 | -12 | |
| I _{OL} | Low-level output current | V _{CC} = 2 V | | 50 | 50 | μA |
| | | V _{CC} = 2.3 V to 2.7 V | | 2 | 2 | mA |
| | | V _{CC} = 3 V to 3.6 V | | 6 | 6 | |
| | | V _{CC} = 4.5 V to 5.5 V | | 12 | 12 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 2.3 V to 2.7 V | | 200 | 200 | ns/V |
| | | V _{CC} = 3 V to 3.6 V | | 100 | 100 | |
| | | V _{CC} = 4.5 V to 5.5 V | | 20 | 20 | |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | SN54LV32A | | | SN74LV32A | | | UNIT |
|------------------|---|-----------------|----------------------|-----|------|----------------------|------|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{OH} | I _{OH} = -50 μA | 2 V to 5.5 V | V _{CC} -0.1 | | | V _{CC} -0.1 | | V | |
| | I _{OH} = -2 mA | 2.3 V | 2 | | | 2 | | | |
| | I _{OH} = -6 mA | 3 V | 2.48 | | | 2.48 | | | |
| | I _{OH} = -12 mA | 4.5 V | 3.8 | | | 3.8 | | | |
| V _{OL} | I _{OL} = 50 μA | 2 V to 5.5 V | | | 0.1 | | 0.1 | V | |
| | I _{OL} = 2 mA | 2.3 V | | | 0.4 | | 0.4 | | |
| | I _{OL} = 6 mA | 3 V | | | 0.44 | | 0.44 | | |
| | I _{OL} = 12 mA | 4.5 V | | | 0.55 | | 0.55 | | |
| I _I | V _I = 5.5 V or GND | 0 to 5.5 V | | | ±1 | | ±1 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 20 | | 20 | μA | |
| I _{off} | V _I or V _O = 0 to 5.5 V | 0 | | | 5 | | 5 | μA | |
| C _i | V _I = V _{CC} or GND | 3.3 V | | 3.3 | | 3.3 | | pF | |
| | | 5 V | | 3.3 | | 3.3 | | | |

SN54LV32A, SN74LV32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54LV32A | | SN74LV32A | | UNIT |
|-----------|--------------|-------------|----------------------|--------------------------|-------|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A or B | Y | $C_L = 15\text{ pF}$ | 7.1* | 12.8* | 1* | 16* | 1 | 15 | ns | |
| | | | $C_L = 50\text{ pF}$ | 9.6 | 16.2 | 1 | 20 | 1 | 19 | | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54LV32A | | SN74LV32A | | UNIT |
|-----------|--------------|-------------|----------------------|--------------------------|------|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A or B | Y | $C_L = 15\text{ pF}$ | 5* | 7.9* | 1* | 9.5* | 1 | 9.5 | ns | |
| | | | $C_L = 50\text{ pF}$ | 6.9 | 11.4 | 1 | 13 | 1 | 13 | | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54LV32A | | SN74LV32A | | UNIT |
|-----------|--------------|-------------|----------------------|--------------------------|------|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A or B | Y | $C_L = 15\text{ pF}$ | 3.6* | 5.5* | 1* | 6.5* | 1 | 6.5 | ns | |
| | | | $C_L = 50\text{ pF}$ | 4.9 | 7.5 | 1 | 8.5 | 1 | 8.5 | | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 6)

| PARAMETER | | SN74LV32A | | | UNIT |
|-------------|--|-----------|------|-----|------|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | 0.2 | 0.8 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | -0.1 | -0.8 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | 3.1 | | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.99 | | V |

NOTE 6: Characteristics are for surface-mount packages only.

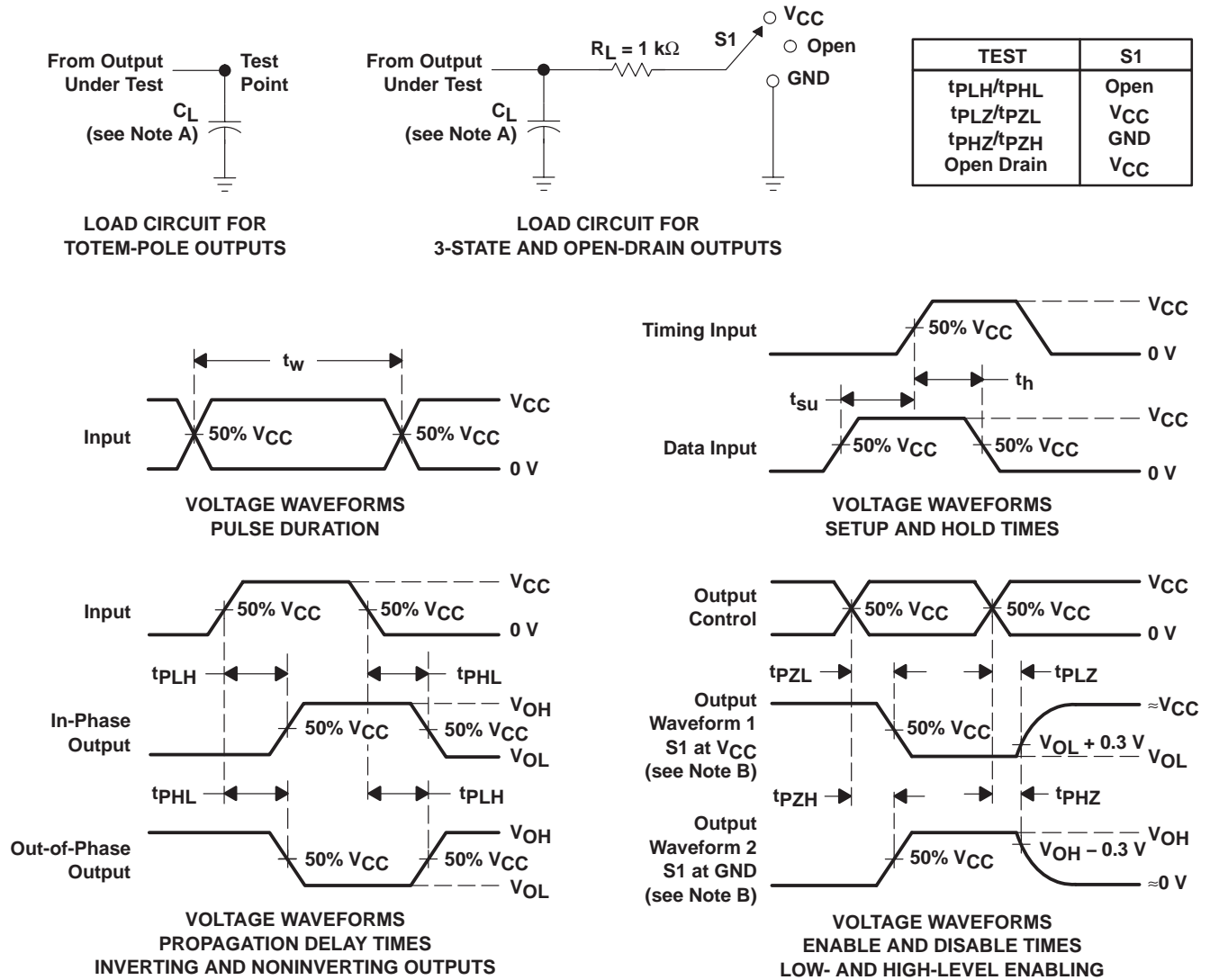
operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|-----------|-------------------------------|--|----------|------|------|
| C_{pd} | Power dissipation capacitance | $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$ | 3.3 V | 9.5 | pF |
| | | | 5 V | 11.5 | |

SN54LV32A, SN74LV32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 - The outputs are measured one at a time, with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LV32AD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32ADBLE | OBSOLETE | SSOP | DB | 14 | | TBD | Call TI | Call TI |
| SN74LV32ADBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32ADBRE4 | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32ADE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32ADGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32ADGVRE4 | ACTIVE | TVSOP | DGV | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32ADR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32ANSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32ANSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32APW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32APWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32APWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32APWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI |
| SN74LV32APWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32APWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32APWT | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32APWTE4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32APWTG4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV32ARGYR | ACTIVE | QFN | RGY | 14 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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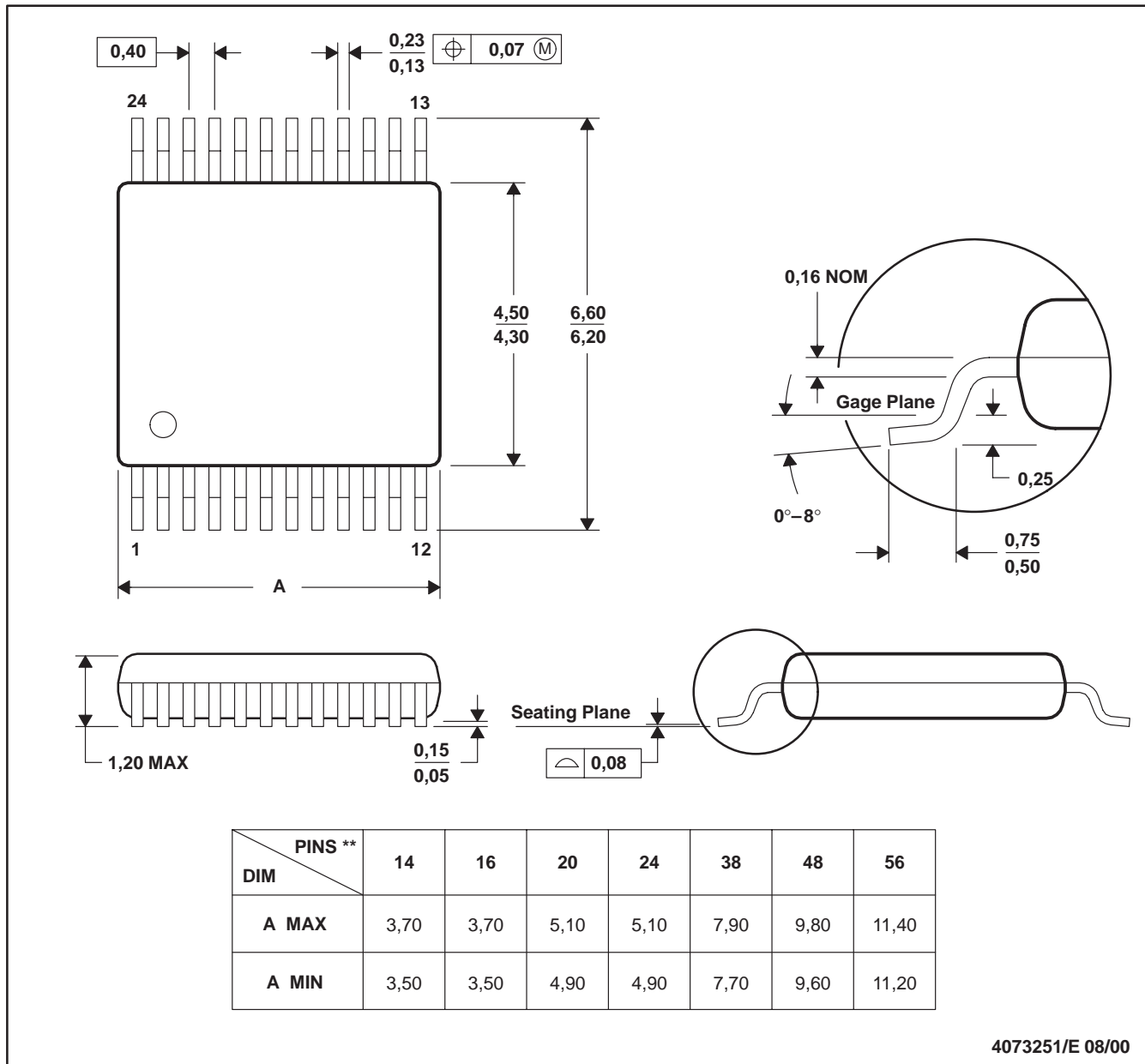
MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

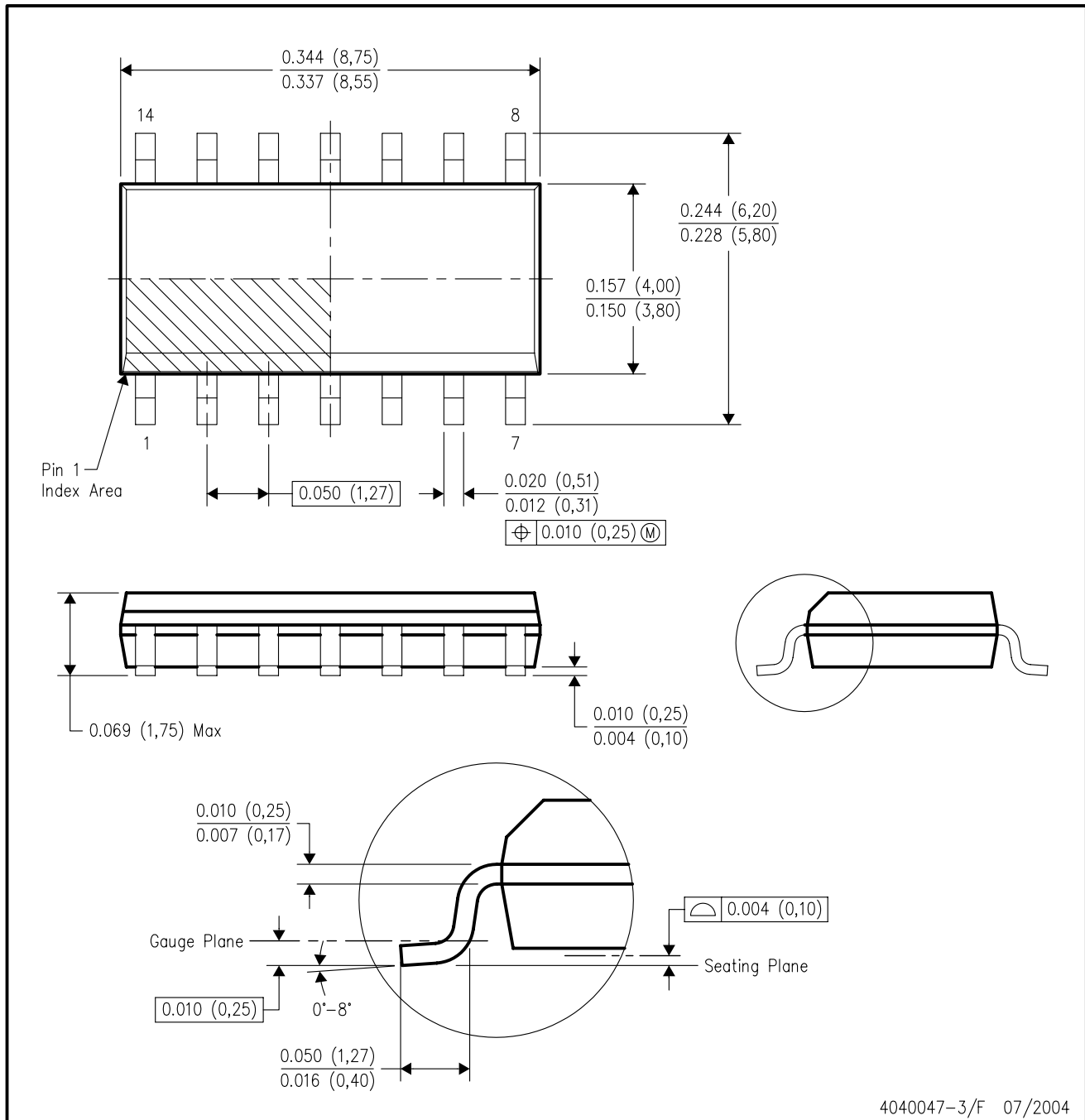


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

MECHANICAL DATA

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE

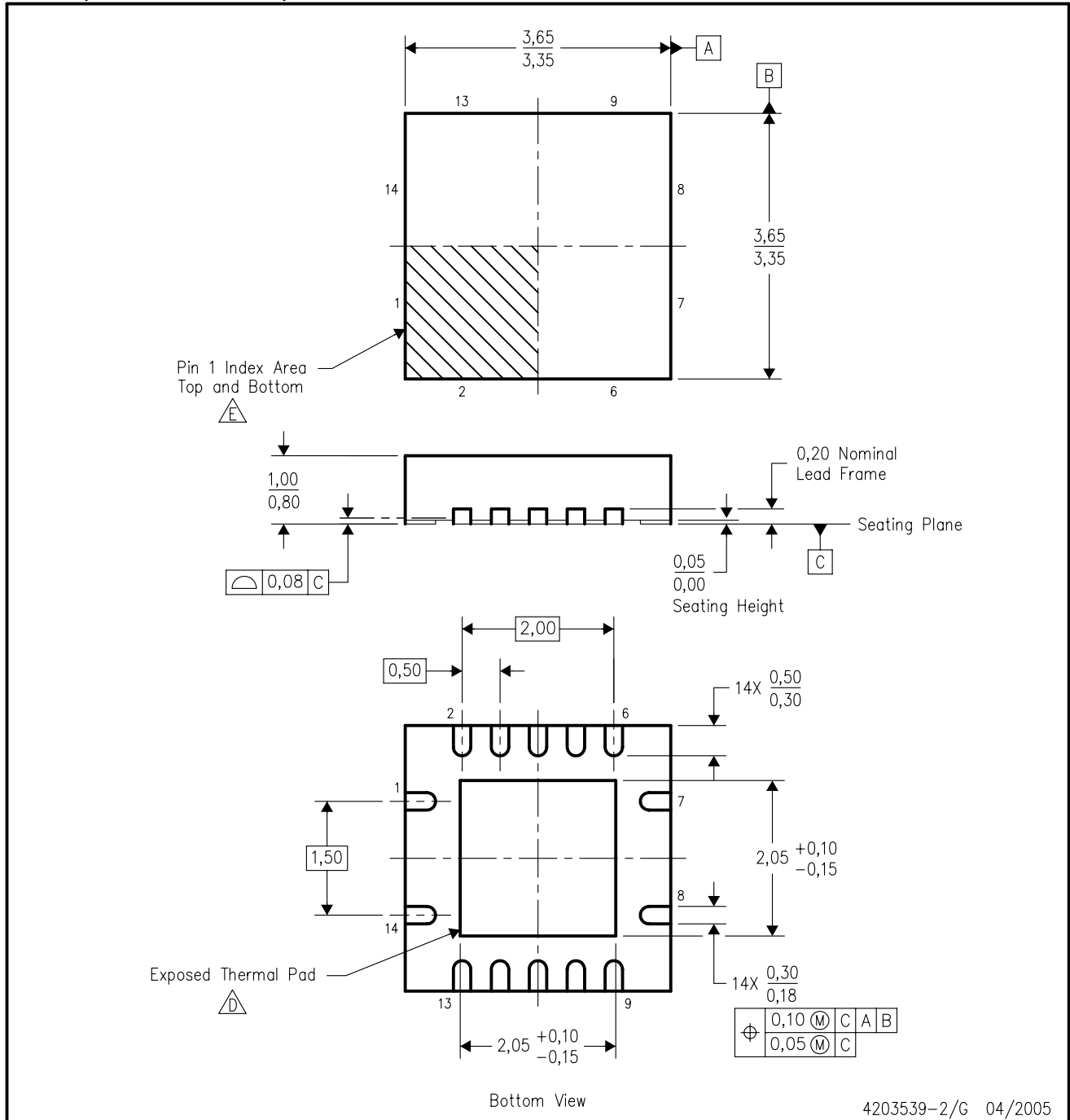


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



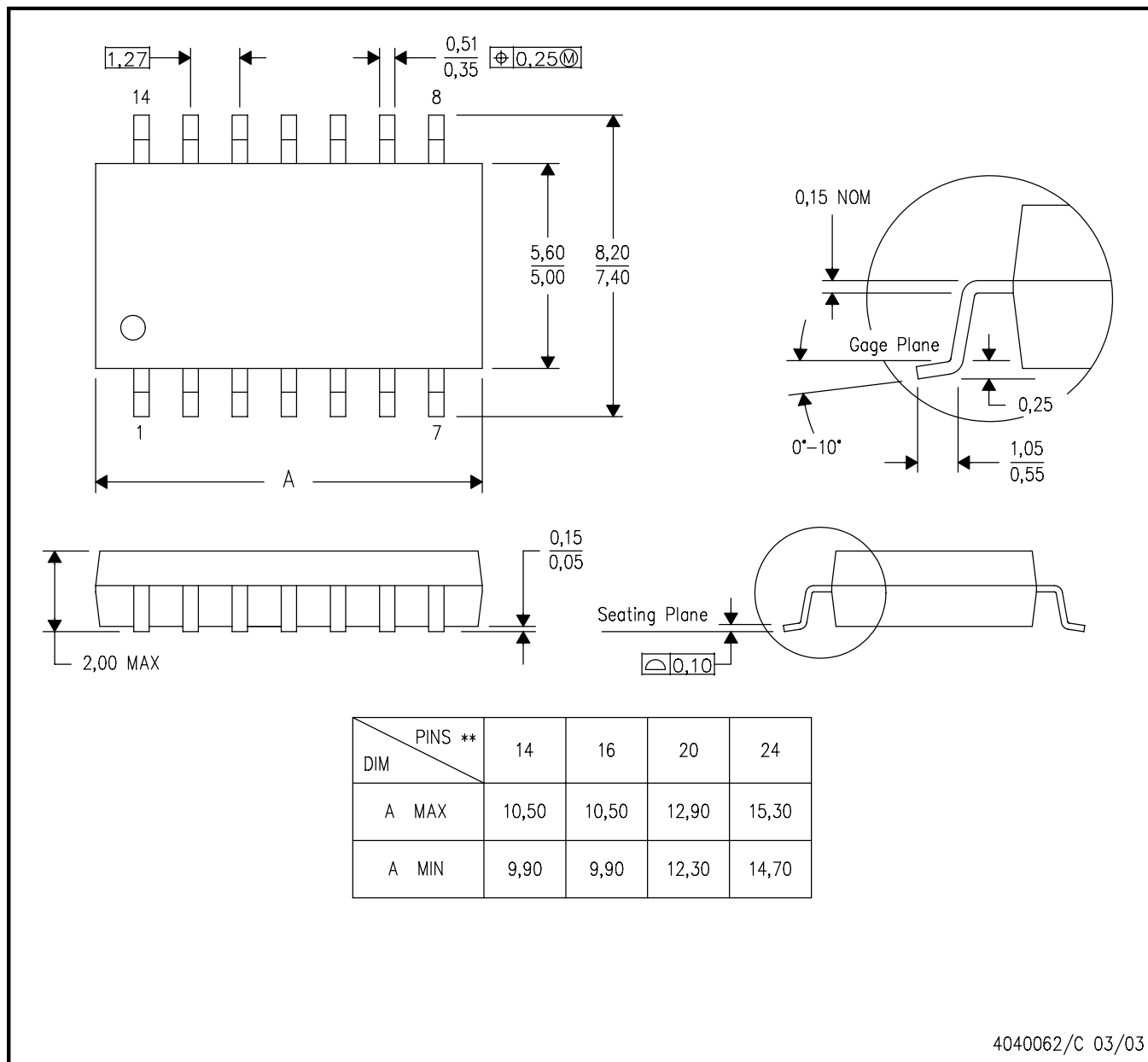
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



4040062/C 03/03

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

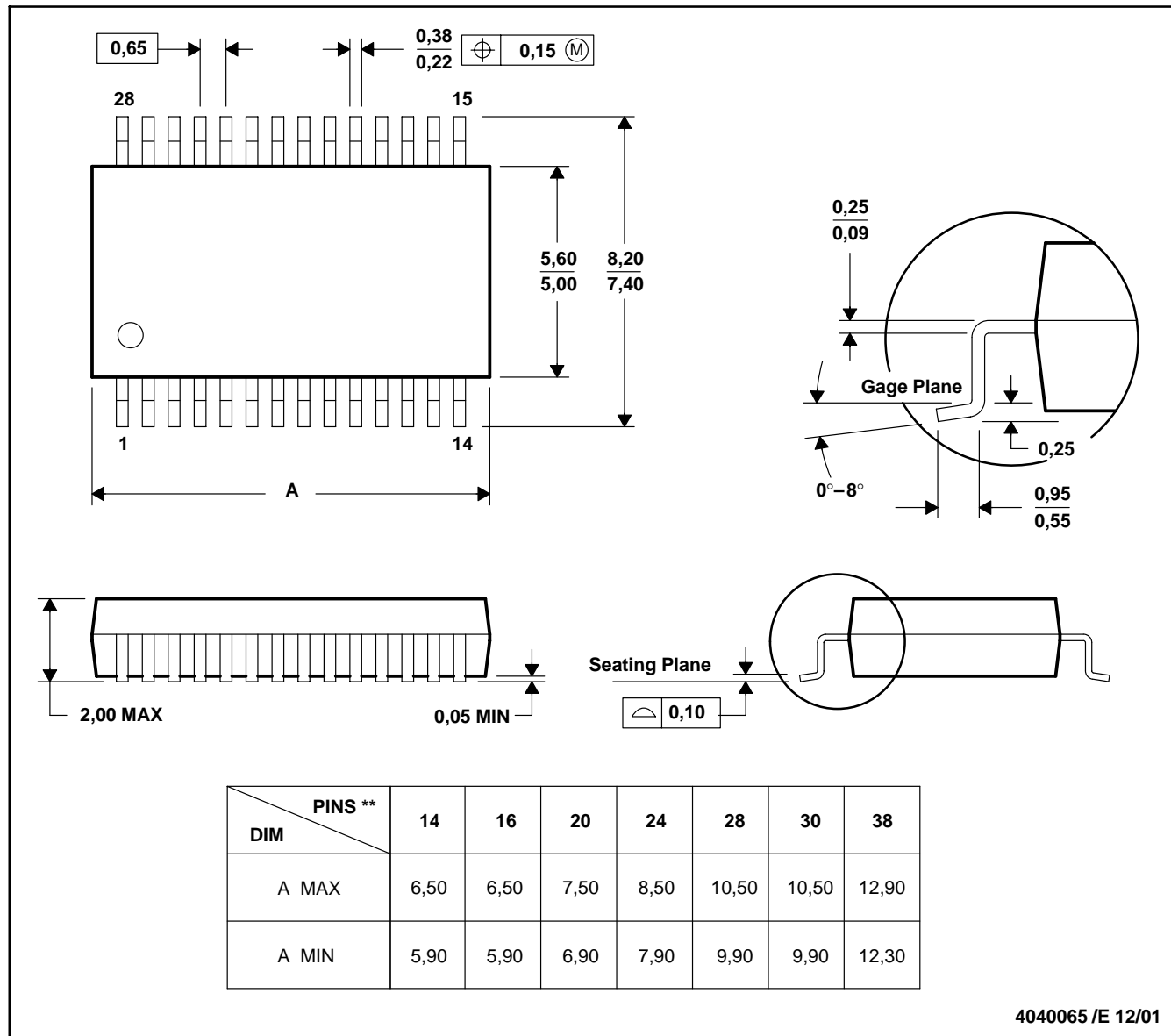
MECHANICAL DATA

MSS0002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

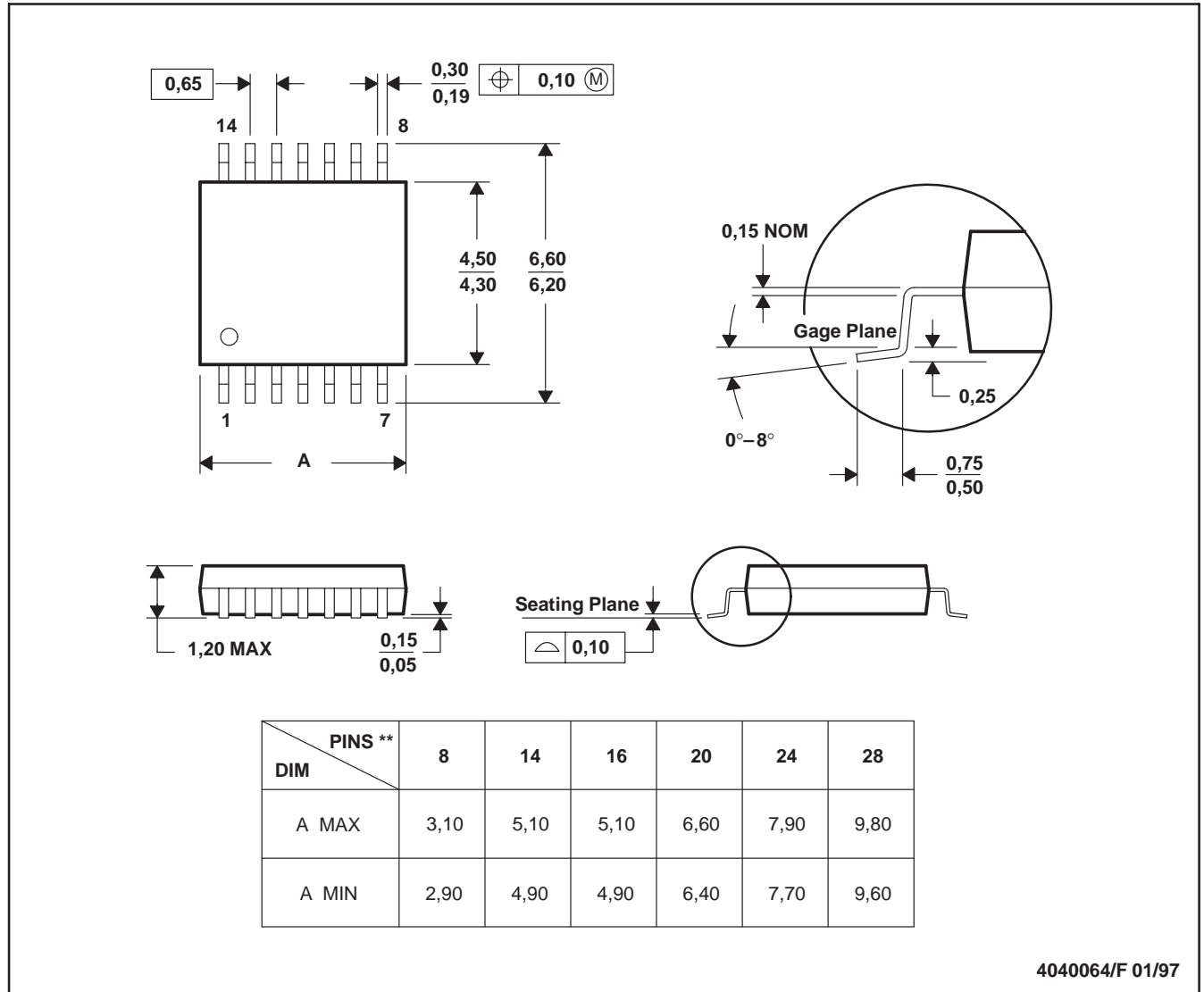
MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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