

# SN54ALS112A SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS199A – APRIL 1982 – REVISED DECEMBER 1994

- Fully Buffered to Offer Maximum Isolation From External Disturbance
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS112A	50	6

## description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse (CLK). Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

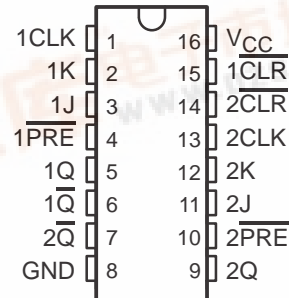
The SN54ALS112A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS112A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE  
(each flip-flop)

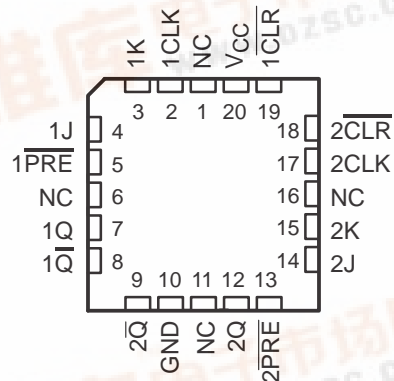
INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	$\text{H}^{\dagger}$	$\text{H}^{\dagger}$
H	H	$\downarrow$	L	L	$\text{Q}_0$	$\overline{\text{Q}}_0$
H	H	$\downarrow$	H	L	H	L
H	H	$\downarrow$	L	H	L	H
H	H	$\downarrow$	H	H	Toggle	
H	H	H	X	X	$\text{Q}_0$	$\overline{\text{Q}}_0$

$\dagger$  The output levels in this configuration may not meet the minimum levels for  $\text{V}_{\text{OH}}$ . Furthermore, this configuration is nonstable; that is, it does not persist when either  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.

SN54ALS112A ... J PACKAGE  
SN74ALS112A ... D OR N PACKAGE  
(TOP VIEW)



SN54ALS112A ... FK PACKAGE  
(TOP VIEW)



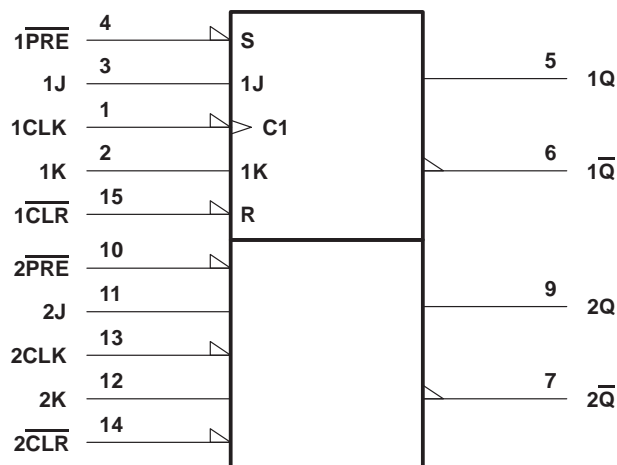
NC – No internal connection

# SN54ALS112A, SN74ALS112A

## DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

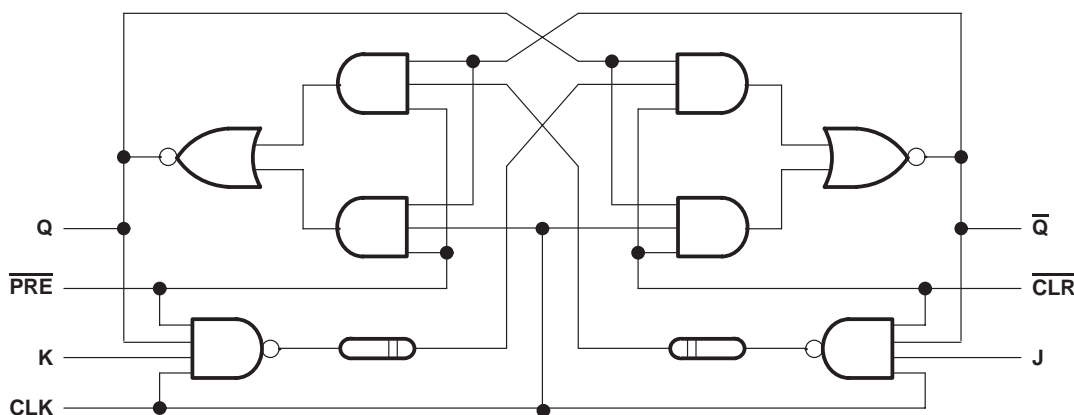
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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, and N packages.

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54ALS112A	–55°C to 125°C
SN74ALS112A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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## recommended operating conditions

			SN54ALS112A			SN74ALS112A			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V		
V <sub>IH</sub>	High-level input voltage		2			2			V		
V <sub>IL</sub>	Low-level input voltage		0.7			0.8			V		
I <sub>OH</sub>	High-level output current		−0.4			−0.4			mA		
I <sub>OL</sub>	Low-level output current		4			8			mA		
f <sub>clock</sub>	Clock frequency		0	25		0	30		MHz		
t <sub>w</sub>	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	15			10			ns		
		CLK high	20			16.5					
		CLK low	20			16.5					
t <sub>su</sub>	Setup time before CLK↓	Data	25			22			ns		
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	22			20					
t <sub>h</sub>	Hold time after CLK↓	Data	0			0			ns		
T <sub>A</sub>	Operating free-air temperature		−55			125			0	70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS112A			SN74ALS112A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA				–1.5			–1.5	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = –0.4 mA		V <sub>CC</sub> – 2			V <sub>CC</sub> – 2			V
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 4 mA		0.25	0.4		0.25	0.4		V
			I <sub>OL</sub> = 8 mA				0.35	0.5		
I <sub>I</sub>	J, K, or CLK	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V			0.1			0.1		mA
	PRE or CLR				0.2			0.2		
I <sub>IH</sub>	J, K, or CLK	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			20			20		μA
	PRE or CLR				40			40		
I <sub>IL</sub>	J, K, or CLK	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V			–0.2			–0.2		mA
	PRE or CLR				–0.4			–0.4		
I <sub>O</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V		–20		–112	–30		–112	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, See Note 1			2.5	4.5		2.5	4.5	mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

NOTE 1: I<sub>CC</sub> is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

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## DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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### switching characteristics (see Figure 1)

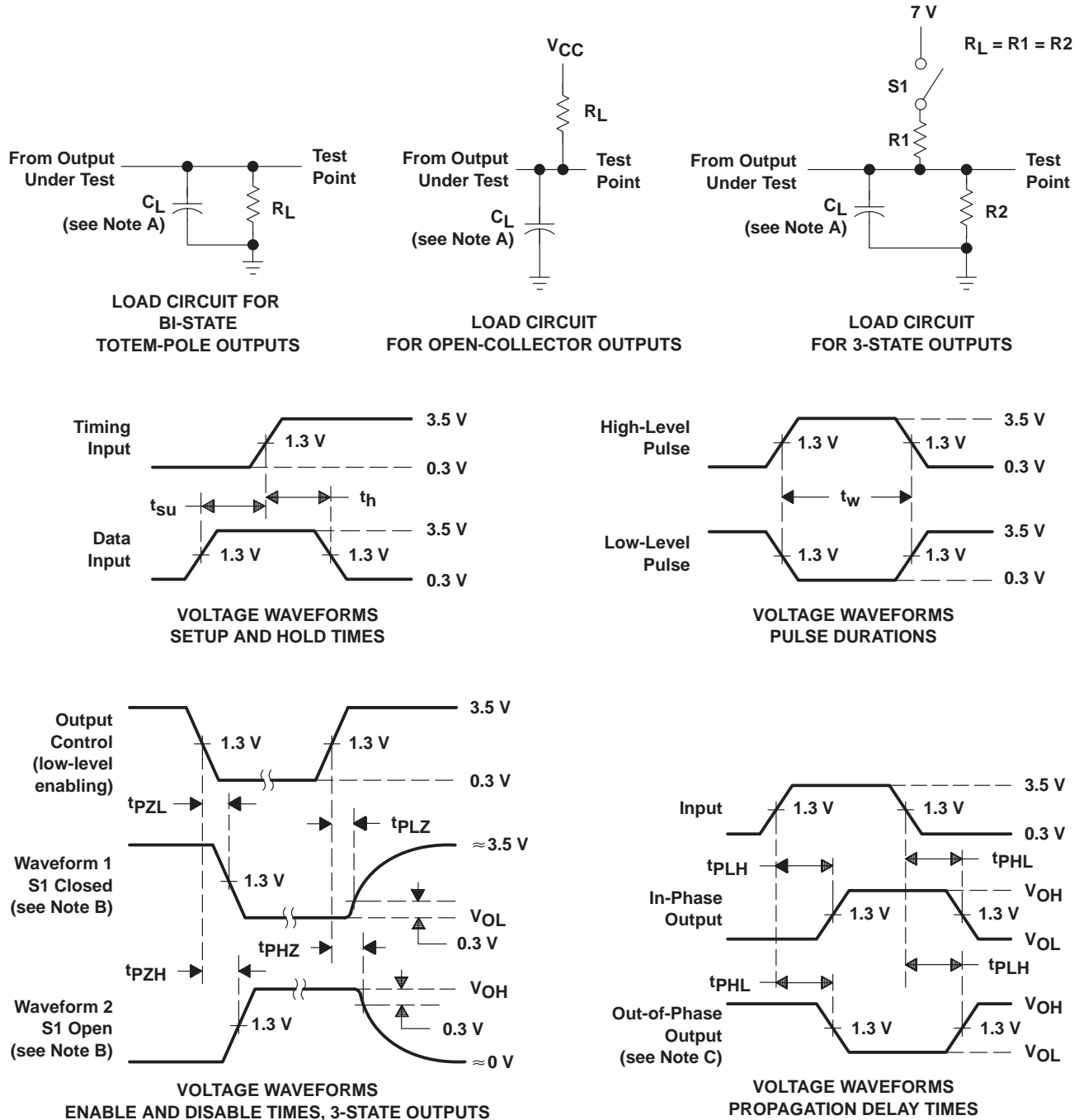
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS112A		SN74ALS112A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			25		30		MHz
t <sub>PLH</sub>	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	3	26	3	15	ns
t <sub>PHL</sub>			4	23	4	18	
t <sub>PLH</sub>	CLK	Q or $\overline{\text{Q}}$	3	23	3	15	ns
t <sub>PHI</sub>			5	24	5	19	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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