DG441/883, DG442/883

June 1994

Monolithic Quad SPST CMOS Analog Switches

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **ON-Resistance 85Ω Max**
- **Low Power Consumption (P_D <1.6mW)**
- **Fast Switching Action**
  - **t_{ON} <250ns**
  - **t_{OFF} <120ns (DG441/883)**
- **Low Charge Injection**
- **Upgrade from DG201A/883/DG202/883**
- **TTL, CMOS Compatible**
- **Single or Split Supply Operation**

Applications

- **Audio Switching**
- **Battery Operated Systems**
- **Data Acquisition**
- **Hi-Rel Systems**
- **Sample and Hold Circuits**
- **Communication Systems**
- **Automatic Test Equipment**

Description

The DG441/883 and DG442/883 monolithic CMOS analog switches are drop-in replacements for the popular DG201A/883 and DG202/883 series devices. They include four independent single pole single throw (SPST) analog switches, TTL and CMOS compatible digital inputs, and a voltage reference for logic thresholds.

These switches feature lower analog ON resistance (<85Ω) and faster switch time (t_{ON} <250ns) compared to the DG201A/883 and DG202/883. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG441/883 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 40V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

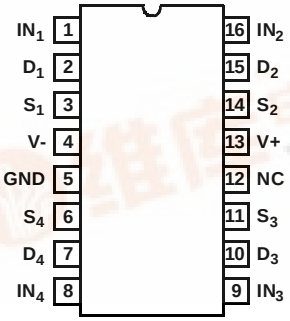
The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range. The switches in the DG441/883 and DG442/883 are identical, differing only in the polarity of the selection logic.

Ordering Information

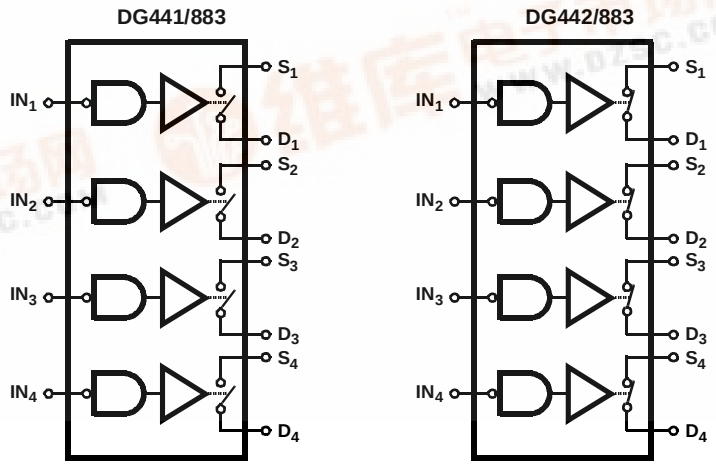
PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG441AK/883	-55°C to +125°C	16 Lead CerDIP
DG442AK/883	-55°C to +125°C	16 Lead CerDIP

Pinout

DG441/883, DG442/883
(CERDIP)
TOP VIEW



Functional Diagrams



SWITCHES SHOWN FOR LOGIC "1" INPUT

Pin Description

PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic Control for Switch 1
2	D_1	Drain (Output) Terminal for Switch 1
3	S_1	Source (Input) Terminal for switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S_4	Source (Input) Terminal for Switch 4
7	D_4	Drain (Output) Terminal for Switch 4
8	IN_4	Logic Control for Switch 4
9	IN_3	Logic Control for Switch 3
10	D_3	Drain (Output) Terminal for Switch 3
11	S_3	Source (Input) Terminal for Switch 3
12	NC	No Internal Connection
13	V+	Positive Power Supply Terminal (Substrate)
14	S_2	Source (Input) Terminal for Switch 2
15	D_2	Drain (Output) Terminal for Switch 2
16	IN_2	Logic Control for Switch 2

TRUTH TABLE

LOGIC	V_{IN}	DG441	DG442
0	$\leq$0.8V	ON	OFF
1	$\geq$2.4V	OFF	ON

Absolute Maximum Ratings

V+ to V- 44V
GND to V- 25V
Digital Inputs, (Note 1) . . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current, S or D (Note 1) . . . . . ±30mA
Peak Current, S or D (Note 1) . . . . . ±100mA
Storage Temperature Range (A Suffix) . . . . . -65^oC to $+150^oC$
Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Thermal Information

Thermal Resistance (Max, Note 3)	θ_{JA}	θ_{JC}
CerDIP Package	$85^oC/W$	$25^oC/W$

Junction Temperature . . . . . $+175^oC$
Operating Temperature (A Suffix) . . . . . -55^oC to $+125^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . ±20V Max
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Input Low Voltage . . . . . 0.8V Max
Input High Voltage . . . . . 2.4V Min
Input Rise and Fall Time 20ns

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $-55^oC \le T_A \le +125^oC$, V+ = +15V, V- = -15V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
Drain-to-Source ON Resistance DG441/883	$R_{DS(ON)}$	V_{IN} = 0.8V	V+ = +13.5V, V- = -13.5V, I_S = -10mA, V_D = ±8.5V	1, 3	$+25^oC$, -55^oC	-	85	Ω
				2	$+125^oC$	-	100	Ω
DG442/883		V_{IN} = 2.4V	V+ = +13.5V, V- = -13.5V, I_S = -10mA, V_D = ±8.5V	1, 3	$+25^oC$, -55^oC	-	85	Ω
				2	$+125^oC$	-	100	Ω
DG441/883		V_{IN} = 0.8V	V+ = +10.8V, V- = 0V, I_S = -10mA, V_D = 3.0V	1, 3	$+25^oC$, -55^oC	-	160	Ω
				2	$+125^oC$	-	200	Ω
			V+ = +10.8V, V- = 0V, I_S = -10mA, V_D = 8.0V	1, 3	$+25^oC$, -55^oC	-	160	Ω
				2	$+125^oC$	-	200	Ω
DG442/883		V_{IN} = 2.4V	V+ = +10.8V, V- = 0V, I_S = -10mA, V_D = 3.0V	1, 3	$+25^oC$, -55^oC	-	160	Ω
				2	$+125^oC$	-	200	Ω
			V+ = +10.8V, V- = 0V, I_S = -10mA, V_D = 8.0V	1, 3	$+25^oC$, -55^oC	-	160	Ω
				2	$+125^oC$	-	200	Ω
Source OFF Leakage Current DG441/883	$I_{S(OFF)}$	V_{IN} = 2.4V	V+ = +16.5V, V- = -16.5V, V_S = ∓15.5V, V_D = ±15.5V	1	$+25^oC$	-0.5	0.5	nA
				2, 3	$+125^oC$, -55^oC	-20	20	nA
DG442/883		V_{IN} = 0.8V	V+ = +16.5V, V- = -16.5V, V_S = ∓15.5V, V_D = ±15.5V	1	$+25^oC$	-0.5	0.5	nA
				2, 3	$+125^oC$, -55^oC	-20	20	nA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $-55^oC \le T_A \le +125^oC$, V+ = +15V, V- = -15V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
Drain OFF Leakage Current	$I_{D(OFF)}$	V_{IN} = 2.4V	V+ = +16.5V, V- = -16.5V, $V_S = \mp 15.5V$, $V_D = \pm 15.5V$	1	$+25^oC$	-0.5	0.5	nA
DG441/883				2, 3	$+125^oC$, -55^oC	-20	20	nA
DG442/883		V_{IN} = 0.8V	V+ = +16.5V, V- = -16.5V, $V_S = \mp 15.5V$, $V_D = \pm 15.5V$	1	$+25^oC$	-0.5	0.5	nA
				2, 3	$+125^oC$, -55^oC	-20	20	nA
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	V_{IN} = 0.8V	V+ = +16.5V, V- = -16.5V, $V_S = V_D = \pm 15.5V$	1	$+25^oC$	-0.5	0.5	nA
DG441/883				2, 3	$+125^oC$, -55^oC	-40	40	nA
DG442/883		V_{IN} = 2.4V	V+ = +16.5V, V- = -16.5V, $V_S = V_D = \pm 15.5V$	1	$+25^oC$	-0.5	0.5	nA
				2, 3	$+125^oC$, -55^oC	-40	40	nA
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-0.5	0.5	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-0.5	0.5	µA
Positive Supply Current	I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	mA
		V+ = 16.5V, V- = -16.5V, V_{IN} = 5V				-	0.1	mA
		V+ = 13.2V, V- = 0V, V_{IN} = 0V				-	0.1	mA
		V+ = 13.2V, V- = 0V, V_{IN} = 5V				-	0.1	mA
Negative Supply Current	I-	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V		1, 3	$+25^oC$, -55^oC	-1.0	-	µA
				2	$+125^oC$	-100	-	µA
		V+ = 16.5V, V- = -16.5V, V_{IN} = 5V		1, 3	$+25^oC$, -55^oC	-1.0	-	µA
				2	$+125^oC$	-100	-	µA
		V+ = 13.2V, V- = 0V, V_{IN} = 0V		1, 3	$+25^oC$, -55^oC	-1.0	-	µA
				2	$+125^oC$	-100	-	µA
		V+ = 13.2V, V- = 0V, V_{IN} = 5V		1, 3	$+25^oC$, -55^oC	-1.0	-	µA
				2	$+125^oC$	-100	-	µA
Ground Current	I_{GND}	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-100	-	µA
		V+ = 16.5V, V- = -16.5V, V_{IN} = 5V				-100	-	µA
		V+ = 13.2V, V- = 0V, V_{IN} = 0V				-100	-	µA
		V+ = 13.2V, V- = 0V, V_{IN} = 5V				-100	-	µA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $-55^oC \leq T_A \leq +125^oC$, V+ = +15V, V- = -15V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn ON Time	t_{ON}						
DG441		C_L = 35pF, V_S = ±10V, R_L = 1kΩ	9	+25°C	-	250	ns
DG442					-	315	ns
DG441		C_L = 35pF, V_S = ±10V, R_L = 1kΩ	10, 11	+125°C, -55°C	-	300	ns
DG442					-	400	ns
DG441		V+ = 12V, V- = 0V, C_L = 35pF, V_S = 8.0V, R_L = 1kΩ	9	+25°C	-	400	ns
DG442					-	450	ns
DG441		V+ = 12V, V- = 0V, C_L = 35pF, V_S = 8.0V, R_L = 1kΩ	10, 11	+125°C, -55°C	-	600	ns
DG442					-	675	ns
Turn OFF Time	t_{OFF}						
DG441		C_L = 35pF, V_S = ±10V, R_L = 1kΩ	9	+25°C	-	120	ns
DG442					-	210	ns
DG441		C_L = 35pF, V_S = ±10V, R_L = 1kΩ	10, 11	+125°C, -55°C	-	150	ns
DG442					-	250	ns
DG441, DG442		V+ = 12V, V- = 0V, C_L = 35pF, V_S = 8.0V, R_L = 1kΩ	9, 10, 11	+25°C, +125°C, -55°C	-	200	ns

NOTES:

1. All leads soldered to PC Board.
2. Room: +25°C. Cold: A suffix -55°C, D suffix -40°C. Hot: A suffix +125°C, D suffix +85°C.
3. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor production tested.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 3 Intentionally Left Blank.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:
2760µm x 1780µm x 485 ± 25µm

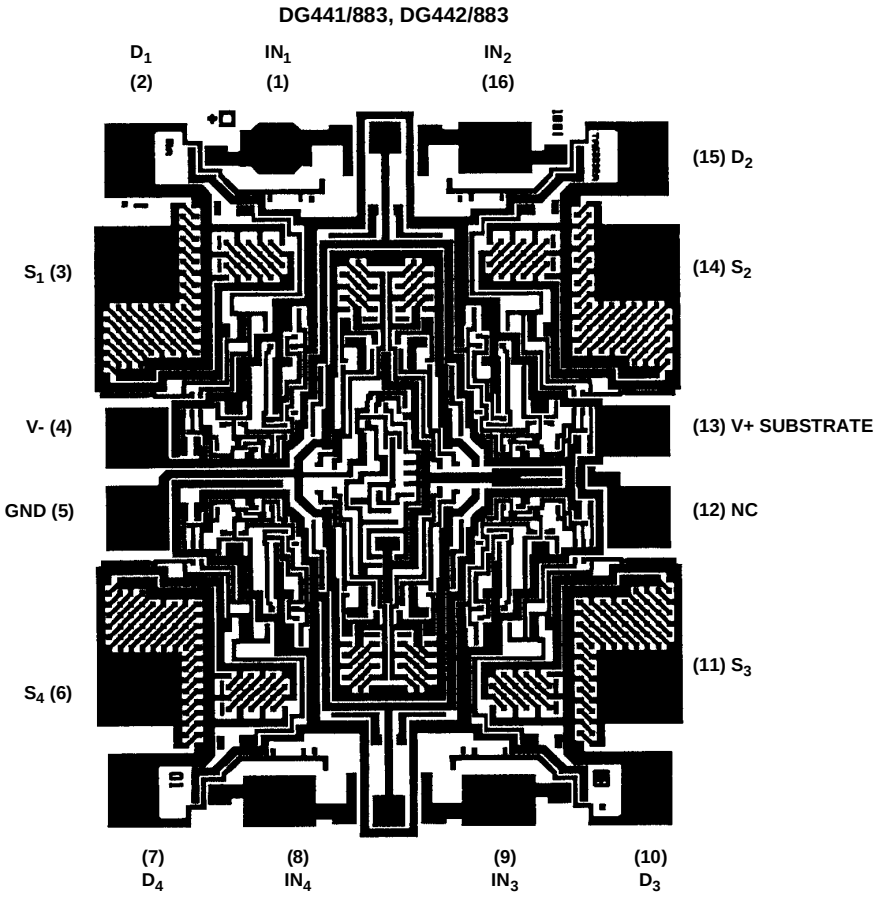
METALLIZATION:
Type: SiAl
Thickness: 12kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
1.5 x 10^5A/cm^2

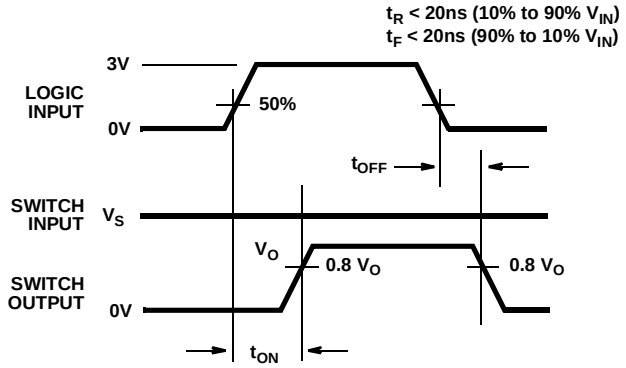
Metallization Mask Layout

DG441/883, DG442/883



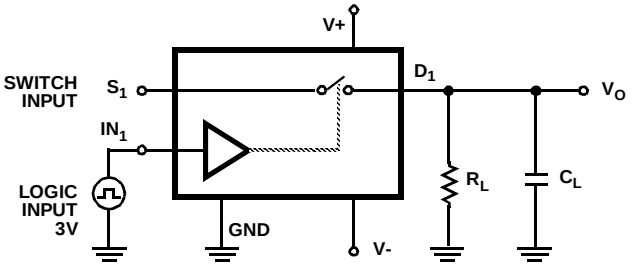
Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A.



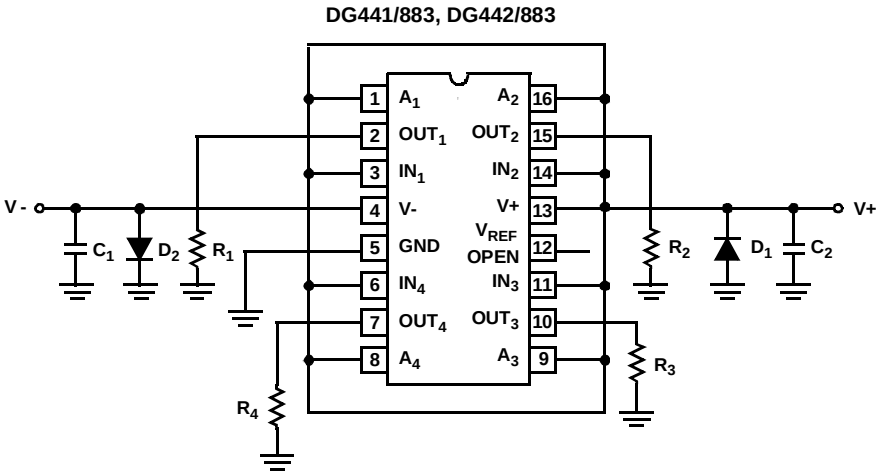
Repeat test for Channels 2, 3 and 4.
For load conditions, see Specifications C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

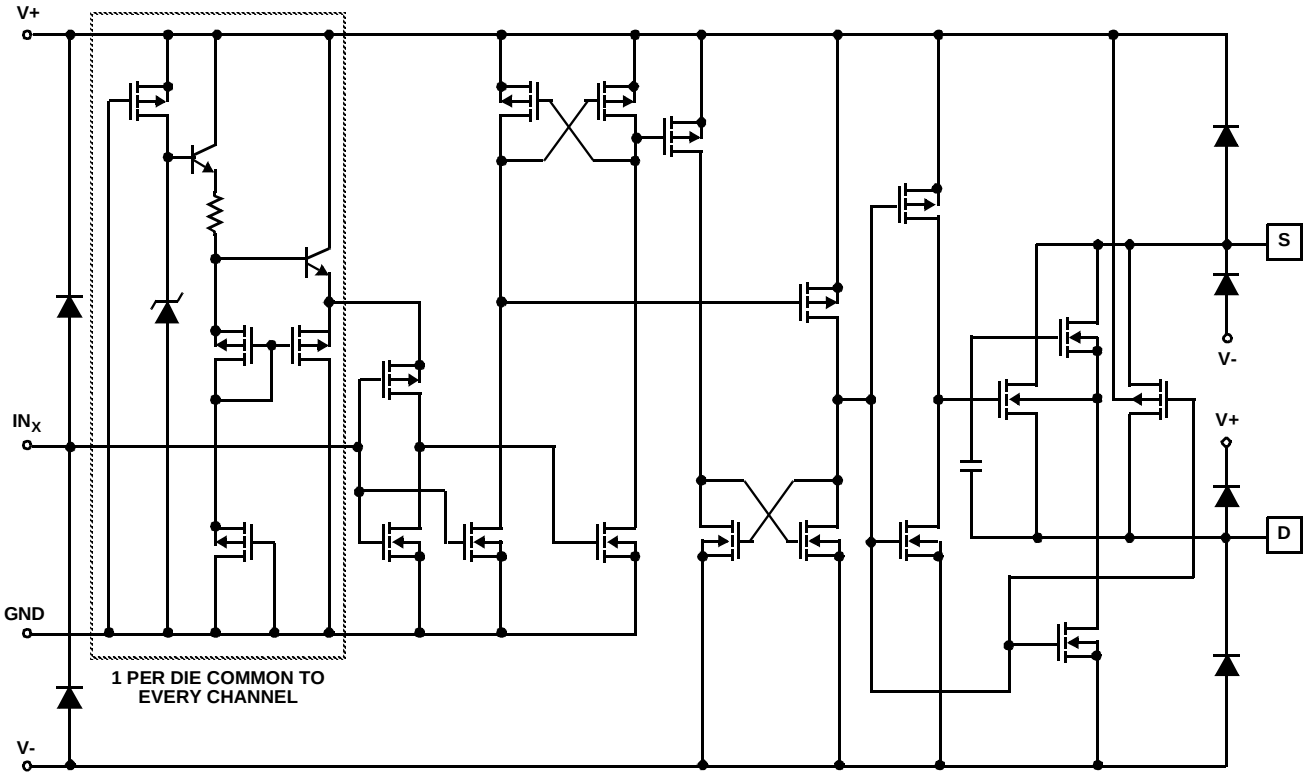
FIGURE 1B.

FIGURE 1. SWITCHING TIME

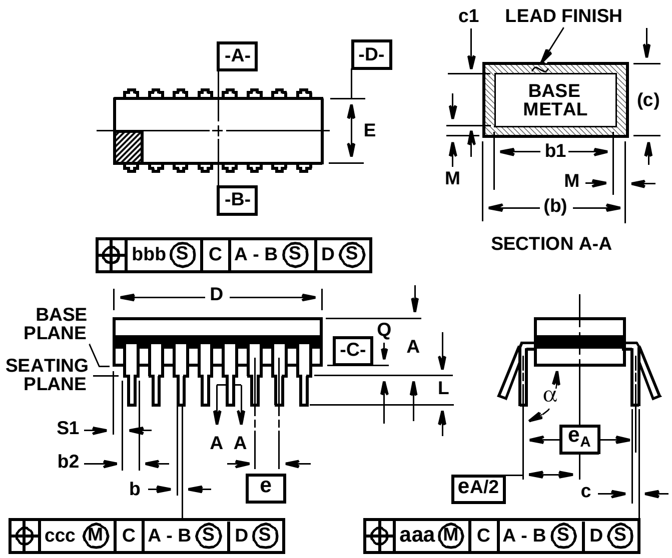
Burn-In Circuit



Schematic Diagram (One Channel)



Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



F16.3 **MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)**
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

DG441, DG442

DESIGN INFORMATION

June 1994

Monolithic Quad SPST CMOS Analog Switches

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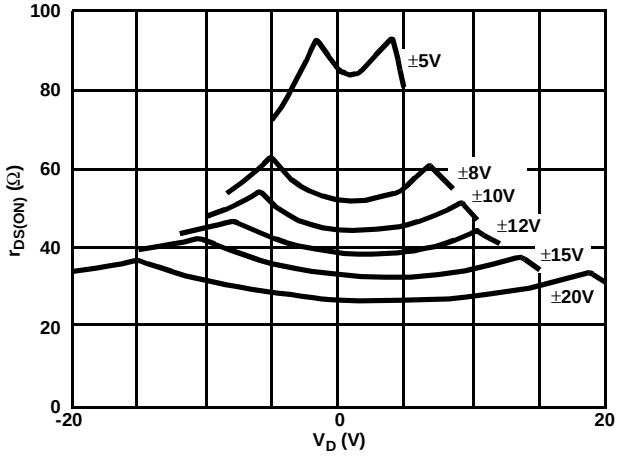
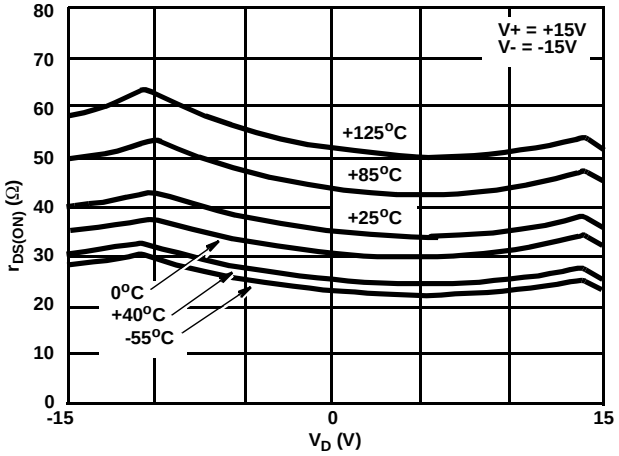
Typical Performance Curves

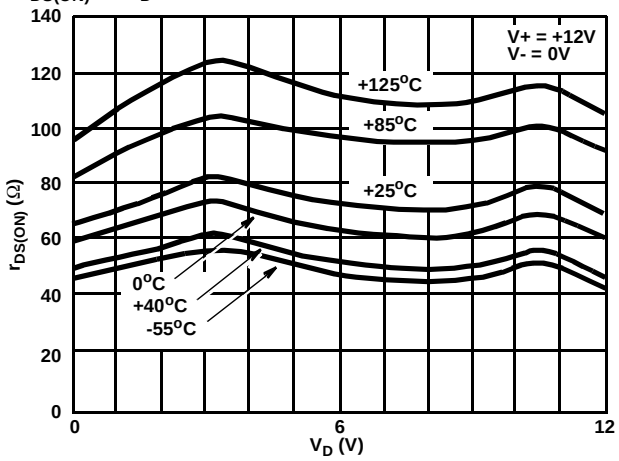
$R_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE



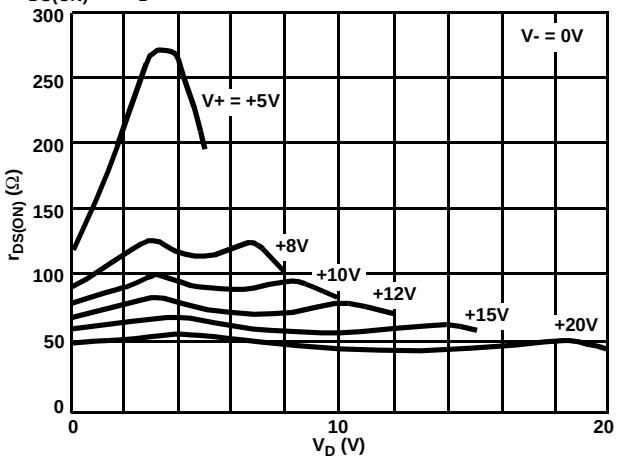
$R_{DS(ON)}$ vs V_D AND TEMPERATURE



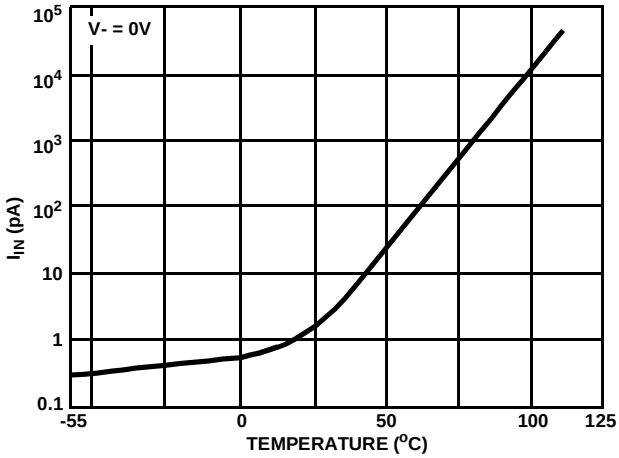
$R_{DS(ON)}$ vs V_D AND TEMPERATURE (SINGLE 12V SUPPLY)



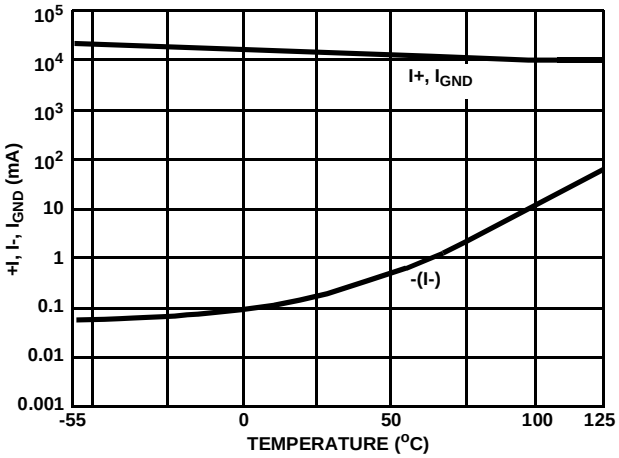
$R_{DS(ON)}$ vs V_D AND UNIPOLAR POWER SUPPLY VOLTAGE



INPUT CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



DESIGN INFORMATION (Continued)

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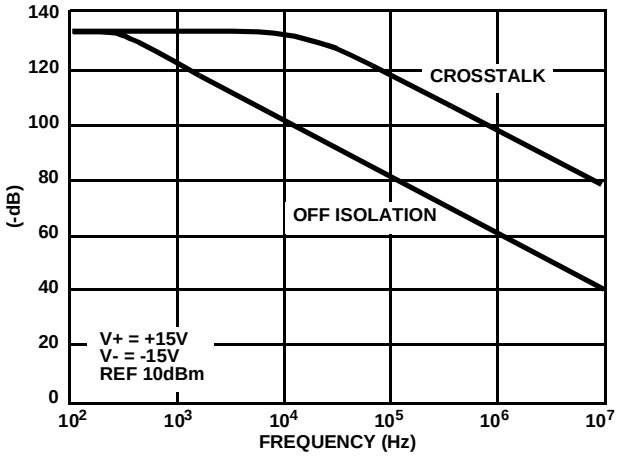
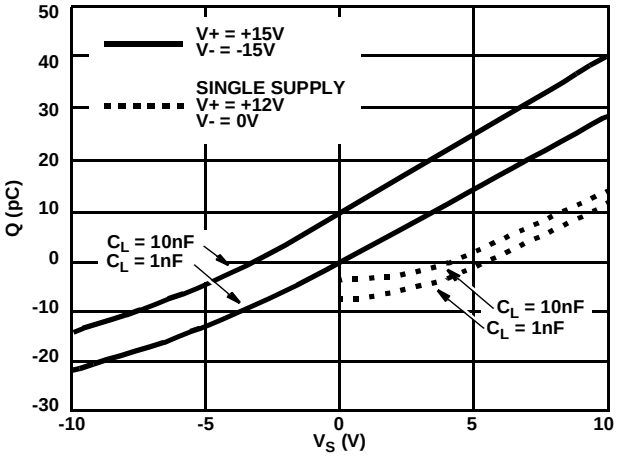
Typical Performance Curves (Continued)

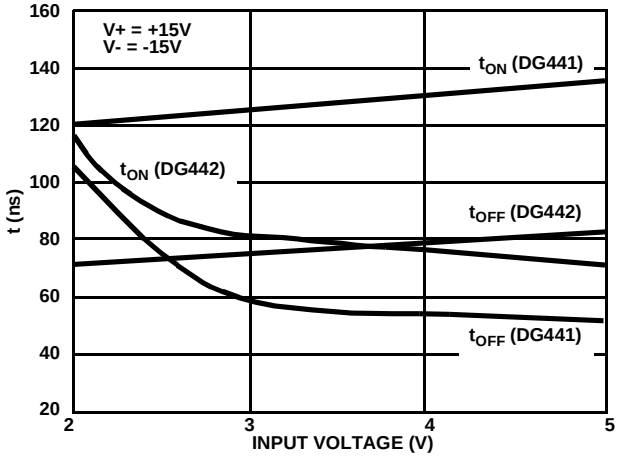
CROSSTALK AND OFF ISOLATION vs FREQUENCY



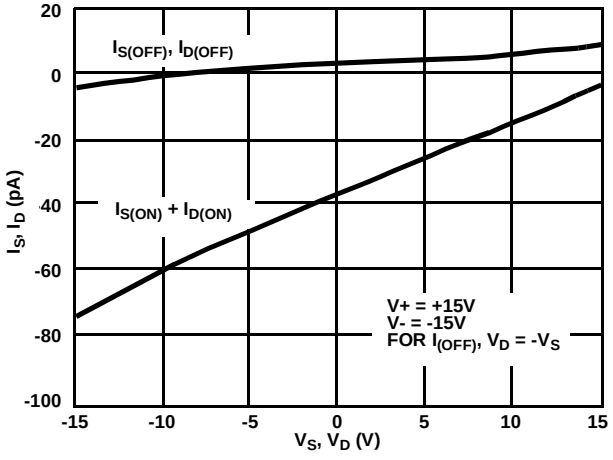
CHARGE INJECTION vs SOURCE VOLTAGE



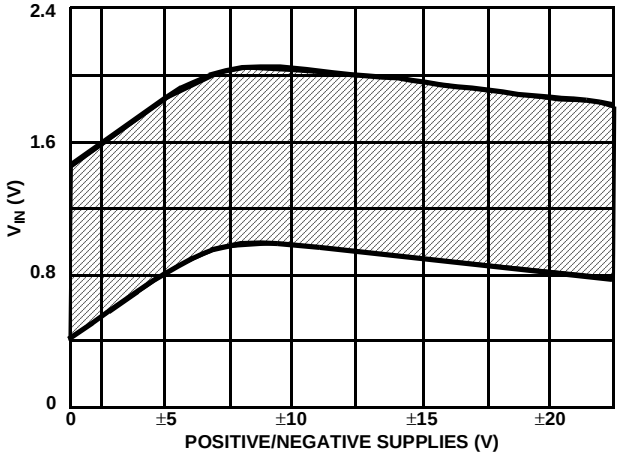
SWITCHING TIMES vs INPUT VOLTAGE



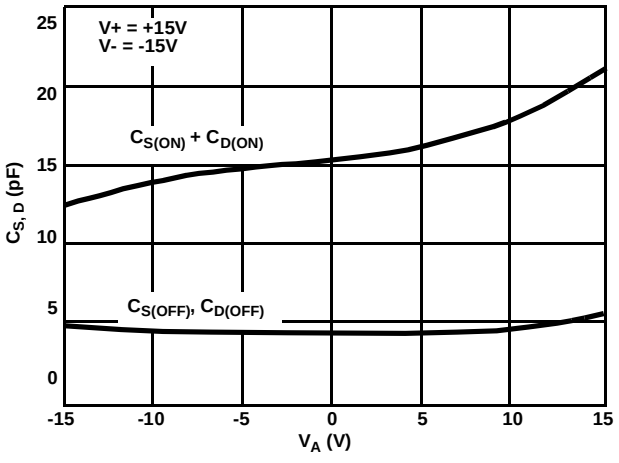
SOURCE/DRAIN LEAKAGE CURRENTS



SWITCHING THRESHOLD vs SUPPLY VOLTAGE



SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

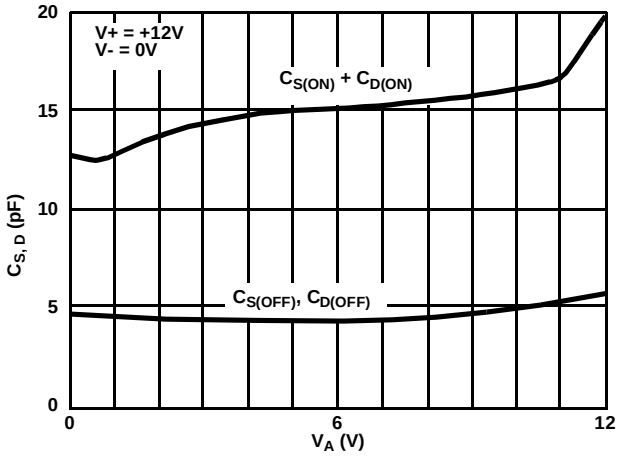


DESIGN INFORMATION (Continued)

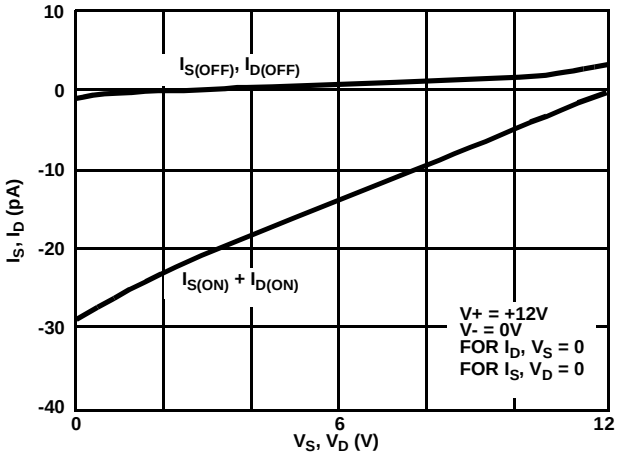
The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves (Continued)

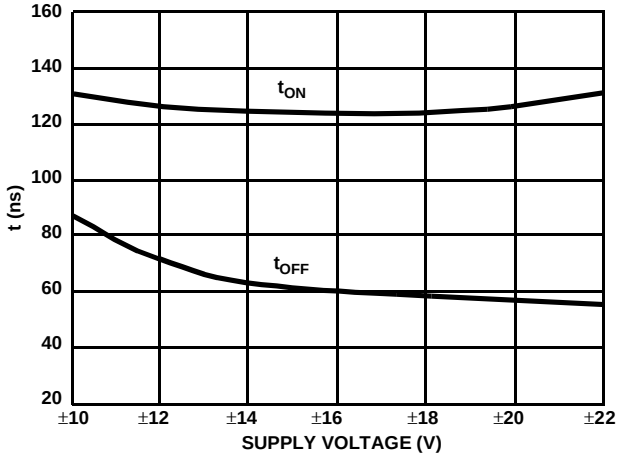
SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)



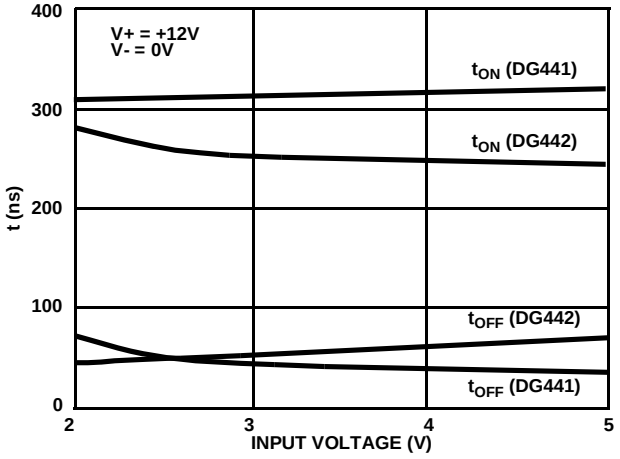
SOURCE/DRAIN LEAKAGE CURRENTS (SINGLE 12V SUPPLY)



SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG441)



SWITCHING TIMES vs INPUT VOLTAGE



SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG441)