CMOS Single Supply Rail-to-Rail Input/Output Operational Amplifiers with Shutdown

AD8591/AD8592/AD8594

FEATURES

Single Supply Operation: +2.5 V to +6 V
High Output Current: ±250 mA
Extremely Low Shutdown Supply Current: 100 nA
Low Supply Current: 750 µA/Amp
Wide Bandwidth: 3 MHz
Slew Rate: 5 V/µs
No Phase Reversal
Very Low Input Bias Current
High Impedance Outputs When in Shutdown Mode
Unity Gain Stable

APPLICATIONS

Mobile Communication Handset Audio
PC Audio
PCMCIA/Modem Line Driving
Battery Powered Instrumentation
Data Acquisition
ASIC Input or Output Amplifier
LCD Display Reference Level Driver

GENERAL DESCRIPTION

The AD8591, AD8592 and AD8594 are single, dual and quad rail-to-rail input and output single supply amplifiers featuring 250 mA output drive current and a power saving shutdown mode. The AD8592 includes an independent shutdown function for each amplifier. When both amplifiers are in shutdown mode the total supply current is reduced to less than 1 µA. The AD8591 and AD8594 include a single master shutdown function that reduces total supply current to less than 1 µA. All amplifier outputs are in a high impedance state when in shutdown mode.

These amplifiers have very low input bias currents, making them suitable for integrators and diode amplification. Outputs are stable with virtually any capacitive load. Supply current is less than 750 µA per amplifier in active mode.

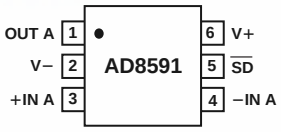
Applications for these amplifiers include audio amplification for portable computers, portable phone headsets, sound ports, sound cards and set-top boxes. The AD859x family is capable of driving heavy capacitive loads such as LCD panel reference levels.

The ability to swing rail-to-rail at both the input and output enables designers to buffer CMOS DACs, ASICs and other wide output swing devices in single supply systems.

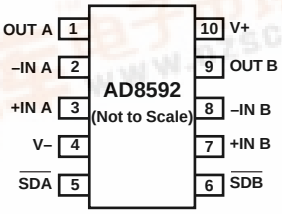
The AD8591, AD8592 and AD8594 are specified over the industrial (–40°C to +85°C) temperature range. The AD8591, single, is available in the tiny 6-lead SOT package. The AD8592, dual, is available in the 10-lead µSOIC surface mount package. The AD8594, quad, is available in 16-lead narrow SOIC and 16-lead TSSOP packages.

PIN CONFIGURATIONS

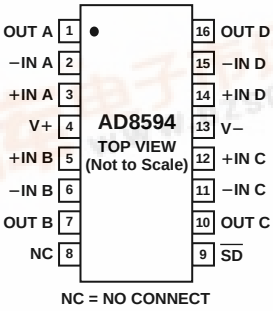
6-Lead SOT
(RT Suffix)



10-Lead µSOIC
(RM Suffix)

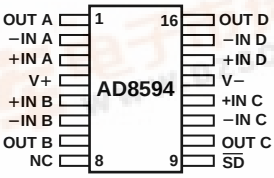


16-Lead Narrow SOIC
(R Suffix)



NC = NO CONNECT

16-Lead TSSOP
(RU Suffix)



NC = NO CONNECT

REV. A

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Tel: 781/329-4700 World Wide Web Site: http://www.analog.com

AD8591/AD8592/AD8594–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = +2.7 V, V_{CM} = +1.35 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				25	mV
		–40°C < T_A < +85°C			30	mV
Input Bias Current	I_B			5	50	pA
		–40°C < T_A < +85°C			60	pA
Input Offset Current	I_{OS}			1	25	pA
		–40°C < T_A < +85°C			30	pA
Input Voltage Range			0		+2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to +2.7 V	38	45		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ , V_O = +0.3 V to +2.4 V		25		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			20		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			50		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA	+2.55	+2.61		V
		–40°C to +85°C	+2.5			V
Output Voltage Low	V_{OL}	I_L = 10 mA		60	100	mV
		–40°C to +85°C			125	mV
Output Current	I_{OUT}			±250		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		60		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.5 V to +6 V	45	55		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V			1	mA
		–40°C < T_A < +85°C			1.25	mA
Supply Current Shutdown Mode	I_{SD}	All Amplifiers Shut Down		0.1	1	µA
		–40°C < T_A < +85°C			1	µA
	I_{SD1}	Amplifier 1 Shut Down (AD8592)			1.4	mA
	I_{SD2}	Amplifier 2 Shut Down (AD8592)			1.4	mA
SHUTDOWN INPUTS						
Logic High Voltage	V_{INH}	–40°C < T_A < +85°C	+1.6			V
Logic Low Voltage	V_{INL}	–40°C < T_A < +85°C			+0.5	V
Logic Input Current	I_{IN}	–40°C < T_A < +85°C			1	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		3.5		V/µs
Settling Time	t_S	To 0.01%		1.4		µs
Gain Bandwidth Product	GBP			2.2		MHz
Phase Margin	Φo			67		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		65		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		45		nV/$\sqrt{\text{Hz}}$
		f = 10 kHz		30		nV/$\sqrt{\text{Hz}}$
Current Noise Density	i_n	f = 1 kHz		0.05		pA/$\sqrt{\text{Hz}}$

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = +5.0 V, V_{CM} = +2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2	25	mV
		–40°C < T_A < +85°C			30	mV
Input Bias Current	I_B			5	50	pA
		–40°C < T_A < +85°C			60	pA
Input Offset Current	I_{OS}			1	25	pA
		–40°C < T_A < +85°C			30	pA
Input Voltage Range			0		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to +5 V	38	47		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ , V_O = +0.5 V to +4.5 V	15	30		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +85°C		20		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			50		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA	+4.9	+4.94		V
		–40°C to +85°C	+4.85			V
Output Voltage Low	V_{OL}	I_L = 10 mA		50	100	mV
		–40°C to +85°C			125	mV
Output Current	I_{OUT}			±250		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		40		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.5 V to +6 V	45	55		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V			1.25	mA
		–40°C < T_A < +85°C			1.75	mA
Supply Current-Shutdown Mode	I_{SD}	All Amplifiers Shut Down		0.1	1	µA
		–40°C < T_A < +85°C			1	µA
	I_{SD1}	Amplifier 1 Shut Down (AD8592)			1.6	mA
	I_{SD2}	Amplifier 2 Shut Down (AD8592)			1.6	mA
SHUTDOWN INPUTS						
Logic High Voltage	V_{INH}	–40°C < T_A < +85°C	+2.4			V
Logic Low Voltage	V_{INL}	–40°C < T_A < +85°C			+0.8	V
Logic Input Current	I_{IN}	–40°C < T_A < +85°C			1	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		5		V/µs
Full-Power Bandwidth	BW_P	1% Distortion		325		kHz
Settling Time	t_S	To 0.01%		1.6		µs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	Φo			70		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 10 kΩ		65		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
		f = 10 kHz		30		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +6 V
Input Voltage . . . . . GND to V_S
Differential Input Voltage . . . . . ±6 V
Output Short Circuit
Duration to GND[2] . . . . . Observe Derating Curves
Storage Temperature Range
R, RT, RM, RU Packages . . . . . –65°C to +150°C
Operating Temperature Range
AD8591/AD8592/AD8594 . . . . . –40°C to +85°C
Junction Temperature Range
R, RT, RM, RU Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supplies less than ±5 V the differential input voltage is limited to the supplies.

Package Type	θ_{JA}[1]	θ_{JC}	Units
6-Lead SOT-23 (RT)	230	92	°C/W
10-Lead μSOIC (RM)	200	44	°C/W
16-Lead SOIC (R)	120	36	°C/W
16-Lead TSSOP (RU)	180	35	°C/W

NOTE
[1]θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device in socket for surface mount packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8591ART	–40°C to +85°C	6-Lead SOT-23	RT-6
AD8592ARM	–40°C to +85°C	10-Lead μSOIC	RM-10
AD8594AR	–40°C to +85°C	16-Lead SOIC	R-16A
AD8594ARU	–40°C to +85°C	16-Lead TSSOP	RU-16

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8591/AD8592/AD8594 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Performance Characteristics

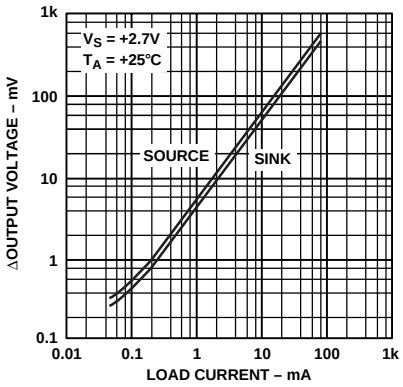


Figure 1. Output Voltage to Supply Rail vs. Load Current

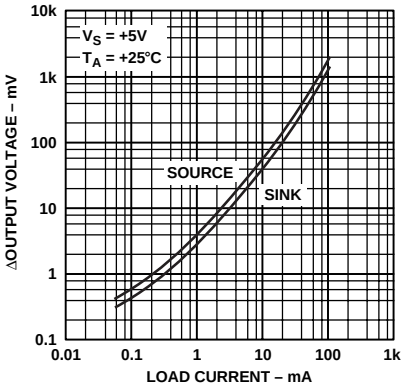


Figure 2. Output Voltage to Supply Rail vs. Load Current

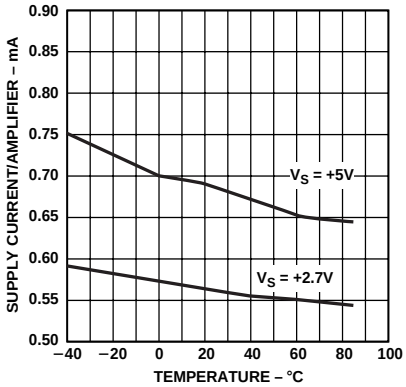


Figure 3. Supply Current per Amplifier vs. Temperature

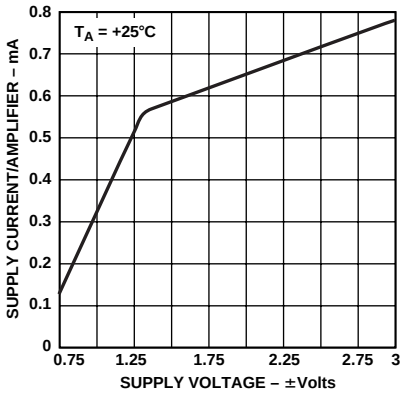


Figure 4. Supply Current per Amplifier vs. Supply Voltage

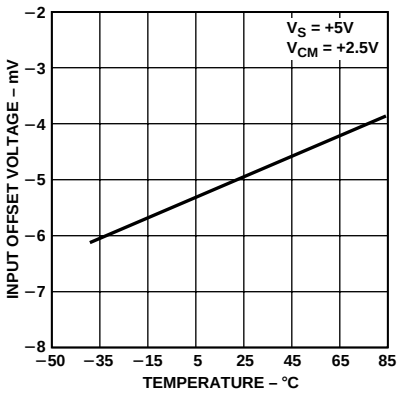


Figure 5. Input Offset Voltage vs. Temperature

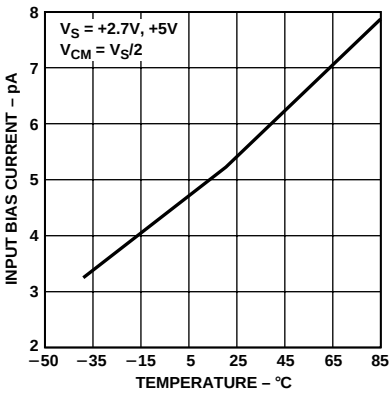


Figure 6. Input Bias Current vs. Temperature

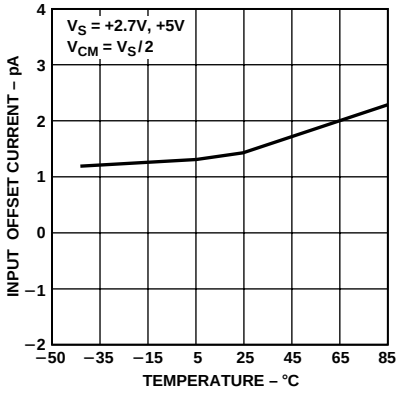


Figure 7. Input Offset Current vs. Temperature

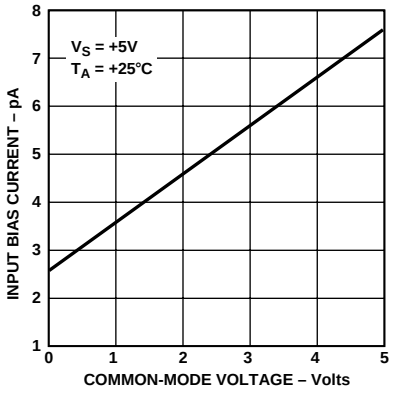


Figure 8. Input Bias Current vs. Common-Mode Voltage

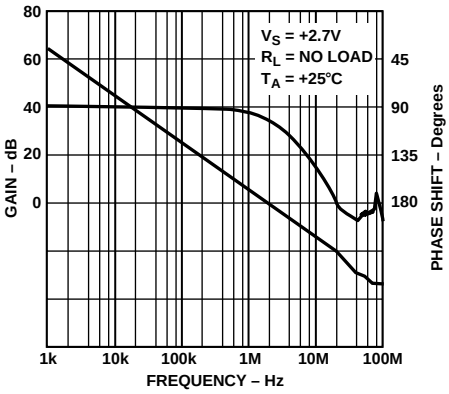


Figure 9. Open-Loop Gain and Phase vs. Frequency

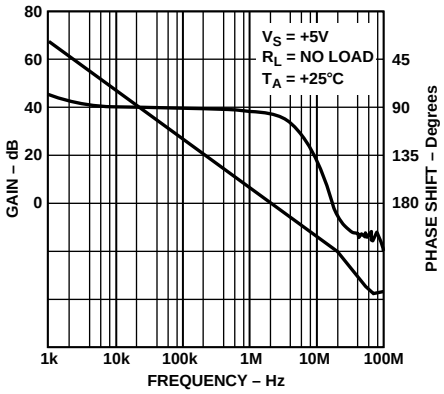


Figure 10. Open-Loop Gain and Phase vs. Frequency

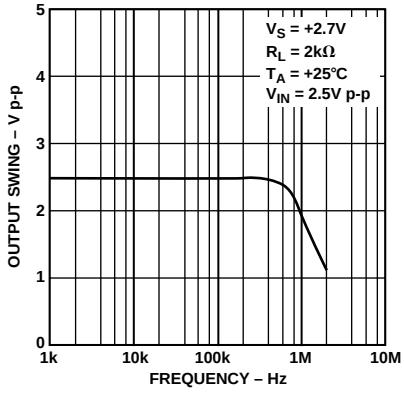


Figure 11. Closed-Loop Output Voltage Swing vs. Frequency

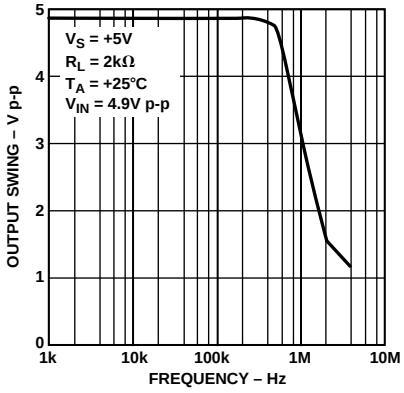


Figure 12. Closed-Loop Output Voltage Swing vs. Frequency

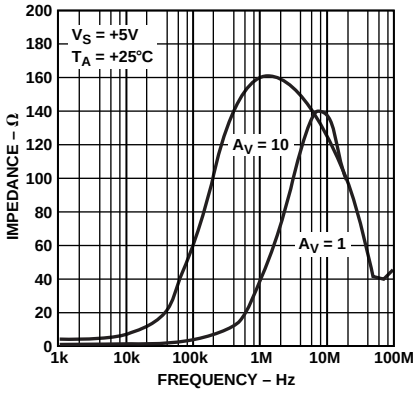


Figure 13. Closed-Loop Output Impedance vs. Frequency

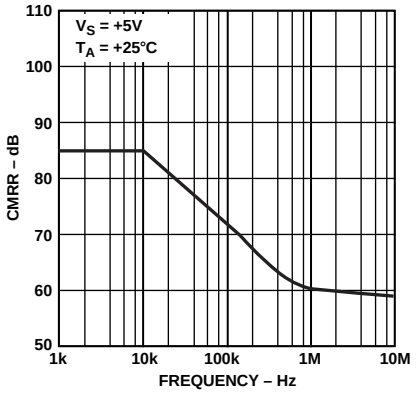


Figure 14. Common-Mode Rejection Ratio vs. Frequency

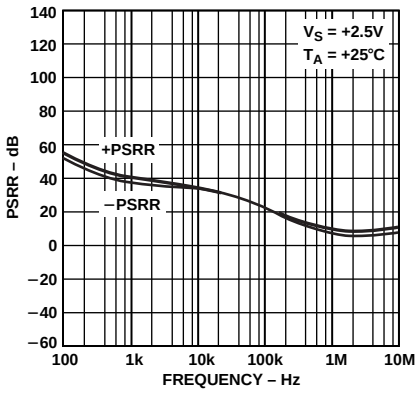


Figure 15. Power Supply Rejection Ratio vs. Frequency

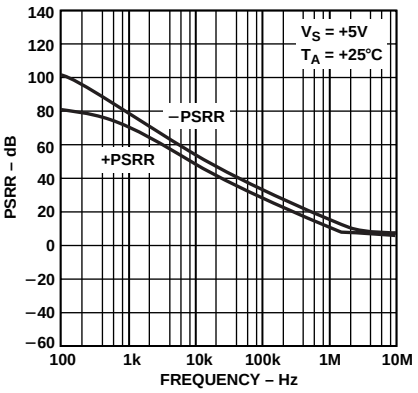


Figure 16. Power Supply Rejection Ratio vs. Frequency

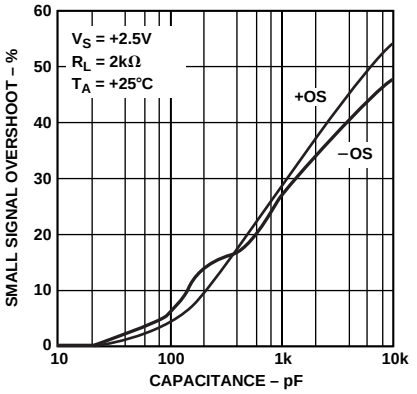


Figure 17. Small Signal Overshoot vs. Load Capacitance

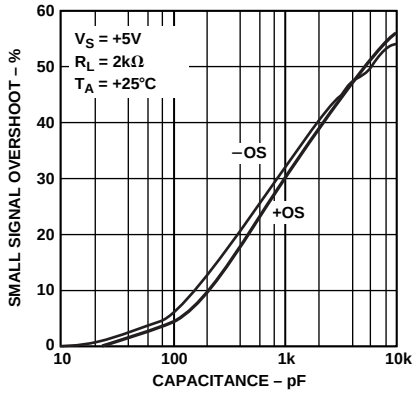


Figure 18. Small Signal Overshoot vs. Load Capacitance

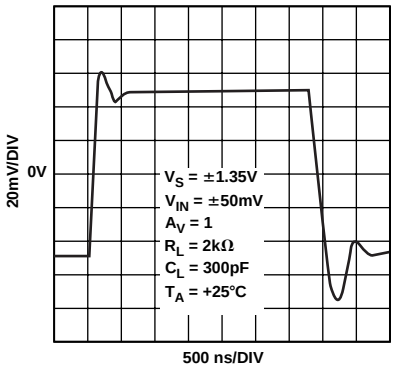


Figure 19. Small Signal Transient Response

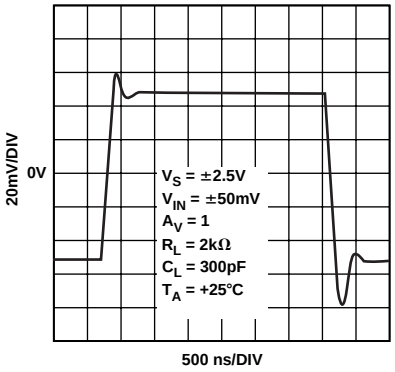


Figure 20. Small Signal Transient Response

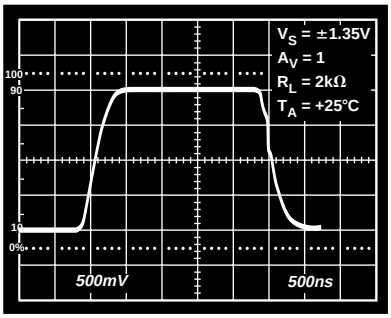


Figure 21. Large Signal Transient Response

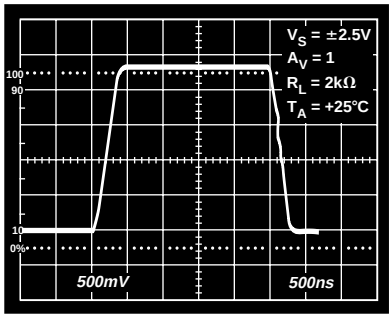


Figure 22. Large Signal Transient Response

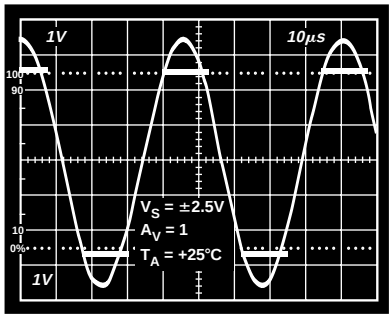


Figure 23. No Phase Reversal

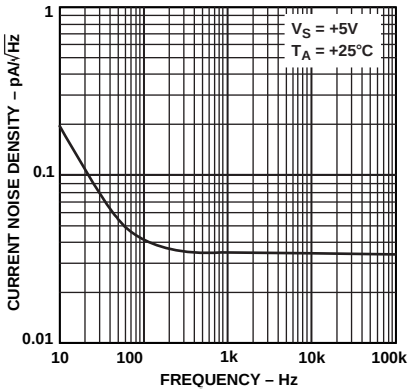


Figure 24. Current Noise Density vs. Frequency

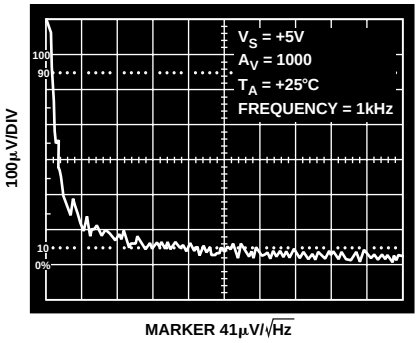


Figure 25. Voltage Noise Density vs. Frequency

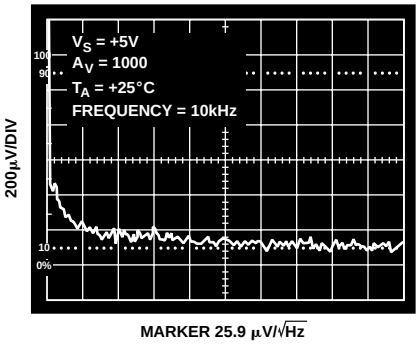


Figure 26. Voltage Noise Density vs. Frequency

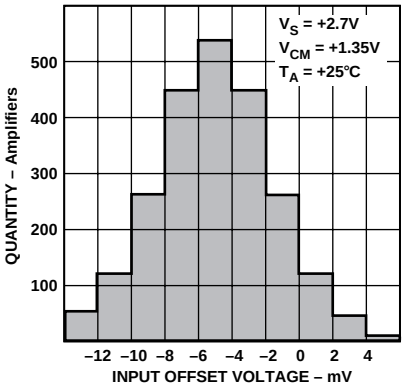


Figure 27. Input Offset Voltage Distribution

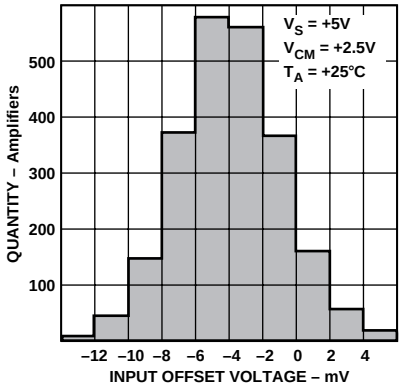


Figure 28. Input Offset Voltage Distribution

AD8591/AD8592/AD8594 APPLICATION SECTION

Theory of Operation

The AD859x family of amplifiers are all CMOS, high output drive, rail-to-rail input and output single supply amplifiers designed for low cost and high output current drive. The parts include a power saving shutdown function making the AD8591/AD8592/AD8594 op amps ideal for portable multimedia and telecom applications.

Figure 29 shows the simplified schematic for an AD8591/AD8592/AD8594 amplifier. Two input differential pairs, consisting of an n-channel pair (M1-M2) and a p-channel pair (M3-M4), provide a rail-to-rail input common-mode range. The outputs of the input differential pairs are combined in a compound folded-cascode stage, which drives the input to a second differential pair gain stage. The outputs of the second gain stage provide the gate voltage drive to the rail-to-rail output stage.

The rail-to-rail output stage consists of M15 and M16, which are configured in a complementary common-source configuration. As with any rail-to-rail output amplifier, the gain of the output stage, and thus the open-loop gain of the amplifier, is dependent on the load resistance. Also, the maximum output voltage swing is directly proportional to the load current. The difference between the maximum output voltage to the supply rails, known as the dropout voltage, is determined by the AD8591/AD8592/AD8594 output transistors' on-channel resistance. The output dropout voltage is given in Figure 1 and Figure 2.

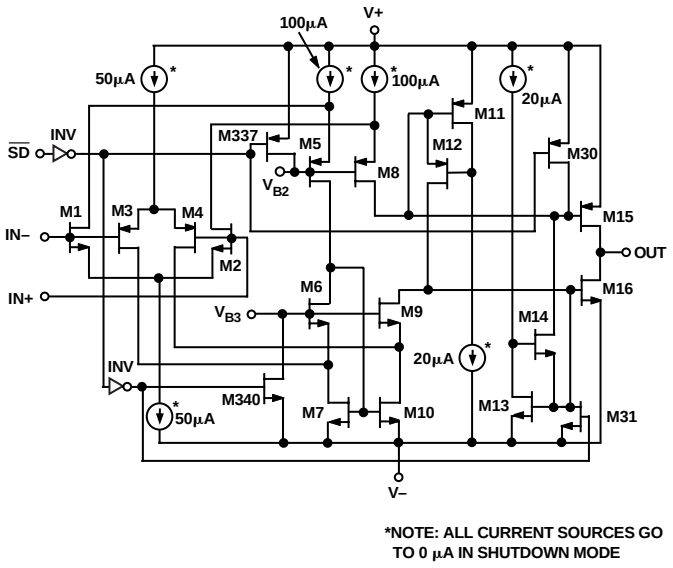


Figure 29. AD8591/AD8592/AD8594 Simplified Schematic

Input Voltage Protection

Although not shown on the simplified schematic, ESD protection diodes are connected from each input to each power supply rail. These diodes are normally reverse biased, but will turn on if either input voltage exceeds either supply rail by more than +0.6 V. Should this condition occur, the input current should be limited to less than ±5 mA. This can be done by placing a resistor in series with the input(s). The minimum resistor value should be:

$$R_{IN} \geq \frac{V_{IN,MAX}}{5\ mA} \quad (1)$$

Output Phase Reversal

The AD8591/AD8592/AD8594 are immune to output voltage phase reversal with an input voltage within the supply voltages of the device. However, if either of the device's inputs exceeds +0.6 V outside of the supply rails, the output could exhibit phase reversal. This is due to the ESD protection diodes becoming forward biased, thus causing the polarity of the input terminals of the device to switch.

The technique recommended in the Input Overvoltage Protection section should be applied in applications where the possibility of input voltages exceeding the supply voltages exists.

Output Short Circuit Protection

To achieve high output current drive and rail-to-rail performance, the outputs of the AD859x family do not have internal short circuit protection circuitry. Although these amplifiers are designed to sink or source as much as 250 mA of output current, shorting the output directly to the positive supply could damage or destroy the device. To protect the output stage, the maximum output current should be limited to ±250 mA.

By placing a resistor in series with the output of the amplifier as shown in Figure 30, the output current can be limited. The minimum value for R_X can be found from Equation 2.

$$R_X \geq \frac{V_{SY}}{250\ mA} \quad (2)$$

For a +5 V single supply application, R_X should be at least 20 Ω. Because R_X is inside the feedback loop, V_{OUT} is not affected. The tradeoff in using R_X is a slight reduction in output voltage swing under heavy output current loads. R_X will also increase the effective output impedance of the amplifier to $R_O + R_X$, where R_O is the output impedance of the device.

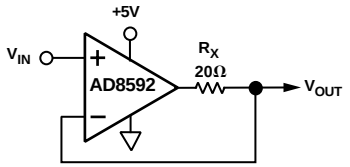


Figure 30. Output Short Circuit Protection

Power Dissipation

Although the AD859x family of amplifiers are able to provide load currents of up to 250 mA, proper attention should be given to not exceeding the maximum junction temperature for the device. The equation for finding the junction temperature is given as:

$$T_J = P_{DISS} \times \theta_{JA} + T_A \quad (3)$$

Where T_J = AD859x junction temperature
P_{DISS} = AD859x power dissipation
θ_{JA} = AD859x junction-to-ambient thermal resistance of the package; and
T_A = The ambient temperature of the circuit

In any application, the absolute maximum junction temperature must be limited to +150°C. If this junction temperature is exceeded, the device could suffer premature failure. If the output voltage and output current are in phase, for example, with a purely resistive load, the power dissipated by the AD859x can be found as:

$$P_{DISS} = I_{LOAD} \times \left(V_{SY} - V_{OUT}\right) \quad (4)$$

Where I_{LOAD} = AD859x output load current
V_{SY} = AD859x supply voltage; and
V_{OUT} = The output voltage

By calculating the power dissipation of the device and using the thermal resistance value for a given package type, the maximum allowable ambient temperature for an application can be found using Equation 3.

Capacitive Loading

The AD859x exhibits excellent capacitive load driving capabilities and can drive up to 10 nF directly. Although the device is stable with large capacitive loads, there is a decrease in amplifier bandwidth as the capacitive load increases. Figure 31 shows a graph of the AD8592 unity gain bandwidth under various capacitive loads.

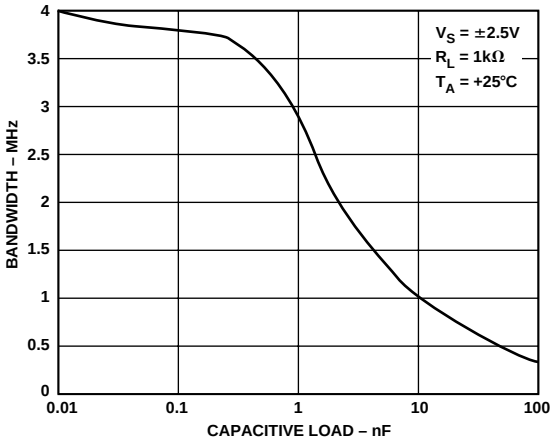


Figure 31. Unity Gain Bandwidth vs. Capacitive Load

When driving heavy capacitive loads directly from the AD859x output, a snubber network can be used to improve transient response. This network consists of a series R-C connected from the amplifier's output to ground, placing it in parallel with the capacitive load. The configuration is shown in Figure 32. Although this network will not increase the bandwidth of the amplifier, it will significantly reduce the amount of overshoot, as shown in Figure 33.

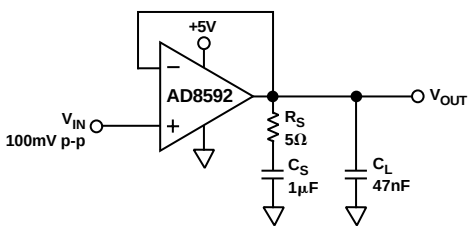


Figure 32. Configuration for Snubber Network to Compensate for Capacitive Loads

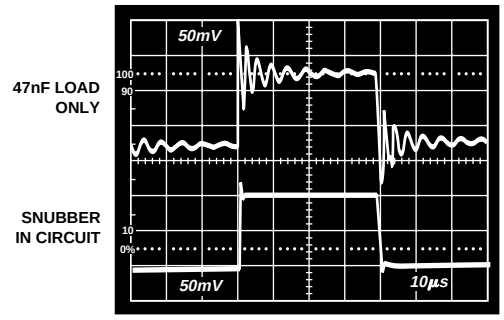


Figure 33. Snubber Network Reduces Overshoot and Ringing Caused from Driving Heavy Capacitive Loads

The optimum values for the snubber network should be determined empirically based on the size of the capacitive load. Table I shows a few sample snubber network values for a given load capacitance.

Table I. Snubber Networks for Large Capacitive Loads

Load Capacitance (C_L)	Snubber Network (R_S, C_S)
0.47 nF	300 Ω, 0.1 µF
4.7 nF	30 Ω, 1 µF
47 nF	5 Ω, 1 µF

A PC-98 Compliant Headphone/Speaker Amplifier

Because of its high output current performance and shutdown feature, the AD8592 makes an excellent amplifier for driving an audio output jack in a computer application. Figure 34 shows how the AD8592 can be interfaced with an AC97 codec to drive headphones or speakers.

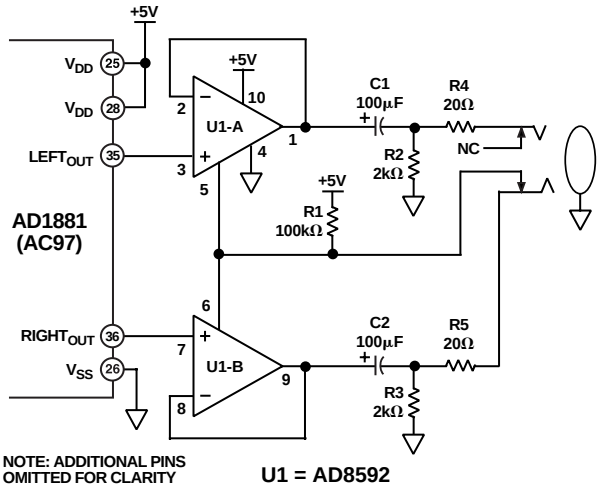


Figure 34. A PC-98 Compliant Headphone/Line Out Amplifier

When headphones are plugged into the jack, the normalizing contacts disconnect from the audio contacts. This allows the voltage to the AD8592 shutdown pins to be pulled up to +5 V, activating the amplifiers. With no plug in the output jack, the shutdown voltage is pulled to 100 mV through the R1 and R3 + R5 voltage divider. This powers the AD8592 down when it is not needed, saving current from the power supply or battery.

If gain is required from the output amplifier, four additional resistors should be added as shown in Figure 35. The gain of the AD8592 can be set as:

$$A_V = \frac{R7}{R6} \quad (5)$$

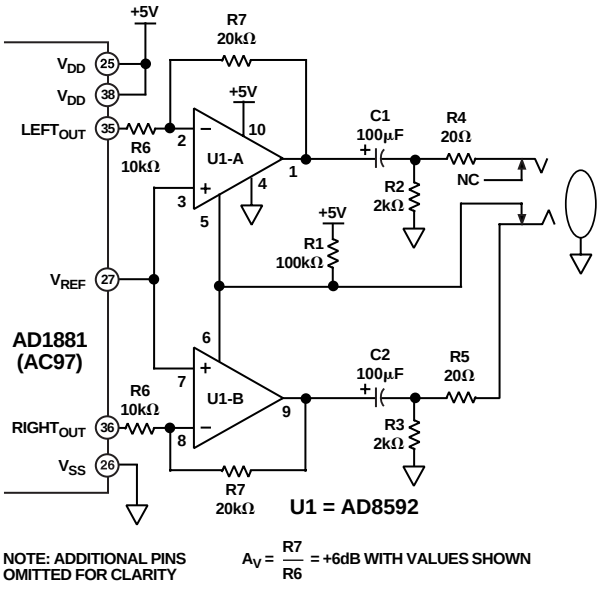


Figure 35. A PC-98 Compliant Headphone/Line Out Amplifier With Gain

Input coupling capacitors are not required for either circuit as the reference voltage is supplied from the AD1881.

R4 and R5 help protect the AD8592 output in case the output jack or headphone wires accidentally get shorted to ground. The output coupling capacitors C1 and C2 block dc current from the headphones and create a high-pass filter with a corner frequency of:

$$f_{-3\,dB} = \frac{1}{2\pi\ C1\left(R4 + R_L\right)} \quad (6)$$

Where R_L is the resistance of the headphones.

A Combined Microphone and Speaker Amplifier for Cellphone and Portable Headsets

The dual amplifiers in the AD8592 make an efficient design for interfacing with a headset containing a microphone and speaker. Figure 36 demonstrates a simple method for constructing an interface to a codec.

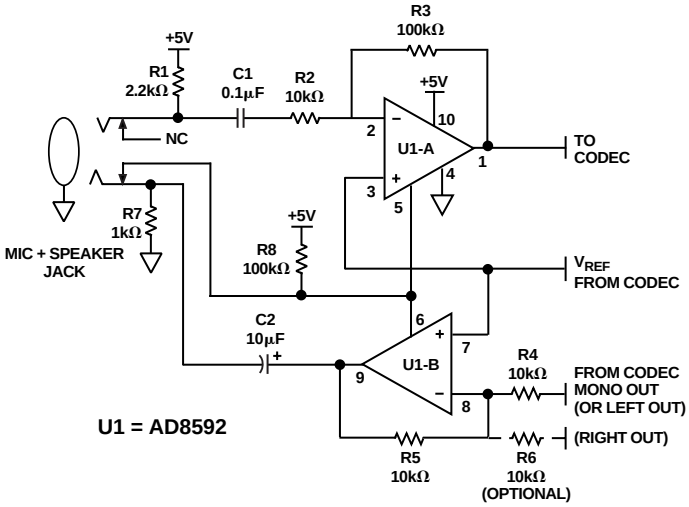


Figure 36. A Speaker/Mic Headset Amplifier Circuit

U1-A is used as a microphone preamplifier, where the gain of the preamplifier is set as R3/R2. R1 is used to bias an electret microphone and C1 blocks any dc voltages from the amplifier. U1-B is the speaker amplifier, and its gain is set at R5/R4. To sum a stereo output, R6 should be added, equal in value to R4.

Using the same principle as described in the previous section, the normalizing contact on the microphone/speaker jack can be used to put the AD8592 into shutdown when the headset is not plugged in. The AD8592 shutdown inputs can also be controlled with TTL or CMOS compatible logic, allowing microphone or speaker muting if desired.

An Inexpensive Sample-and-Hold Circuit

The independent shutdown control of each amplifier in the AD8592 allows a degree of flexibility in circuit design. One particular application for which this feature is useful is in designing a sample-and-hold circuit for data acquisition. Figure 37 shows a schematic of a simple, yet extremely effective sample-and-hold circuit using a single AD8592 and one capacitor.

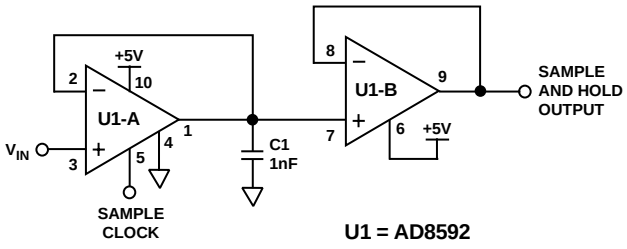


Figure 37. An Efficient Sample-and-Hold Circuit

The U1-A amplifier is configured as a unity gain buffer driving a 1 nF capacitor. The input signal is connected to the noninverting input, while the sample clock controls the shutdown for that amplifier. When the sample clock is high, the U1-A amplifier is active and the output follows V_{IN}. Once the sample clock goes low, U1-A shuts down with the output of the amplifier going to a high impedance state, holding the voltage on the C1 capacitor.

The U1-B amplifier is used as a unity gain buffer to prevent loading on C1. Because of the low input bias current of the U1-B CMOS input stage and the high impedance state of the U1-A output in shutdown, there is very little voltage droop from C1 during the Hold period. This circuit can be used with sample frequencies as high as 500 kHz and as low as below 1 Hz. Even lower voltage droop can be achieved for very low sample rates by increasing the value of C1.

Direct Access Arrangement for PCMCIA Modems (Telephone Line Interface)

Figure 38 illustrates a +5 V transmit/receive telephone line interface for 600 Ω systems. It allows full duplex transmission of signals on a transformer-coupled 600 Ω line in a differential manner. Amplifier A1 provides gain that can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured to apply the largest possible signal on a single supply to the transformer. Because of the AD8594's high output current drive and low dropout voltages, the largest signal available on a single +5 V supply is approximately 4.5 V p-p into a 600 Ω transmission system. Amplifier A3 is configured as a difference amplifier for two reasons: (1) It prevents the transmit signal from interfering with the receive signal and (2) it extracts the receive signal from the transmission line for amplification by A4. Amplifier A4's gain can be adjusted in the same manner as A1's to meet the modem's input signal requirements. Standard resistor values permit the use of SIP (Single In-line Package) format resistor arrays. Couple this with the AD8594 16-lead TSSOP or SOIC footprint, and this circuit offers a compact, cost effective solution.

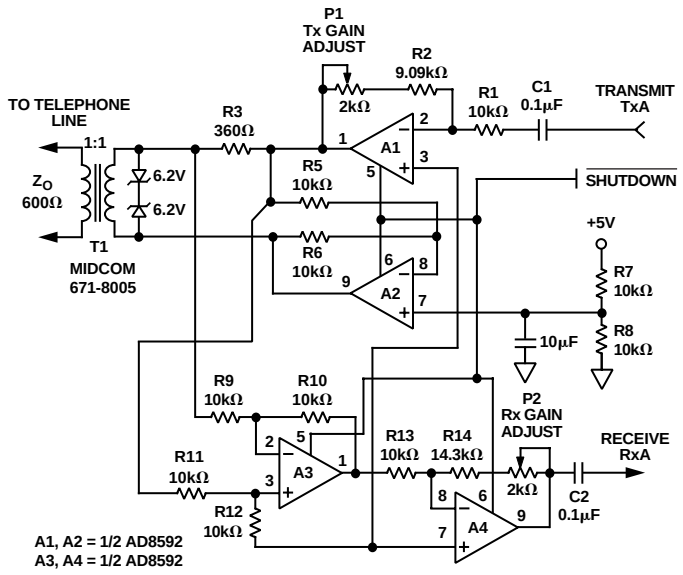


Figure 38. A Single Supply Direct Access Arrangement for PCMCIA Modems

Single Supply Differential Line Driver

Figure 39 shows a single supply differential line driver circuit that can drive a 600 Ω load with less than 0.7% distortion from 20 Hz to 15 kHz with an input signal of 4 V p-p and a single +5 V supply. The design uses an AD8594 to mimic the performance of a fully balanced transformer based solution. However, this design occupies much less board space while maintaining low distortion and can operate down to dc. Like the transformer based design, either output can be shorted to ground for unbalanced line driver applications without changing the circuit gain of 1.

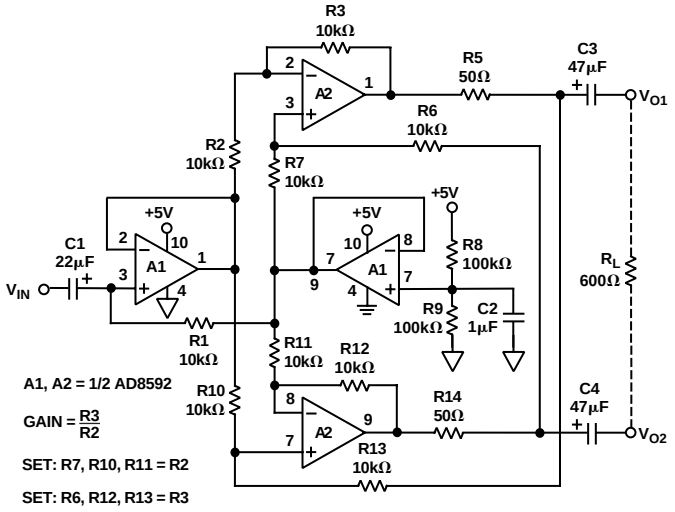


Figure 39. A Low Noise, Single Supply Differential Line Driver

R8 and R9 set up the common-mode output voltage equal to half of the supply voltage. C1 is used to couple the input signal and can be omitted if the input's dc voltage is equal to half of the supply voltage.

The circuit can also be configured to provide additional gain if desired. The gain of the circuit is:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R3}{R2} \quad (7)$$

Where: $V_{OUT} = V_{O1} - V_{O2}$,
$R2$ = R7 = R10 = R11 and,
$R3$ = R6 = R12 = R13

SPICE Model for the AD8591/AD8592/AD8594 Amplifier

The SPICE model for the AD8591/AD8592/AD8594 amplifier is one of the more realistic computer simulation macro-models available, providing a high degree of realism with respect to characteristics of the actual amplifier. This model, shown in Listing 1, is based on typical values for the device and can be downloaded from Analog Devices' Internet site at **www.analog.com**.

The model uses a common source output stage to provide rail-to-rail performance. This allows realistic simulation of open-loop gain dependency on load resistance as well as maximum output voltage versus output current. Two differential pairs are used in the input stage of the model, simulating the rail-to-rail input stage of the AD8591/AD8592/AD8594 amplifier.

The EOS voltage source establishes the input offset voltage and is also used to simulate the common-mode rejection power supply rejection, and input voltage noise characteristics for the model. In addition, G2, R2 and CF are used to help set the open-loop gain and gain-bandwidth product of the model.

A number of secondary characteristics are also accurately portrayed in the SPICE model. Flicker noise is accurately modeled with the 1/f corner frequency set through the KF and AF terms in the input stage transistors. C1 and C2 are used in the input section to create secondary poles to achieve an accurate phase margin characteristic for the model.

The AD8591/AD8592/AD8594 shutdown circuitry is included in the model. Switches S1 through S7 deactivate the op amp circuitry in shutdown mode. The logic threshold for the shutdown circuitry is accurately modeled through the VSWITCH model parameters near the end of the listing. The active supply current versus supply voltage is also modeled through the voltage-controlled current source GSY.

Characteristics of this model are based on typical values for the AD8591/AD8592/AD8594 amplifier at +27°C. The model's characteristics are optimized specifically at +27°C, and may lose accuracy at different simulation temperatures.

Listing 1: AD859x SPICE Macro-Model

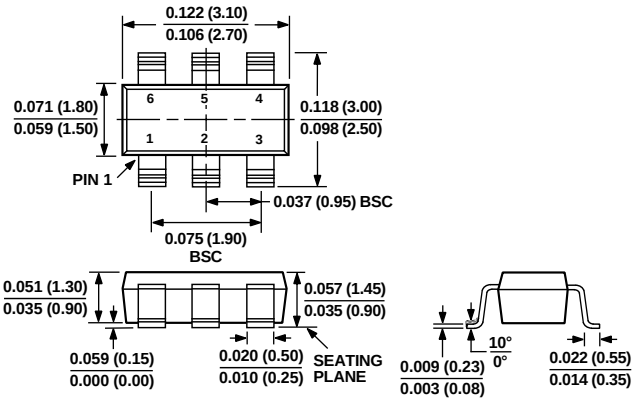
```
* AD8592 SPICE Macro-Model Typical Values
* 9/98, Ver. 1
* TAM / ADSC
*
* Copyright 1998 by Analog Devices
*
* Refer to “README.DOC” file for License
* Statement.  Use of this
* model indicates your acceptance of the
* terms and provisions in
* the License Statement.
*
* Node Assignments
*                      noninverting input
*                      |   inverting input
*                      |   |    positive supply
*                      |   |    |   negative supply
*                      |   |    |   |  output
*                      |   |    |   |  |   shutdown
*                      |   |    |   |  |   |
.SUBCKT AD8592         1   2   99  50  45  80
*
* INPUT STAGE
*
M1   4  1 3 3 PIX L=0.8E-6 W=125E-6
M2   6  7 3 3 PIX L=0.8E-6 W=125E-6
RC1  4 50 4E3
RC2  6 50 4E3
C1   4  6 2E-12
I1  99  8 100E-6

M3  10  1 12 12 NIX L=0.8E-6 W=125E-6
M4  11  7 12 12 NIX L=0.8E-6 W=125E-6
RC3 10 99 4E3
RC4 11 99 4E3
C2  10 11 2E-12
I2  13 50 100E-6

EOS  7  2 POLY(3) (21,98) (73,98) (61,0)
+1E-3 1 1 1
IOS  1  2 2.5E-12
V1  99  9 0.9
D1   3  9 DX
V2  14 50 0.9
D2  14 12 DX
S1   3  8 (82,98) SOPEN
S2  99  8 (98,82) SCLOSE
S3  12 13 (82,98) SOPEN
S4  13 50 (98,82) SCLOSE
*
* CMRR=64dB, ZERO AT 20kHz
*
ECM1 20 98 POLY(2) (1,98) (2,98) 0 .5 .5
RCM1 20 21 79.6E3
CCM1 20 21 100E-12
RCM2 21 98 50
*
* PSRR=80dB, ZERO AT 200Hz
*
RPS1 70  0 1E6
RPS2 71  0 1E6
CPS1 99 70 1E-5
```

```
CPS2 50 71 1E-5
EPSY 98 72 POLY(2) (70,0) (0,71) 0 1 1
RPS3 72 73 1.59E6
CPS3 72 73 500E-12
RPS4 73 98 80
*
* INTERNAL VOLTAGE REFERENCE
*
EREF 98  0 POLY(2) (99,0) (50,0) 0 .5 .5
GSY  99 50 POLY(1) (99,50) 20E-6 10E-7
*
* SHUTDOWN SECTION
*
E1 81 98 (80,50) 1
R1 81 82 1E3
C3 82 98 1E-9
*
* VOLTAGE NOISE REFERENCE OF 30nV/rt(Hz)
*
VN1 60 0 0
RN1 60 0 16.45E-3
HN  61 0 VN1 30
RN2 61 0 1
*
* GAIN STAGE
*
G2  98 30 POLY(2) (4,6) (10,11) 0 2.19E-5 +2.19E-5
R2  30 98 13E6
CF  45 30 5E-12
S5  30 98 (98,82) SCLOSE
D3  30 31 DX
D4  32 30 DX
V3  99 31 0.6
V4  32 50 0.6
*
* OUTPUT STAGE
*
M5  45 46 99 99 POX L=0.8E-6 W=16E-3
M6  45 47 50 50 NOX L=0.8E-6 W=16E-3
EG1 99 48 POLY(1) (98,30) 1.06 1
EG2 49 50 POLY(1) (30,98) 1.05 1
RG1 48 46 10E3
RG2 49 47 10E3
S6  46 99 (98,82) SCLOSE
S7  47 50 (98,82) SCLOSE
*
* MODELS
*
.MODEL PIX PMOS (LEVEL=2,KP=20E-6,VTO=-0.7, LAMBDA=0.01,AF=1,KF=1E-31)
.MODEL NIX NMOS (LEVEL=2,KP=20E-6,VTO=0.7, LAMBDA=0.01,AF=1,KF=1E-31)
.MODEL POX PMOS (LEVEL=2,KP=8E-6,VTO=-1, LAMBDA=0.067)
.MODEL NOX NMOS (LEVEL=2,KP=13.4E-6,VTO=1, LAMBDA=0.067)
.MODEL SOPEN VSWITCH(VON=2.4,VOFF=0.8, RON=10,ROFF=1E9)
.MODEL SCLOSE VSWITCH(VON=-0.8,VOFF=-2.4, RON=10,ROFF=1E9)
.MODEL DX D(IS=1E-14)
.ENDS AD8592
```

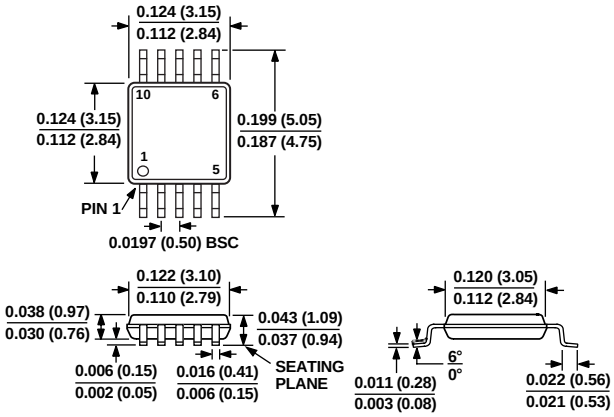
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

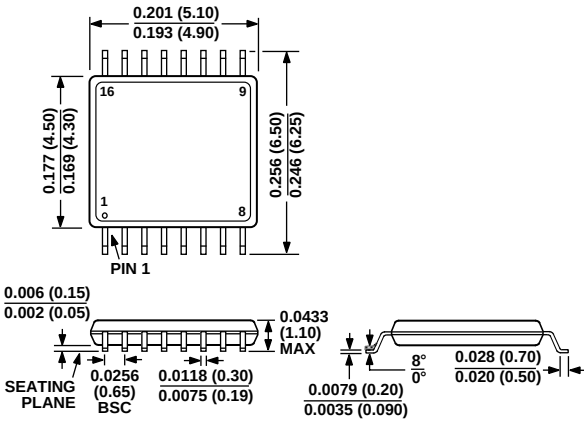
6-Lead SOT
(RT-6)



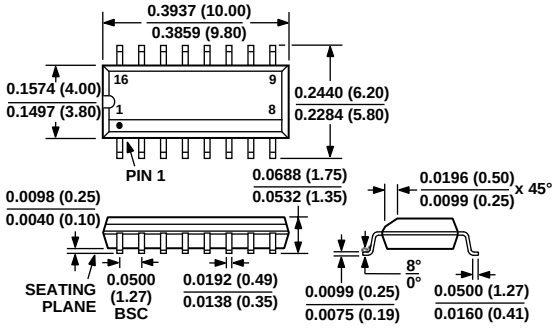
10-Lead µSOIC
(RM-10)



16-Lead Thin Shrink Small Outline
(RU-16)



16-Lead Narrow Body SO
(R-16A)



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