

TLC5602C TLC5602M VIDEO 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS023C – FEBRUARY 1989 – REVISED MAY 1995

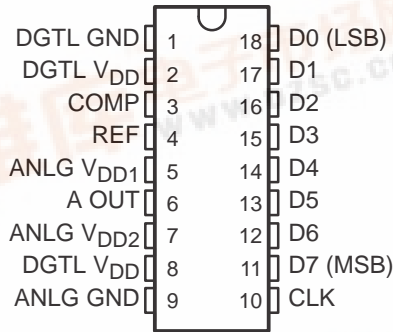
- **8-Bit Resolution**
- **±0.2% Linearity**
- **Maximum Conversion Rate**
30 MHz Typ
20 MHz Min
- **Analog Output Voltage Range**
 V_{DD} to $V_{DD} - 1$ V
- **TTL Digital Input Voltage**
- **5-V Single Power-Supply Operation**
- **Low Power Consumption . . . 80 mW Typ**
- **Interchangeable With Fujitsu MB40778**

description

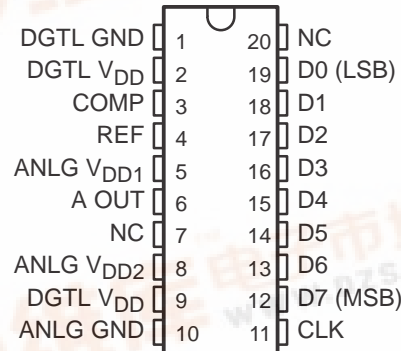
The TLC5602x devices are low-power, ultra-high-speed video, digital-to-analog converters that use the LinEPIC™ 1- μ m CMOS process. The TLC5602x converts digital signals to analog signals at a sampling rate of dc to 20 MHz. Because of high-speed operation, the TLC5602x devices are suitable for digital video applications such as digital television, video processing with a computer, and radar-signal processing.

The TLC5602C is characterized for operation from 0°C to 70°C. The TLC5602M is characterized over the full military temperature range of -55°C to 125°C.

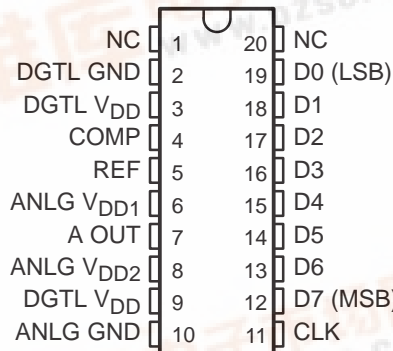
**N PACKAGE
(TOP VIEW)**



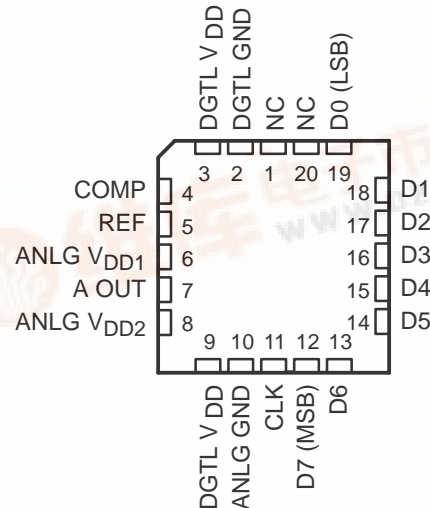
**DW PACKAGE
(TOP VIEW)**



**J PACKAGE
(TOP VIEW)**



**FK PACKAGE
(TOP VIEW)**



NC—No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



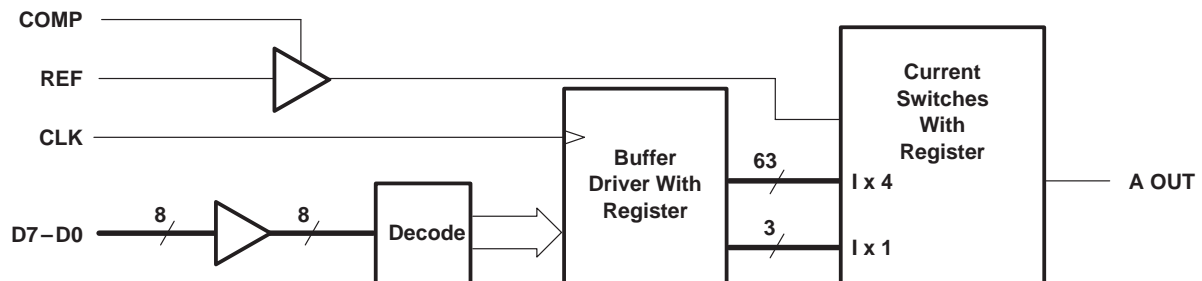
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AVAILABLE OPTIONS

PACKAGE				
T _A	WIDE-BODY SMALL OUTLINE (DW)	CERAMIC CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	TLC5602CDW			TLC5602CN
-55°C to 125°C		TLC5602MFK	TLC5602MJ	

functional block diagram



FUNCTION TABLE

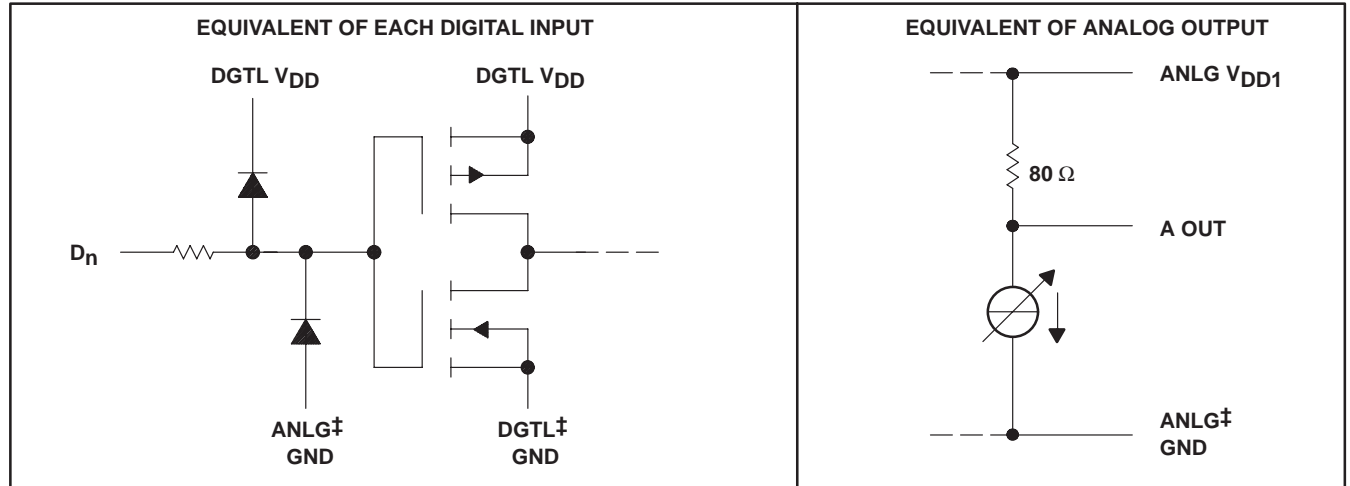
STEP	DIGITAL INPUTS								OUTPUT VOLTAGE†
	D7	D6	D5	D4	D3	D2	D1	D0	
0	L	L	L	L	L	L	L	L	3.980 V
1	L	L	L	L	L	L	L	H	3.984 V
127	L	H	H	H	H	H	H	H	4.488 V
128	H	L	L	L	L	L	L	L	4.492 V
129	H	L	L	L	L	L	L	H	4.496 V
254	H	H	H	H	H	H	H	L	4.996 V
255	H	H	H	H	H	H	H	H	5.000 V

† V_{DD} = 5 V and V_{ref} = 4.02 V

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schematics of equivalent input and output



‡ ANLG GND and DGTL GND do not connect internally and should be tied together as close to the device terminals as possible.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, ANLG V_{DD} , DGTL V_{DD}	-0.5 V to 7 V
Digital input voltage range, V_I	-0.5 V to 7 V
Analog reference voltage range, V_{ref}	$V_{DD} - 1.7$ V to $V_{DD} + 0.5$ V
Operating free-air temperature range, T_A : TLC5602C	0°C to 70°C
TLC5602M	-55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75	5	5.25	V
Analog reference voltage, V_{ref}	3.8	4	4.2	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Pulse duration, CLK high or low, t_w	25			ns
Setup time, data before $CLK\uparrow$, t_{su}	16.5			ns
Hold time, data after $CLK\uparrow$, t_h	12.5			ns
Phase compensation capacitance, C_{comp} (see Note 1)	1			μ F
Load resistance, R_L	75k			Ω
Operating free-air temperature, T_A	TLC5602C		0	°C
	TLC5602M		-55	

NOTE 1: The phase compensation capacitor should be connected between COMP and ANLG GND.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
I _{IH}	High-level input current	Digital inputs V _I = 5 V			±1	μA	
I _{IL}	Low-level input current		V _I = 0 V		±1	μA	
I _{ref}	Input reference current	V _{ref} = 4 V			10	μA	
V _{FS}	Full-scale analog output voltage	V _{DD} = 5 V, V _{ref} = 4.02 V	V _{DD} - 15	V _{DD}	V _{DD} + 15	mV	
V _{ZS}	Zero-scale analog output voltage	V _{DD} = 5 V, V _{ref} = 4.02 V, T _A = full range§	TLC5602C	3.919	3.98	4.042	V
			TLC5602M	3.919	3.98	4.042	
			TLC5602M	3.919	3.98	4.062	
r _o	Output resistance	T _A = 25°C	TLC5602C	60	80	120	Ω
		T _A = full range§					
C _i	Input capacitance	f _{clock} = 1 MHz, T _A = 25°C		15		pF	
I _{DD}	Supply current	f _{clock} = 20 MHz, V _{ref} = V _{DD} - 0.95 V		16	25	mA	

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

§ Full range for the TLC5602C is 0°C to 70°C, and full range for the TLC5602M is -55°C to 125°C.

operating characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E _{L(adj)}	Linearity error, best-straight-line	T _A = full range‡	TLC5602C		±0.2%	
		T _A = 25°C	TLC5602M		±0.2%	
		T _A = full range‡			±0.4%	
E _L	Linearity error, end point			±0.15%		
E _D	Linearity error, differential			±0.2%		
G _{diff}	Differential gain	NTSC 40-IRE modulated ramp,		0.7%		
f _{diff}	Differential phase	f _{clock} = 14.3 MHz, Z _L ≥ 75 kΩ		0.4°		
t _{pd}	Propagation delay time, CLK to analog output	C _L = 10 pF		25		ns
t _s	Settling time to within 1/2 LSB	C _L = 10 pF		30		ns

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

‡ Full range for the TLC5602C is 0°C to 70°C, and full range for the TLC5602M is -55°C to 125°C.

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PARAMETER MEASUREMENT INFORMATION

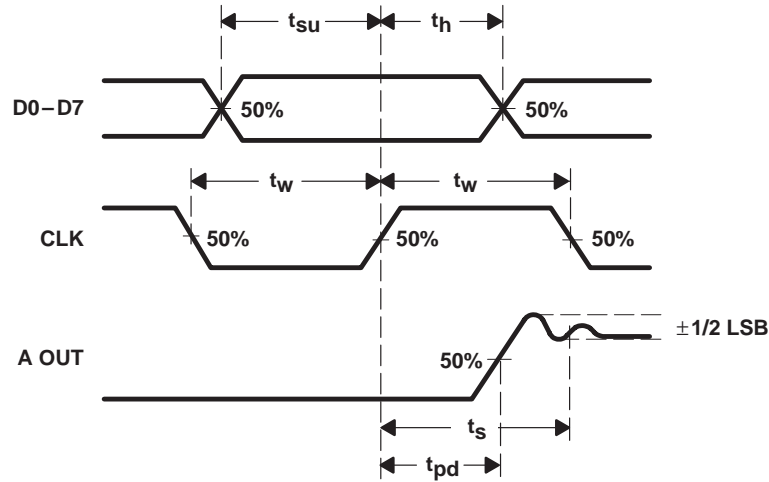


Figure 1. Voltage Waveforms

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TYPICAL CHARACTERISTICS

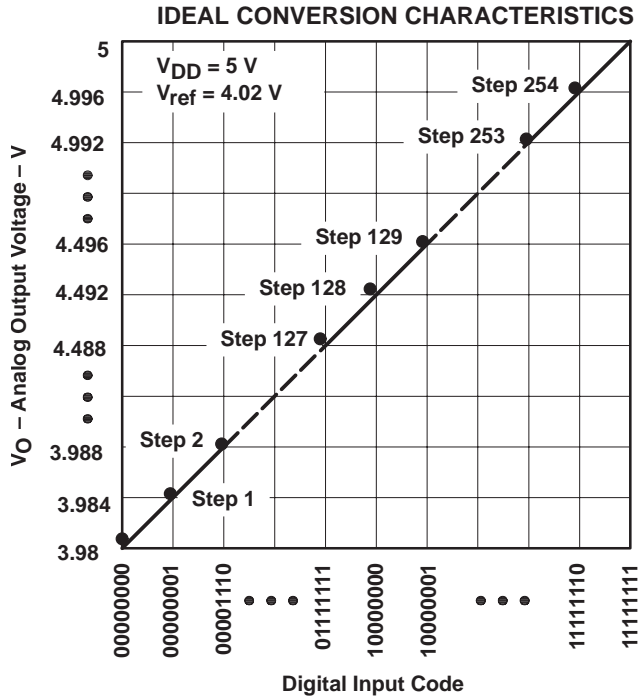


Figure 2

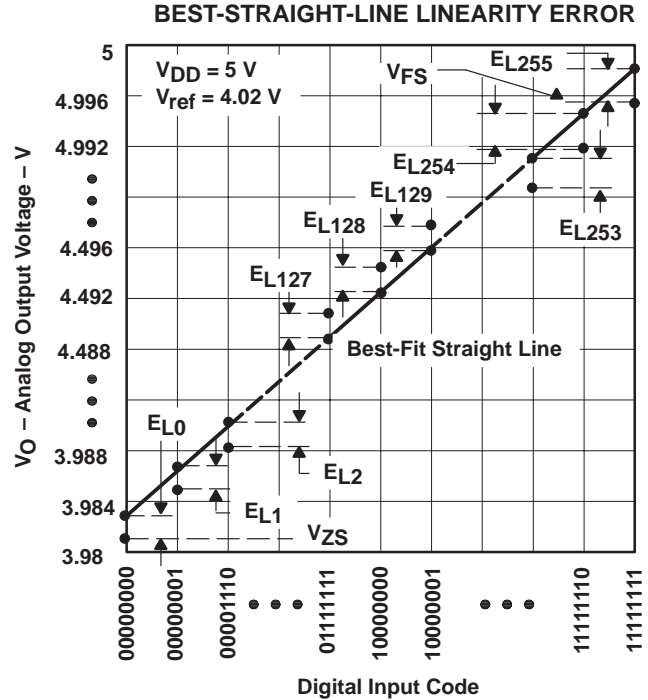


Figure 3

ZERO-SCALE OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

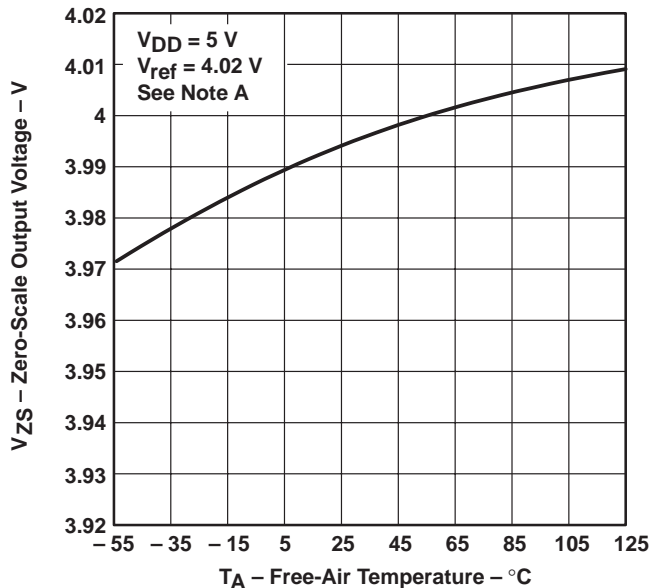


Figure 4

OUTPUT RESISTANCE vs FREE-AIR TEMPERATURE

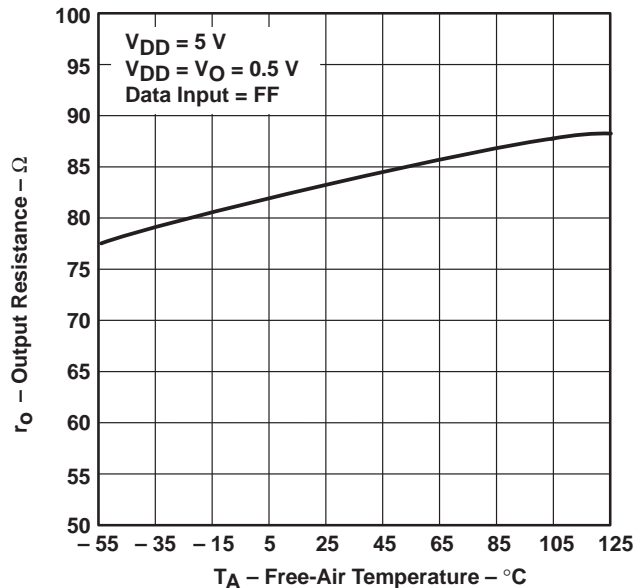


Figure 5

NOTE A: V_{ref} is relative to ANLG GND. V_{DD} is the voltage between ANLG V_{DD} and DGTL V_{DD} tied together and ANLG GND and DGTL GND tied together.

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TYPICAL CHARACTERISTICS

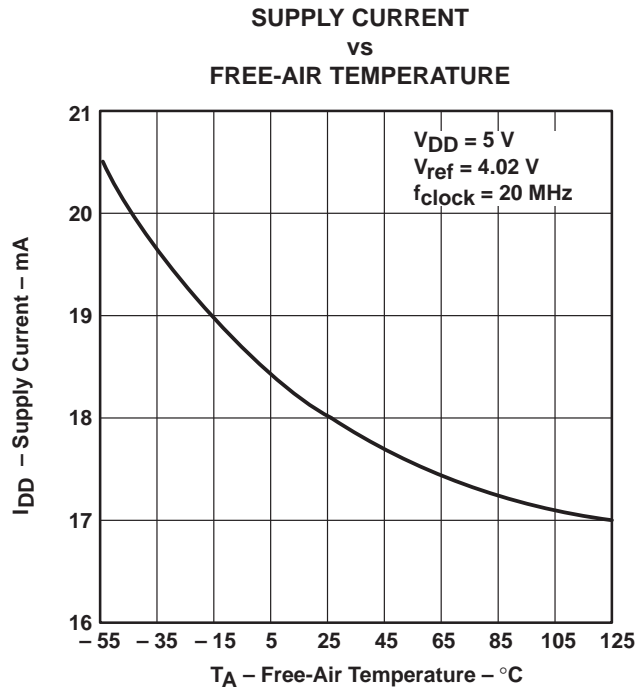
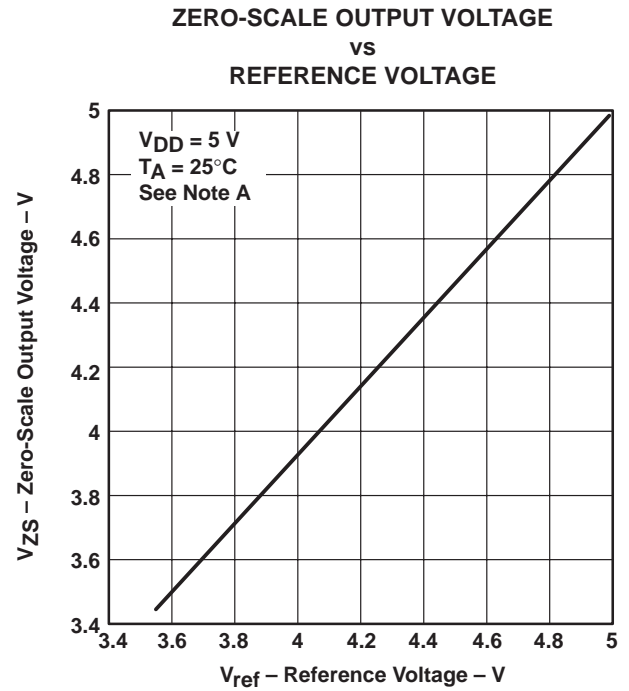


Figure 6



NOTE A: V_{ref} is relative to ANLG GND. V_{DD} is the voltage between ANLG V_{DD} and DGTL V_{DD} tied together and ANLG GND and DGTL GND tied together.

Figure 7

TLC5602C, TLC5602M

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APPLICATION INFORMATION

The following design recommendations benefit the TLC5602 user:

- Physically separate and shield external analog and digital circuitry as much as possible to reduce system noise.
- Use RF breadboarding or RF printed-circuit-board (PCB) techniques throughout the evaluation and production process.
- Since ANLG GND and DGTL GND are not connected internally, these terminals need to be connected externally. With breadboards, these ground lines should connect to the power-supply ground through separate leads with proper supply bypassing. A good method is to use a separate twisted pair for the analog and digital supply lines to minimize noise pickup.

Use wide ground leads or a ground plane on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.

- ANLG V_{DD} and DGTL V_{DD} are also separated internally, so they must connect externally. These external PCB leads should also be made as wide as possible. Place a ferrite bead or equivalent inductance in series with ANLG V_{DD} and the decoupling capacitor as close to the device terminals as possible before the ANLG V_{DD} and DGTL V_{DD} leads are connected together on the board.
- Decouple ANLG V_{DD} to ANLG GND and DGTL V_{DD} to DGTL GND with a 1- μ F and 0.01- μ F capacitor, respectively, as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.01- μ F capacitor.
- Connect the phase compensation capacitor between COMP and ANLG GND with as short a lead-in as possible.
- The no-connection (NC) terminals on the small-outline package should be connected to ANLG GND.
- Shield ANLG V_{DD} , ANLG GND, and A OUT from the high-frequency terminals CLK and D7–D0. Place ANLG GND traces on both sides of the A OUT trace on the PCB.

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